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Low Thermal Budget Gate Stack for Atomic Precision Devices

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Introduction

Need:

Atomic precision advanced manufacturing (APAM), enables high dopant density to support high currents and atomic precision (AP) control in engineering the transistor channel. Switching the highly conductive channel on and off requires large electric fields. Thus, integration of a metal-oxide-semiconductor (MOS) surface gate with AP devices is necessary.

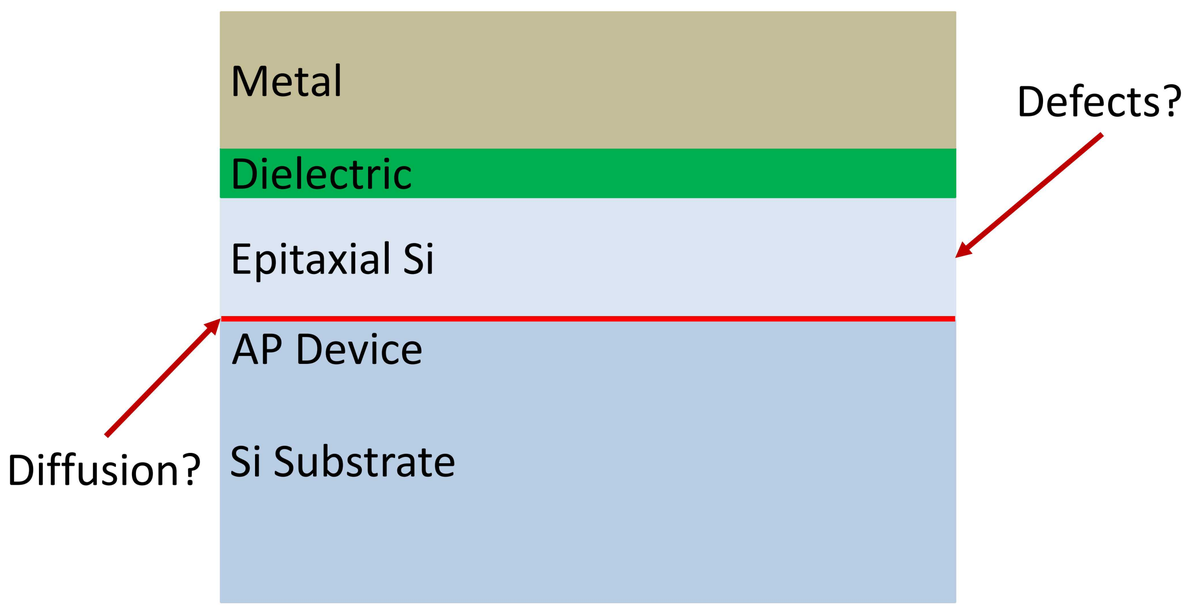
Impact:

Combining MOS surface gates with AP devices creates a platform to study the mapping of atomic-scale structure to device physics in a revolutionary way.

Gaps:

There is a tradeoff between using higher temperatures in processing to improve the quality of the materials for the surface gate, and using lower temperatures to preserve the precision and density of the dopants.

Challenge

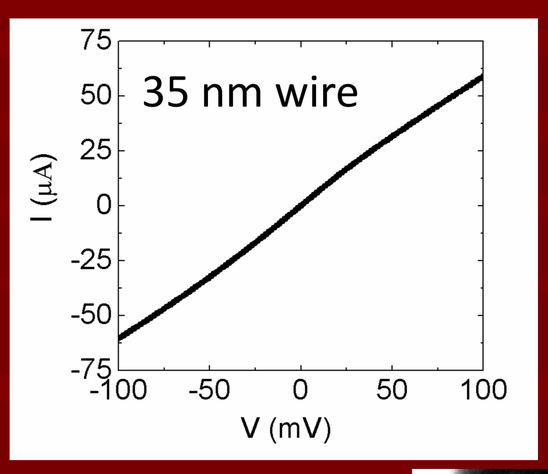


Goal	Challenge
Surface gates	Quality at non-optimal process conditions
Channel engineering	Dopants diffuse away
RT Operation	Isolate leakage paths

Traditional tradeoff between high quality material and minimal dopant diffusion

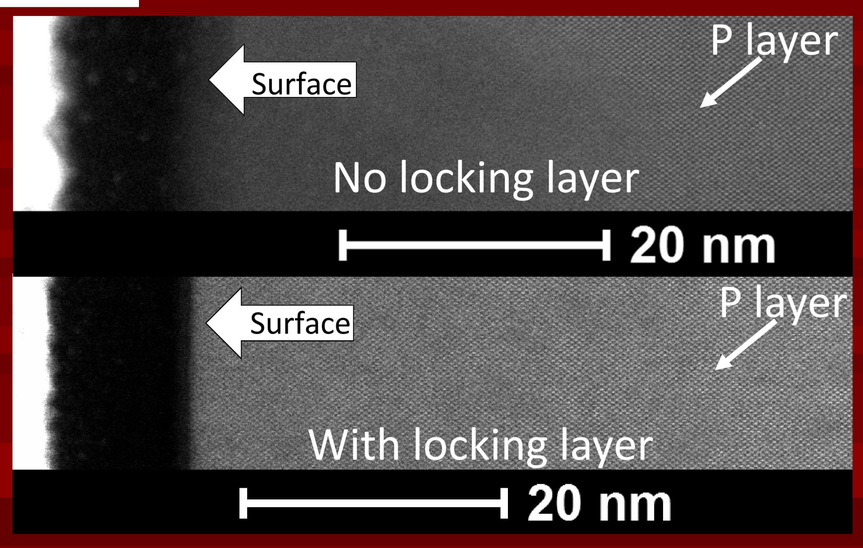
***Path:** Understand how channel and gate stack characteristics map to relevant electrical measurements*

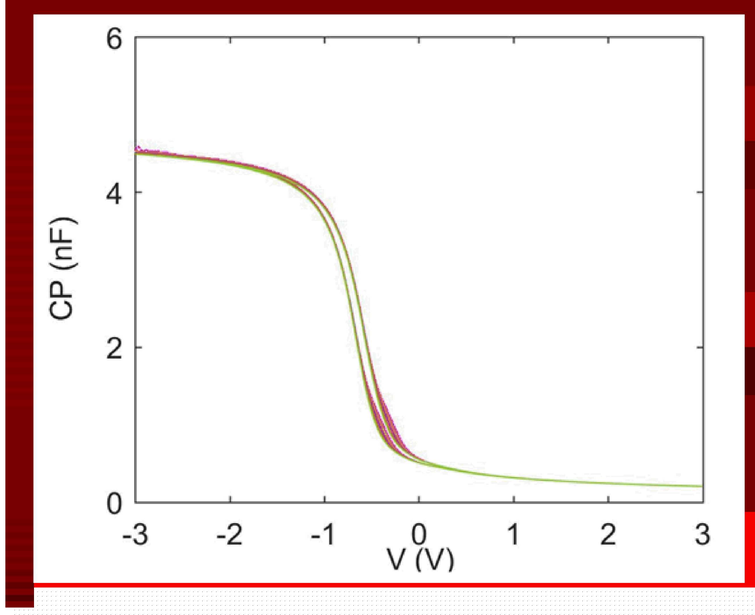
Accomplishments



AP nanowires can achieve high current density ~ 2 mA/μm at cryogenic temperatures

We can control defects in the channel and cap without losing the P layer

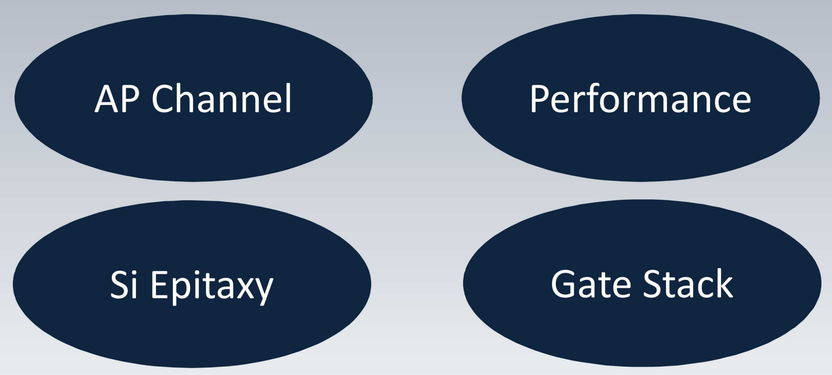




High-k dielectric: We have a low thermal budget gate stack with ~10^{11}/cm^2 defect density at RT

Next Steps

We are in the process of understanding the critical characteristics required for AP channel control, a low thermal budget gate stack, and RT device operation.



Can we combine all of these into a RT APAM-MOS device?

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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