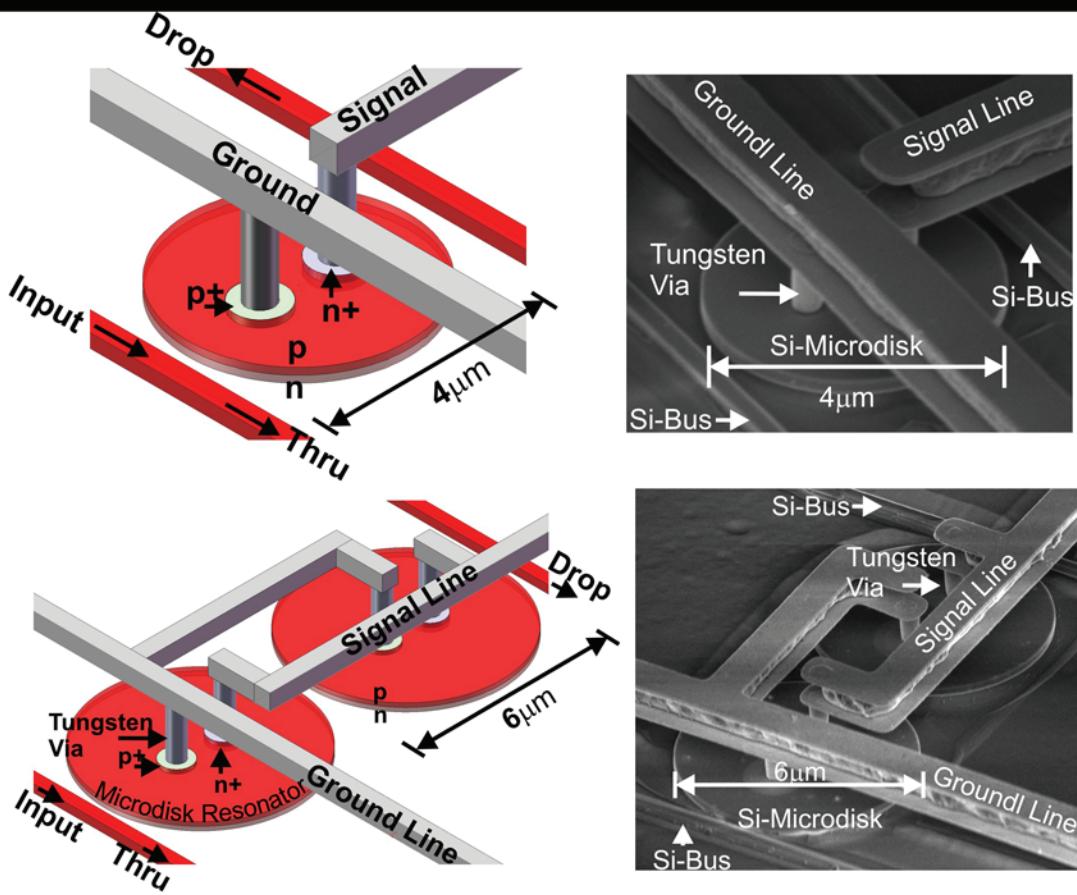


Ultralow-Power Silicon Micromophotonic Communications Platform

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Sandia
National
Laboratories

Ultralow-Power Silicon Microphotonic Communications Platform

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2009

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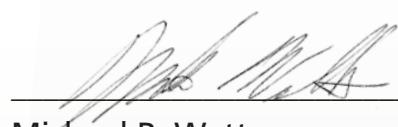
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AFFIRMATION: I affirm that all information submitted as a part of, or supplemental to, this entry is a fair and accurate representation of this product.



Michael R. Watts

Joint Entry

Not applicable

Product Name

Ultralow-Power Silicon Microphotonic Communications Platform

Brief Description

We have developed an ultralow-power, high-bandwidth silicon microphotonic communications platform that addresses the bandwidth and power consumption limitations of future microelectronic inter-chip networks.

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Product First Marketed or Available for Order

April 2008

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Product Price

Licensing fees will be determined based on field of use and market potential within that field.

Patents or Patents Pending

Yes, we have had claims accepted by the U.S. Patent Office on a patent submitted on our silicon modulators and switches.



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Product's Primary Function

Our silicon microphotonic modulators are the smallest demonstrated to date and first to achieve sub-100fJ/bit data transmission (a 100X reduction compared to electrical inter-chip communications). Further, our silicon bandpass switches represent the first demonstration of optical data routing on a silicon platform at nanosecond switching speeds, opening up the possibility for ultralow power optical domain routing of high-performance computer and data communications network traffic. Moreover both our modulators and bandpass switches, can be driven with complementary metal-oxide-semiconductor (CMOS) drive voltages, another first for a CMOS compatible microphotonics. Together, these devices establish, for the first time, a platform of ultralow-power silicon microphotonic communication elements capable of addressing the bandwidth and power consumption problems of high performance computer and data communications networks.

Computer performance is increasingly being dominated by interconnect limitations. Existing electrical communication links provide insufficient bandwidth and consume far too much power to keep pace with the continued Moore's Law scaling (i.e., the doubling of transistor density every couple of years) of multi-core microprocessors. Microphotonic communication networks interfaced to CMOS electronics can, in principle, enable two-to-three orders of magnitude reduction in communications power with bandwidths exceeding 1-Terabit/second/line, or about 100-times the bandwidth of a high-speed electrical line.

Electrical intra-and inter-chip communication links have been the standard communication method between CMOS circuits since their inception. Yet, the continued Moore's Law scaling of microelectronics is challenging the limits of both on- and off-chip electrical communication links in terms of both power consumption and raw bandwidth. Nowhere is this problem more pronounced than in high-performance, massively parallel, computers. The current highest performing computers are the IBM Roadrunner (Los Alamos National Laboratory) and the Cray XT5 Jaguar (Oak Ridge National Laboratory), each achieving just over 1-Peta-FLOP/second (10^{15} FLOP/s or one-thousand trillion Floating Point Operations per second). These peta-scale machines are critical for advanced scientific modelling of climate change, biological simulations, advanced materials, and our universe, to name just a few impact areas. Exa-scale machines (10^{18} or one million

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trillion calculations per second) which represent the next generation of high-performance, massively parallel, computers are anticipated by 2018 according to past trending of machine performance. Such computing power could, for example, enable *ab initio* modelling of drug interactions in humans, allowing drug discovery to be achieved at a far greater pace, with greater certainty, and without the moral dilemma raised by animal testing.

However, current peta-scale machines consume approximately 1 Megawatt (MW) of power in network (i.e., processor-to-processor) communications alone. Given that electrical communications efficiency is more-or-less fixed (at about 10pJ/bit, or 10^{-11} J/bit), and balanced machines require approximately 1-byte of communications for every FLOP performed for each link in the system (e.g., 7 links/node in a 3-D mesh), reaching exa-FLOP performance using electrical communications will require approaching a Gigawatt (GW) of power (i.e., 10^{-11} J/bit \times 1-byte/FLOP \times 8bits/byte \times 10^{18} FLOPs \times 7 = 0.56GW) just to power the network of an exa-scale machine.

For comparison, the Hoover Dam produces approximately 1-Gigawatt of power. It is highly unlikely any organization would be willing, or able, to devote such a large resource to power a computer. As a result, without a fundamental change in the way inter-chip communications are performed, exa-scale computing and the substantial scientific benefits they enable will not be realized. Moreover, this problem extends beyond supercomputers. Commercial data centers suffer from similar power consumption problems. A recent quote from the New York Times, clearly illustrates this point:

"Based on current trends, by 2011 data center energy consumption will nearly double again, requiring the equivalent of 25 power plants. The world's data centers, according to recent study from McKinsey & Company, could well surpass the airline industry as a greenhouse gas polluter by 2020." ("Demand for Data Puts Engineers in Spotlight," *New York Times*, June 17, 2008).

The world's data centers, such as Google and Yahoo!, which empower the internet, are suffering from the same power consumption problem as supercomputers. In fact, large data centers are being built near renewable

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power sources such as Google's recent investment by the Columbia River for its hydroelectric power and Iceland's recent quest to become a data center hub with its vast geothermal resources.

Further, in both supercomputers and data centers the scaling problem extends beyond the issue of power consumption: given the relatively low bandwidth density offered by even the highest-performing electrical communication lines (10Gb/s/line), over a million electrical lines would be required per rack just to meet the network bandwidth requirements for an exa-scale machine. Similarly, in the data center application, considerable inefficiency exists resulting from the insufficient communications between today's multi-core microprocessors, memory, and the network. As a result, most microprocessor compute cycles are spent in "wait-states" (i.e., waiting for data), resulting in on average only 15 percent compute efficiency.

Through the development of an ultralow-power silicon micromechanical communications platform, we have taken some critical steps towards addressing the power consumption and bandwidth problems associated with electrical communications. Our silicon modulator has a diameter of only 4 microns (μm), demonstrates a bit-error-rate below 10^{-12} for 10 gigabit per second (Gb/s) data without signal pre-emphasis, and requires only 85fJ/bit (fJ = femto-joule or 10^{-15}J) for pseudo-random data, making it the smallest, highest-speed, and lowest-power resonant silicon modulator demonstrated to date. The bandpass switch, constructed using pairs of 6 μm microdisk modulators, has a 40 GHz bandpass, a 2.4 nanosecond (ns) switching time, and is the first electrically active high-speed four-port silicon bandpass switch. This compact, low-power (<1mW: less than 1 milliWatt), high-speed optical switch has the potential to dramatically impact data networks, both within high-performance computers and within fiber-optic networks in general, enabling rapid network reconfiguration for efficient use of available optical bandwidth.

The Technical Problem

High-speed inter-chip electrical communications lines generally consist of terminated transmission lines with an energy/bit given by $\tau V^2/(2Z_L)$ where τ is the bit period and Z_L is the impedance of the line. With one-volt signalling on a

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standard 50Ω (ohm) line, the required energy/bit is 10pJ (i.e., 10mW/Gb/s). While in theory the energy-per-bit is decreased as the bit rate is increased—that is, the electrical line dissipation is constant versus frequency—the use of signal pre-emphasis and equalization to compensate for the dispersive nature of high-speed electrical transmission lines from skin-effect losses has led practical circuits to use increasing power at increasing speed. Improved signalling techniques may reduce the energy consumption somewhat over time, but the progress has been slow. Electrical communications links will not likely approach the fundamental limits imposed by Johnson Noise (i.e., thermal-electron fluctuations) because of practical limitations of cross talk and power-line noise. Further, the bandwidth density of these electrical lines is limited by pin-out density (i.e., how tightly electrical pins can be packed) also difficult to increase in practice because of cross talk, loss, and manufacturing tolerances.

Optical communications offer a path toward greatly reduced power consumption while simultaneously providing massive bandwidth density. Given the added complexity required to implement silicon microphotonic communications links, the benefits in both reduced power consumption and increased bandwidth will likely need to be at least two-orders of magnitude or 100fJ/bit and 1Tb/s/line (in a wavelength-division-multiplexed [WDM] communication link one hundred 10 Gb/s communication channels can be transmitted across one silicon waveguide approximately $1\mu\text{m}$ in width). Fundamentally, the energy required per bit in the optical domain is determined by shot noise (the Poisson arrival statistics of photons). Yet, to achieve a bit-error-rate (BER) of 10^{-15} , requires only a few hundred photons per bit at the receiver ($<0.1\text{fJ/bit}$). Still, although the fundamental energy requirements are low, the capacitances of the modulators and receivers impose technological limitations. The intimate integration of silicon microphotonic modulators, detectors, switches, and passive wavelength combining circuits with CMOS electronics offers a potential solution. At the receive end, the required energy/bit is reduced by minimizing the capacitance to the point where a gate can be flipped directly by the incident optical energy, thereby eliminating the need for a transimpedance amplifier at the receiver and its associated static power dissipation.

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Our Innovative Solution

Our silicon modulators operate by depleting (i.e., removing the carriers from) a vertically oriented p-n junction in a micron-scale whispering-gallery mode resonator. While resonant silicon modulators have been demonstrated by others, previous devices had insufficient speed, required signal pre-emphasis, high-drive voltages, and consumed too much power to be useful in low-power inter-chip communication applications. On account of our depletion-mode vertical p-n junction, our silicon modulators are the smallest (diameter of only 4 μ m), fastest (10Gb/s), lowest voltage (only 3.5), and lowest power (85fJ/bit) devices demonstrated to date. As such, they represent a key step towards ultralow power silicon microphotonic inter-chip communication lines. Moreover, because these devices are resonant in nature, they act on a single optical wavelength, or channel, allowing for a direct application of WDM and scaling to over 1-Tb/s/line. In addition, on the same silicon microphotonic platform, we demonstrate the first high-speed silicon microphotonic bandpass switches, enabling high-speed optical domain routing on a CMOS compatible platform for the first time.

In our modulators, the use of a depletion mode approach departs from previous resonant modulator devices based on the injection of carriers (i.e., driving carriers into the junction). Since depleted carriers do not suffer from free-carrier lifetime issues, the depletion mode enables faster device response time and therefore higher bit rates without requiring signal pre-emphasis. Essentially applied voltage carriers are extracted, increasing the depletion width and resulting in a negative shift in the resonant frequency. The magnitude of the shift is determined by the doping density, the change in the depletion width, and the overlap with the resonant mode. By using a vertical p-n junction (figure 1a), we maximize the overlap of the depletion width with the optical mode (figure 1b) which serves to minimize the voltage required to get the required shift and resulting modulation. Our device is the first vertically oriented p-n junction resonant modulator.

Further, with no inner wall and a hard outer wall, our use of a step-index microdisk enables the maximum confinement possible in a whispering-gallery mode resonator (term comes from the circular galleries of ancient monasteries supporting circumferential acoustic modes) to enable large free-spectral-ranges

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(FSRs) or separations between resonances in the structure. The small device sizes, therefore, maximize the available communication line bandwidths while simultaneously reducing device area and minimizing capacitance (and thus energy/bit). A vertical p-n junction can be formed in a microdisk by implantation, and contacts can then be made to the junction using tungsten vias, with n+ and p+ plugs, as shown in figure 1a. Under reverse bias, the depletion width can be quite substantial. Finite element simulations predict that under an applied reverse bias of 3.5 V (volts), the depletion width will increase in size by a factor of approximately two, with nearly half the junction depleted (figure 1c). Inserting these results into the finite-difference calculation of the disk mode (figure 1b), the frequency shift of the resonance can be modelled and predicted with great accuracy. In addition, the finite element electrical device simulations provide accurate predictions of the switching speed and energy.

We built the structure depicted in figure 1a in a standard CMOS fabrication facility using optical lithography. A micrograph of the structure is shown in figure 2a. The resonant frequency was measured as a function of applied reverse bias in the Thru (i.e., pass-through port) and plotted in figure 2b alongside the numerical predictions (dashed curves). Under an applied reverse bias of 3.5 V and 7 V, frequency shifts of -20GHz and -34.5GHz, respectively, were observed. Importantly, with a bias of only 3.5 V, nearly complete extinction of the signal was observed. Given that CMOS drive voltages up to 3.3 V can be readily obtained even in advanced technology nodes, our modulators can be driven with standard CMOS compatible drive solutions vastly simplifying the drive circuitry and minimizing the required power consumption.

We measured the bandwidth and switching energy using a time domain reflectometer with a step voltage output. The measurements indicate a 3 dB (decibel) bandwidth of 5 gigahertz (GHz). The switching energy was then determined by integrating the reflected power, and found to be 340 fJ, slightly more than the finite-element method prediction of 230 fJ, both shown in figure 2c. Importantly, in a Non-Return-to-Zero (NRZ) Pseudo Random Bit Stream (PRBS), 0-to-0, 0-to-1, 1-to-0, and 1-1 transitions are all equally probable. Since an energy

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of CV^2 is only consumed on the 0-to-1 transitions, the energy/bit is quite simply $CV^2/4$ or 85fJ/bit, representing the first demonstration below 100fJ/bit, a 100-fold reduction compared to electrical inter-chip communications power.

The 5GHz device bandwidth was sufficient to demonstrate "error-free" 10 gigabit per second (Gb/s) non-return-to-zero (NRZ) data transmission using the direct drive output of a pseudo-random bit stream (PRBS) generator with a voltage level of 1.8 V. The eye-diagram is shown in figure 2c. A bit-error-rate-tester (BERT) at the output of the receiver demonstrated bit-error-rates below 10^{-12} and 10^{-9} for PRBS pattern lengths of $2^{15}-1$ and $2^{31}-1$. The increased error rate at longer pattern lengths (with lower frequency content) was due to a combination of thermo-optic effects and the low received power level resulting from poor fiber-to-chip coupling.

For high-performance computing (HPC) applications, the addition of high-speed bandpass switches to low-power modulators will enable fine-grain routing of information without an optical-to-electrical-to-optical (OEO) conversation step, thereby potentially significantly reducing the power consumption of routing circuits. Further, a bandpass switch can be constructed within the same process flow using nearly identical structures as the modulators already discussed. A pair of microdisk modulators can be coupled together to provide a second-order flat-top response with the sharp roll-off necessary to minimize channel spacing, cross talk, and dispersion. While very-high-order filters can be constructed, second-order filters offer the most straightforward fabrication because the microdisks can be made to be identical, whereas higher-order filters require adjustments to the size of the interior resonators to maintain frequency alignment. Further, a second-order response is sufficient to minimize cross talk and enable dense channel counts for most datacom and telecom applications.

We fabricated a second-order microdisk bandpass switch using a pair of 6 μ m diameter disks coupled to a pair of bus waveguides. Tungsten vias were used to contact the active elements and the active region was composed of a vertical p-n junction. A diagram of the basic structure is shown alongside a micrograph cross-section of the device in figures 3a and 3b. The filter bandpasses, separated by an

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FSR of 32 nanometer (nm), shown in figures 3c and 3d, exhibited flat-top responses with a sharp, second-order roll-off and 33 GHz and 46 GHz 1-dB bandwidths, respectively. The bandpasses achieved peak extinctions of 20 dB in the Thru port and losses of only a few decibels. Because of the much wider bandpasses, we used forward bias operation to shift the filter functions out of band. Frequency shifts of 135 GHz and 200 GHz were achieved with applied currents of 0.5 milliampere (mA) and 1 mA, respectively. At an applied current of 1 mA, an extinction in the Drop (or filtered) port of >30dB was achieved at $\lambda_0 = 1501$ nanometer (nm) and >25dB at $\lambda_0 = 1533$ nm. Importantly, the filter shape at each resonance was maintained largely independent of the applied bias.

We demonstrated the switch operation with a 10-Gb/s $2^{31}-1$ PRBS and a switching voltage of only 0.6 V. While the high impedance of the unterminated device nearly doubled the applied microwave voltage, the required voltage remained well within available CMOS drive levels. The switch state was switched every 6.4 ns in square wave fashion, and the Thru and Drop port responses are depicted in figure 4a. We observed extinctions of 16 dB in the Thru port and 20 dB in the Drop port, along with 10-to-90 percent switch times of approximately 2.4 ns. Wide-open eye-diagrams of the transmitted data in the Thru and Drop ports, shown in figure 4b, indicate that data integrity was maintained through both states and ports of the switch. Further, bit-error-rates (BERs) below 10^{-12} were measured in both states of the switch. To assess the power penalty (i.e., the required increase in received power necessary to maintain a constant BER), the BER as a function of received power was measured for the static switched states in the Thru port (blue line) and Drop ports (red line) and compared to the off-resonant case in the Thru port (see figure 4c). As shown in the figure, the power penalty in the switched state of the Thru port was almost imperceptible. In the Drop port, at a BER of 10^{-12} , the power penalty was less than 0.4 dB. In either case, the impact was minimal.

The switching time of this forward-biased bandpass switch was slower compared to the reverse-biased modulator due to the increased capacitance of forward-biased operation and the long carrier recombination lifetime in silicon. However, typical latencies in the routing of data in computing applications are in the

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many hundreds of nanoseconds due primarily to communication protocols and, to a lesser extent, physical latency. So, while forward-biased operation is undesirable for modulators, a switching time of a few nanoseconds is more than sufficient for routing applications, and the large frequency shifts offered by the forward-biased operation are necessary to achieve large extinction ratios with 40 GHz bandpasses.

Moreover, the static power consumption of the bandpasses switches is only approximately 1 milliwatt (mW) and can be considerably reduced by only injecting current in the outer portions of the microdisk. That said, for bandpass switches with narrower pass-bands, reverse-biased operation would certainly be possible, and desirable.

Ultralow-power resonant modulators and high-speed silicon bandpass switches have the potential to significantly impact interconnection networks.

Ultralow-power resonant modulators and high-speed silicon bandpass switches have the potential to significantly impact interconnection networks between nodes of a supercomputer, microprocessors and memory, and other high-speed data networks. By integrating vertical p-n junctions in silicon microdisk resonant modulators, we minimized the device size and maximized the modal overlap with the depletion region to enable reverse-biased operation with CMOS-compatible drive voltages at data rates of 10 Gb/s without the need for signal pre-emphasis or amplification. Importantly, these same qualities led to a power consumption of only 85fJ/bit, the first demonstration of silicon modulator power consumption below 100fJ/bit. With further optimization of the modulator structure, a power consumption of 10fJ/bit (10 μ W/Gb/s) is likely to be achieved. Moreover, their resonant nature directly lends the structures to wavelength division multiplexed (WDM) systems. WDM data links of this type can readily exceed 1-Tb/s/line (terabit/second/line). With a nominal waveguide pitch of 2 μ m, bandwidth densities of 1-Tb/s/ μ m are certainly possible. Finally, by coupling a pair of microdisk modulators, we demonstrated the first electrically active high-speed (~2.4 ns) bandpass switches. With the addition of high-speed bandpass switches, we envision richly interconnected reconfigurable networks with many terabits/s of bandwidth consuming only milliwatts of power. Silicon microphotonics networks are on track to solve the bandwidth limitation and power consumption issues limiting electrical inter- and intra-chip networks today.

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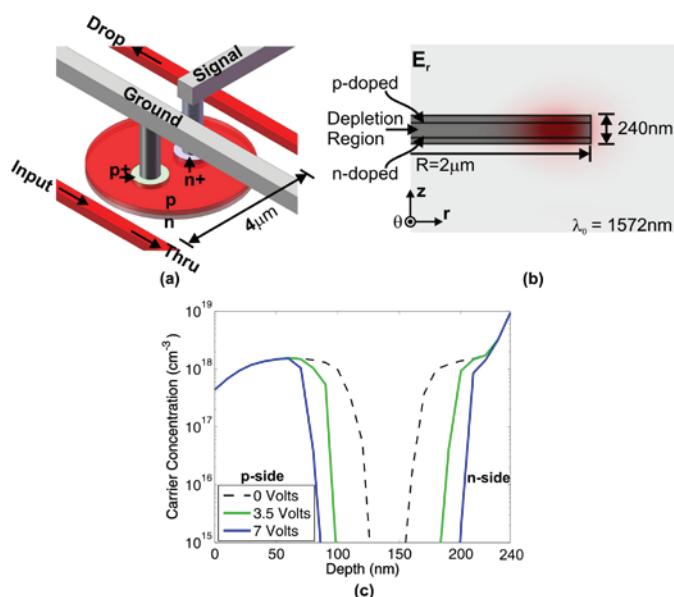


Figure 1. (a) A diagram of the silicon microdisk modulator. A vertical p - n junction is formed in the modulator through implantation, with p^+ and n^+ implants for making contact between the vias and the p and n layers, respectively. (b) The vertical junction provides a strong overlap between the optical mode and the depletion region. (c) The width of the depletion region is controlled with an applied reverse bias voltage.

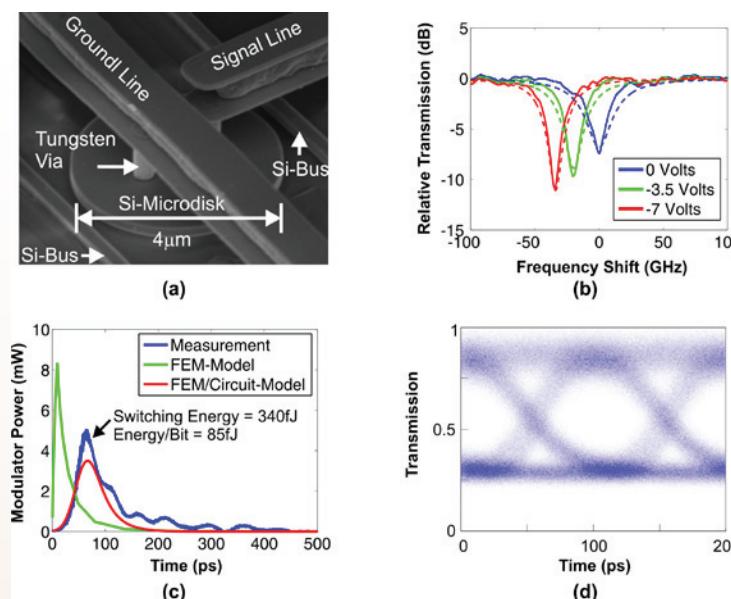


Figure 2. (a) A scanning electron micrograph (SEM) of the microdisk modulator. The modulator is only $4\mu\text{m}$ in diameter and was fabricated with CMOS-style processing and optical lithography. (b) The numerically obtained (dashed lines) and measured (solid lines) Thru-Port filter responses under applied bias. (c) The power required to switch the modulator at a voltage of 3.5 V from a 0 to a 1 state was measured using electrical time domain reflectometry. Since only the 0-to-1 transition requires energy, the measured energy-per-bit is 85 fJ . (d) The modulator eye-diagram from a 10Gb/s NRZ $2^{31}-1$ pseudo-random-bit-stream (PRBS).

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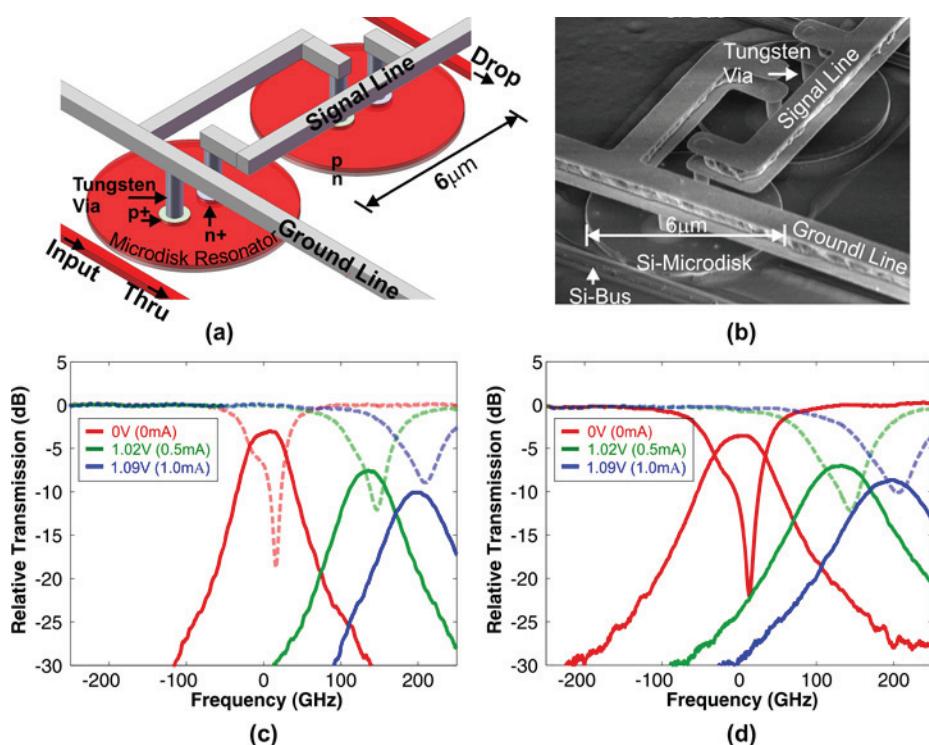


Figure 3. A diagram (a) and an SEM (b) of a 2nd order microdisk bandpass switch formed from a pair of coupled microdisk modulators. The switch operates by applying a forward bias across the p-n junction. The response of short (1501nm) and long wavelength (1533nm) bandpasses, separated by a free-spectral-range (FSR) are depicted in (c) and (d), respectively. With an applied bias of only 1.09V/1mA, the bandpasses are shifted fully out of the channel. The filter responses have 1dB bandwidths of 33GHz and 46GHz, respectively.

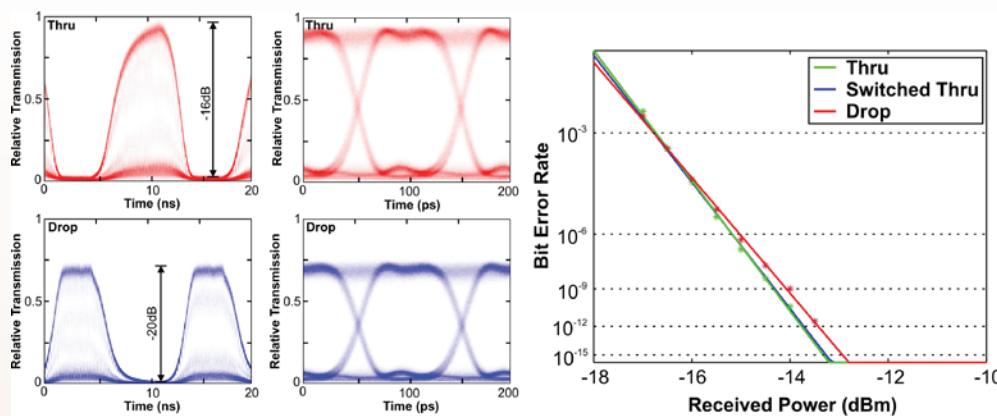


Figure 4. A 10Gb/s NRZ PRBS was generated by an external lithium niobate modulator and sent through the 1533 nm bandpass of the switch depicted in figure 3. The switch was then activated with a square-wave modulation. The outputs of both the Thru (red) and Drop (blue) ports are shown in (a). Extinctions of -16dB and -20dB are achieved in the Thru and Drop ports, respectively. (b) Eye diagrams of the 10 Gb/s PRBS were obtained in the Thru and Drop ports under switch activation. No perceptible degradation in the eye diagram was observed in either port. (c) The bit-error-rate (BER) of the switch as a function of received power in the static states of the Thru and Drop ports were compared to that of the off-resonance Thru port. A power penalty close to 0dB was observed in the Thru port and a power penalty of only -0.4dB was observed in the Drop port at a BER of $<10^{-12}$.

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Product's Competitors

Competing products include traditional electrical interconnects, such as those used by many manufacturers of computer and datacom equipment, including IBM, RAMBUS, and Intel. On the photonics front, a silicon photonic startup, Luxtera Inc., has demonstrated a 40 Gb/s active cable (electrical plug-in, but optical cable), however, Luxtera's devices are inherently large in size and consume considerably more power. Lightwire Inc. has demonstrated similar functionality.

Our technology differs considerably from that of Luxtera and Lightwire who use a very conservative approach based on large, high-power, Mach-Zehnder-based silicon modulators. These devices are approximately 100-times larger and consume approximately 100-times more power than our silicon microphotonic modulators. Moreover, neither of these organizations has demonstrated a wavelength-based-routing capability as we have shown with our high-speed silicon bandpass switches. Therefore, compared to the competition, our approach enables over approximately 100-times reduction in power consumption, while offering a 100-times improvement in available bandwidth through the use of wavelength division multiplexing.

For bandpass switches, the only real competition exists from Micro-Electro-Mechanical (MEMS) and Thermo-Optic Switches used in reconfigurable optical add drop multiplexers in fiber-based telecom applications. Among the best of these switches comes from JDSU Corporation which is capable of routing channels at a 5 ms switching speed. Since all of these switches were designed for telecom applications where channels are reconfigured infrequently, the switching speeds are universally quite slow and not applicable for the high-speed networks needed for high-performance computing applications. Our switches enable reconfiguration at nanosecond switching speeds.



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Comparison Matrix

10-1. Comparison Matrix

(Modulators)

	Bandwidth	Energy/bit	Bandwidth Density
Traditional Electrical	0.01Tb/s	~10pJ	0.001Tb/s/µm
Luxtera	0.04Tb/s	~50pJ	0.01Tb/s/µm
Lightwire	0.01Tb/s	~40pJ	0.01Tb/s/µm
Cornell Silicon Modulators	0.01Tb/s	>1pJ/bit	0.4Tb/s/µm
Sandia Silicon Modulators	0.01Tb/s	0.085pJ	1Tb/s/µm

10-2. Comparison Matrix

(Optical Bandpass Switches)

	Bandpass	Switching Speed	Switch Power
JDSU ROADM	40GHz	5ms (i.e. 0.005s)	Unspecified
Sandia Silicon Modulators	40GHz	2.5ns (i.e. 0.000000025s)	~1mW

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How Product Improves on Competition

Our silicon microphotonic communications platform dramatically improves upon previous attempts at low-power silicon photonic modulators. Our modulators are the first silicon modulators to achieve sub-100fJ/bit operation and the first resonant silicon modulators to reach 10Gb/s without signal pre-emphasis (as was required by previous resonant modulator demonstrations and which dramatically increases the required voltages and energies/bit). Further, they are the smallest silicon modulators, demonstrated to date with an outer diameter of only 4 μ m, occupying <5 times the area of previous silicon modulators which had an outer diameter of 10 μ m. Since our devices are smaller, our device free-spectral-range (FSR) is equivalently larger, enabling up to 2.5X the bandwidth density. Further, our modulators are the first silicon resonant modulators that can be driven with low, CMOS compatible drive voltages. Moreover, compared to commercial silicon photonic components, from companies such as Luxtera and Lightwire, our modulators are <100X the size and consume <100X the power at a given data-rate, and since they are resonant modulators, they enable wavelength-division-multiplexing directly and therefore unto 100X the bandwidth density or 1Tb/s/ μ m. Finally, compared to traditional electrical interconnects, they enable well over 100X the bandwidth density at less than 100X the power consumption.

With regard to our high-speed bandpass switches, the only real competition exists from MEMS and Thermo-Optic Switches used in reconfigurable optical add drop multiplexers in fiber-based telecom applications. Since all of these switches were designed for telecom applications where channels are reconfigured infrequently, the switching speeds are universally quite slow and not applicable for the high-speed networks needed for high performance computing applications. Our switches enable reconfiguration at nanosecond switching speeds.



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Product's Principal Applications

Data communications and high-performance computing networks

Datacom and high-performance computer networks suffer from a scaling problem. Microelectronics is continuing to scale nearly logarithmically, while the electrical interconnects that supply information to these microelectronic chips are not scaling at all. As a result, a greater fraction of computer power consumption is going to the network, leaving less for actual computation. Moreover, the bandwidth of these inter-chip networks is insufficient to keep these high-performance microelectronic chips supplied with information, leading to bandwidth-starved cores.

Our modulators are the smallest, lowest power, and highest-speed silicon modulators demonstrated to date.

Our silicon microphotonic modulators and bandwidth switches directly address the power consumption and bandwidth limitations of current datacom and high-performance computer inter-chip networks, replacing low-bandwidth, high-power electrical interconnects, with terabit-per-second, femtojoule-per-bit optical networks. Our modulators are the smallest, lowest power, and highest-speed silicon modulators demonstrated to date. Our silicon bandpass switches are the first high-speed silicon bandpass switches demonstrated to date. Together, these modulators and switches establish an ultralow-power silicon microphotonics communications platform.

Telecommunications networks

Telecom networks are also suffering from a power consumption problem.

The Japan's internet already consumes 1 percent of the country's electrical production. Given the continued scaling of internet bandwidth, efficient low-power, and high-bandwidth networks are critically important. Ultralow-power silicon microphotonic elements can enable these networks by enabling very high-bandwidth, reconfigurable and ultralow power optical communications in network routers. Further, these components can play a pivotal role in the filtering, modulation, and direct reconfiguration of telecom wavelength division multiplexed networks.

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Large-format, High-Speed Digital Imagers

Large-format, high-speed, digital imagers, such as those used in digital movie production have severe inter-chip bandwidth requirements. Due to row-column addressing, image artifacts are produced when movies are taken digitally at low frame-rates. To avoid image artifacts, movies need to be filmed at kilo-frame-per-second speeds. For a 10-Megapixel camera, with 10-bits of information-per-pixel, 100 Giga-bits-per-second of information must be transmitted off of the imager. Electrical communications are strained at these bandwidths, especially if the camera is remotely located. High-speed silicon microphotonic interconnects can alleviate these communication bottlenecks enabling fiber-based communications to remote camera heads.



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Other Applications

Other applications extend across the full spectrum of high-speed digital systems, from chip-to-chip to intra-chip applications. Examples include high-speed signaling with cell phones, receivers and transmitters in wireless networks, and communications with telecommunications routers where many terabits/second of data are being continuously redirected. Also, high-speed analog systems including advanced RADAR and LIDAR systems were high-speed, low-power optical-microwave transmitters and receivers are utilized.



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Summary

The current highest-performing supercomputers have just reached Peta-FLOP (10^{15} floating point operations / second). Exa-FLOP (10^{18} floating point operations / second) machines are expected by 2018, but without a revolutionary change in high-performance computer interconnects, exa-FLOP machines will not be realized. The peta-FLOP machines of today require approximately 5 MW of power (between direct power and cooling) with approximately 20 percent of the power (or 1 MW) going to network communications. The power consumption of electrical communications is not decreasing. For an exa-FLOP machine, the linear scaling of the power required for the network indicates that approximately 1 GW of power will be required. Given that the Hoover Dam produces approximately 1 GW of power, it seems extremely unlikely that any organization will devote such a large resource to power a computer.

Our silicon microphotonic modulators demonstrate *for the first time*, a one-hundred-fold reduction in power consumption for communications power comparable to traditional electrical inter-chip networks in a platform capable of achieving up to seven Terabits-per-second of communications bandwidth per communications line. Further, our high-speed silicon bandpass switches demonstrate *for the first time* that the optical data can be routed on a silicon chip at nano-second switching speeds with less than 1 mW of power consumption.

This silicon microphotonics communications platform can be applied to high-performance computers, high-speed digital imagers, and other high-bandwidth applications. In high-performance computers, such low-power, high-bandwidth communications will enable the continued scaling of massively parallel machines into the exa-FLOP era. The impact of reaching exa-FLOP machines to physics, chemistry, and biology, will be dramatic. For example at exa-scale, high-performance computers will enable *ab initio* simulations of drug interactions in the human body for the first time. Our silicon microphotonic modulators and switches represent a key step towards exa-scale computing.

The impact of reaching exa-FLOP machines to physics, chemistry, and biology, will be dramatic.

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Appendices Items

Appendix Item A

Letters of Support

Sun Microsystems

IBM

Columbia University

Appendix Item B

Article about this Technology

Appendix Item C

References



Ultralow-Power Silicon Microphotonic Communications Platform 2009

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Appendix Item A Letters of Support

Sun Microsystems, Inc.



Sun Microsystems, Inc.
CTO Physical Sciences Center
9515 Towne Centre Drive, USAN 10-107, San Diego CA 92127

9th February 2009

Award Committee
R&D Magazine's R&D 100 Awards

To Whom It May Concern:

I am writing to support the nomination of the work of Dr. Michael Watts of Sandia National Labs in the area of Ultralow-power, high-speed silicon microphotonic modulators and switches for a potential R&D 100 award. I have known Michael since early 2007.

As you may be aware, current interconnects in high performance computers represent a key impediment to continuing improvements in computing systems. The interconnects provide insufficient bandwidth for many server and supercomputer applications leading to performance bottlenecks and wasted compute cycles – in certain instances computing efficiency can be as low as 10%. Further, the lack of scaling in interconnect performance has led to an even larger waste of power. For computer performance to scale, dramatic changes in interconnect performance and energy efficiency will be needed. Optical interconnects represent one possible alternative.

While silicon photonic modulators have previously been demonstrated, Dr. Watts and his team at Sandia National Labs have taken a new approach to modulator design. By tightly confining the optical mode in highly compact microdisc and microring modulators, and by using novel vertical p-n junction devices, they have shown, for the first time, that sub-100 fJ/bit switching energies are possible with CMOS compatible drive voltage. This represents a key first step towards high-bandwidth, power-efficient optical links for high-performance computers, data center servers, and eventually even personal computers.

Furthermore, Dr. Watts and his colleagues at Sandia have demonstrated the first electrically driven bandpass switch that has the potential to enable high-speed, channel-based data routing in the optical domain by avoiding the need for optical-to-electrical conversions at the switch points.

Finally, Dr. Watts has demonstrated a new class of ultra-low power whispering gallery mode resonators, which he refers to as adiabatic resonators that enable efficient operation and modulation without requiring extra fabrication steps.

In all, Dr Watts and his team at Sandia National Labs have demonstrated exciting and innovative silicon microphotonic devices that are likely to prove key to future high performance interconnects in high performance computing systems and data centers. It is with great enthusiasm that I recommend Michael Watts and his work an R&D 100 award.

Sincerely,

A handwritten signature in blue ink, appearing to read 'Anil' or 'Anil' with a small 'A' above it.

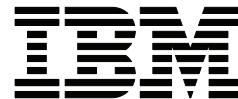
A. V. Krishnamoorthy, Ph.D.
Distinguished Engineer

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IBM

2009



International Business Machines Corporation

Dr. Jeffrey A. Kash

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FAX 914-945-2141
email jeffkash@us.ibm.com

February 10, 2009

Re: Letter of Support for Sandia National Laboratories' Ultralow Power, High-Speed Silicon Microphotonic Modulators and Switches

To whom it may concern:

Future generations (circa 2018) of advanced CMOS microprocessors chips are likely to utilize on-chip optical communications for moving data between the many individual processors (cores) on the chip. While today's advanced microprocessors, such as the IBM Cell™, have up to about 8 individual processors on each chip, there will be something like 100 cores in these future chips. Optical communications has the potential to reduce the energy required (by as much as a factor of 50) to move a bit of information between the cores (on-chip) and also to move information from the chip to the outside world, as compared to moving the data electrically over copper wires as is done today.

There are several challenges for the hardware required to make this vision of on-chip optical communications a reality. These include processing that is compatible with the electrical (CMOS) logic, insensitivity to temperature changes and ultrasmall, low-power devices to create optical bits (i.e., ones and zeros) and subsequently detect those optical bits. Mike Watts and his team at Sandia have shown a key piece of this puzzle: they have demonstrated an ultrasmall and ultralow power modulator to create optical bits in a CMOS-compatible process. At IBM and elsewhere, similar devices have been explored, but the Sandia team is the first to fabricate devices that require tiny amounts of power and yet can operate at the necessary high frequencies.

I am very enthusiastic about this outstanding result, and expect the concept to be a key part of the technologies that are being developed to continue "Moore's Law" improvements in computing while reducing power consumption to allow heat to be removed and conserve energy.

Sincerely,

A handwritten signature in black ink that reads "Jeff A. Kash".

Dr. Jeffrey Kash
Manager, Optical Link and Systems Design
IBM Research

Ultralow-Power Silicon Microphotonic Communications Platform

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Columbia University

2009

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

CENTER FOR INTEGRATED SCIENCE AND ENGINEERING

R&D Magazine's R&D 100 Awards

Letter of Support: Sandia National Laboratories' Ultralow Power, High-Speed Silicon Microphotonic Modulators and Switches

I would like to express my outmost enthusiastic support for including the work led by Dr. Michael Watts at Sandia on ultralow power silicon photonic modulators and switches among the R&D Magazing 100 Awards. Recent advances in the integration of active photonic devices in the silicon platform have led to the consideration of photonic on-chip interconnects for alleviating the ever growing power consumption bottleneck in future multicore processors. In the continual drive toward improved computing performance, power efficiency has emerged as a prime design consideration. In fact, the limitations on power dissipation have become so paramount that performance metrics are now typically measured *per unit power*. At the chip scale, the trend toward multicore architectures and chip multiprocessors for driving performance-per-watt by increasing the number of parallel computational cores is dominating new commercial releases. In this context, the role of the interconnect and associated global communication infrastructure is becoming paramount to the chip performance. However, the realization of a scalable on-chip communication infrastructure faces critical challenges in meeting the large bandwidth capacities and stringent latency requirements demanded by these processors in a power efficient fashion. With vastly increasing on-chip and off-chip communication bandwidths, the interconnect power consumption is widely seen as the key limitation to future scaling of processor performance.

In this context, CMOS compatible integrated photonic interconnects represent a critical path toward a solution that can deliver very large communication bandwidths in a highly energy efficient and scalable manner. Despite the major advances in a myriad of silicon photonic devices, the potential for realizing reductions in the power dissipation have not been demonstrated until this breakthrough work at Sandia. The experimental demonstration of 85fJ/bit represents a key and critically important milestone toward the realization of chip scale ultra-energy efficient, high bandwidth optical interconnects for future generations of multicore processors.

Sincerely,



Keren Bergman
Professor, Electrical Engineering
Columbia University
500 West 120th Street, New York, NY 10027

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Appendix Item B Article

Ultralow Power Silicon Micordisk Modulators and Switches

EXCERPT

WA2 (Invited)
9.15–9.45

Ultralow Power Silicon Microdisk Modulators and Switches

Michael R. Watts, Douglas C. Trotter, Ralph W. Young, and Anthony L. Lentine
Sandia National Labs, P.O. Box 3800, Albuquerque New Mexico 87185
mwatts@sandia.gov

Abstract: We demonstrate a $4\mu\text{m}$ silicon microdisk modulator with a power consumption of 85fJ/bit . The modulator utilizes a reverse-biased, vertical p - n junction to achieve 10Gb/s data transmission, with 3.5V drive voltage, $\text{BER} < 10^{-12}$, and without signal pre-emphasis. High-speed silicon bandpass switches are constructed from pairs of modulators.

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1. Introduction

Communications links on high performance computers currently use electrical or directly modulated laser optical communication links that are connected to microprocessors indirectly through electrical transmission lines. In either case, powering an electrical communication line is necessary. Further, the bandwidth densities offered by multi-mode fibers do not substantially improve upon that provided by electrical transmission lines. However, optics, closely integrated with CMOS electronics has been proposed as a means for substantially improving upon the power consumption of electrical communications links [1]. Further, with silicon microphotonics, wavelength division multiplexing can readily be implemented [2] to drastically increase bandwidth density by enabling multi-terabit per second communication links that are compatible with CMOS electronics.

While many silicon modulator designs have been implemented [3–5], to date, all such devices, both resonant and non-resonant, have consumed a considerable amount of power, and, in the case of forward biased structures [3,5], required signal pre-emphasis in order to achieve data rates of 10Gb/s . Here, we demonstrate a new class of silicon microdisk modulators that utilize a vertical p - n junction. The vertical p - n junction in a $4\mu\text{m}$ diameter microdisk modulator enables sufficient modal overlap to achieve 10Gb/s reverse-biased operation with a low, 3.5V , drive voltage and without signal pre-emphasis. A bit-error-rate (BER) below 10^{-12} was demonstrated along with a measured power consumption of only 85fJ/bit ($85\mu\text{W/Gb/s}$), a new record for silicon modulators. Further, recent finite element simulations demonstrate the potential for 10fJ/bit communications with drive voltages of only 2.5V . Finally, we demonstrate the first high-speed silicon bandpass switches by coupling a pair of these modulator structures [6]. All of these devices were fabricated on a CMOS fabrication line using optical lithography.

2. Discussion and Experimental Results

A cross-sectional diagram and a scanning electron micrograph (SEM) of the fabricated silicon microdisk modulator are presented in Fig. 1a and 1b, respectively. The modulator consists of a $4\mu\text{m}$ diameter microdisk resonator with a vertically oriented p - n junction coupled to a pair of silicon bus waveguides. The modulator was fabricated from a

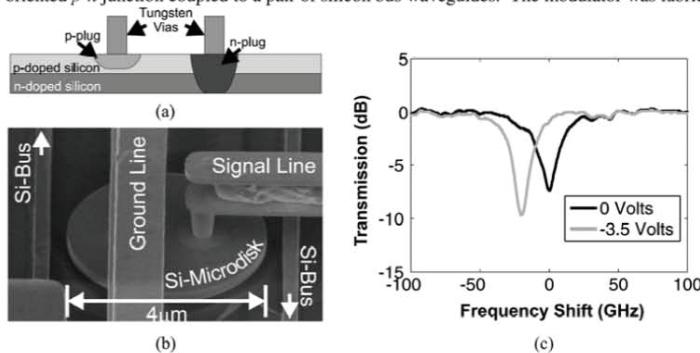


Figure 1. (a) Cross-sectional diagram of the microdisk modulator highlighting the vertical p - n junction and method of contact. (b) A scanning electron micrograph of the fabricated $4\mu\text{m}$ diameter microdisk modulator and (c) the optical spectra of the microdisk with no bias and a 3.5V reverse bias applied. The center wavelength of the unbiased resonance is 1578nm .

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Appendix Item C

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