Guidelines for Essential Functionality

1. ☐ Verify quantities of components on the bill of materials.
2. ☐ Schematic symbol pins match component datasheets.
3. ☐ Schematic symbol pin numbers correctly transfer to the footprint pad or plated thru hole numbers.
4. ☐ The footprint pad or plated thru hole size match those suggested in datasheet (unless specific instructions are received).
5. ☐ The footprint spacing of holes and pads are correct for each component.
6. ☐ The schematic symbol has the desired footprint option selected (some symbols have multiple footprint options).
7. ☐ Check for hidden pins on the schematic symbol and verify their connection in the netlist and PCB layout (common for Vcc and GND pins).
8. ☐ The components are placed where they will not touch other components.
9. ☐ Verify every net on the netlist by checking that at every point of connection for the net, that it is intended to be connected together based on the schematic. Use a marking on a print out of the schematic near every point of connection (such as IC pins or resistor ends) as you come across it on the netlist. Scan the schematic to verify that each used point of contact has only one mark. If there is more than one mark, something is wrong. Verify that all points of connection without a mark are supposed to be no connects. Highlight each net in the layout to verify that something got routed for the net (do not check to see where the traces go).
10. ☐ Consider any traces that may carry significant current and verify that the traces are wide enough.
11. ☐ Verify that LVDS traces are routed side by side and have the correct impedance (see LVDS specification). Look at the traces and try to get them routed directly to their destination (no loops, rats nests, ….). Route them on as few layers as possible (avoid excessive vias).
12. ☐ Place LVDS termination resistors as close as possible to their respective LVDS inputs.
13. ☐ Place crystals and pillar capacitors as close as possible to the pins they connect to. Try to route the traces directly to their destination. Route them on as few layers as possible (avoid excessive vias).
14. ☐ Identify any other critical traces and look at them in layout.
15. ☐ Verify that all connectors with Vcc and GND connections are properly connected (i.e. one side should be sourcing current while the other side should be sinking current)
16. ☐ Place decoupling capacitors as close as possible to the circuits they decouple. Place the smaller capacitors even closer than the larger capacitors.
17. ☐ There should be a Vcc or GND plane at least every 3rd layer.
18. ☐ Verify that all components have longer leads than the thickness of the board.

Guidelines for Ease of Use

19. ☐ DIP switches, push buttons, and headers with jumpers are placed where the user can access them with their fingers.
20. ☐ Mictor headers are placed where the cable can be easily connected.
21. ☐ All right angle connectors are on an edge of the board.
22. ☐ Verify that the spacing of connectors allows all cables to be plugged in at one time.
23. ☐ Test points spaced far enough apart to allow clipping of neighboring test points.
24. ☐ Silk screen labels for all the significant components and connectors (exclude resistors and capacitors).
25. ☐ Silk screen ALL the reference designators.
26. ☐ Reference designator pre-fixes should follow some standard.
27. ☐ Silk screens should be visible after the board has been stuffed.
28. ☐ Every header using jumpers should have a silk screen table indicating all possible configurations.
29. ☐ Try to orient headers in a consistent fashion (i.e. pin 1 always being the top left)
30. ☐ Silk screen the rev number on the board and any other desired identifiers.
31. ☐ Group associated LEDs together and place a silk screen box around them. If it is a bus, indicate the LSb and MSb. Order them with the LSb on the right (or bottom) ascending to the MSb on the left (or top).
32. ☐ Group associated test points together and place a silk screen box around them. Ifit is a bus, indicate the LSb and MSb. Order them with the LSb on the right (or bottom) ascending to the MSb on the left (or top).
33. ☐ Spread GND test points across the board.
34. ☐ Use red test points for Vcc and black test points for GND. Use a dissimilar test point for other signals.

Application Specific Guidelines (may or may not apply)

35. ☐ Components in sockets have the socket footprint associated with the schematic symbol rather than the component's footprint .
36. ☐ The socket lids can open completely without any obstruction.
37. ☐ Since the ASIC socket pressure mounts with a backing plate, verify no components have been placed in that area on the reverse side of the board.
38. ☐ Sockets are accessible to insert and remove chips.
39. ☐ Reset button placed far away from other buttons to avoid accidental assertions.
40. ☐ Put all right angle connectors angle connectors on one side for ease of connection in the temperature chamber.
41. ☐ Verify that nets with different names that should be connected together are manually shorted in the layout.
42. ☐ In order to measure current draw of the ASIC, verify that only the ASIC, its decoupling capacitors, and its pull up/down resistors are connected to the unique Vcc plane.
43. ☐ Avoid arms and legs in all Vcc and GND planes as much as possible to keep the plane resistance lower.
44. ☐ Verify that the unique Vcc planes have plated thru holes and a mate plated thru hole for connecting to the main Vcc plane to solder in a wire for clipping on a current probe (~3cm separation between holes).
45. ☐ Make the board as thick as possible to prevent flexing and offer more mechanical support.
46. ☐ Verify spacing of single socket Vcc and GND to allow use of a double banana plug.
47. ☐ Reference designator numbers will follow a scheme (odds pertain to one ASIC, evens pertain to another ASIC)
48. ☐ Verify the board is small enough to fit into the temperature chamber while it has the cables connected.
49. ☐ Place standoffs to offer sufficient support, particularly near push buttons, cable connectors, and any other place the user will be applying pressure. Also place them around the ASIC sockets to ensure flatness for the pressure mounted socket.