Ion Trapping Microsystem Development

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Sponsorship:

IARPA

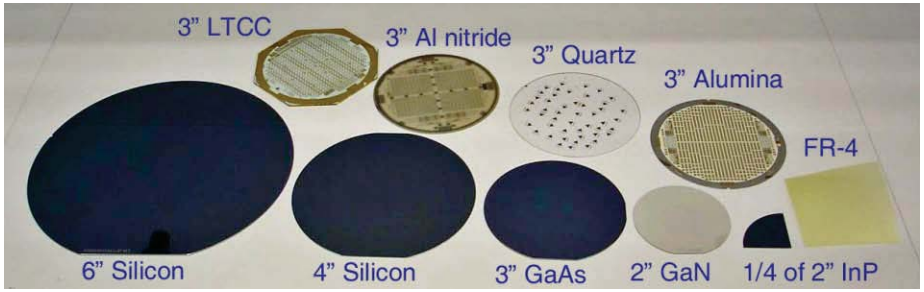
Laboratory Directed Research & Development

Sandia National Laboratories

Facility specifications

- 2 Clean room facilities
- 13000 ft^2 Class 1 clean room for Si CMOS and Si MEMS
- 16,640 sq. ft. Class 10 and Class 100 clean room for Group IV and III/V devices
- Many tools reconfigurable from wafer pieces to 6" wafers
  - Many with little or no hardware changes required
- 6" silicon post-processing and packaging facilities to support device wire-out, hybrid substrates, and 3D integration

The "Machine Shop"



AMO physics lab is here

DiVincenzo criteria

Fortschritte der Physik, 49 **(2000)**

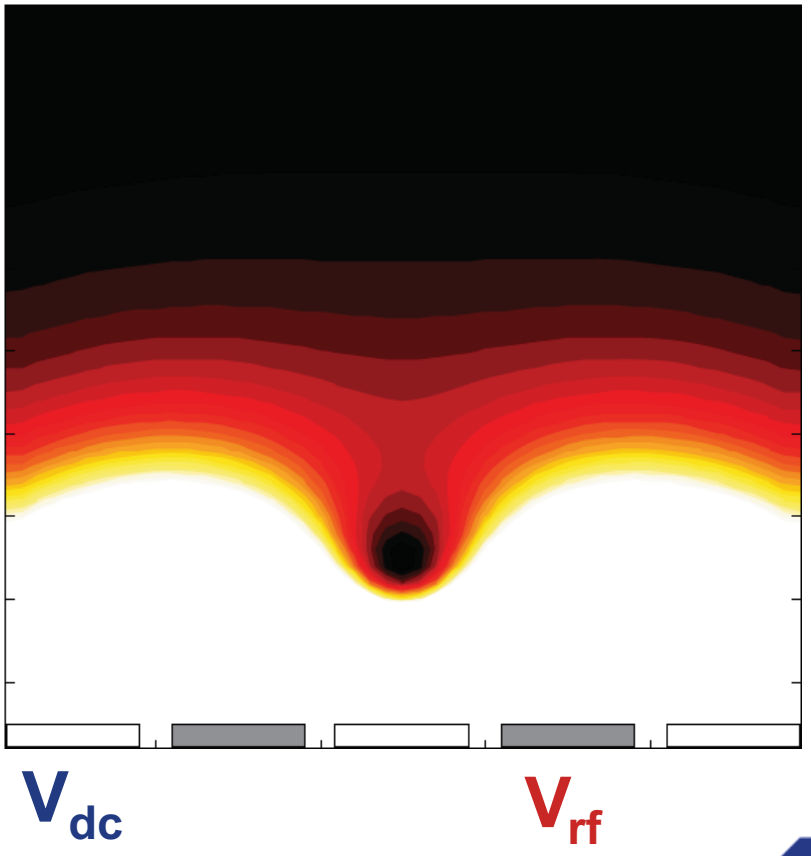
- **Initialization to a pure state**
  - Achieved via optical pumping
  - Error: 3×10^{-5} (PRL 100, 200502, 2008 - Myerson, *et al*)
- **Universal set of quantum gates**
  - Single qubit gate rotations performed with high fidelity
  - Two qubit gate rotations limit overall fidelity
  - Error: 7×10^{-3} (Nature Physics 4, 463, 2008 - Benhelm *et al*)
- **High detection fidelity**
  - Achieved via cycling transition
  - Error: 1×10^{-4} (PRL 100, 200502, 2008 - Myerson, *et al*)
- **Long coherence times**
  - 1000x longer than two qubit gate time (PRA 020304, 2009 - Kirchmair *et al*)

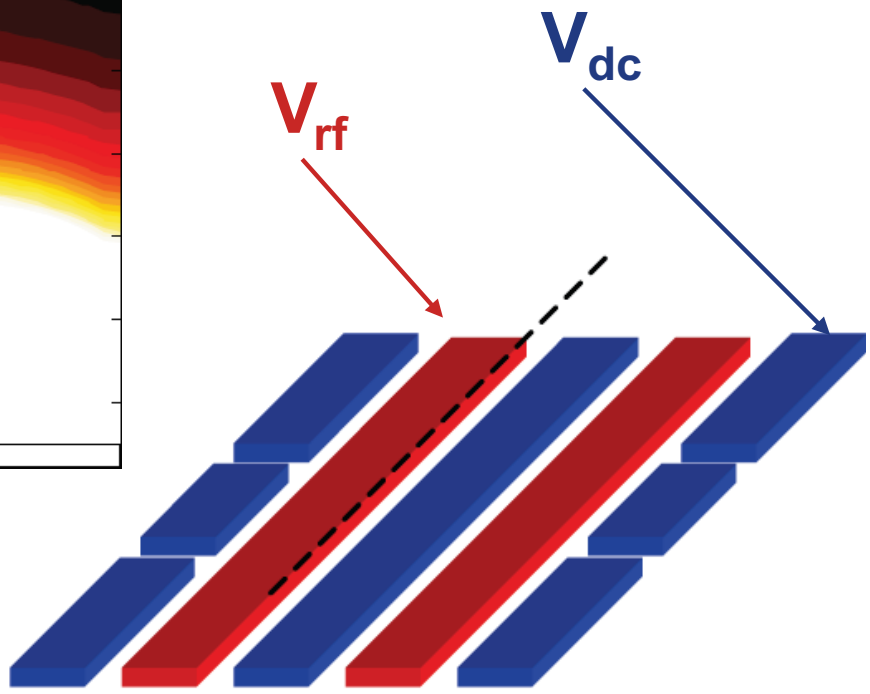
Conclusion: QC operations with small numbers of ions are near or at the fault tolerant regime (Nature 434, 39, 2005 - Knill) for quantum computing, but the final DiVincenzo criterion needs to be addressed:

- **Scalable physical system….**

Ion Trapping 101: Planar trap electrodes

J. Chiaverini, *et al.*
Quant. Inf. Comp. **5**, 419 (2005)

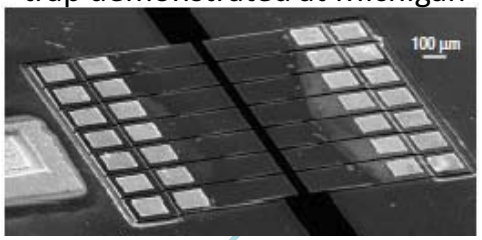


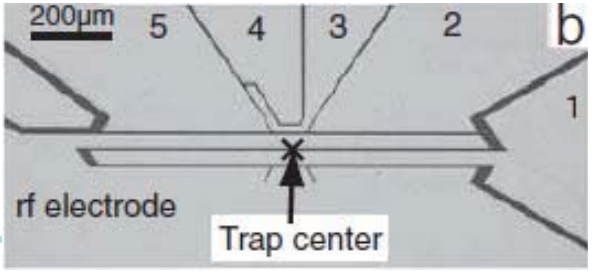


Surface 2-D Trap

Ion Trapping 101: Planar trap development

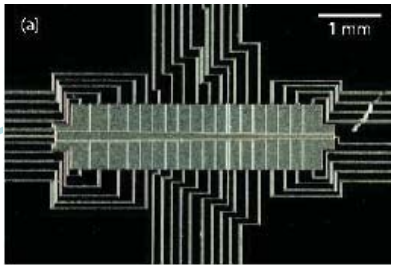
Lithographically fabricated GaAs trap demonstrated at Michigan



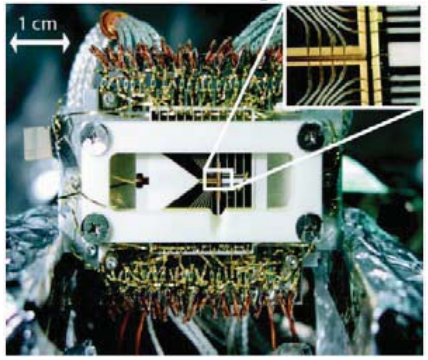


Demonstrated surface trap at NIST

2006



Trap foundry 1 demonstrated a micro-fabricated surface trap



2007

Demonstrated junction shuttling in 3 layer trap at Michigan (~80% success rate)

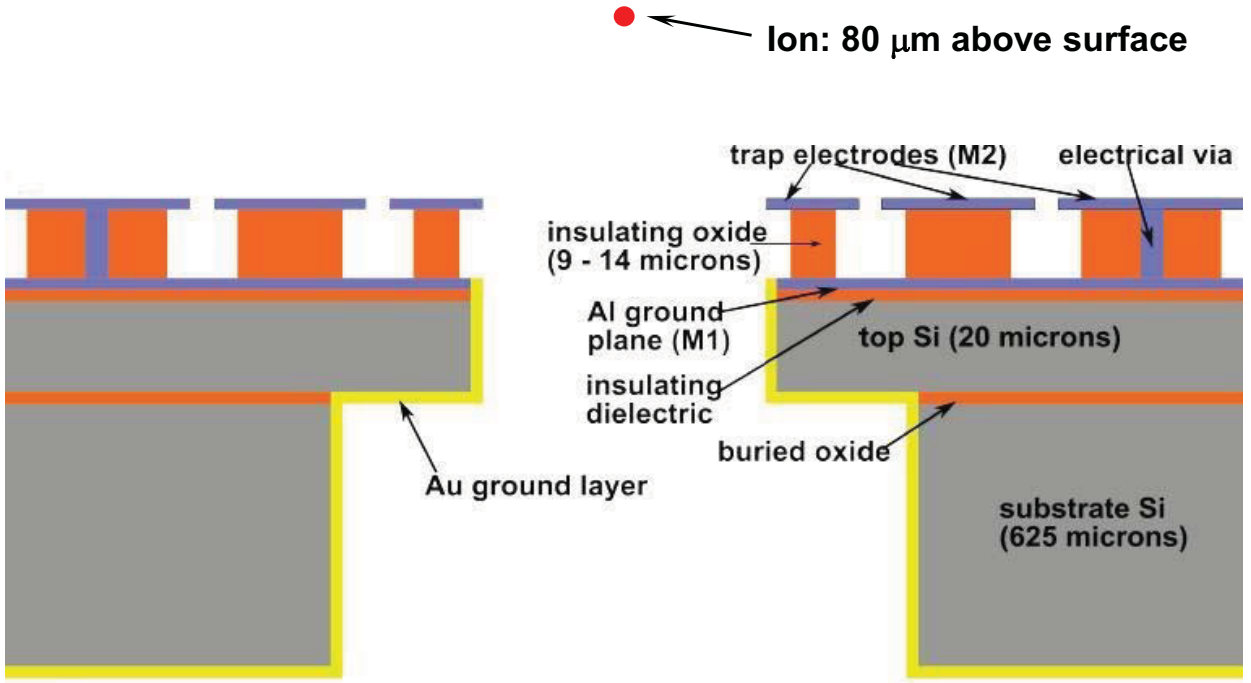
2008

2009

Sandia Ion Trap Foundry 2

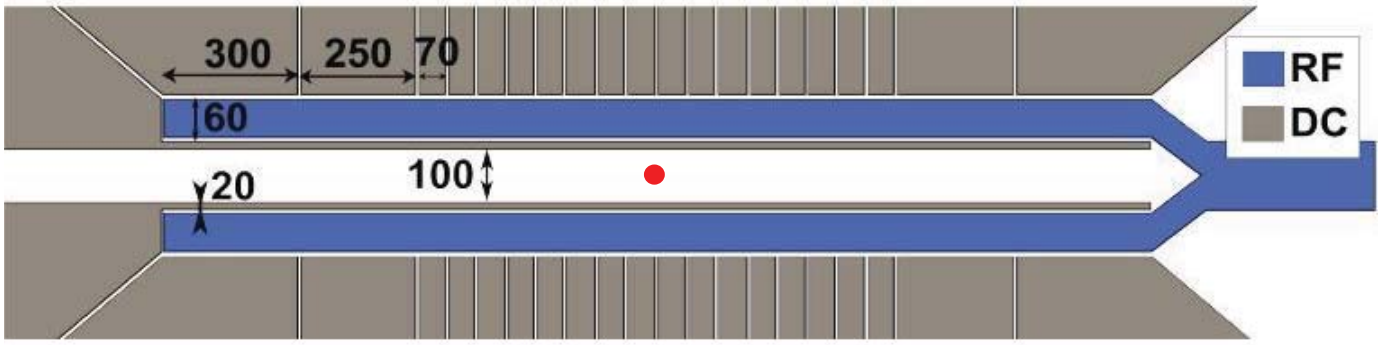
2010

Sandia Ion Trap Foundry: Fabrication



- RF > 300V at 43 MHz
- Total capacitance

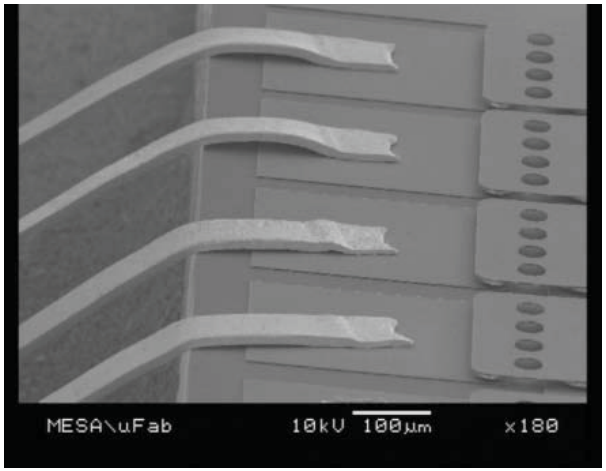
(RF to ground) ≈ 7 pF



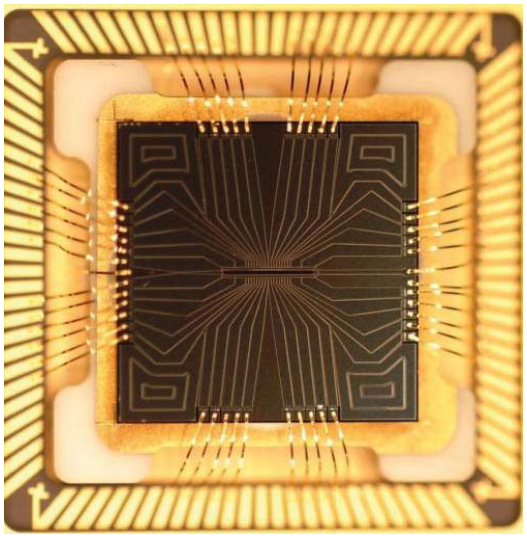
- Precision placement of thru-chip holes for ion loading and optical access
- Thick (9-14 μm) SiO_2 dielectric separation of trap electrodes and ground plane.
- Vertical dielectric sidewalls that are accurately and precisely recessed from the edge of the electrode.

Sandia Ion Trap Foundry: Linear multi-zone surface microtrap

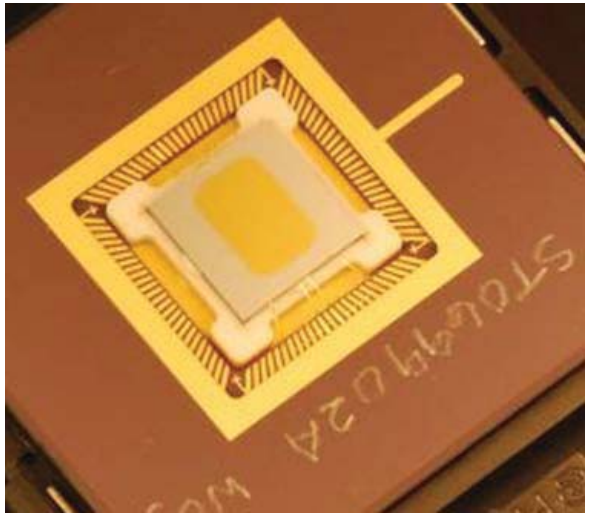
Low profile wire bonding



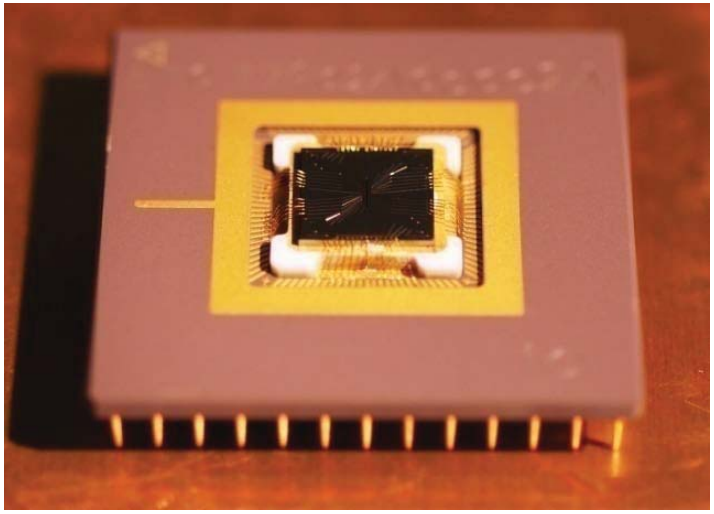
2π beam access



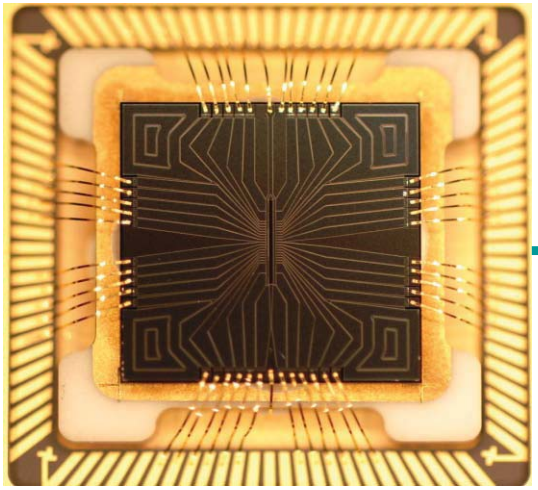
Custom coated electrodes

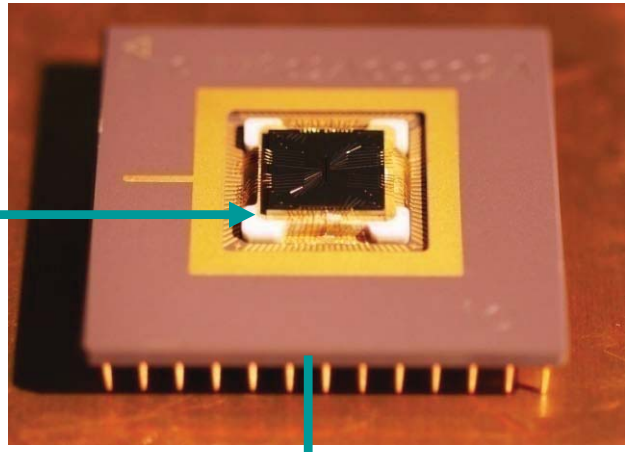


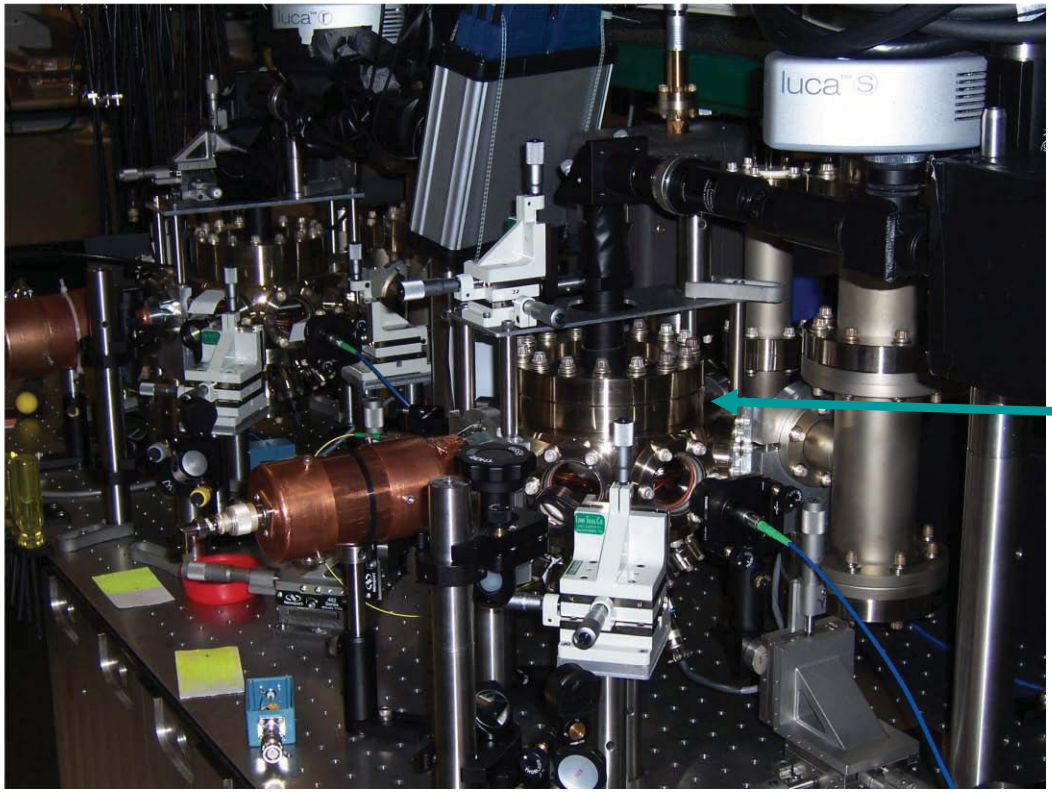
Plug-and-play design

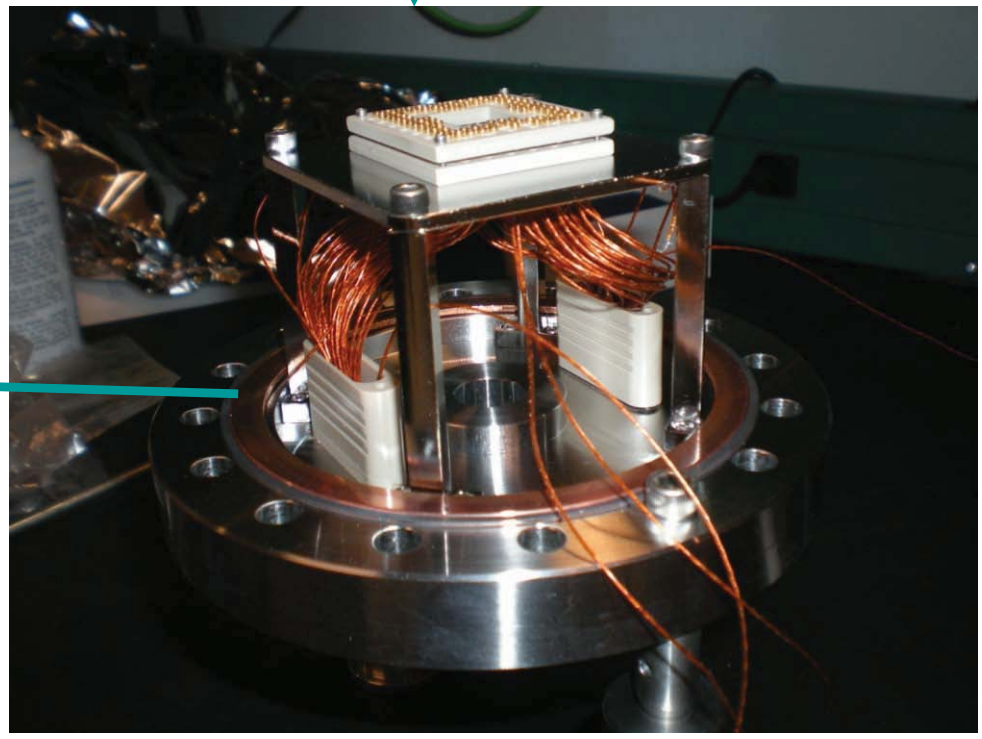


Trap operation and testing

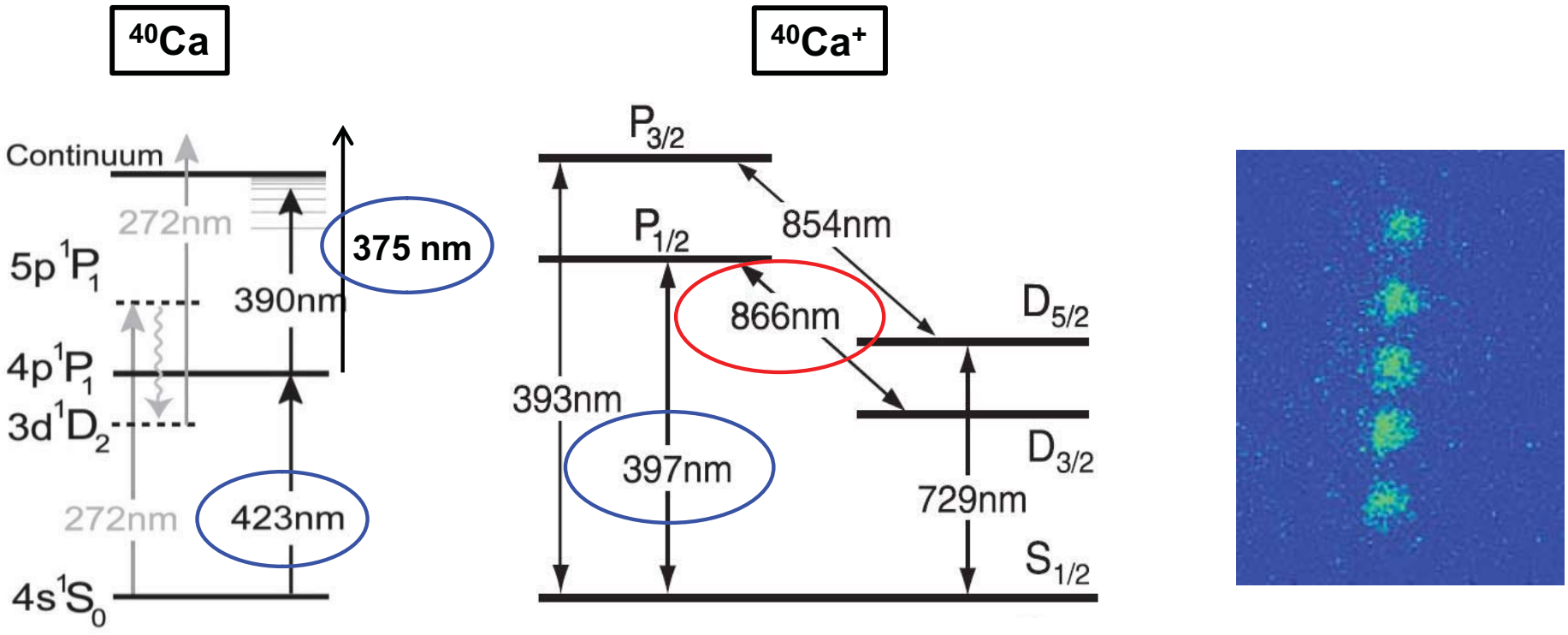








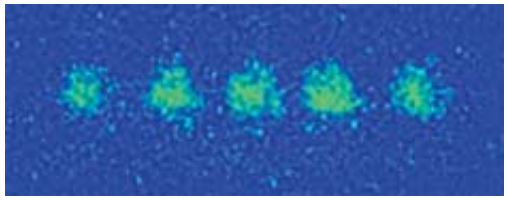
Trap operation and testing



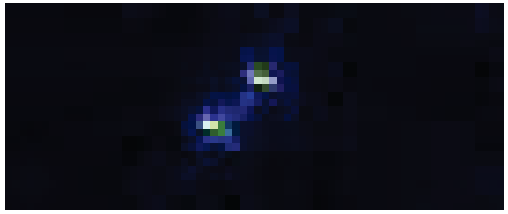
- RF: 150 V amplitude at 30 - 44 MHz
- RF null: 80 microns above surface, principal axes rotated 36°, 750 kHz axial frequency, 5.5 MHz radial frequency
- DC control: 42 independent control electrodes, controlled by NI DAC cards
- ±10 volts, 500 kHz max rep rate

Trap operation and testing: Ion Shuttling

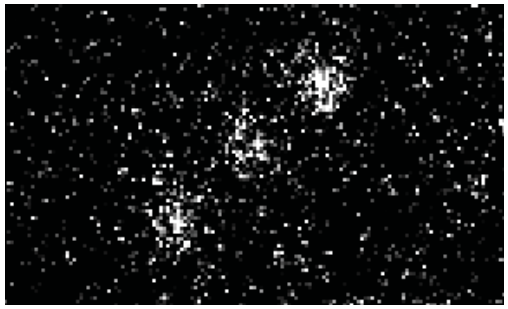
Ca^+ Sandia

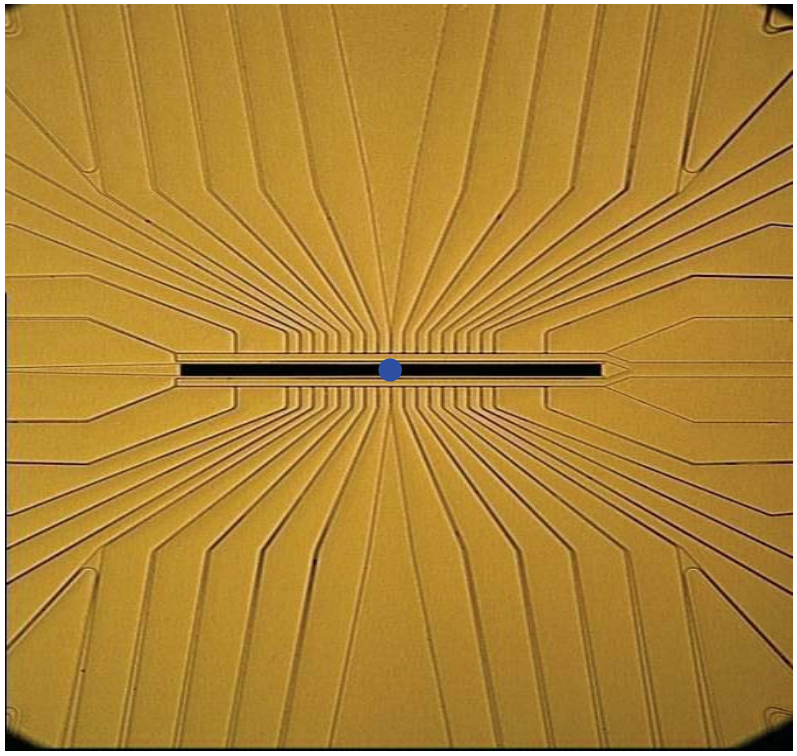


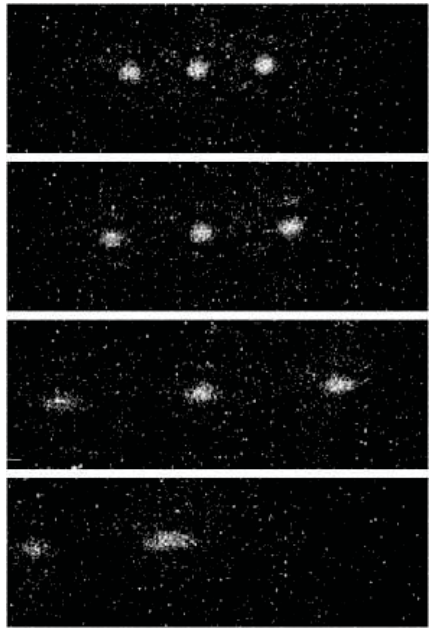
Ca^+ Oxford



Yb^+ UMD







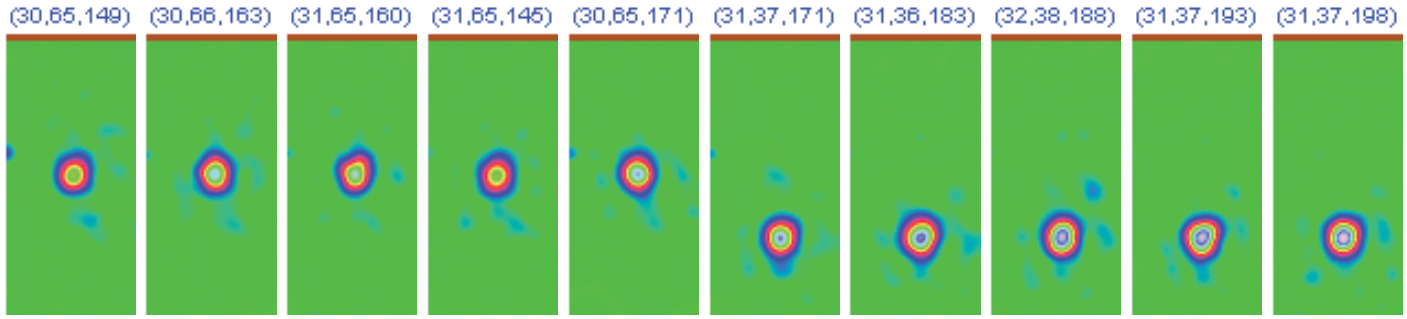
- Ions trapped 80 μm above surface, principal axes rotated 36°, 1 MHz axial and 4 MHz radial frequencies
- DC control: 42 independent control electrodes, controlled by NI DAC cards
- ±10 volts, 500 kHz max rep rate

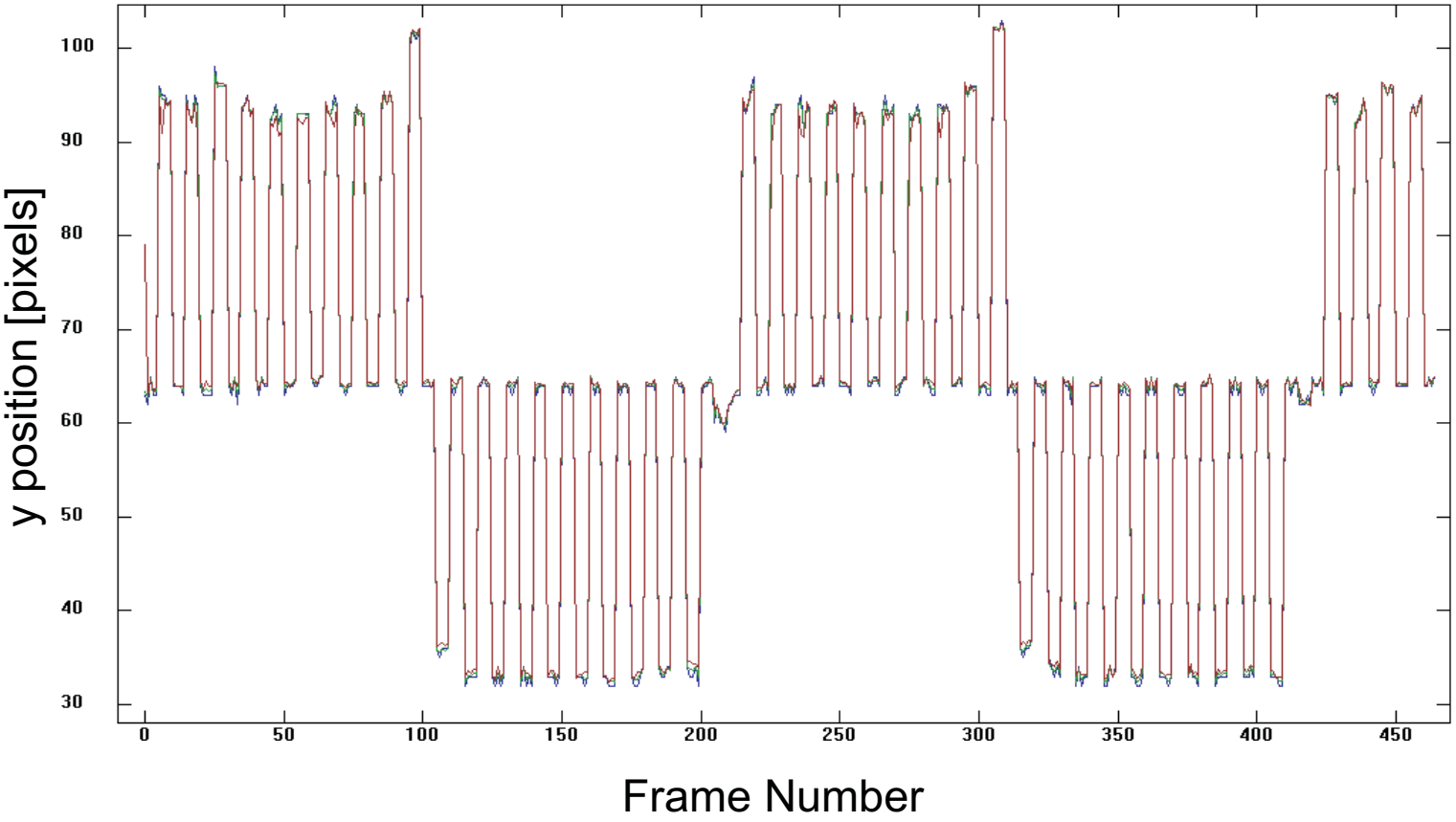
- Shuttled single (multiple) ions across 10 electrodes with $>10^6$ repeat fidelity
- Shuttling speed of 0.75m/s; total travel distance of >1.5 km
- Splitting and recombination of ion chains

- **Trapped and shuttled in *multiple* linear traps, including collaborators, with identical voltage sets!**

Trap operation and testing: Calibration and comparison with simulations

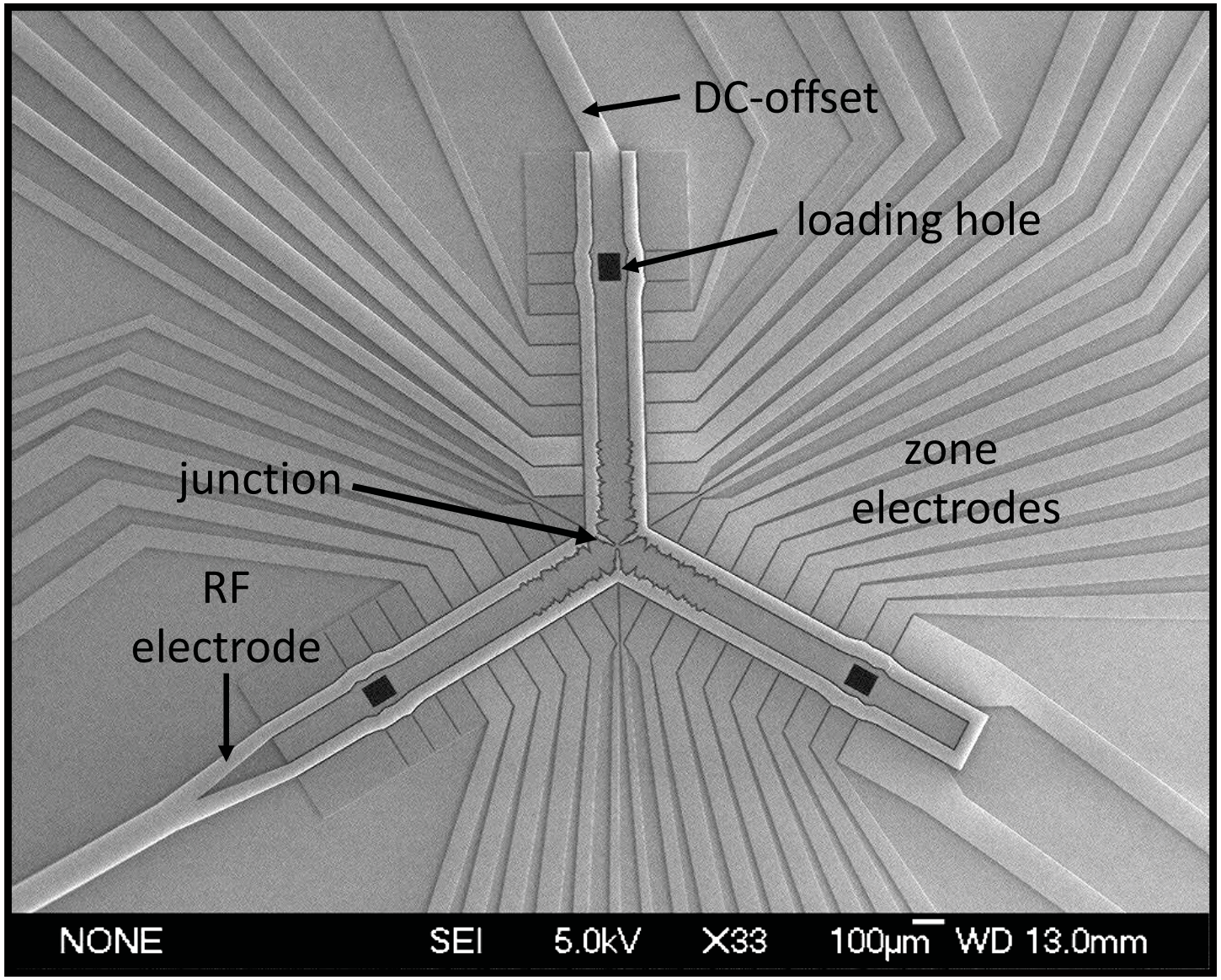
Simulations agree to within 5% of experiment

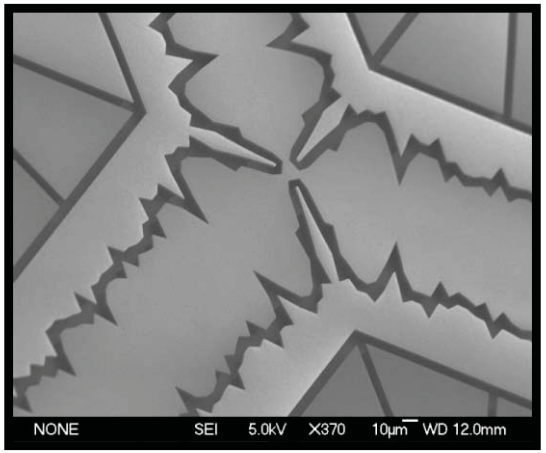


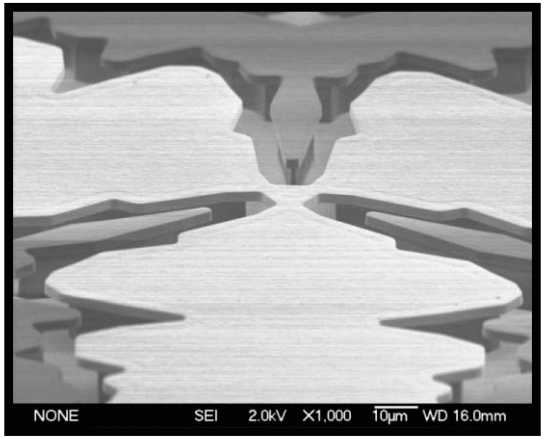


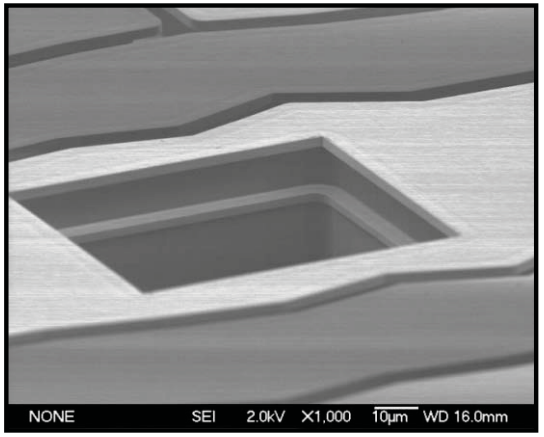
Sandia Ion Trap Foundry: Y-junction surface microtrap

- **Capable of simultaneous trapping of Yb^+ and Ca^+ for studies of sympathetic cooling.**

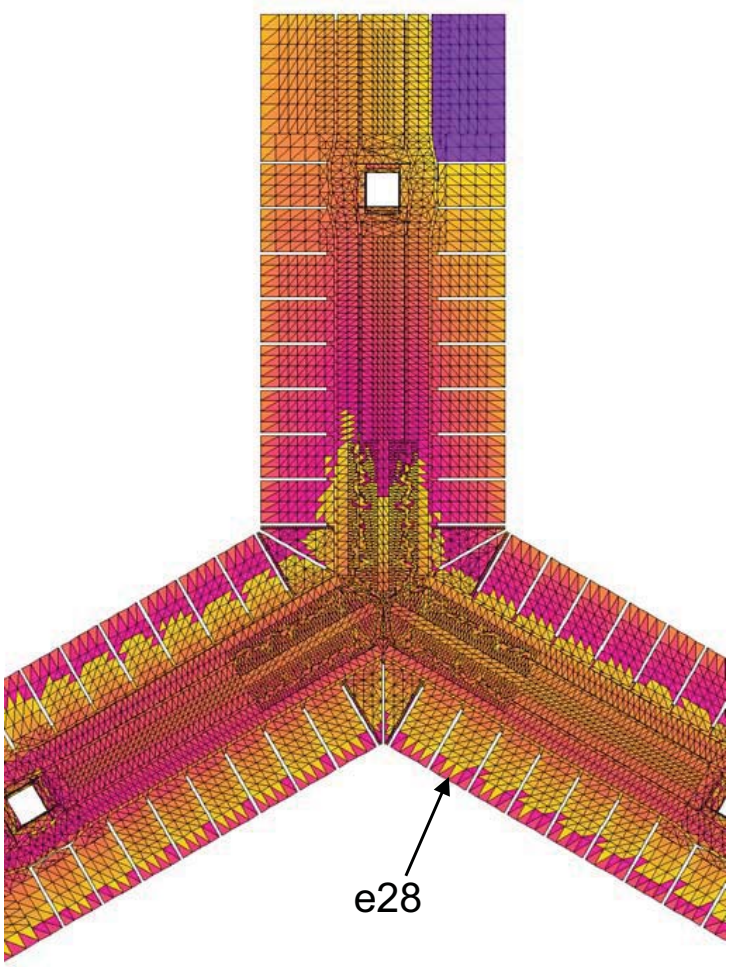




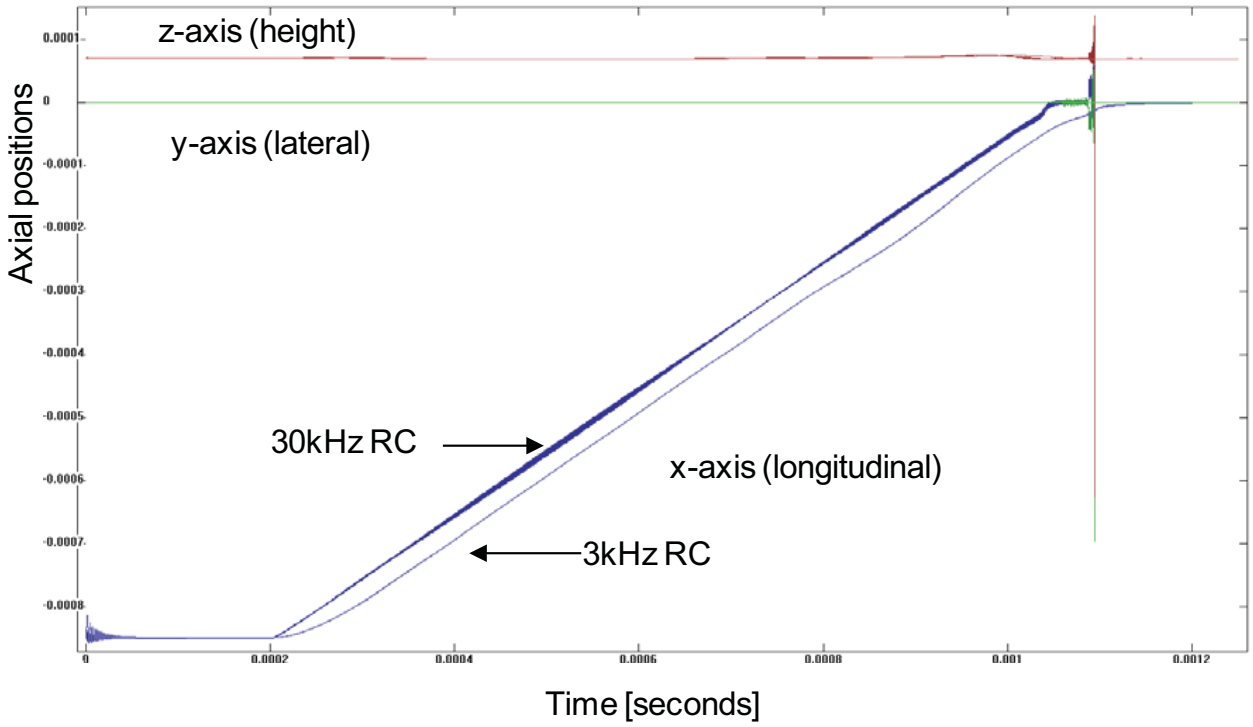




Sandia Ion Trap Foundry: Y-junction surface microtrap - Simulations

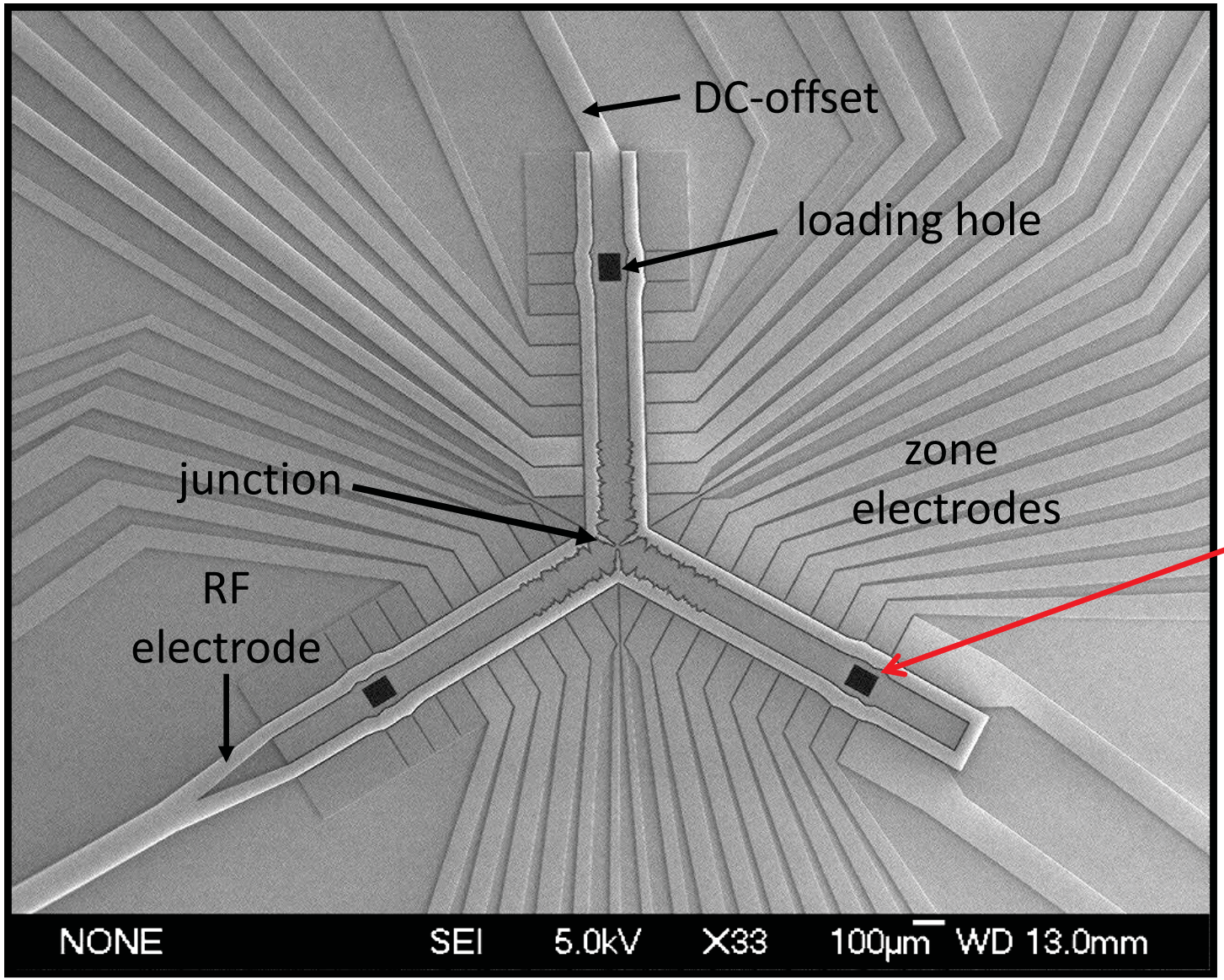


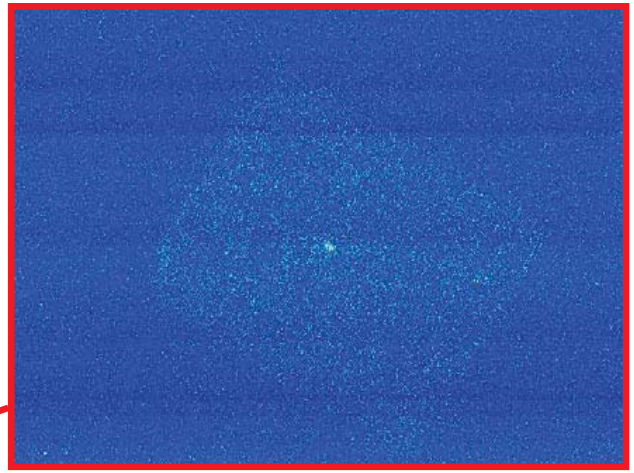
RS816 Y-Junction ion shuttle simulation



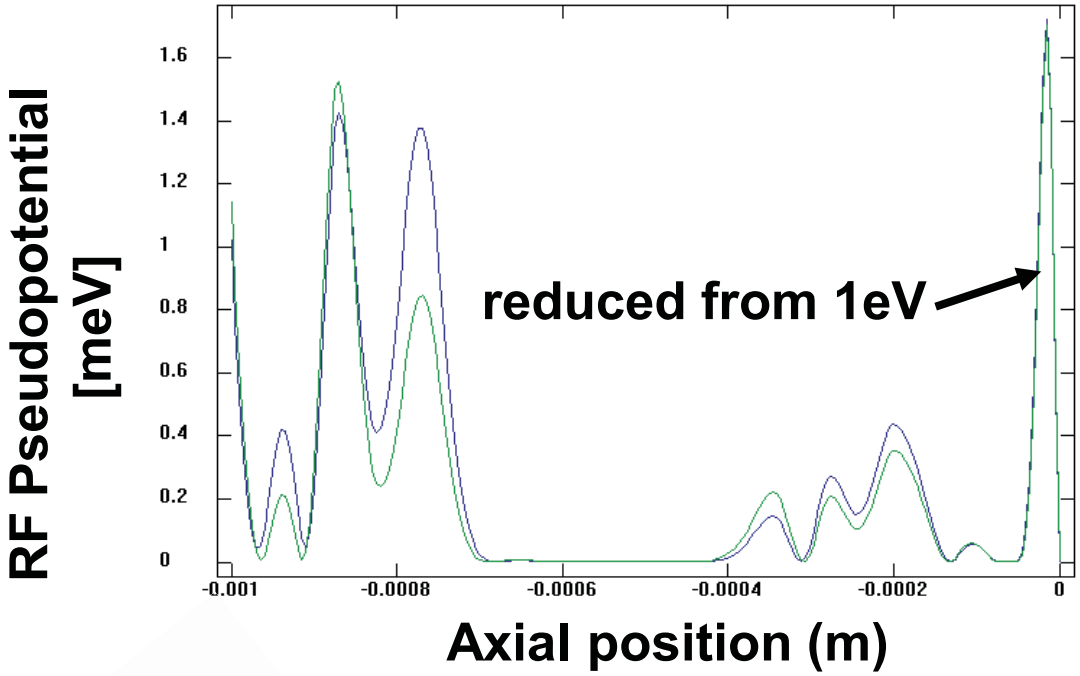
Y-Junction Trap Loading and Shuttling

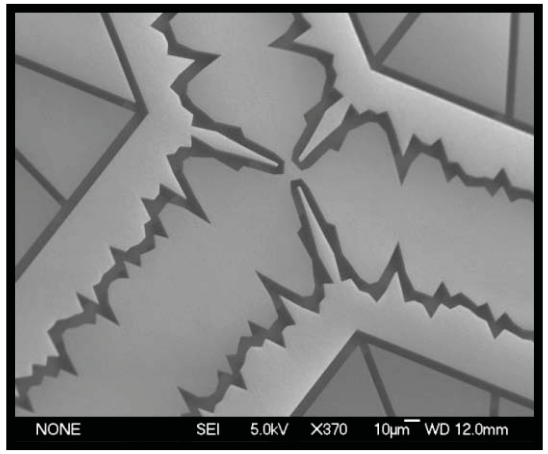
• **Capable of simultaneous trapping of Yb^+ and Ca^+ for studies of sympathetic cooling.**

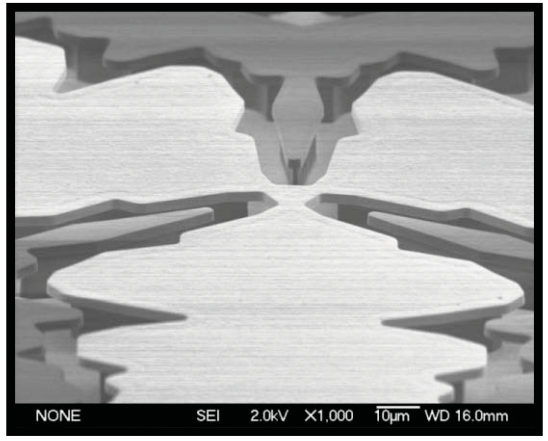


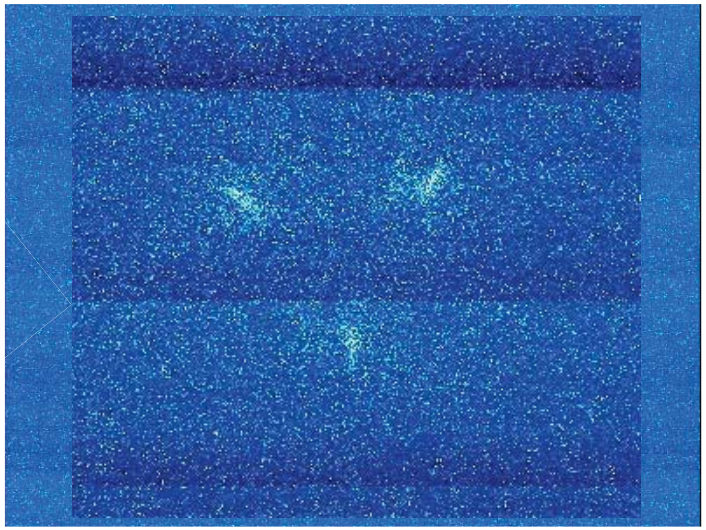


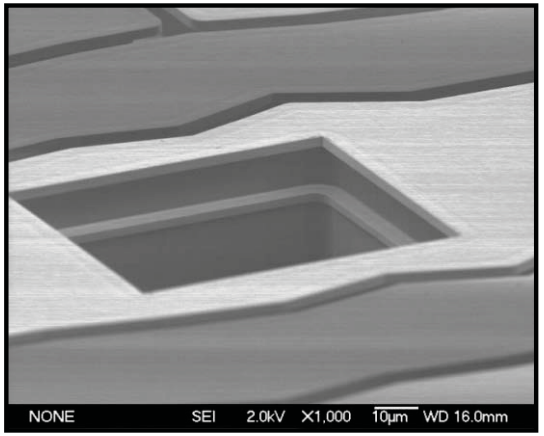
Sandia Ion Trap Foundry: Y-junction surface microtrap



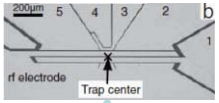


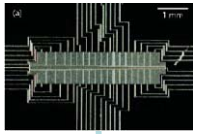




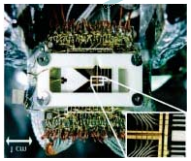


Ion Trapping 101: Planar trap development



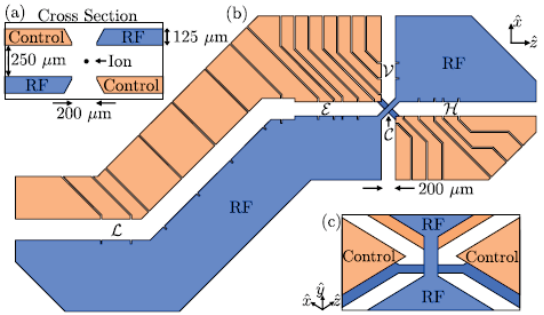


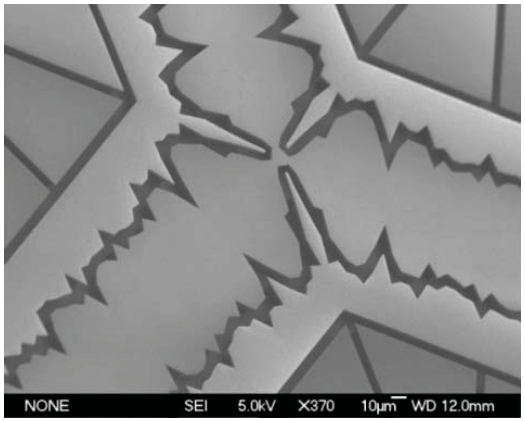
2006



2007

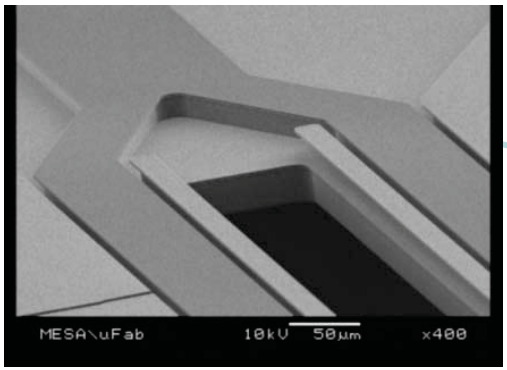
High fidelity junction transport in 2 layer trap at NIST(99.99% success rate)





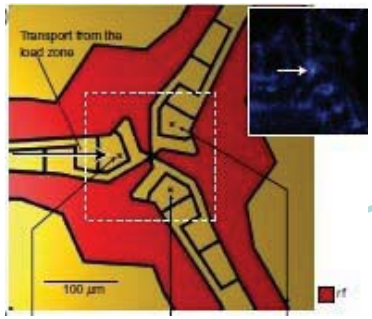
High fidelity junction transport in surface trap at Sandia(99.9999% success rate)

2008



High performance micro-fabricated surface trap demonstrated at Sandia

2009



Successful junction transport in "racetrack" surface trap at NIST

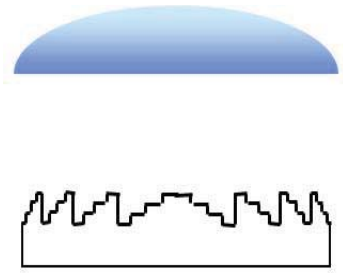
2010

Integrated Optics: Interconnect in fused silica

Why integrate optics?

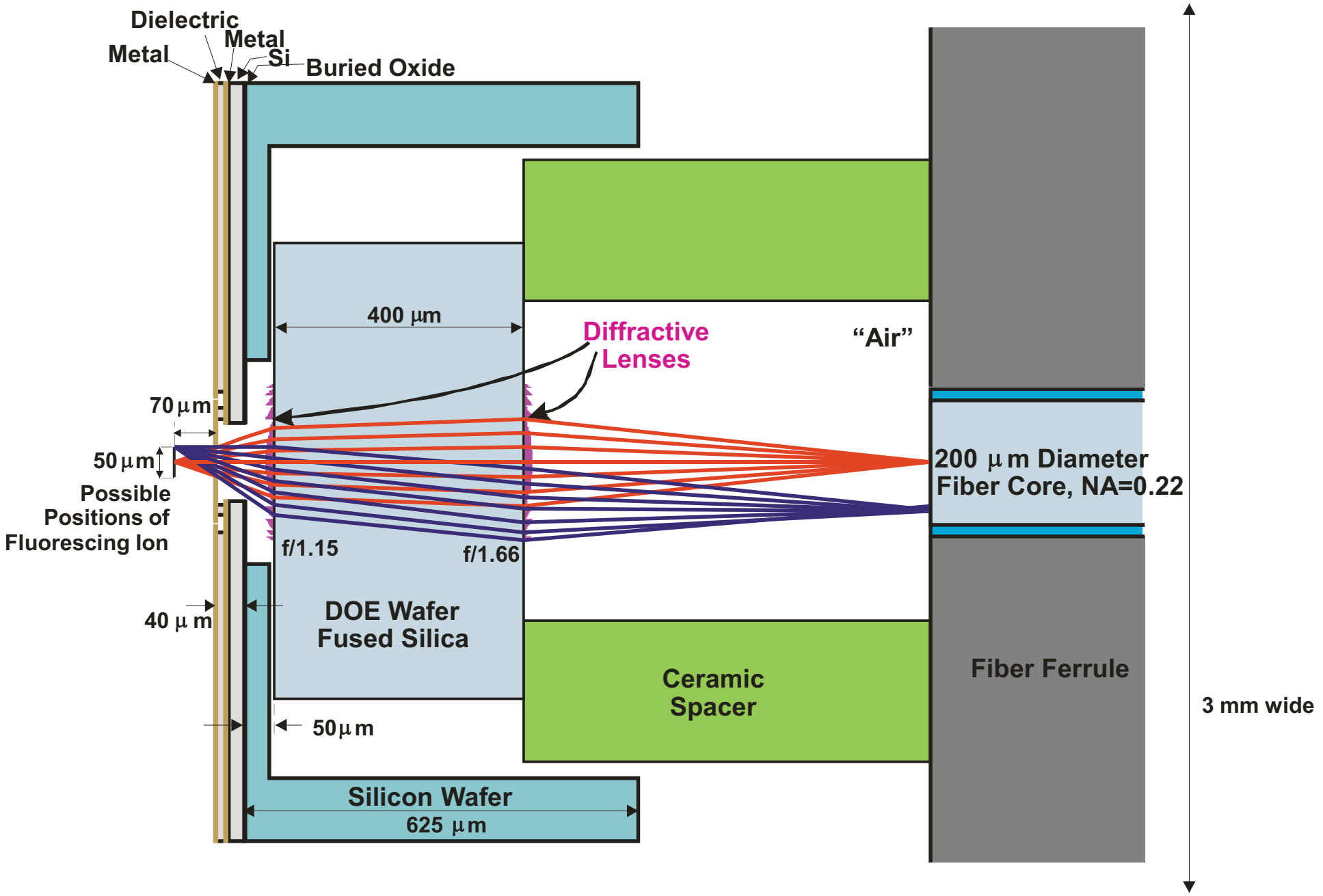
- Can realize transmissive and/or reflective integrated optics
- Because of off-axis capability, can pack lenses densely and with 100% fill factor
- Lens focus need not be a point, can be a volume to accommodate ion motion or integration tolerance

Optical microscope bird's-eye view of a DOE array that Sandia designed and fabricated for cascaded optical computing.

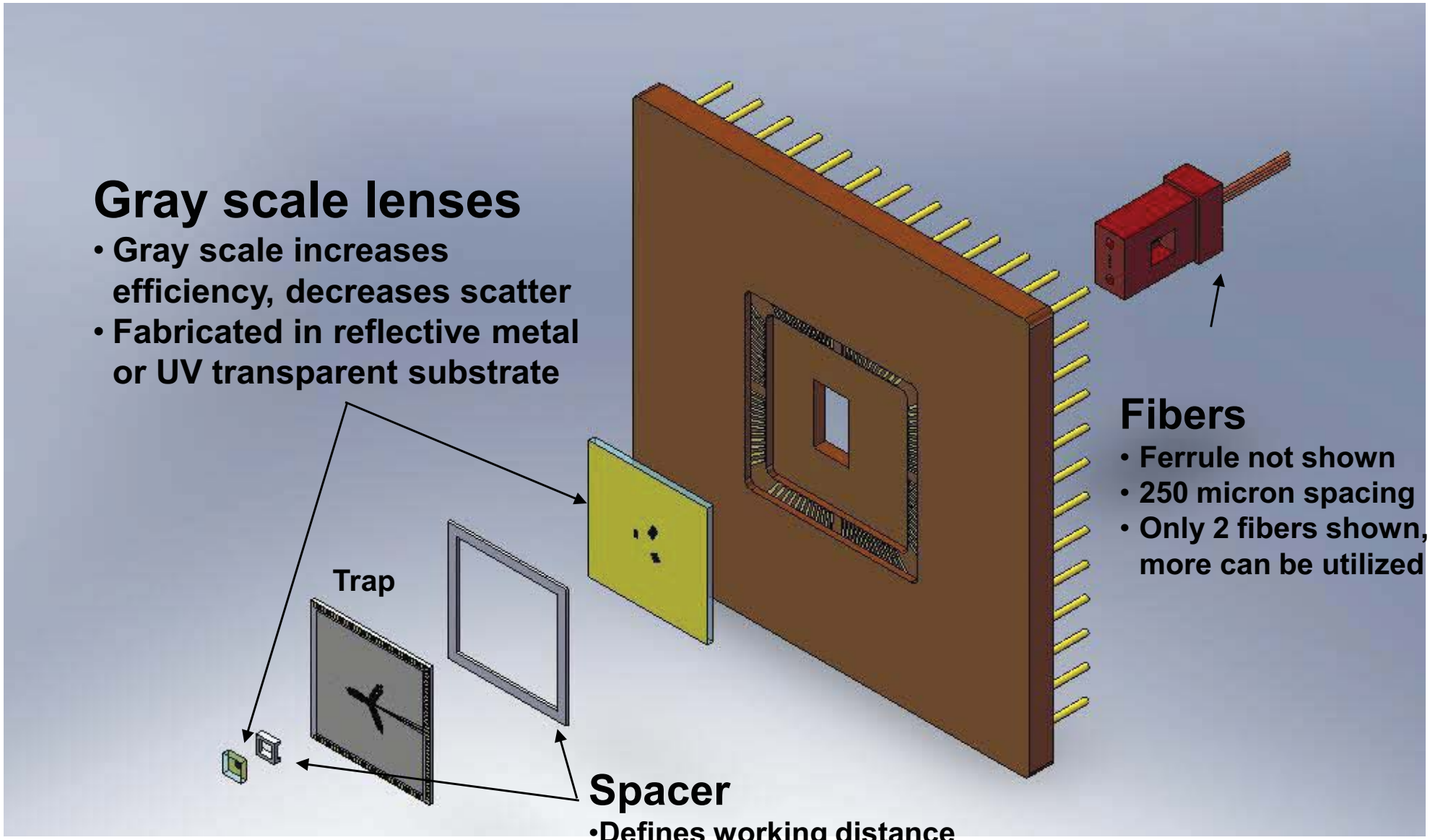


Scanning electron micrograph (SEM) of a portion of the 100% fill-factor optical interconnect array in fused silica, fabricated at Sandia.

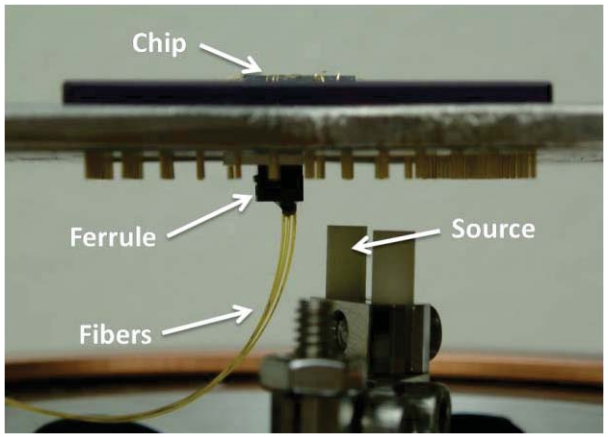
Integrated Optics: Interconnect in fused silica

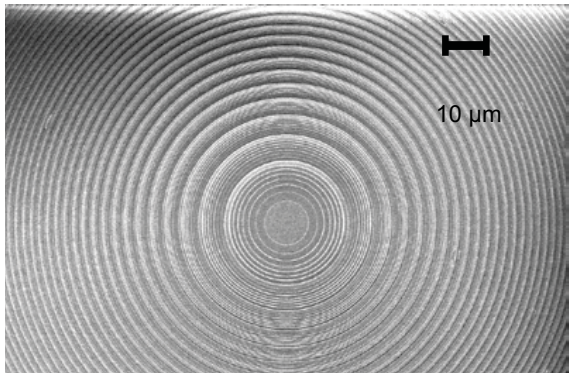


Integrated Optics: Interconnect in fused silica

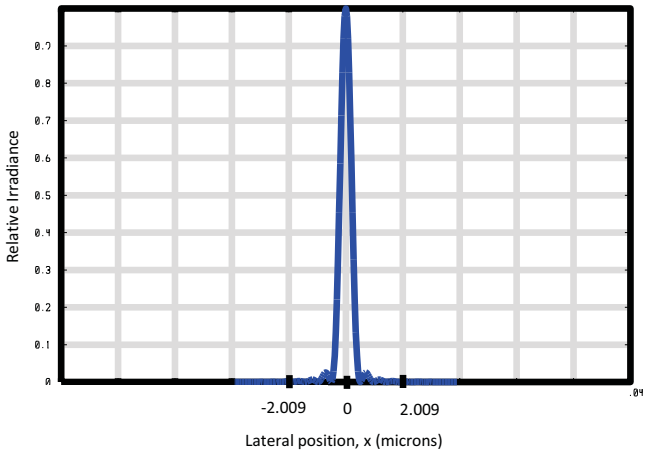


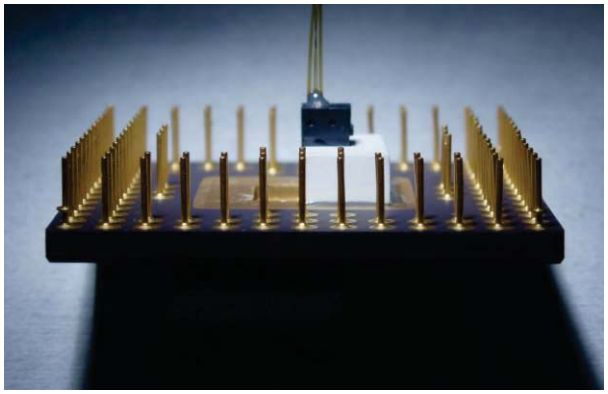
Integrated Optics: Interconnect in fused silica

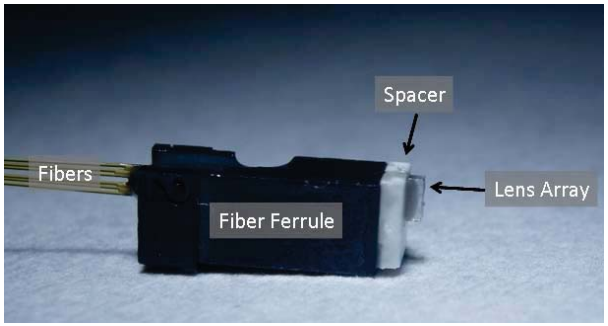


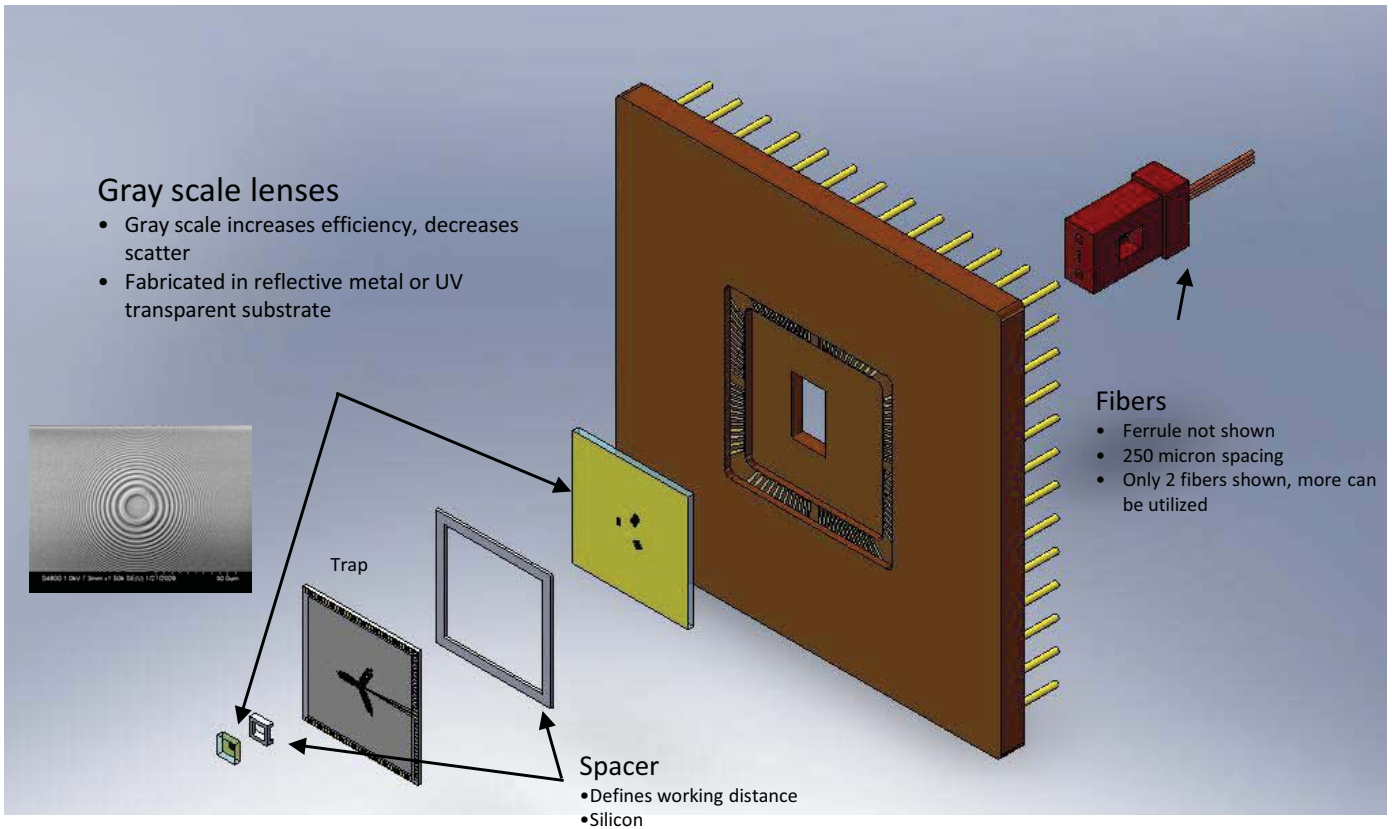


Eight level F/1 fused silica DOE



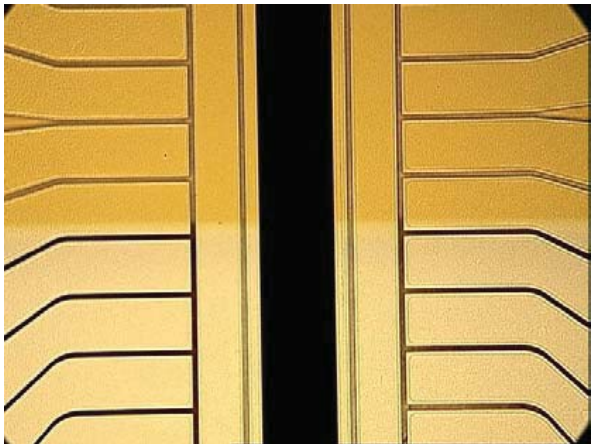






- No line-of-sight between trapped ion and dielectrics
- Loading zones isolated from experiment zones
- Fast ion loading
- Hours-long cooled lifetime
- High fidelity linear and junction shuttling (99.9999%)
- Reliable splitting of ion chains
- Integrated optics without detrimental effects

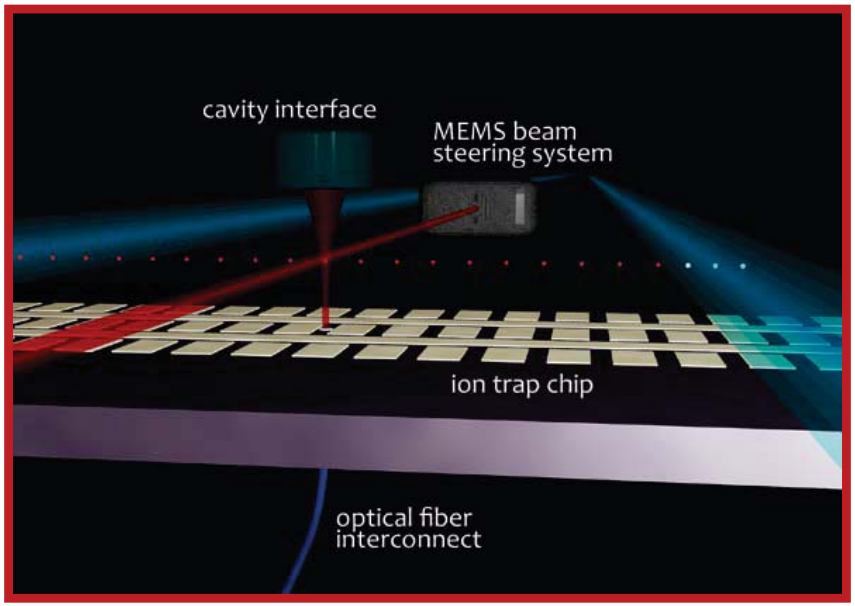
- Still to demonstrate
  - Measure heating rates of trapped and shuttled ions
  - Compare heating rates for different trap electrodes



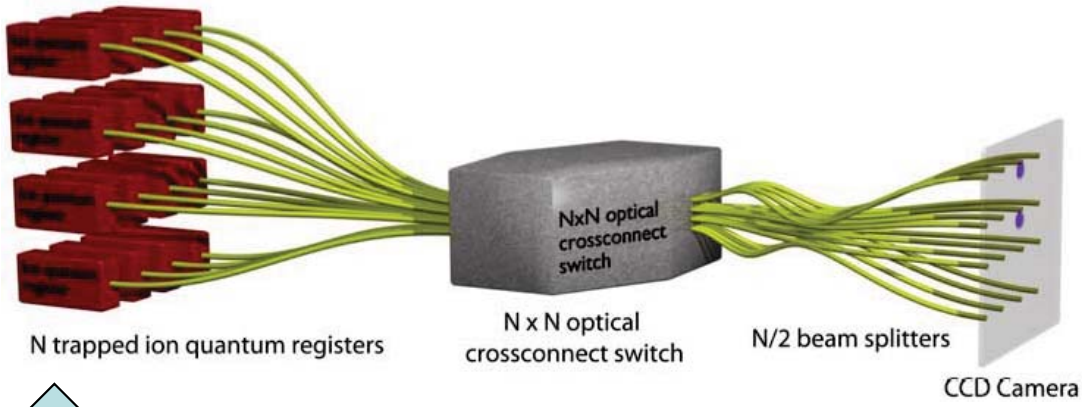
What's next? MQCO MUSIQC Program

Duke University · University of Maryland · Michigan · W · Georgia Tech · UBC · MagiQ

Georgia Tech Research Institute · IARPA · Army Research Office · Sandia National Laboratories



m ~ 10-100 qubits / ELU



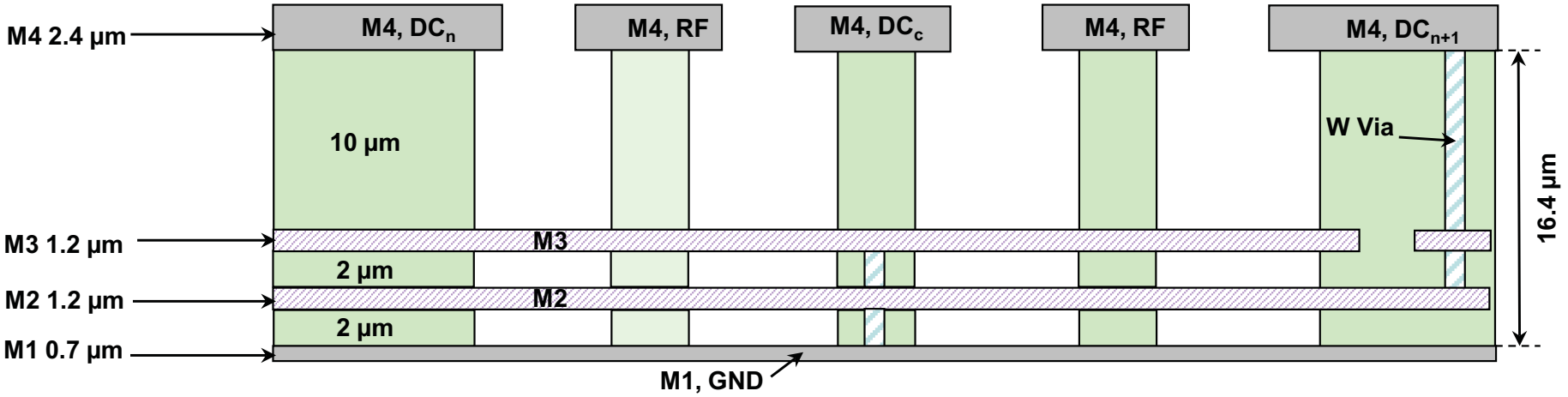
Up to *mN* qubits in a QC

Monroe, Kim and Duan (2009)
Luo et al., arxiv:0906.1032 (2009)

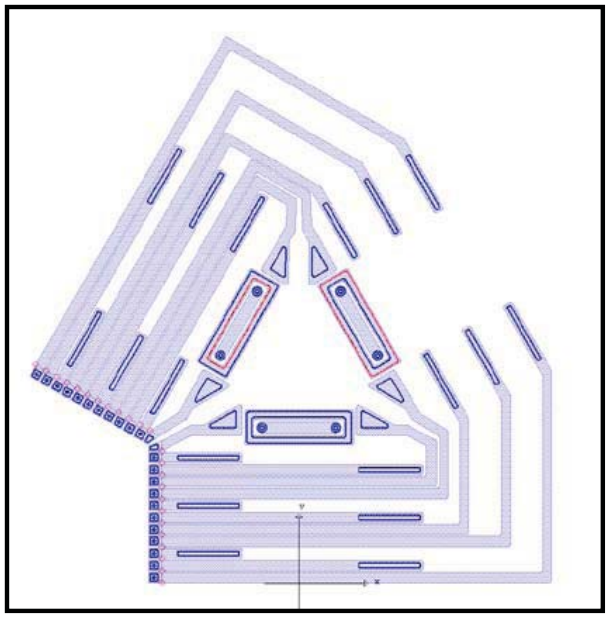
What's next? Multi-level process for electrode crossovers

Routing of RF and Crossing of DC electrodes is required away from trapping regions

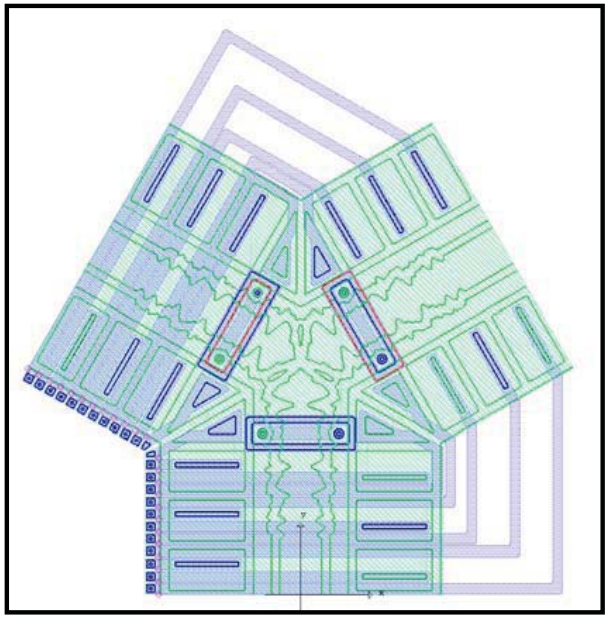
- **DC lead crossings below M4 electrode level and above M1 ground**
- **RF routing occurs in micro-stripline configuration with RF on M4; M4-M3 separation maximized**



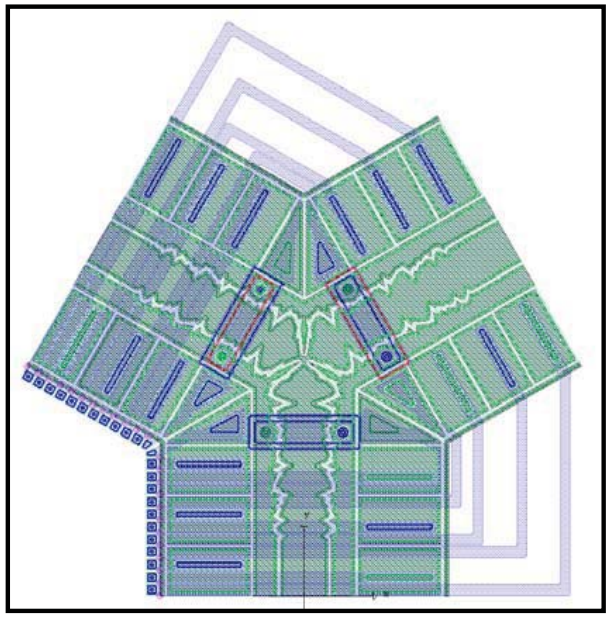
M2



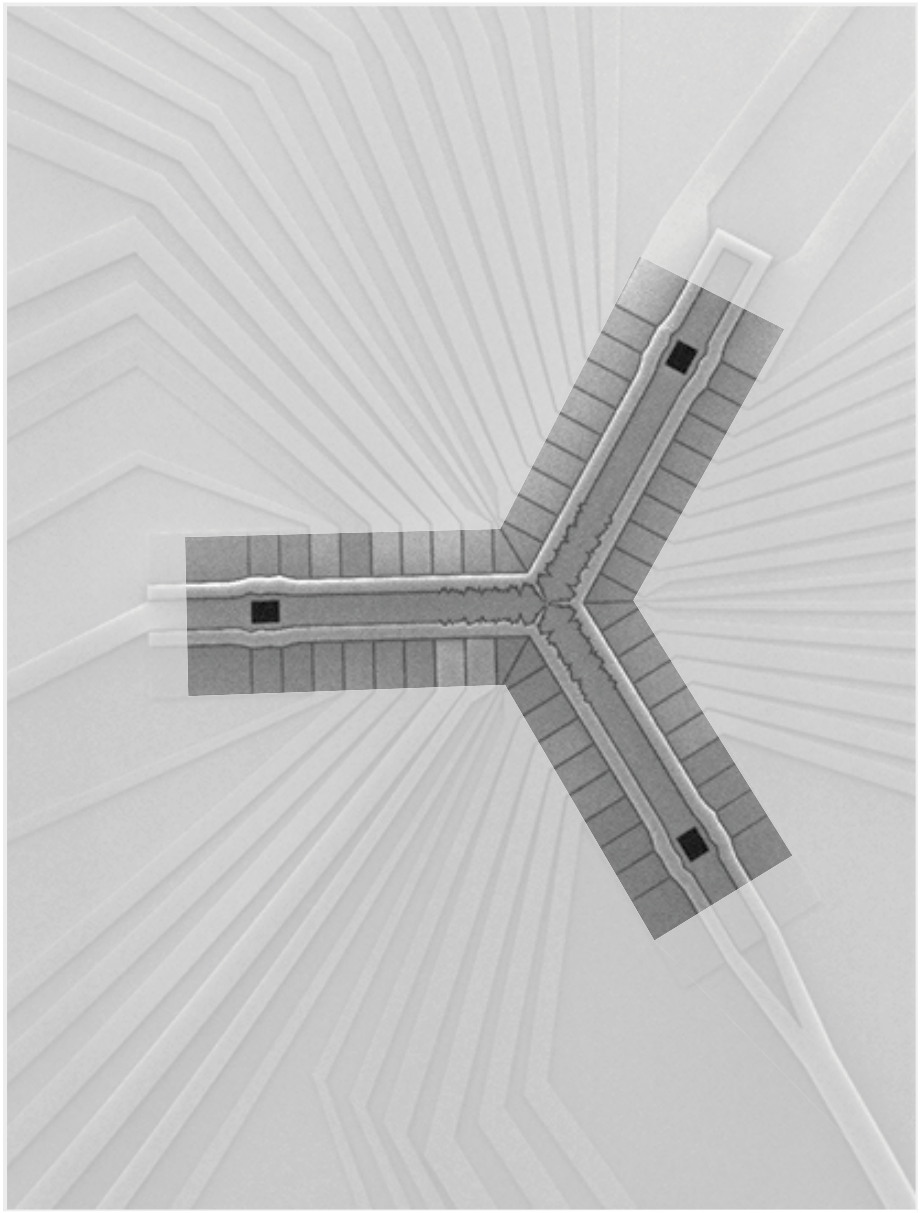
M2 + M3

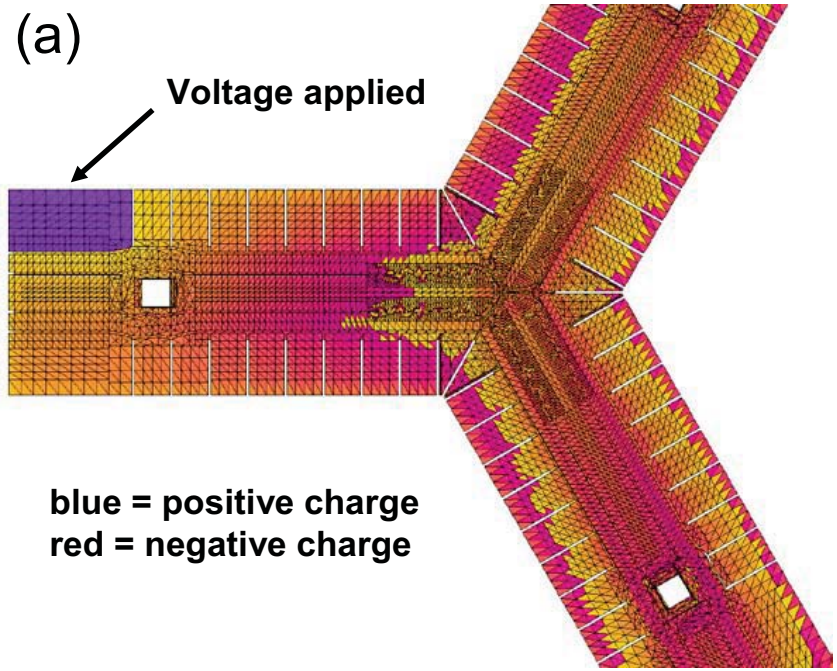


M2 + M3 + M4

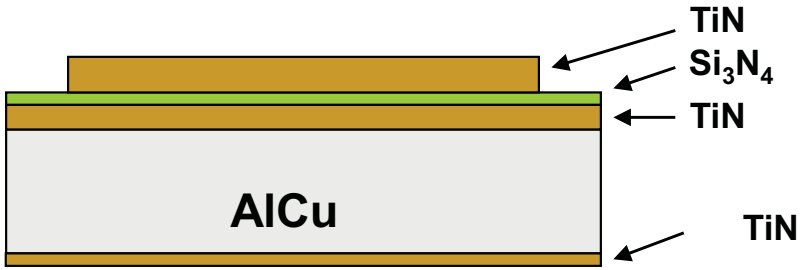


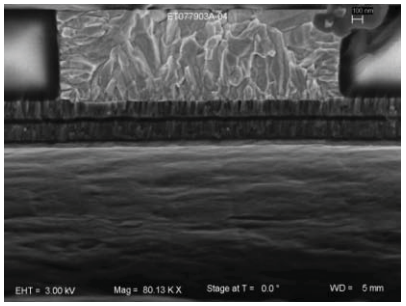
Next generation Y-junction & Improved modelling

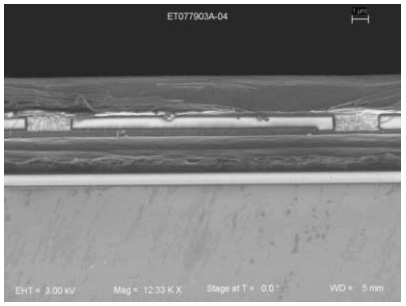




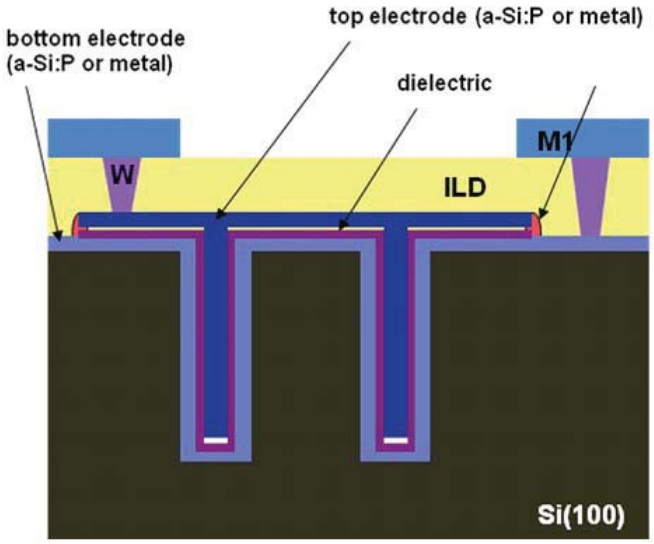
Metal Insulator Metal Capacitors

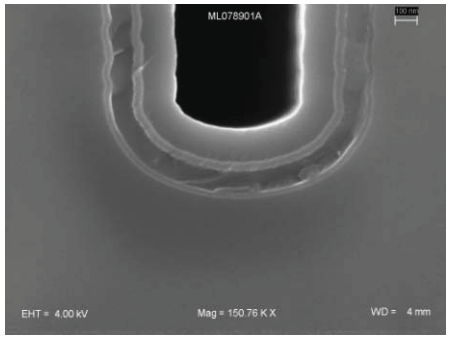


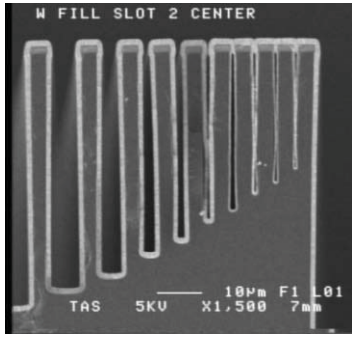




Trench Capacitors





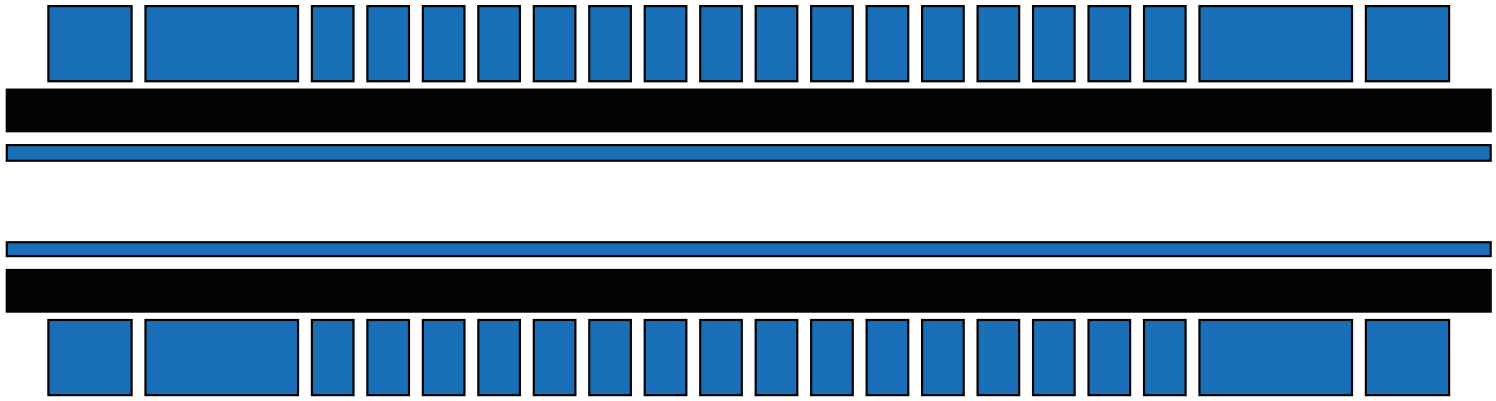


Pros and Cons

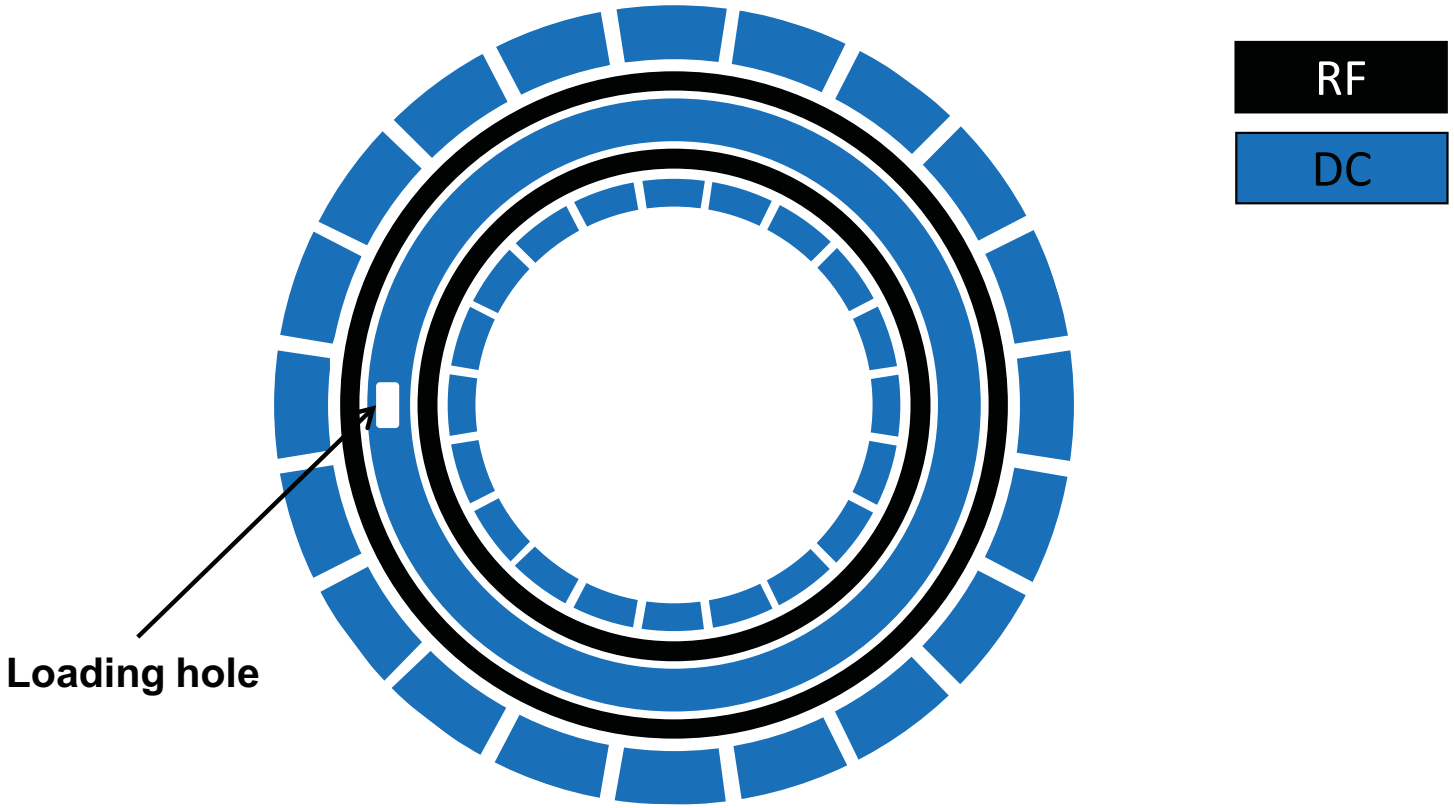
- Higher capacitance density for trench capacitors (94.3 fF/μm^2 vs. 1.3 fF/μm^2)
- Possible RF loss in Silicon in trench capacitors

Sandia Ion Trap Foundry: “Ring trap”

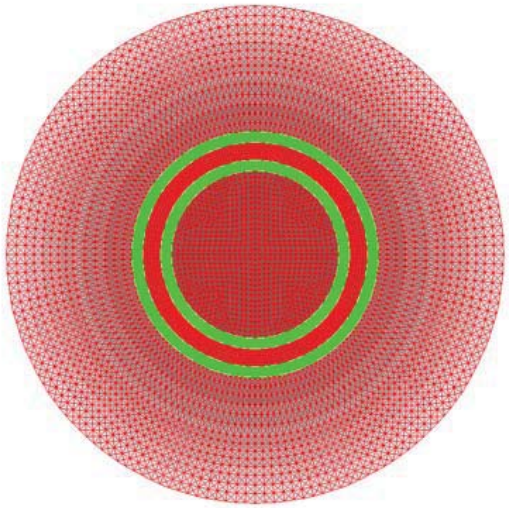
Current linear trap:



Proposed ring-shaped trap:



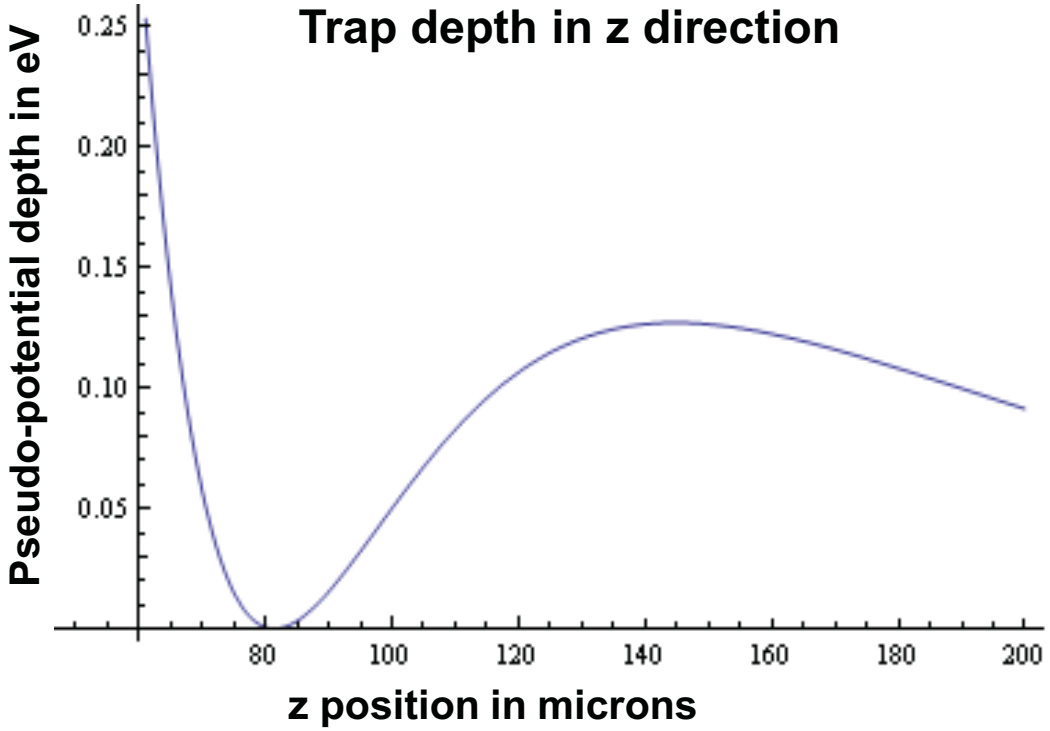
Sandia Ion Trap Foundry: "Ring trap"



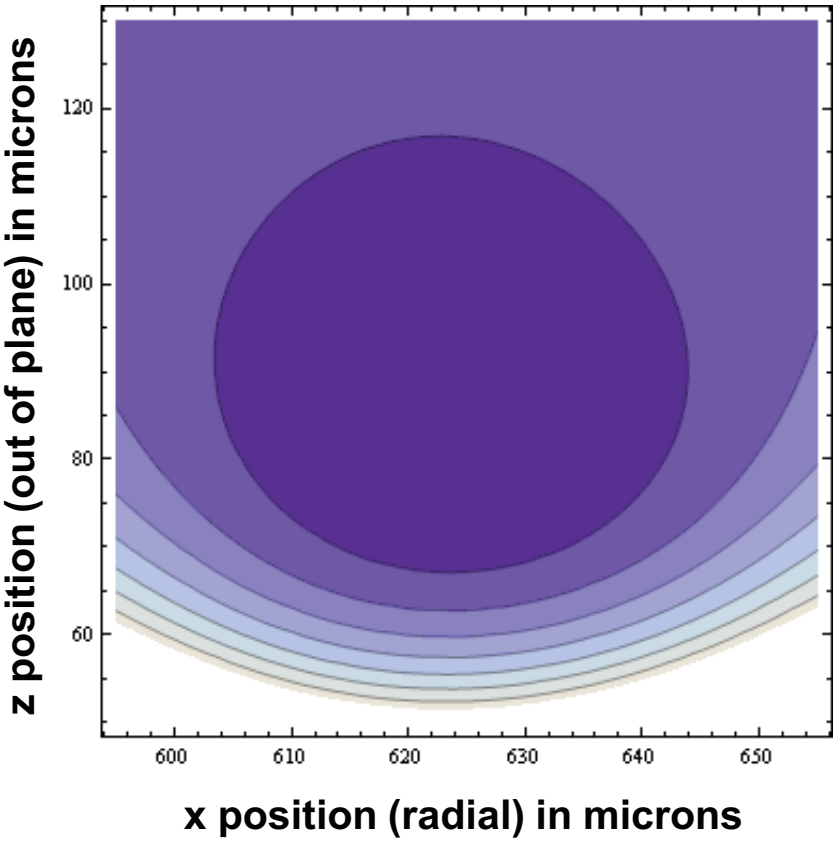
Simulation in CPO using:

- Mass of barium
- RF drive frequency of 40 MHz, 300 V amplitude
- 0.13 eV radial depth, 3.2 MHz radial frequency
- 624 micron radius ring of ions
- 60 micron wide RF electrodes, 100 micron separation

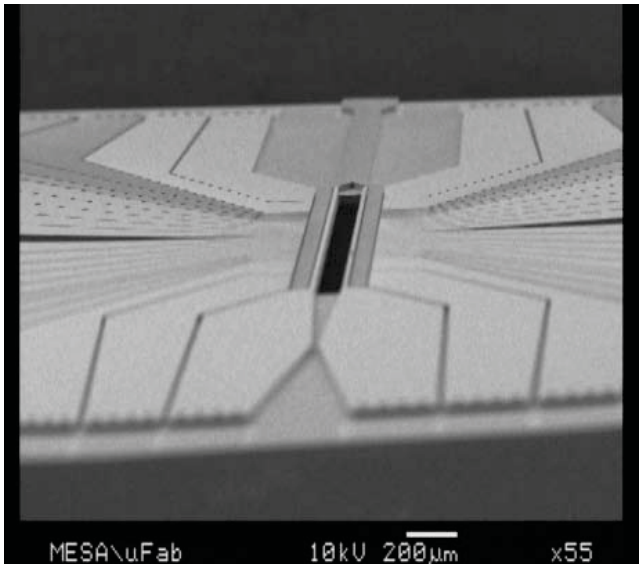
Trap depth in z direction

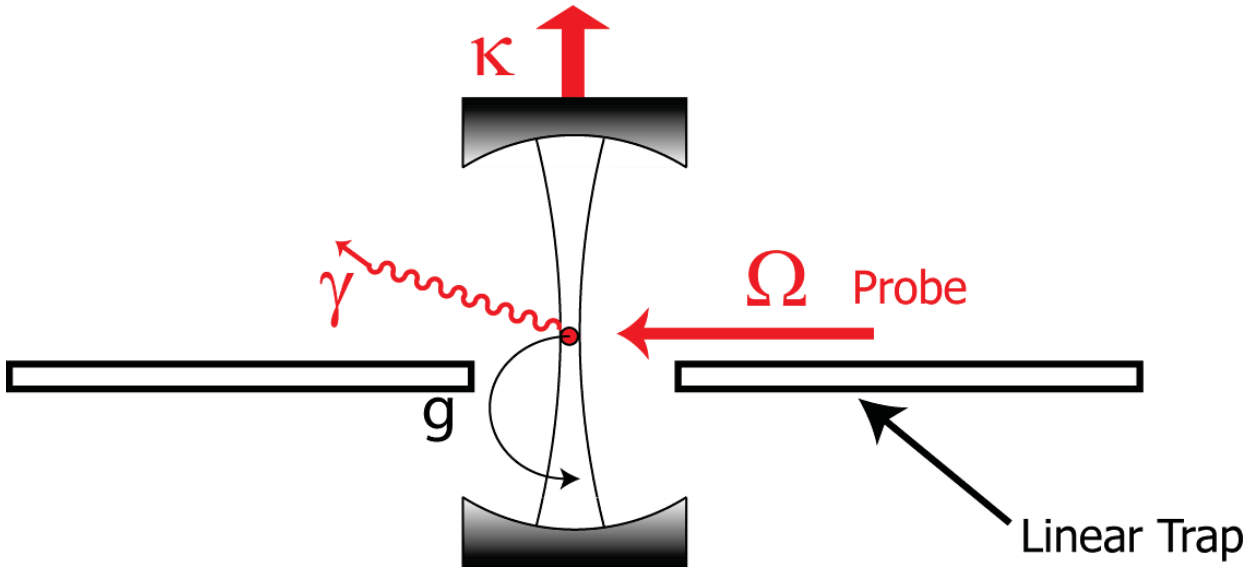


Contour plot of rf pseudo-potential



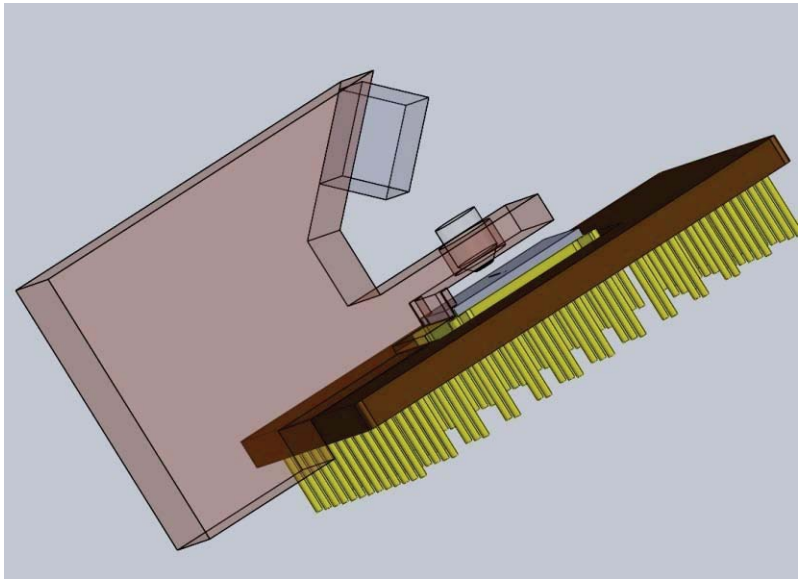
Ion-Cavity System: Task 2.5 Concept of operation



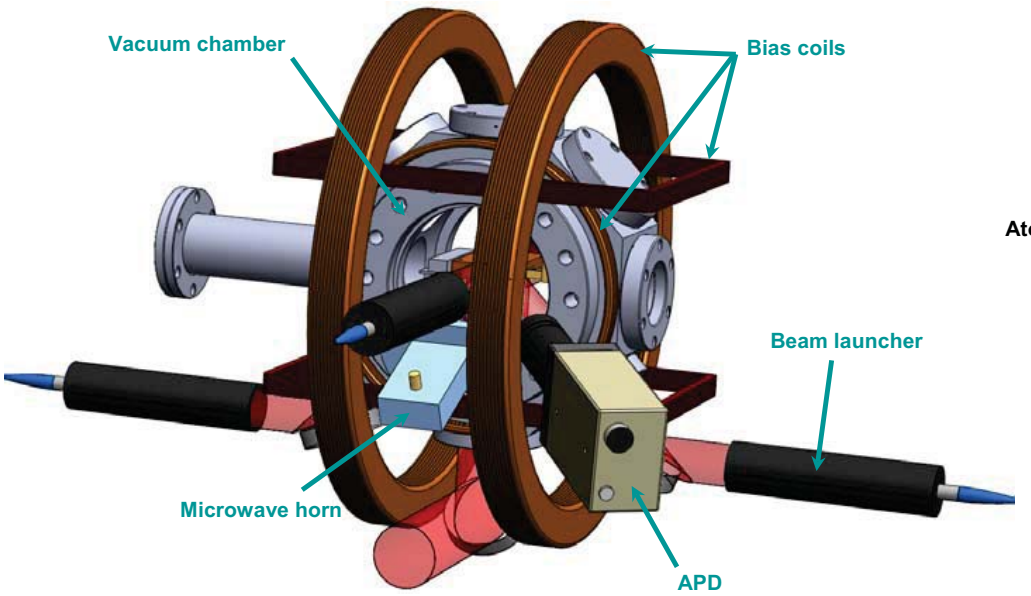


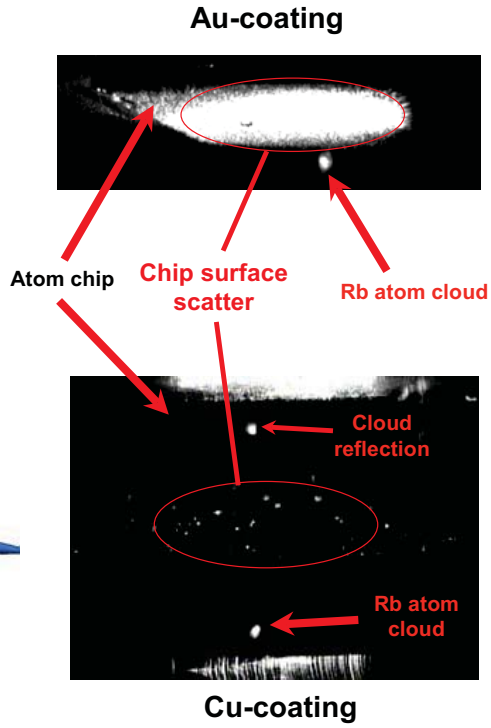
- Use linear trap for cavity integration
- Existing loading slot provides optical access for cavity beam.
- Initial cavity will use 5 mm RoC mirrors, L ~ 2.0 mm with F > 3,000

- Optics already integrated into linear trap with minimal effect on ion.
  - See poster

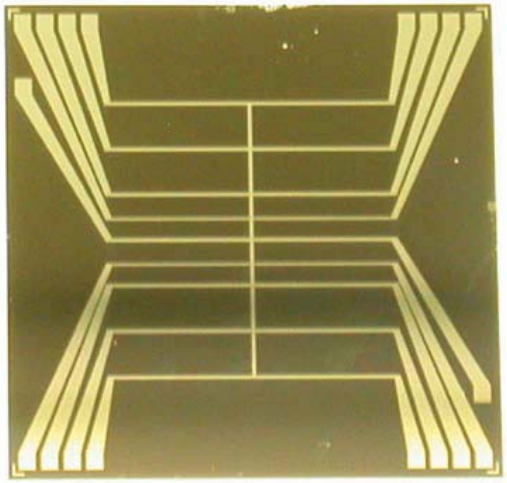


Other AMO work at Sandia: Atom chip conductors





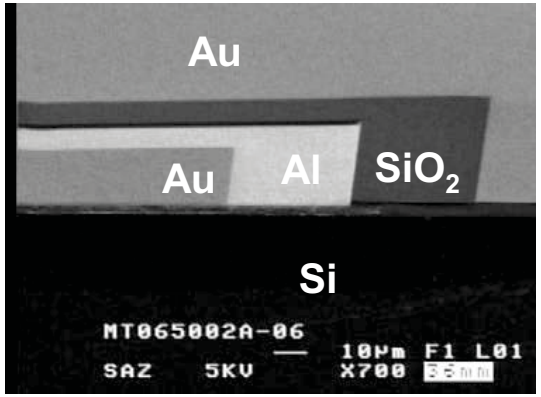
Prior to SiO_2 and Au coating
Caltech conductor pattern



CW performance of Al wires

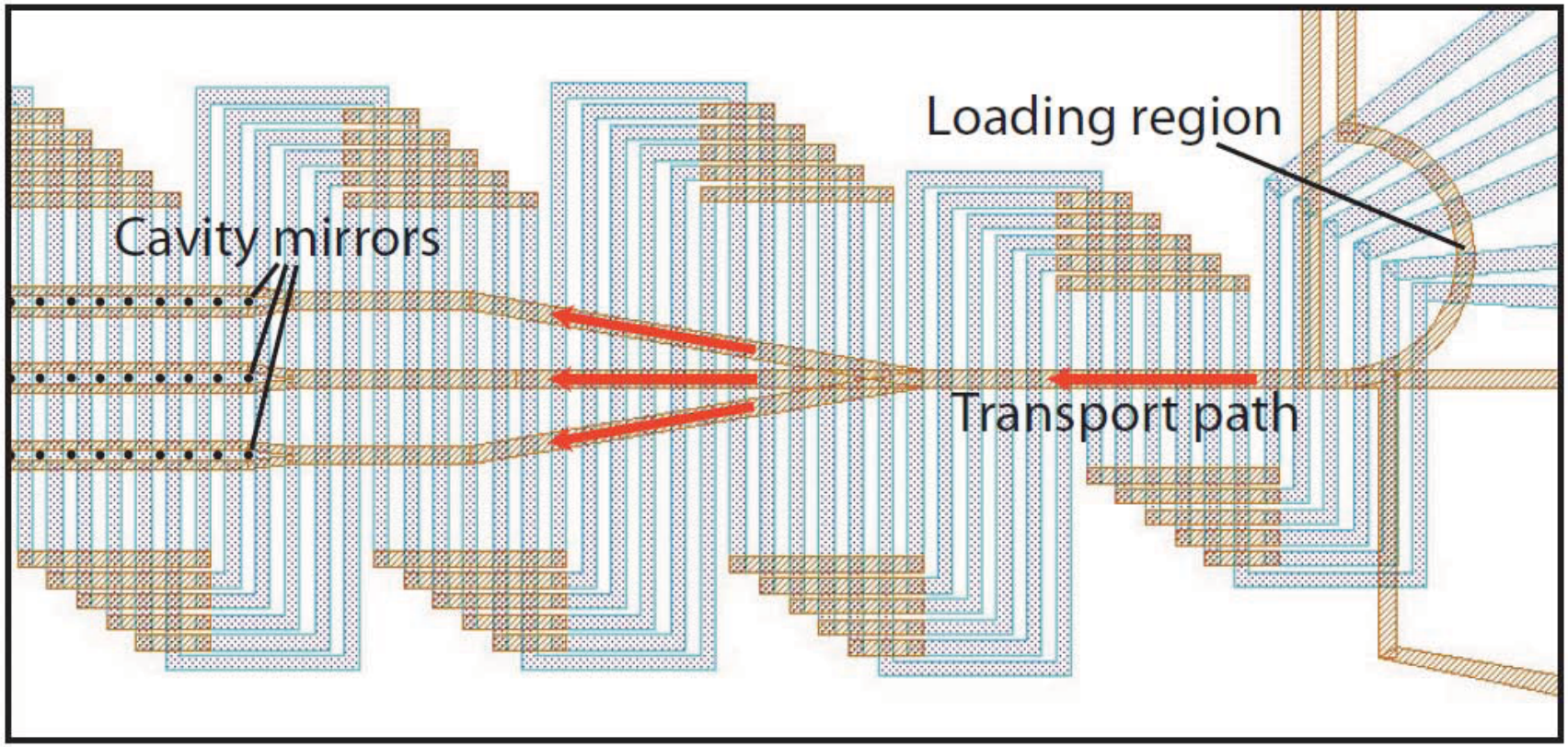
Failure Current	**2.5 A**
Current Density	**1×10^{10} A/m^2**

Cross section of the atom chip across an I/O bonding pad



Atom cavity chip design with integrated mirrors and two metal conductor layers

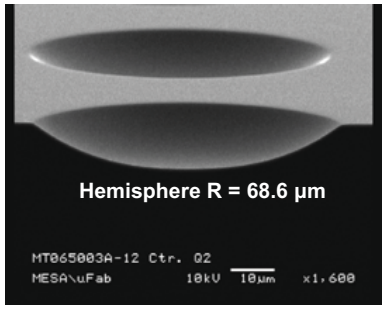
Collaboration with Andrew Geraci at NIST

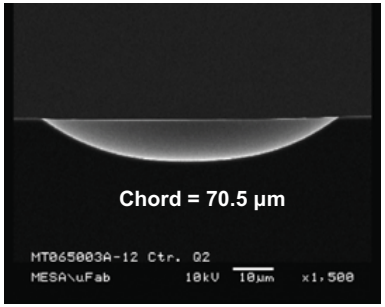


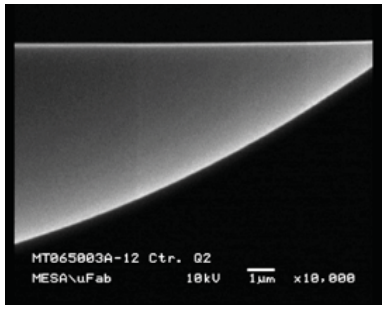
- Two conductor layers in a single chip
- Integrated cavity mirrors
- Redundant cavity array design
- Magnetic conveyor - R. Long, et al, *European Physical Journal D*, 35, 125 (2005)

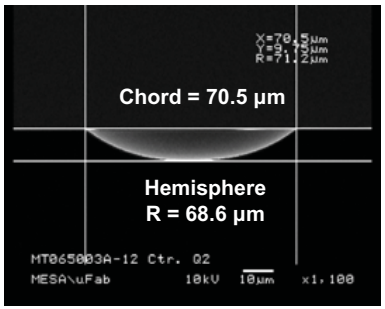
Other AMO work at Sandia: Engineering high finesse micro optical cavities

1 μm SiO_2 aperture, 60 min F^* chemical downstream etch, 100 μm SF_6 plasma smoothing, 2 μm oxidation + strip





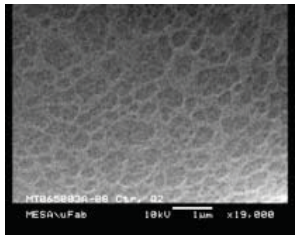




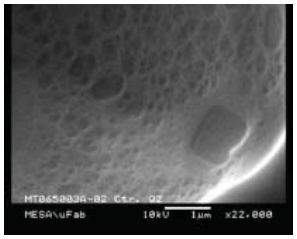
Silicon substrate type

Before plasma etch
1 μm SiO_2 aperture

High resistivity Si



Low resitivity Si



Optimized fabrication parameters give smooth micro-optical cavity templates

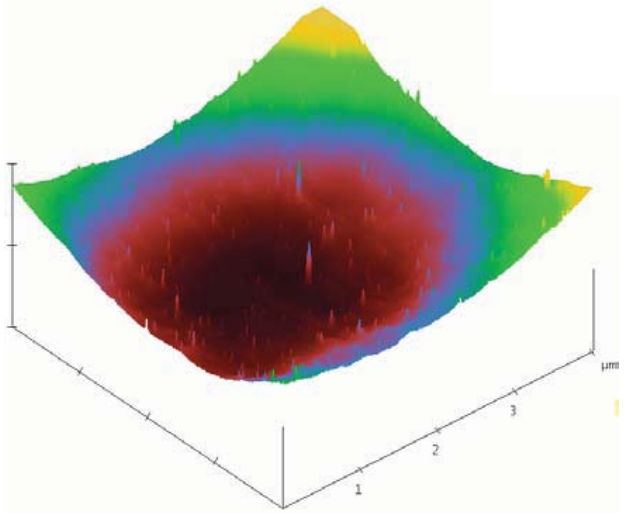
Scattering loss versus surface roughness

AFM measurements at cavity bottom

Units: nm_{rms}; 1 μm SiO_2 aperture

Wafer	1st plasma etch	2nd plasma etch	Oxidation	Anneal	Wet etch
1	1.13	0.67	-	-	0.30 cavity 0.30 field
2	0.98	0.62	0.55	0.48 well 0.66 field	0.46 cavity 0.58 field
3	0.94	0.85	0.48	Yes	0.216 cavity 0.218 field

Post 1st plasma etch
AFM scan, Sample 1



- Yb^+ ion trapping for atomic clocks
- Trapping of individual neutral atoms for QIP
- Neutral atoms for sensing applications
  - Gravitometry
  - Magnetometry

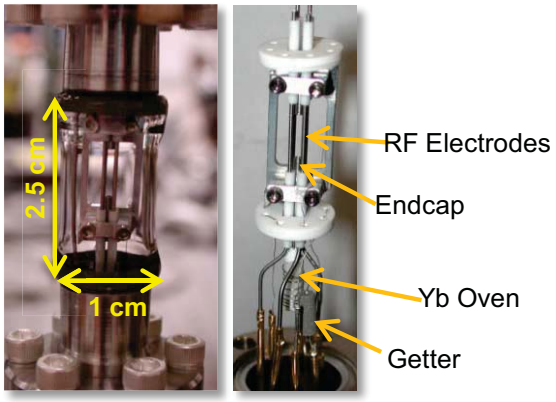


Photo of the small-volume trap made from commercial parts, shown inside the glass metal adapter and before putting inside the vacuum