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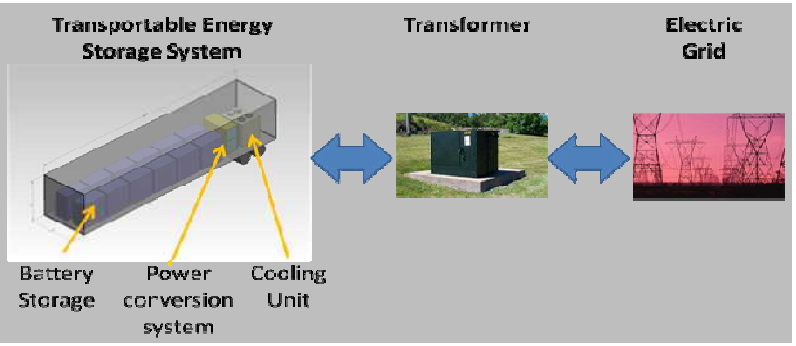

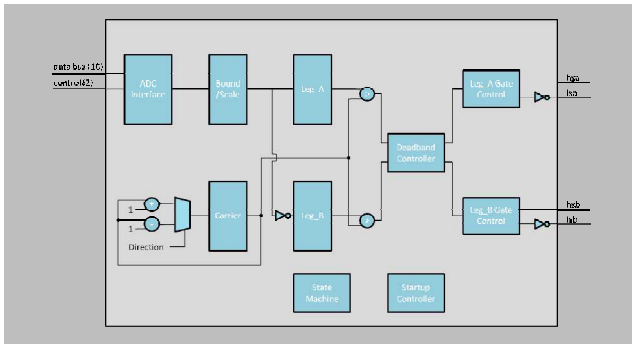

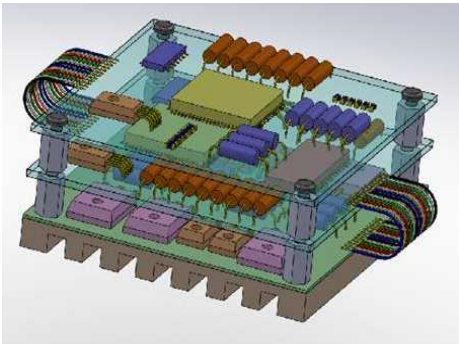

Enhanced High Temperature Power Controller

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U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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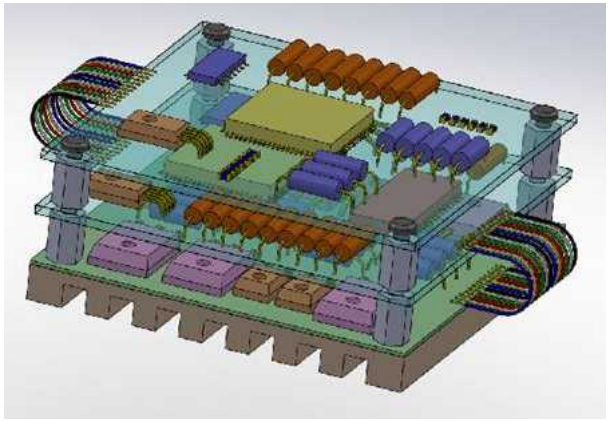
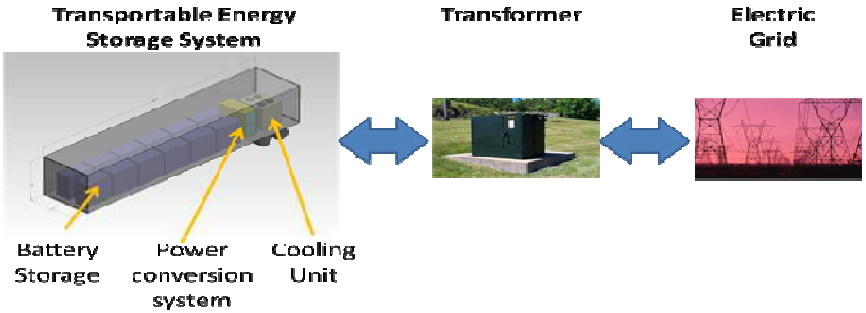
Overview

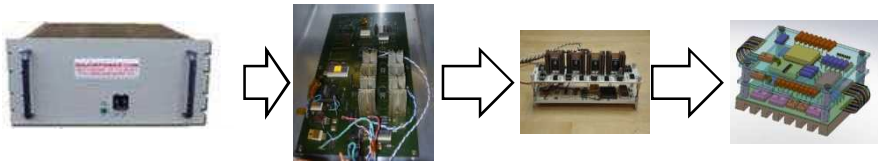
- Background
  - Project Mission
  - PWM Theory
- FPGA Design
  - Component Specifications
  - Design Requirements/Layout
  - Architecture
- Simulation and Testing
- Closing Remarks



Project Mission



- Increase power density and reduce cooling costs of power conversion system
- Design inverter using high temperature electronics to operate up to 240^{o}C
- Minimize space needed for inverter



Industrial Inverter 3325 in.^{3}

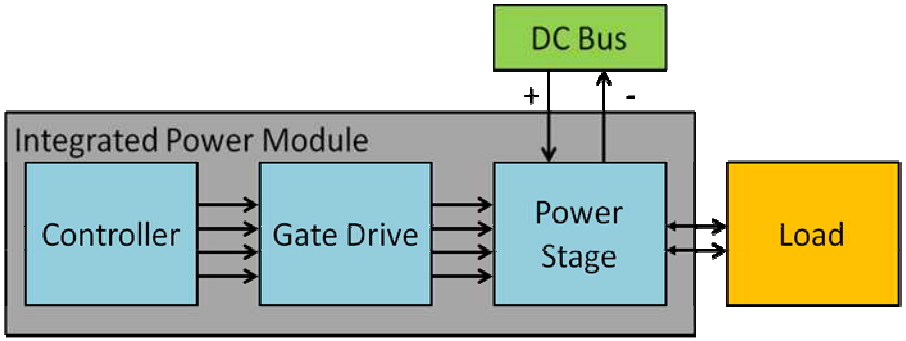
Phase I Inverter 263 in.^{3}

Phase II Inverter 82 in.^{3}

Phase III Inverter 40 in.^{3} Concept

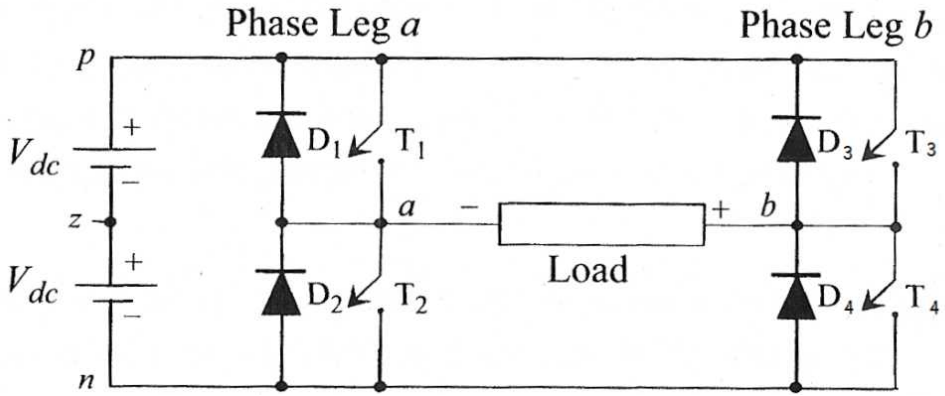
Power Controller

- Development of components being performed simultaneously
- Focus of this presentation is the controller design



PWM Theory (1 of 2)

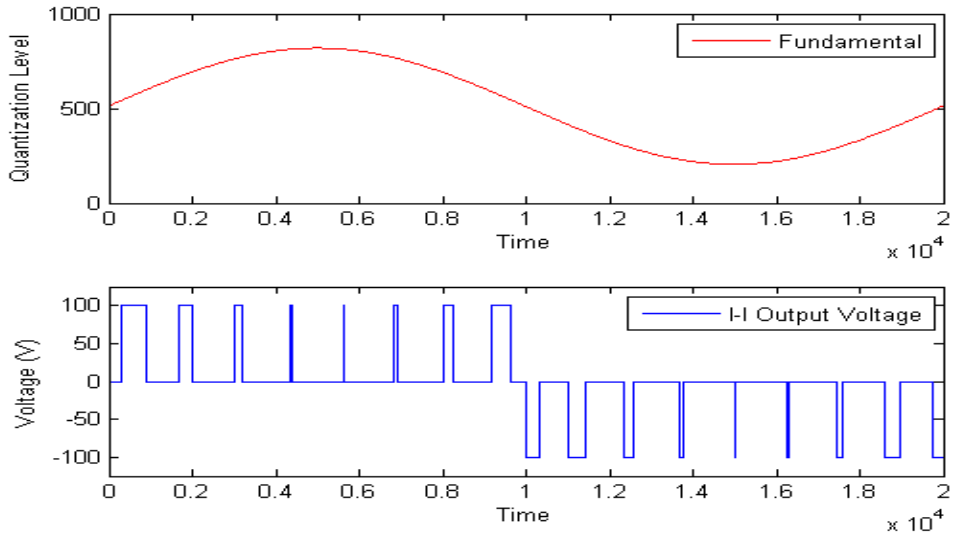
- Voltage Source Inverter (VSI)



- PWM
  - Three-level naturally sampled sine triangle method

PWM Theory (2 of 2)

- Fundamental Reference
- Carrier
- PWM Output
- Dual Leg Switching
- Three-level l-l Output



Component Specifications

- HT Devices severely limit component selection
  - HT devices are qualified to operate at 225°C for 5 years by the manufacturer
  - Many continue to work up to 300°C with reduced lifetime and performance
- HT FPGA
  - None currently exists, working toward first generation device
  - Workaround: LT FPGA with similar architecture and size to HT device

	Xilinx			Actel
Maximum Capability	Artix-7 Family	Kintex-7 Family	Virtex-7 Family	A42MX16
Logic Cells	360K	478K	1,955K	**1.232K**
Block RAM	19Mb	34Mb	68Mb	-
DSP Slices	1,040	1,920	3,600	-
IP Cores	Extensive Library			**2 Available**

- HT Analog-to-Digital Converter (ADC)
  - Maximum sampling speed 25kS/s
  - 10-bit resolution

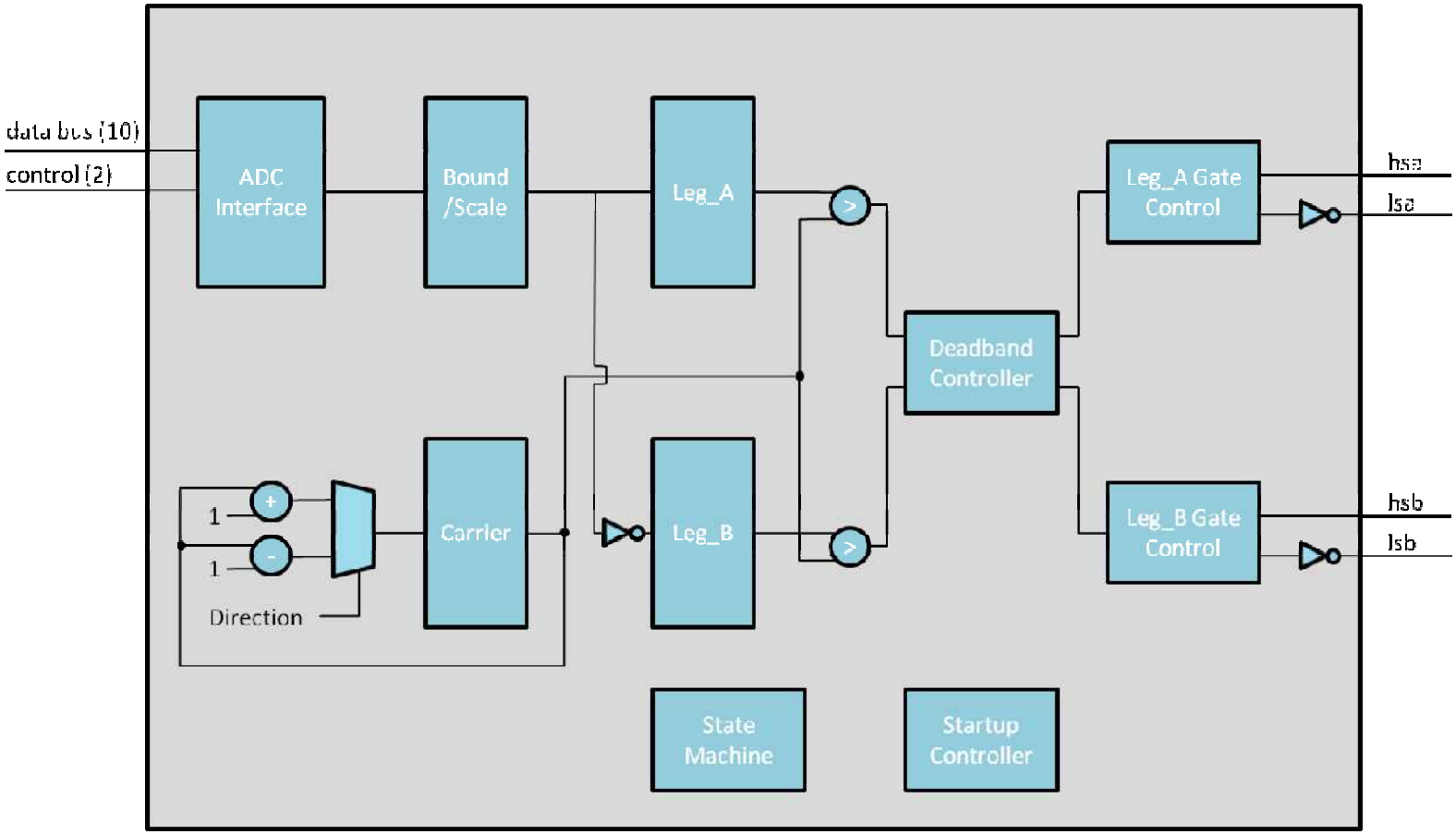
FPGA Design Considerations

- Steps must be taken to protect the switches from glitches and "shoot through" conditions
  - Startup state of switches must be controlled
  - Switching between legs must satisfy a minimum deadtime (1.4us) between modulations
- Minimize space utilization (<50% of logic cells) on the controller to allow for additional functionality to be added in later phases
- Operation at temperatures up to 240^{o}C

FPGA Design Parameters

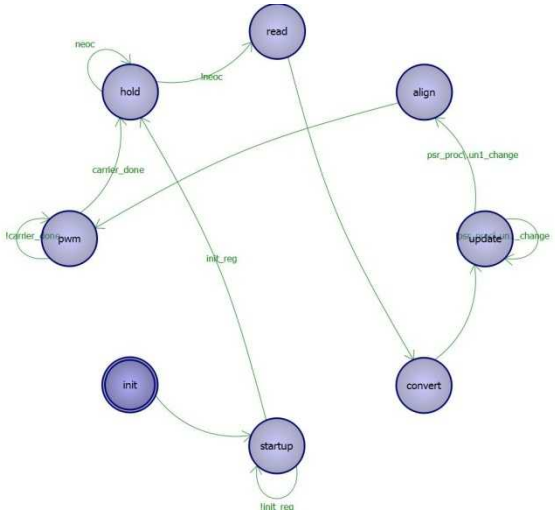
- 20kHz sampling frequency using zero order hold
- 16.384MHz system clock
- Fundamental signal input: 6Vpp, 5V offset
- Using these parameters, there are 333 leg modulations per 60Hz period
- PWM duty cycle ranges from 12.4% to 87.5%

FPGA Design Block Diagram



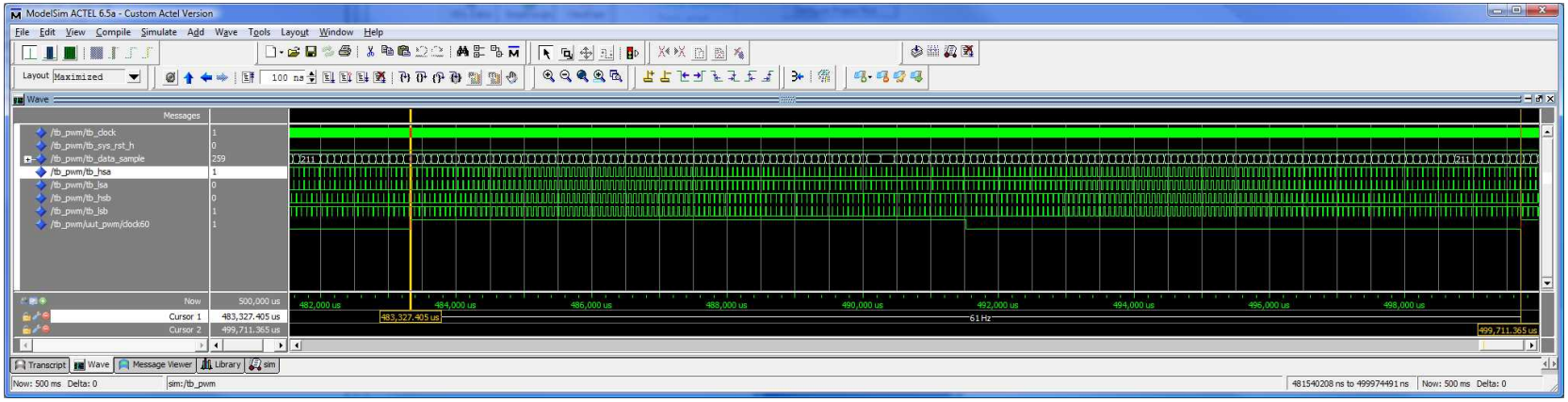
State Machine/Controller Operation

- *Init* = initialize system to know state
- *Startup* = allows time for glitches to settle and conditioning circuit to reach steady state
- *Hold* = wait for ADC control to indicate that a sample is available
- *Read* = read sample from the ADC, this sample is the fundamental waveform
- *Convert* = scale the signal and make sure it is within the carrier boundaries
- *Update* = load Leg_A with the fundamental and Leg_B with an inverted copy of the fundamental; this state waits until control signals indicate the deadband controller is not operating to ensure no lost modulation from the previous pwm period
- *Align* = sets several control signals that operate the gate control signals.
- *PWM*= modulates the carrier depending on a directional signal; every cycle the legs are compared to the carrier and, if a modulation of either leg is triggered, the deadband controller will become active and manage the switching of the gate controls; when the carrier reaches a boundary, the state will switch to *Hold*

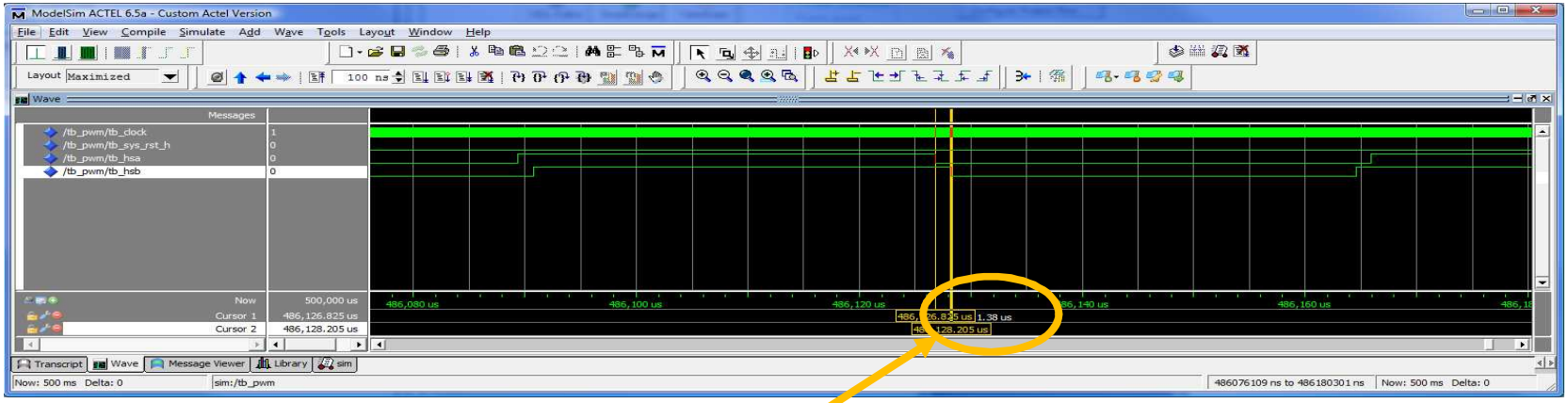


Simulation

- Verified correct switching sequence

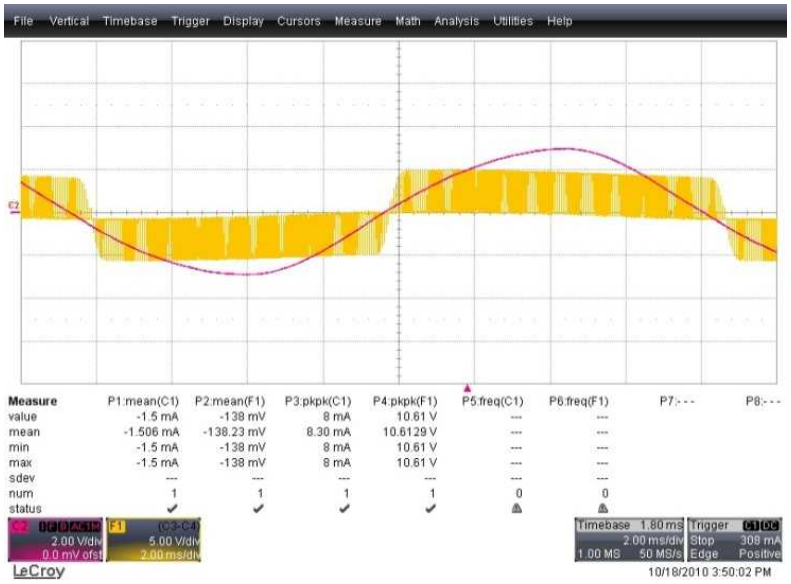


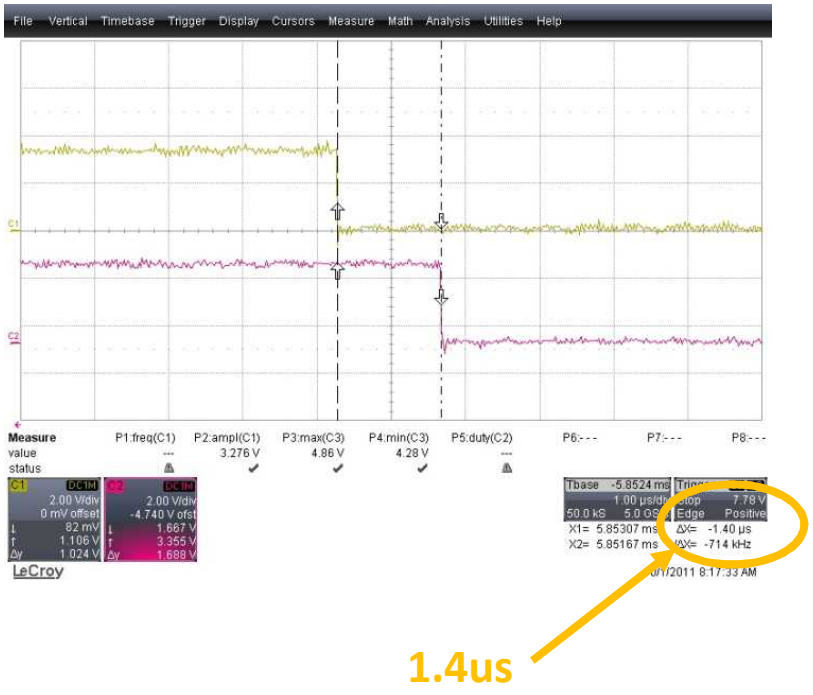
- Verified deadband controller time



Testing

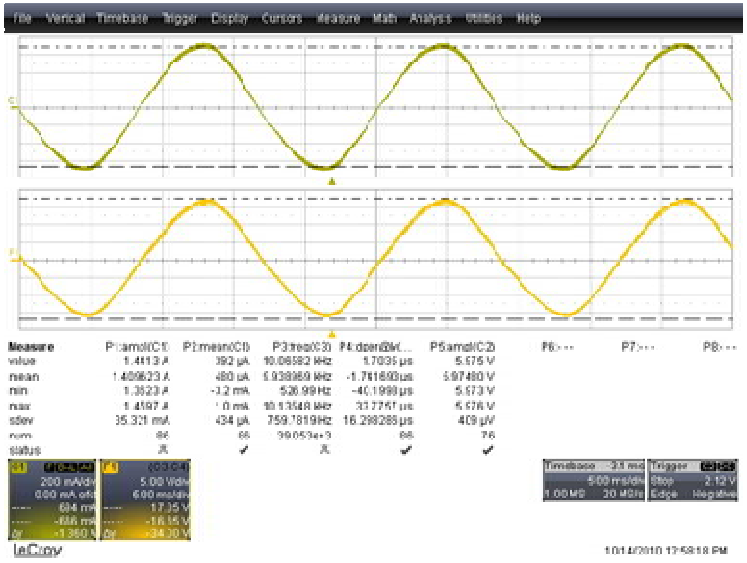
- Open load testing
  - Three-level l-l output voltage
  - Deadband control timing met



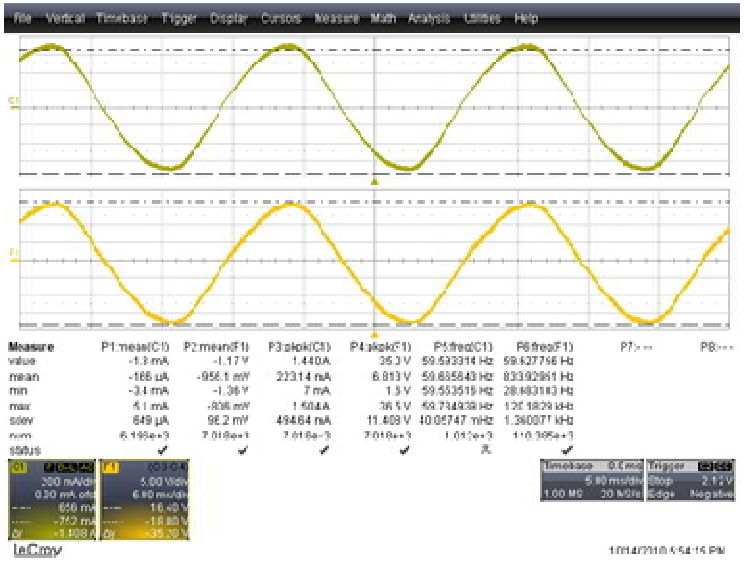


Testing

- Testing with load validated to 240°C
- Currently tested to 3kW



25°C



200°C

Controller Utilization

- Initial Design

```
Target Part: 42mx16-s
Combinational Cells:    450 of 608 (74%)
Sequential Cells:    223 of 624 (36%)
Total Cells:         673 of 1232 (55%)
DSP Blocks:          0
Clock Buffers:       2
IO Cells:            23
```

- Final Design

```
Target Part: 42mx16-s
Combinational Cells:    271 of 608 (45%)
Sequential Cells:    169 of 624 (27%)
Total Cells:         440 of 1232 (36%)
DSP Blocks:          0
Clock Buffers:       2
IO Cells:            23
```

Closing Remarks

- Successfully developed robust PWM scheme
- Minimized controller utilization to allow for additional functionality
- Provides design for HT FPGA when it becomes available

Questions

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