

# Sandia National Laboratories

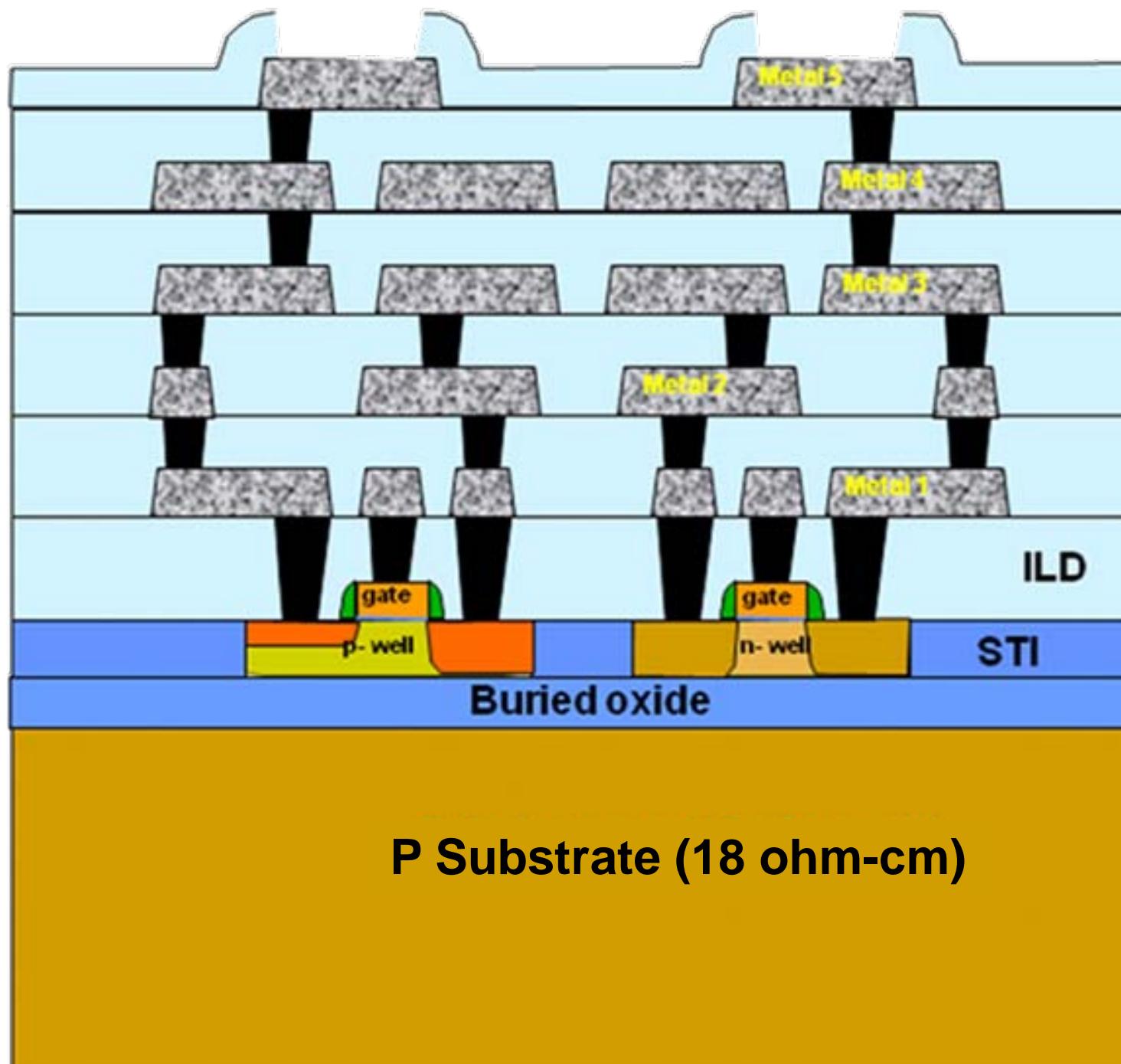
## Critical Capabilities for the Europa-Jupiter System Mission



### Key Capabilities

- The highly-reliable radiation-hardened microelectronics required for nuclear weapons are also extremely well suited for mitigating the issues that occur in many other harsh environments.
- For many decades, Sandia has had a prominent role in advancing the state-of-the-art in microsystems R&D, radiation effects, reliability physics, failure analysis, and both rad-hard-by-design and rad-hard-by-process techniques.
- Sandia has developed and maintains a fully-qualified SOI, radiation-hardened CMOS technology for custom, high reliability digital, analog, and mixed-signal integrated circuits (ICs).
- Sandia's ISO 9001:2008 certified ASIC design, fabrication, packaging and test capabilities include a DMEA accredited Trusted Foundry and Design Center.

### Radiation-Hardened SOI CMOS



Sandia built many key ICs for the Galileo mission

### Sandia's Trusted Foundry and Design Center

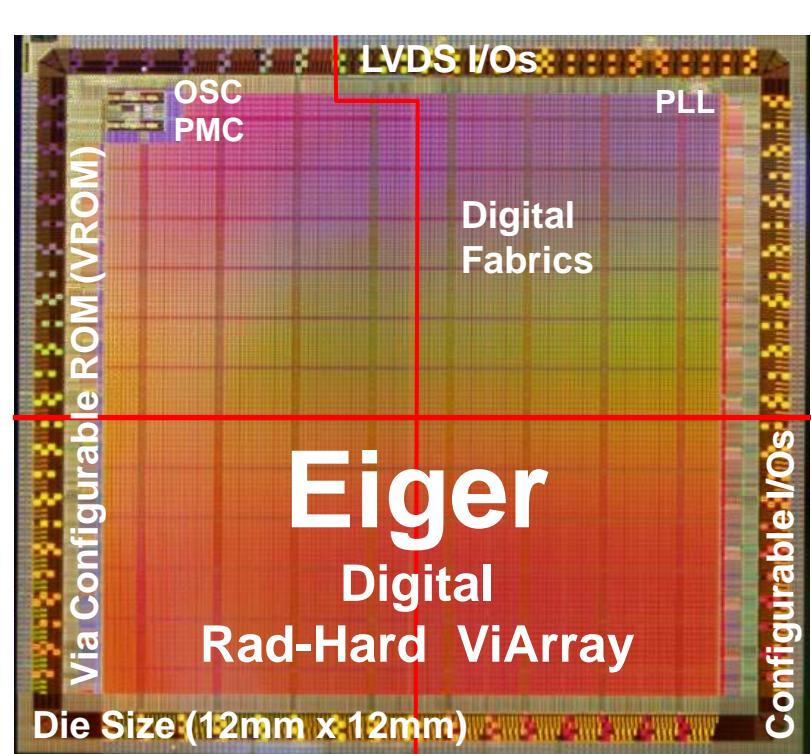


- Multiple ways to engage Sandia's CMOS7 rad-hard foundry
  - Low cost Multi-Project Wafer (MPW) program.
  - Quick-turn Structured ASIC ViArray platforms.
  - Low-volume production ASICs.
- Sandia's CMOS7 technology is NNSA's primary source of custom rad-hard ICs
  - Currently delivering thousands of ASICs.
  - DoD Cat 1A Trusted Design and Fabrication Process.

### Rad Hard, Fast-turn, Low NRE, Via-Configurable Structured ASIC Platform

#### Benefits

- Structured ASIC enables rapid turn-around and lowers the non-recurring engineering (NRE) and development costs.
- Pre-qualified base arrays reduce the development risks.
- ASIC-like performance.
- Regular, fabric-like structure enhances verifiability of trusted parts.

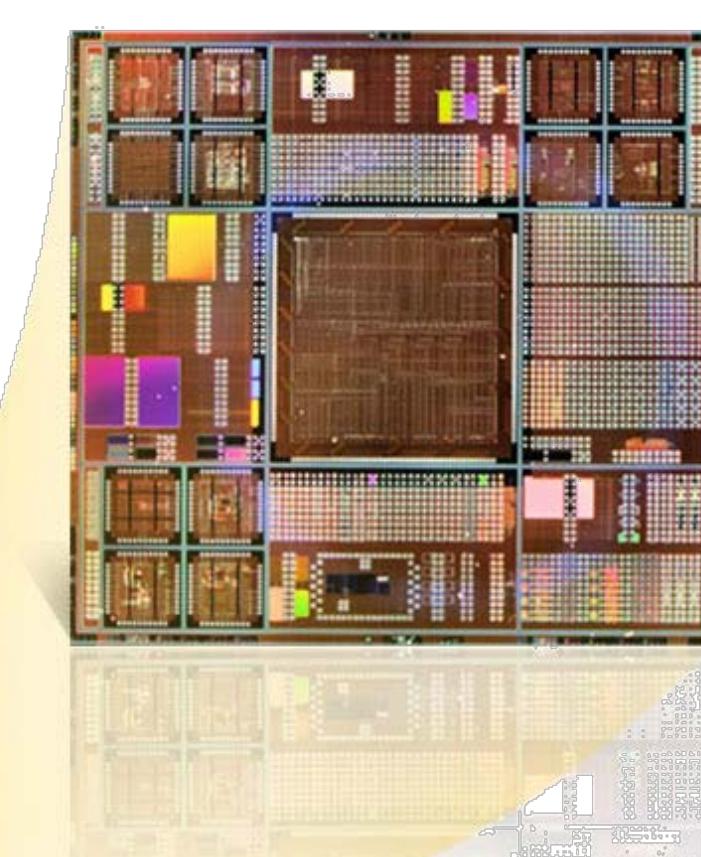
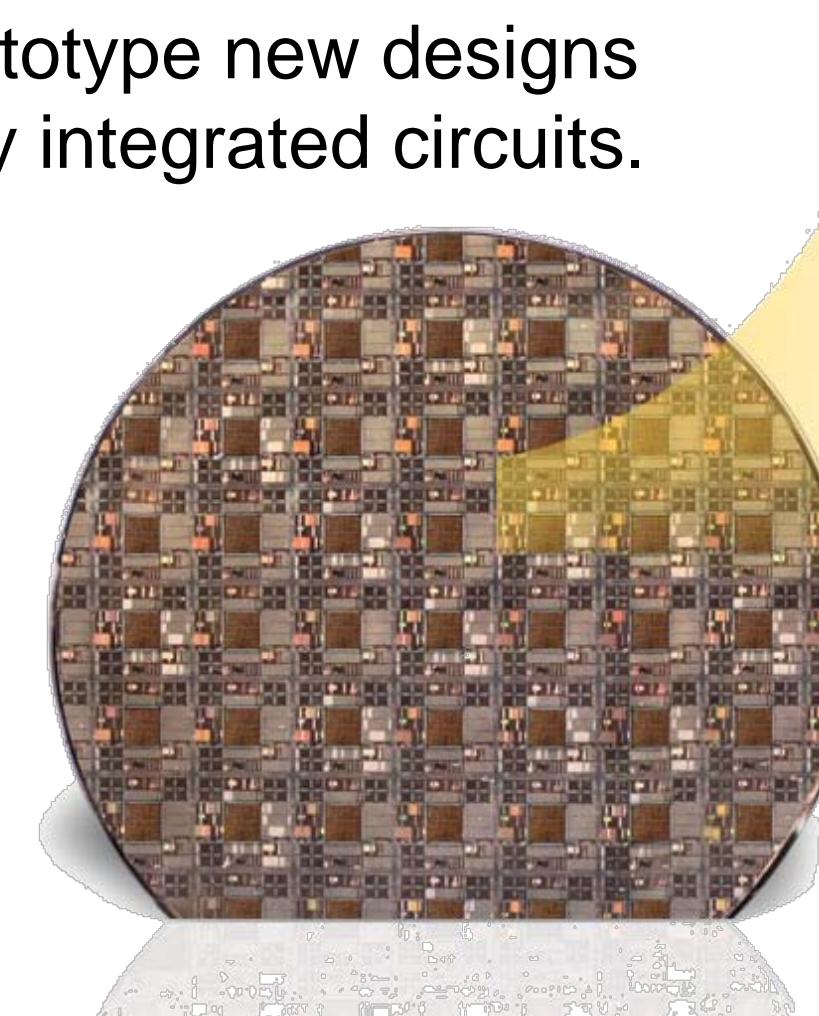


#### Special Features

- Metal-via configurable, fabric-like structure using ViASIC® via-mask technology.
- Four power quadrants with specialized interface circuits that allow up to four independent power supplies for power sequencing.
- Unused transistors and circuits are isolated from power and ground to minimize overall power consumption.
- On-package decoupling capacitors.

### Sandia's Multi-Project Wafer Program

- Multi-Project Wafer (MPW) fabrication runs allow several integrated circuit designs from multiple customers to share the mask and wafer resources, reducing the overall cost per design.
- Cost effective way to prototype new designs or produce small quantity integrated circuits.
- Uses CMOS7 rad-hard, mixed-signal CMOS-SOI technology.



### Radiation-Hardened Application Specific Integrated Circuits (ASICs)

- ISO 9001 Certified ASIC Development Process
  - Disciplined and controlled design process.

#### Process Design Kit (PDK)

- Technology model files and support for custom design, layout, and validation.

#### Standard Cell and I/O Libraries

- Full suite of standard cell and I/O cells with support for simulation, synthesis, and physical design.

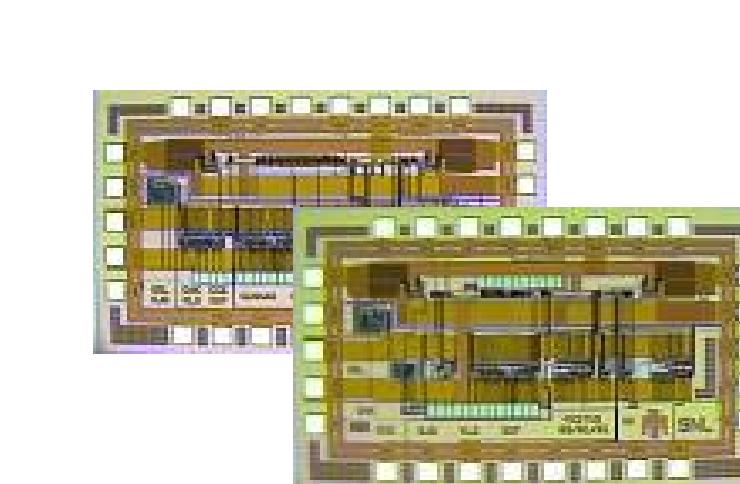
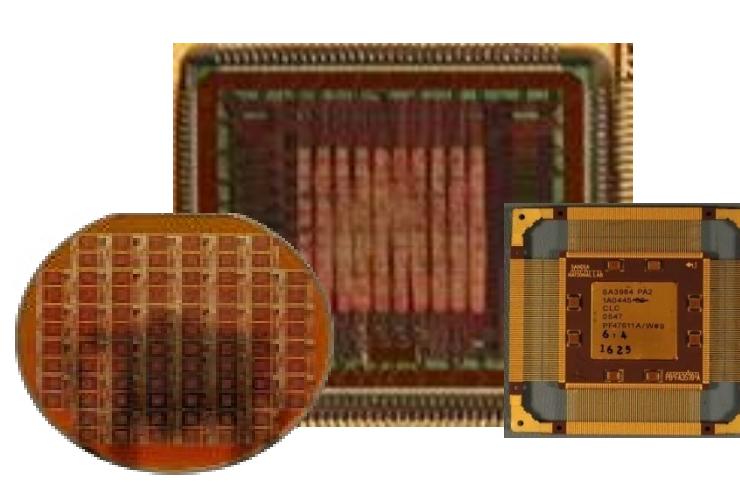
#### Analog Intellectual Property (IP) Modules

- Including A-to-D Converters, PLLs, and D-to-A Converters (contact us for full listing).

#### SRAM and ROM Memory Macros

- Pre-configured memory array macros (contact us for full listing).

For more information contact:  
 Rich Dondero, Manager  
 Rad-Hard CMOS Technology  
 Development Department  
 505-284-1457 [rdonder@sandia.gov](mailto:rdonder@sandia.gov)



Custom Rad-Hard Mixed Signal ASICs