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KEY:

- = NNSA Labs
- = Science
- = Nuclear Energy
- = Environmental Management
- = Fossil Energy
- = Energy Efficiency and Renewable

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Hardware Analysis for Embedded Systems

Nathan Edwards

Embedded Systems Analysis Group

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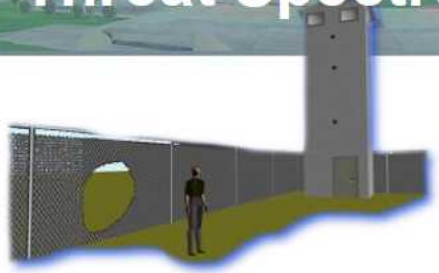
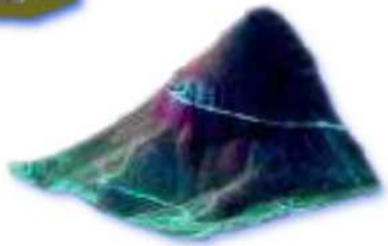
Homeland Security and Defense:

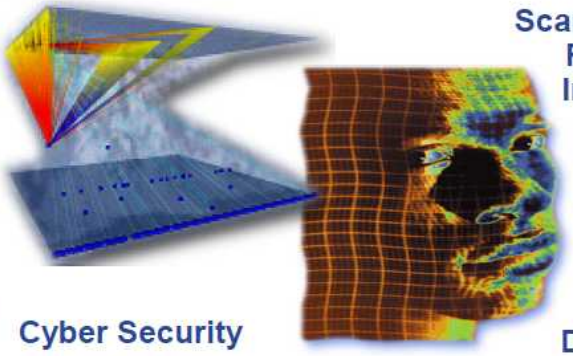
Exploring Solutions Across the Threat Spectrum



Synthetic Aperture Radars

Vulnerability Assessment Mod/Sim Tools





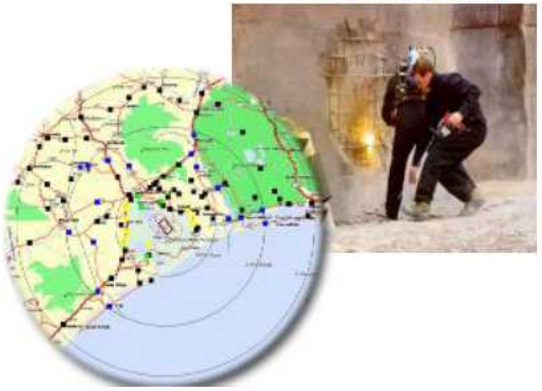
Cyber Security

Scanner-less Range Imager

Explosive Destruction System

Anticipate | **Predict & Prevent** | **Respond** | **Recover**

Access Delay



Critical Infrastructure Protection Systems Analysis Tools

Explosive Detection Portal

Unattended Ground Sensors

Radiation Remediation Foam

Tunnel Characterization

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About Myself

- **BS Computer System Engineering**
  - Arizona State University, December 2009.

- **1995 - 1997, Mechanical Engineering Study**
- **1996 - 2005, Firefighter / Paramedic**
- **2006 - 2007, Medtronic Physio-Control,** Technical Services
- **2007 - 2008, Medtronic Microelectronics Center,** HW Testing
- **2008, Salt River Project,** IT Help Desk
- **2008 - 2010, Boeing IDS – Mesa,** Real-Time SW Engineer
- **2010 – Present, Sandia National Laboratories**

What About You?

What are some of your engineering areas of interest?

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Importance of Embedded Devices

- **Infrastructure - Power Grid, Telecom Networks, Petroleum, NG**
  - Electrical relays, switches, valves, safety systems.
- **Vehicle Control Systems (air, water, land, etc.)**
  - Safety-critical control systems.
- **Industrial Automation & Control**
  - Manufacturing environments.
  - Home Automation and Control, Edge-system Smart Grid devices.
- **Personal Devices**
  - GPS, iPod, Accelerometers, Cell phones, etc.

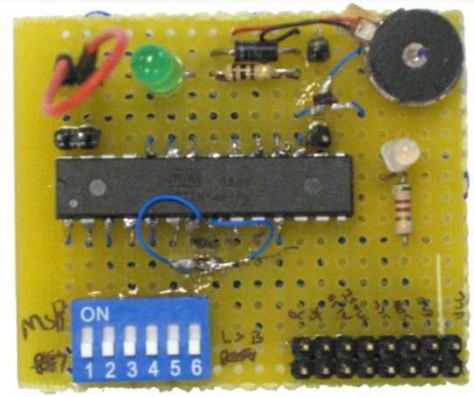
All Modern Technologies are Driven by Embedded Devices!

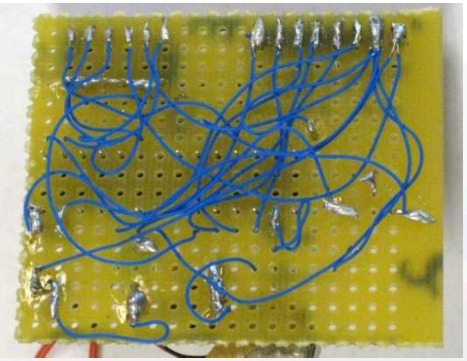
Hardware Example

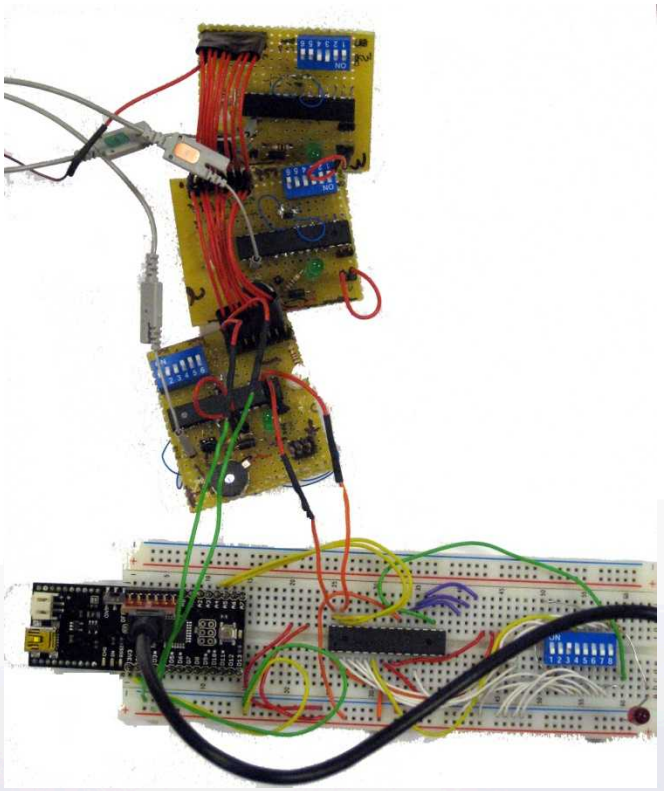
- **Problem as described by your customer:**
  - The low-voltage, constant-speed motor seems to work only some of the time.
  - On occasion, nothing seems to work on a prototype – results in scrapping the device.
  - The on-board peripheral devices (LCD driver, Real-time clock, CMOS sensor) seem to be intermittent.

- **Where do we start?**
- **What tools do we need?**
- **What information do we need from the customer?**

Step 1) Reduce Hardware Failure Modes



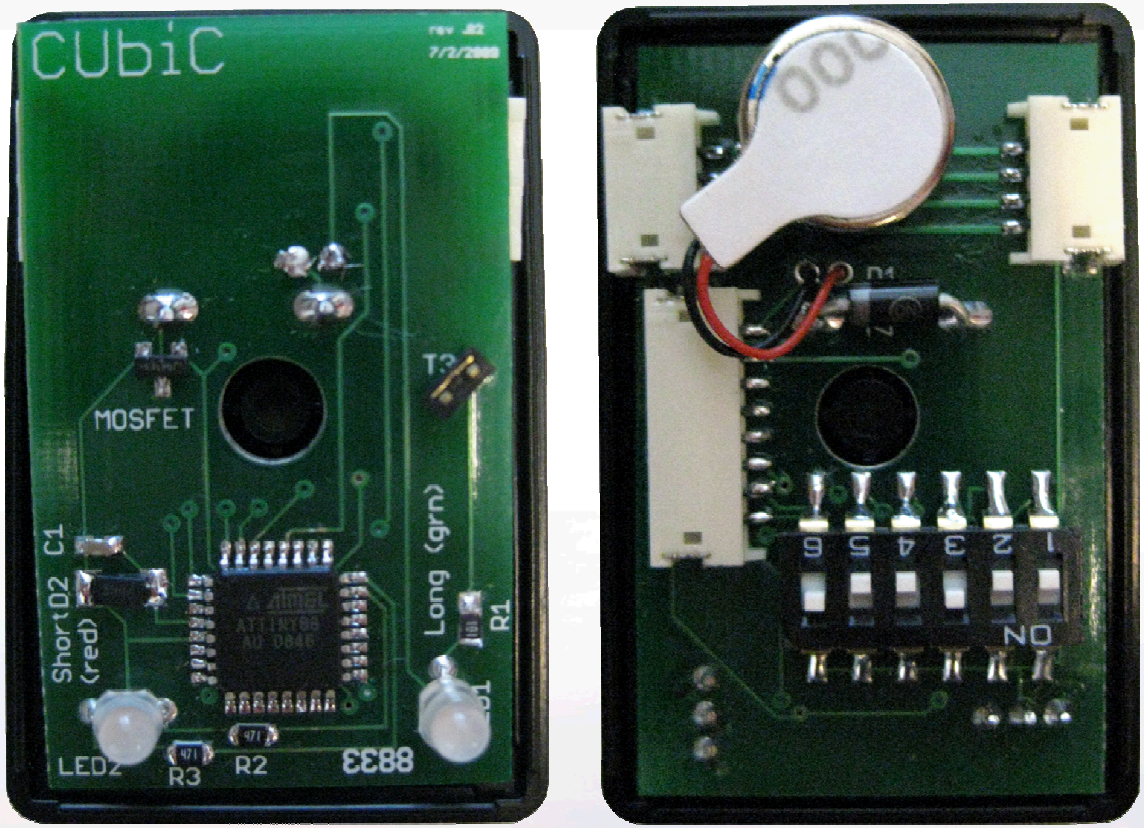




Pictures from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

Lets identify possible modes of failure……

Step 1) Reduce Hardware Failure Modes



Pictures from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

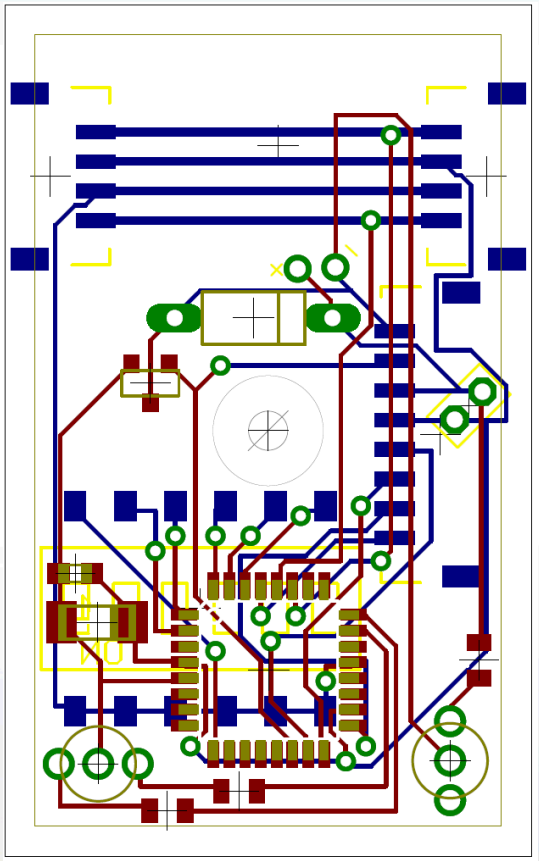
Lets identify possible modes of failure……

Step 1) Reduce Hardware Failure Modes

- **Possible modes of failure:**
  - Loose connections
  - Solder bridges
  - Conflicting sub-system voltages
  - Power supply noise
  - EMI
  - Energy storage devices
  - System clock sources
  - PCB layout and trace clearances (especially multilayer boards).
  - Other…

Step 1) Reduce Hardware Failure Modes

- **Verify conductance of traces:**
  - Start at end points and work your way in.
  - Visual inspection may also be needed.
- **Verify all GND connections:**
  - Are there multiple grounding planes?
  - Are they connected or EM isolated?



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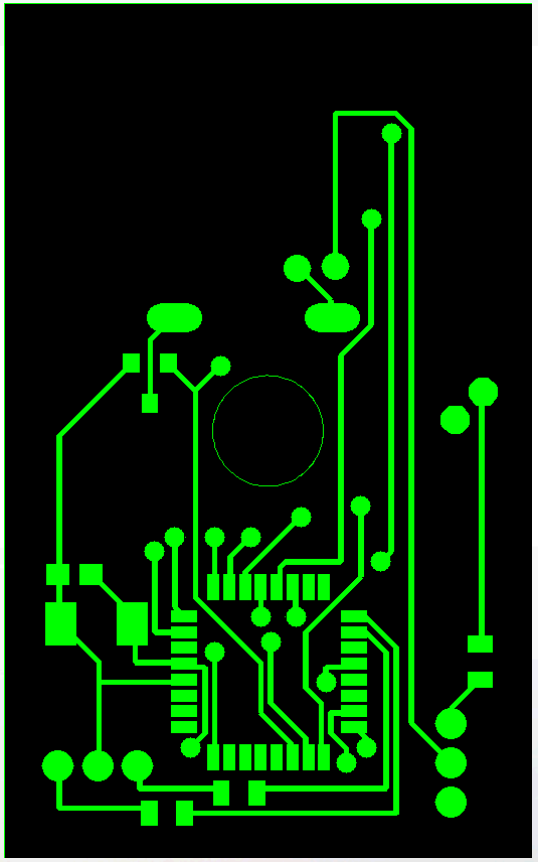
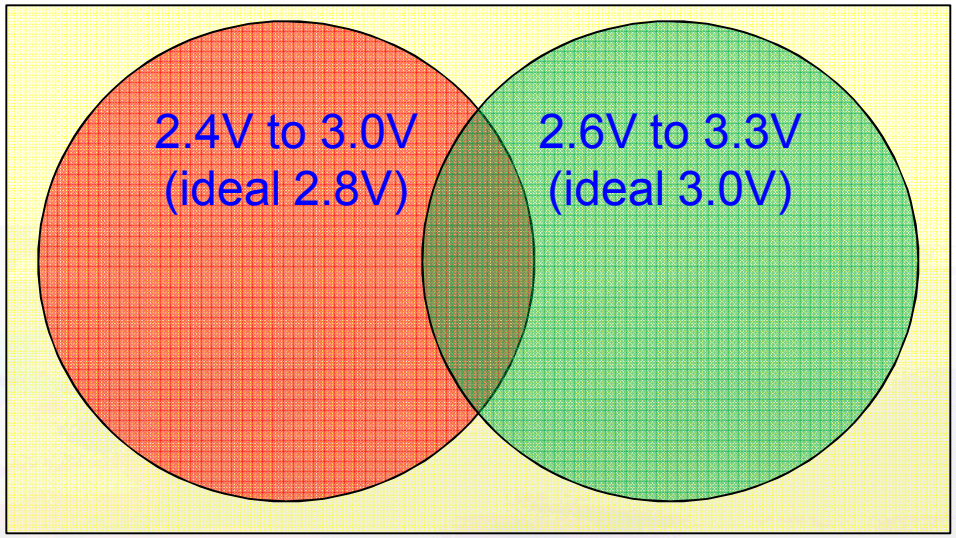


- **Analyze analog components:**
  - Identify the types and ratings of each component (find datasheets).
  - Look at the configuration – is the polarity correct?

Picture from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

Step 1) Reduce Hardware Failure Modes

- **Analyze System and Sub-system voltage requirements:**
  - Need to identify chips & components and find datasheets.
  - Can all devices be sourced from one power supply with regard to voltage and current draw?



  - Is there another solution that will improve the power management and avoid brown-out conditions between devices?

Step 1) Reduce Hardware Failure Modes

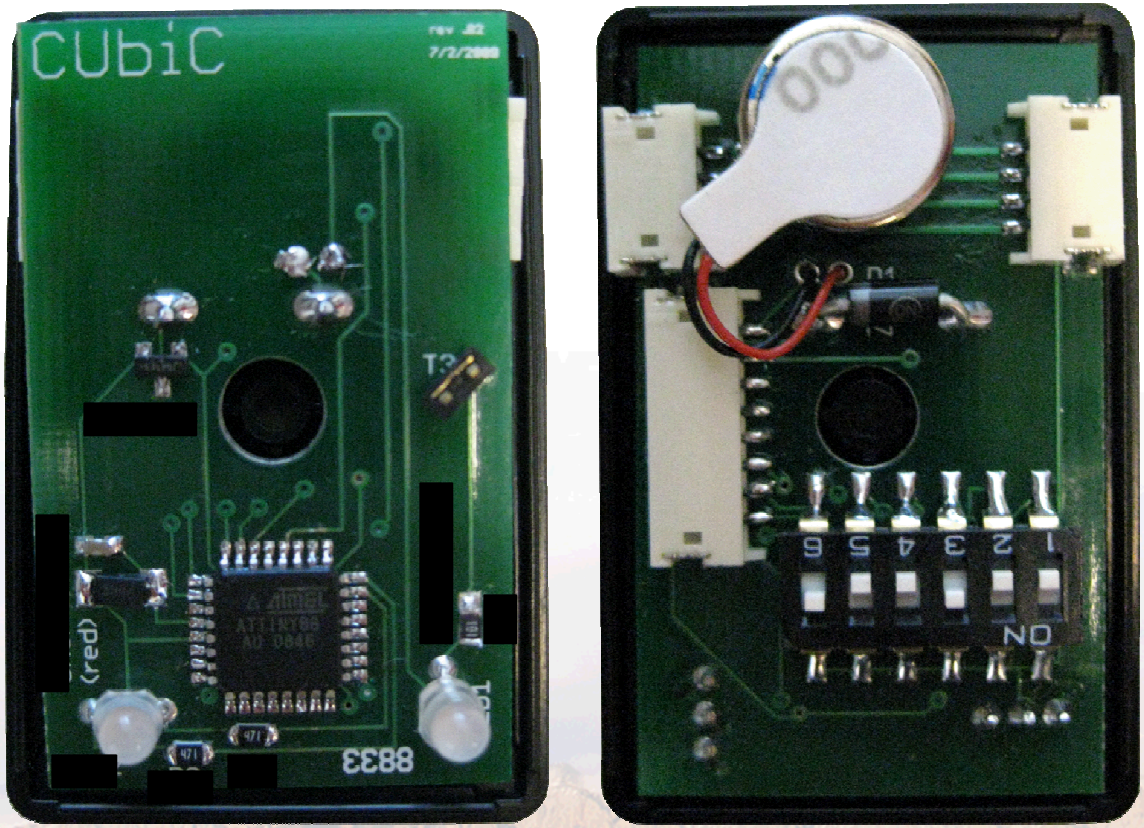
- **Analyze system clock sources:**
  - What type of clock sources are used? MEMS oscillators? Crystal oscillators? Internally configured digital clocks?
  - Are the source clock speeds sufficient for all sub-systems?
  - Is the clock source subject to signal degradation when connected to multiple devices?

- **Analyze energy storage devices:**
  - Identify all the potential storage devices.
  - Identify the types and ratings of each component.
  - Look at the configuration – is the polarity correct? Is there a conflict in current or voltage maximums?
  - What are the storage or discharge characteristics of each?

    (hint – you may need to bench test the component for more data)

Step 1) Reduce Hardware Failure Modes

EXERCISE: Identify the components……



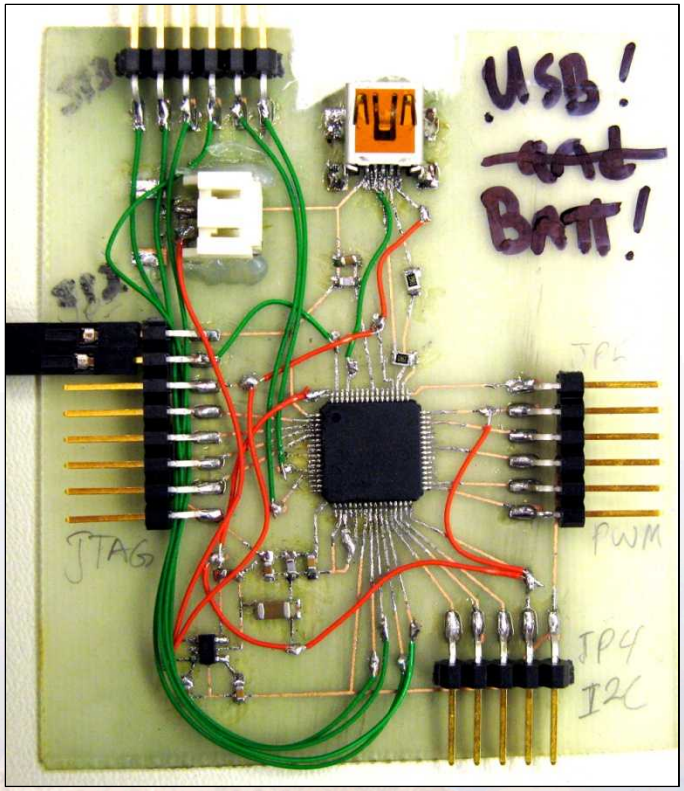
Pictures from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

Step 2) Make Sure You Can Test the Device

- **Test interfaces must be part of the design:**
  - How will you ever know if the system is truly working at all levels?

- **What are possible test interfaces?**
  - Test pins or pads.
  - Joint Test Action Group (JTAG) interface.
  - LED or other visual indicators.
  - Serial outputs.

- **ANOTHER HARDWARE EXAMPLE…**



Picture from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_hapti_c_network_/docs

Step 3) Plan for Access to Digital Interfaces

- **Monitor bus control messages:**
  - With an external device or logic analyzer you can monitor all communication bus messages – (SPI, I2C, SMBus, 1-Wire, 2-Wire)
  - Can also inject bus messages to test and verify control message sequencing.

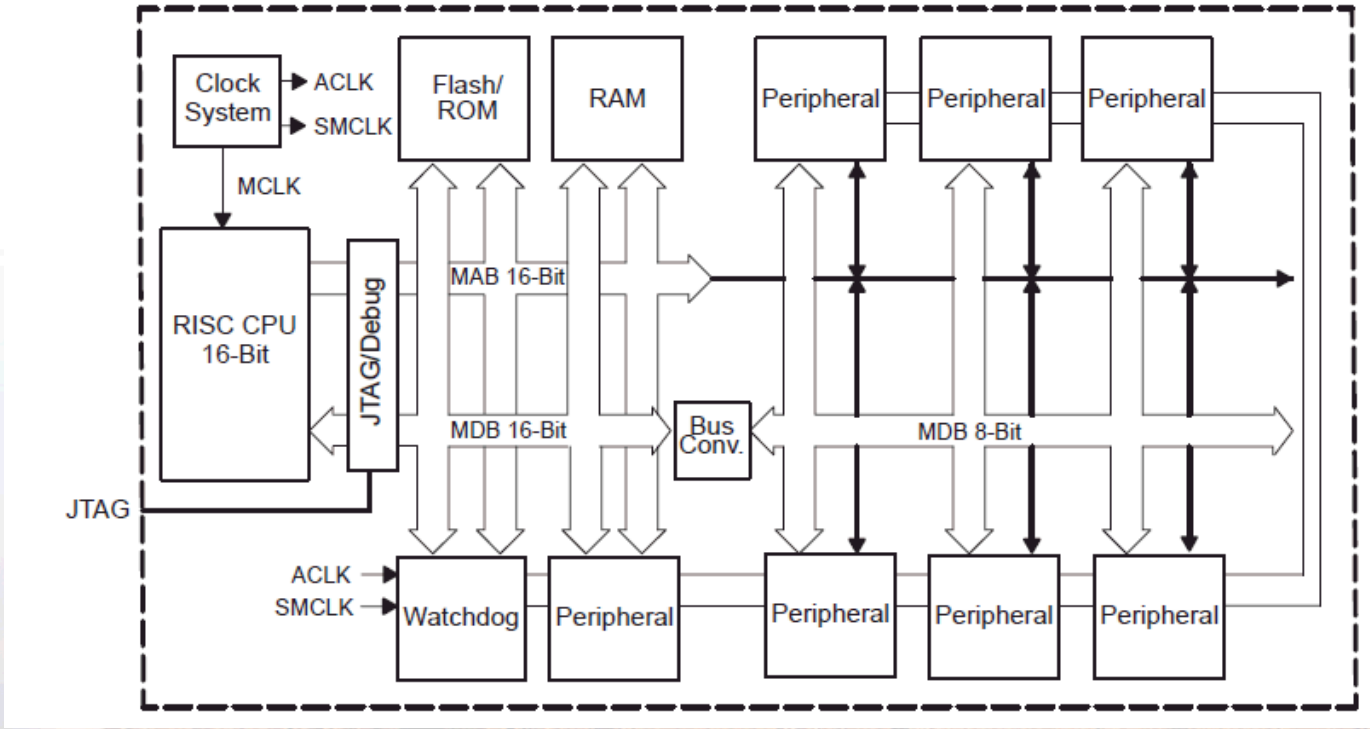
- **Download current state of memory (SRAM and Flash ROM):**
  - Some architectures allow this, some do not.
  - May need to write software to perform memory dump.

- **Software (firmware) debugging:**
  - Can control the execution clock and code that allows you to step through each line of software code while operating directly on the hardware.

Step 3) Plan for Access to Digital Interfaces

- **The power of a JTAG Interface:**

Figure 1−1. MSP430 Architecture



Texas Instruments MSP430x1xx Family User Guide SLAU049F.pdf

Hardware Analysis for Embedded Systems

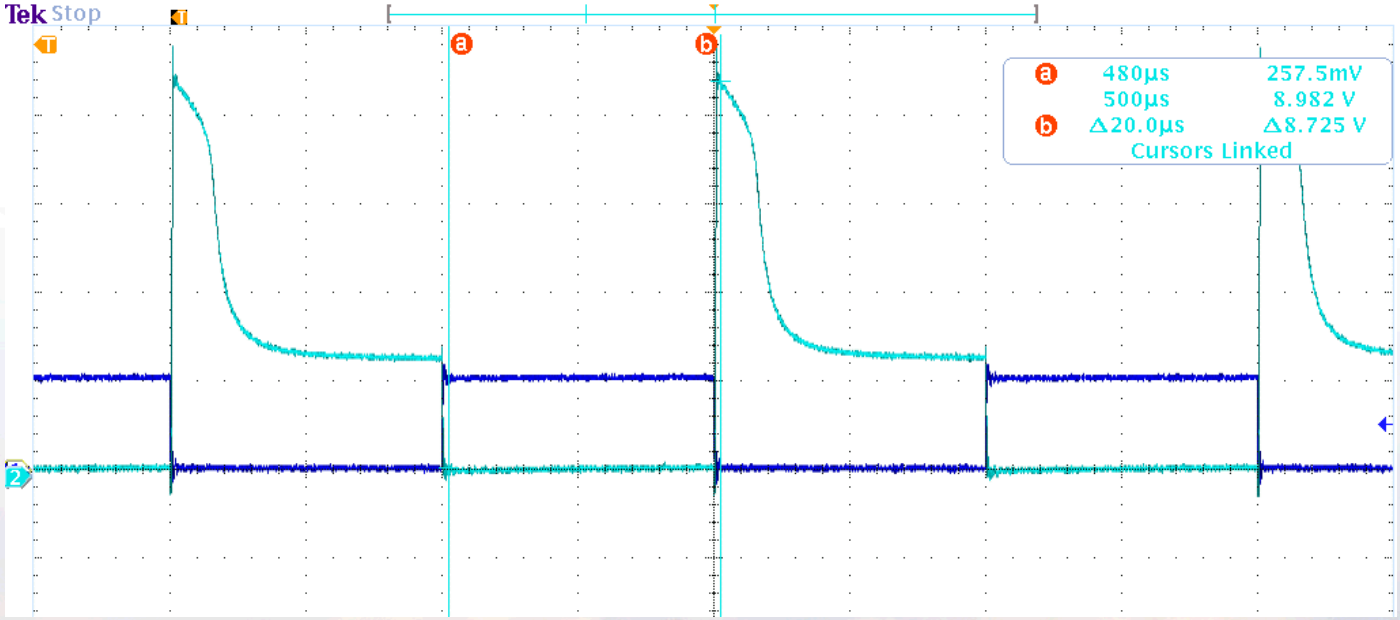
Summary of Steps:

1) Reduce hardware failure modes.
2) Make sure you can test the device.
3) Plan for access to digital interfaces.

If you systematically go through these steps you will find……..

Embedded System Hardware Analysis Results

- **The constant-speed motor is causing transient issues:**
  - Inductive load stores energy when turned off.
  - Resulting power spikes exceed the CMOS devices range and cause permanent damage.

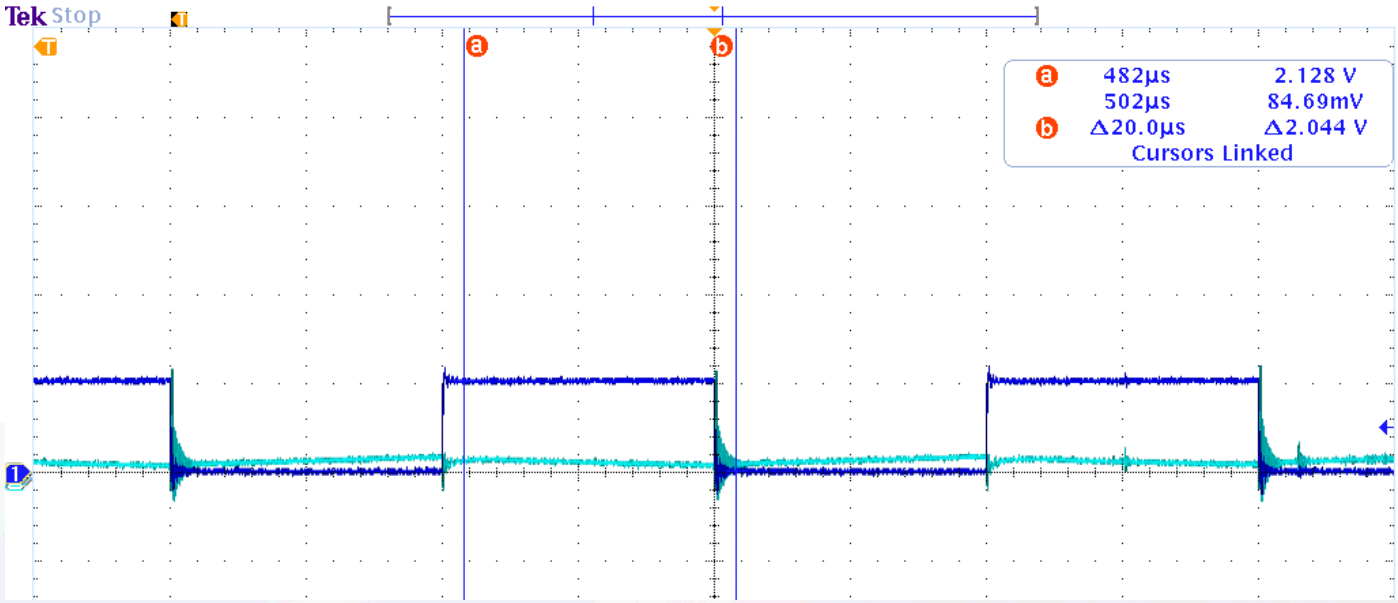


8.982V peak from Back EMF during motor off

Picture from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

Embedded System Hardware Analysis Results

- Solution Ideas???

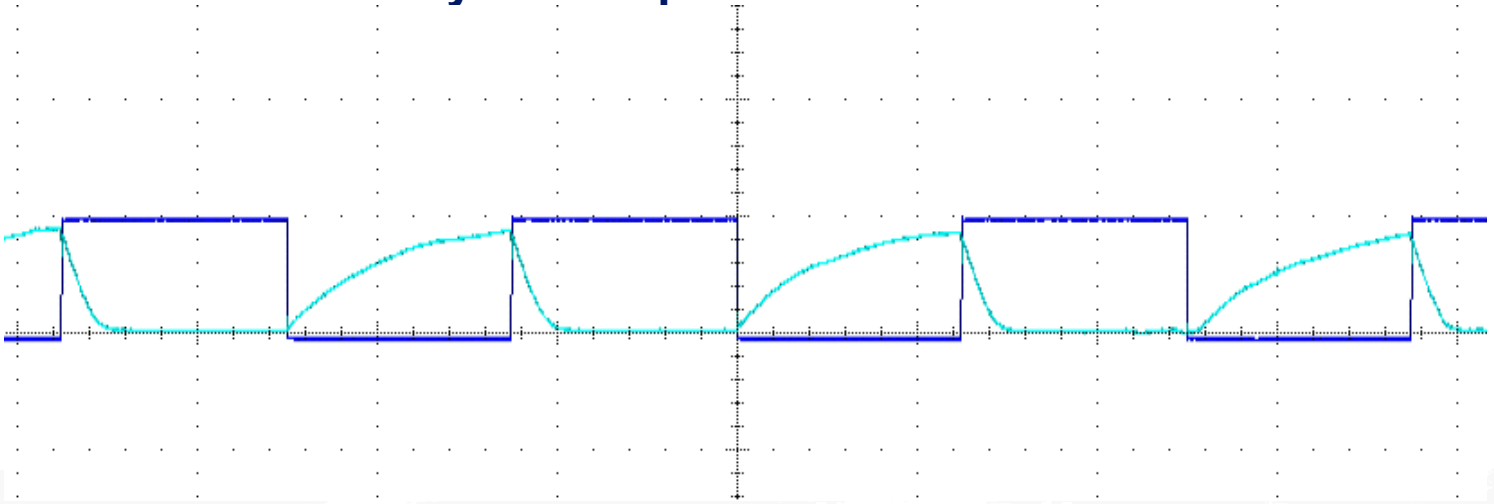


1) Capacitor effectively suppresses Back EMF.
2) Is this a workable solution for the system requirements?

Picture from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

Embedded System Hardware Analysis Results

- Solution Ideas – Flyback Capacitor



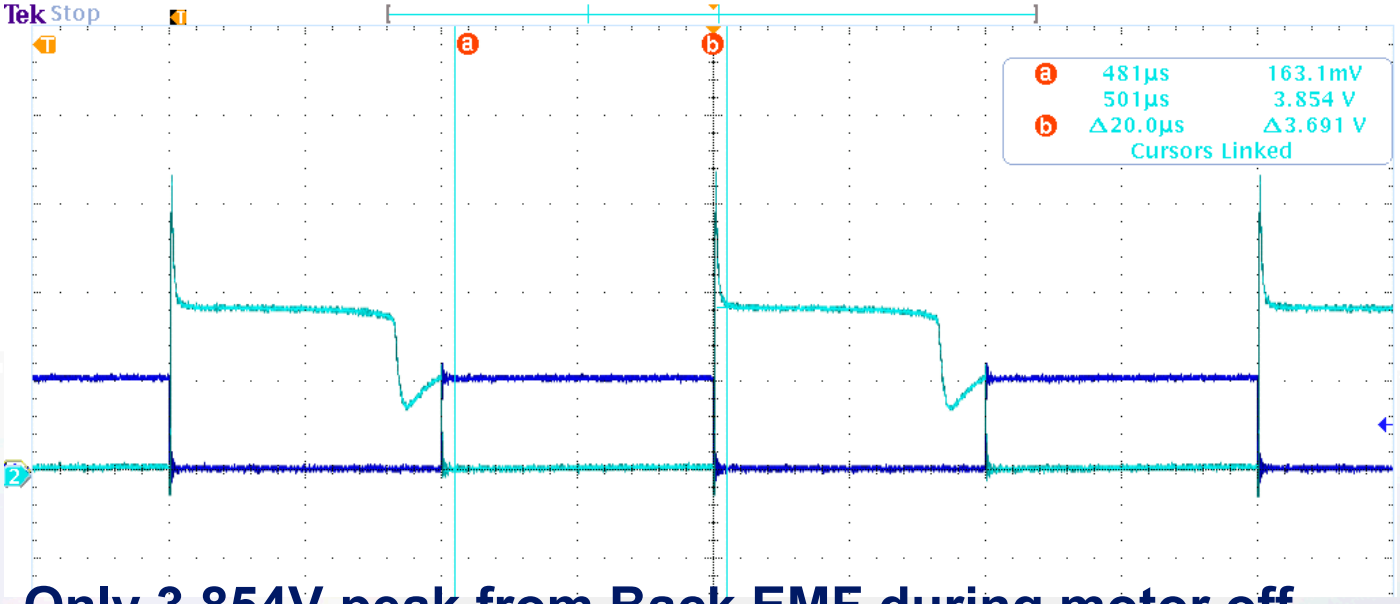
1) At 25kHz capacitor is constantly powering motor (not enough time to discharge).
2) At 1kHz capacitor has enough time to discharge.

Is this a workable solution for the system requirements?

Picture from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

Embedded System Hardware Analysis Results

- **Real Solutions:**
  - Install a 1N4001 voltage regulator diode across the contacts of the motor.



Only 3.854V peak from Back EMF during motor off

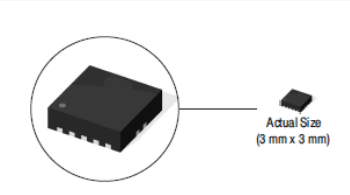
  - Use a MOSFET that has inductive load protection built into its package.
  - Although power isolation is best, sometimes the compromise of solutions is to protect the CMOS devices with bypass capacitors and zener diodes.

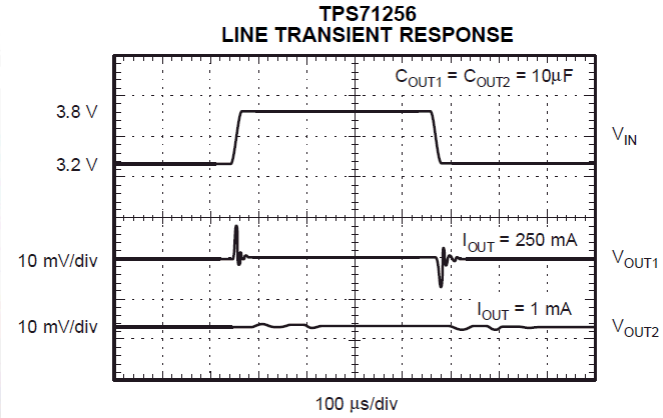
Picture from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs

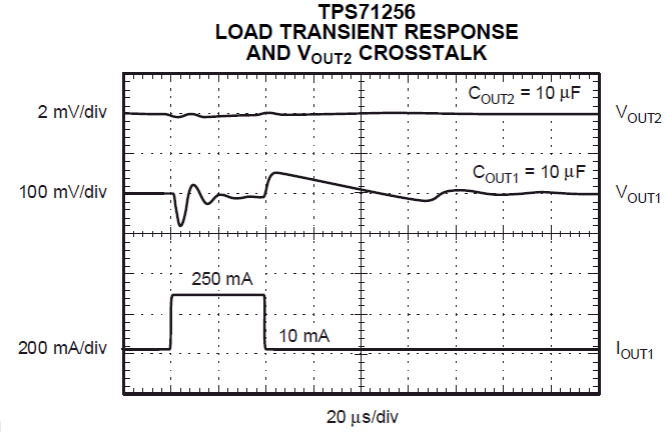
Embedded System Hardware Analysis Results

- **Brown-outs are caused by poor power management:**
  - When the MCU is performing a data write operation to external memory, the power draw is too much for the CMOS sensor (voltage drops below its operational threshold).

- **Solutions:**
  - Use a 2-channel, low-noise ULDO voltage regulator to supply the different voltages.



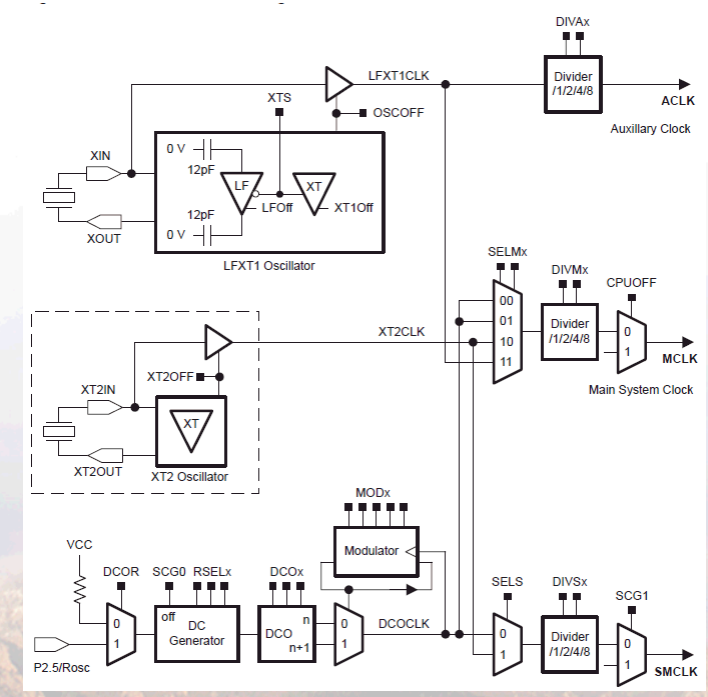




  - Make sure to select one that is rated for the system's current (Amps) requirements.

Embedded System Hardware Analysis Results

- **Intermittent data bus issues caused by system clock configuration:**
  - Discovered an errata sheet for the MCU - the clock divider for the data bus clock can only handle a system clock of < 1 MHz.
  - Same errata sheet states that there is a timing conflict with the software execution when an interrupt occurs at the same time as writing the data bus output buffer.
- **Solutions:**
  - Coordinate system wide clock speeds, maybe even have 2 or more clock sources.
  - Compensate for the errata with software changes (this can be tedious, but necessary).



Summary of Steps for Hardware Analysis

1) Reduce hardware failure modes.
2) Make sure you can test the device.
3) Plan for access to digital interfaces.

Systematically follow the above steps using good science and documentation.

Thank you and stay tuned for recruiting information……

References

[1] Pictures from http://code.google.com/p/haptic-research-group/source/browse/#svn/trunk/wireless_haptic_belt/docs.

[2] Texas Instruments MSP430x1xx Family User Guide SLAU049F.pdf available at http://www.ti.com/

[3] Texas Instruments datasheet for Dual 250 mA Output, UltraLow Noise, High PSRR, Low-Dropout Linear Regulator SBVS049C.pdf available at http://www.ti.com/