# Advanced Packaging/Board-Level Life Prediction and Reliability
## *JMP Five Year Plan for FY11-15*

SAND2010-1850P

Performing Organization: **Sandia National Laboratories**
Principal Investigator: **Rajen Chanchani, PO Box 5800, MS-0352, 505-844-3482, chanchr@sandia.gov**

| Customer | Collaboration |
|---|---|
| ***Dale Brandt,* SNL Org. 05351, Tel: (505) 844-4710, djbrand@sandia.gov** | ***Board-level reliability project from the DOE side was funded by Dale Brandt for insertion of PBGA technology in NW (B-61 Lifetime Extension Project). There is a transition plan:***<br>• ***Develop the board level reliability of PBGAs with manufacturing location at Honeywell, KCP.***<br>• ***Transfer the acceptance and specification documentation for manufacturing by FY12.*** |
| **Richard Flores, SNL Org. 01731, Tel: (505) 844-7220, floresr@sandia.gov** | **Packaged Via-array Structured ASIC Component – level reliability for insertion into wider range of DOE, DOD and Aerospace applications.**<br>**1. Deliver the reliability qualification results to be handed to the end-customers.** |
| **Davd Locker, AMRDEC, Tel: (256) 842-0163, david.Locker@us.army.mil** | **Discussions going on.** |
| **Jason L. Cook, US Army ARDEC, Tel: (973) 724-3920 Jason.Cook@us.army.mil** | **Discussions going on** |

# Advanced Packaging/Board-Level Life Prediction and Reliability *Quad Chart*

## What are you trying to do in this task?

•Develop Life Prediction models and reliability data for new technologies like low-cost PBGAs and CSPs and their reliability when surface mounted on a circuit boards.

•We are currently investigating reliability of 400 I/O PBGAs at component-level and at board-level.

## What makes you think you can do it?

•SNL has all of the skills and infrastucture to do this. SNL also partners with Honeywell KCP to develop and manufacture electronics.

•Component and board-level reliability/life-prediction models will be developed with SNL's manufacturing partner Honeywell, KCP and wherever appropriate with outside vendors.

## What difference will it make?

- This work is applicable to NW (DOE), DOD, aerospace, and consumer electronics.
- The insertion of the latest COTS technologies like PBGAs in these application will improve the circuit performance, and allow higher degree of integration and miniaturization at lower cost.

## What / When / To Whom Will You Deliver?

•We will develop the reliability of new packaging technologies like PBGAs to TRL 6 for delivery to our DOE (NW), DOD and Aerospace customers.

•For Example: PBGAs are being developed for DOE use in B-61 Lifetime Extension Program.

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# Contacts

| Name | Org | Role |
|---|---|---|
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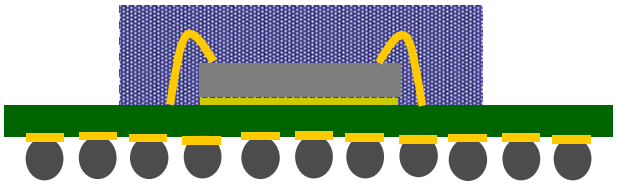
| Steve Wix<br>sdwix@sandia.gov<br>505-844-0778 | Sandia<br>DOE Lab | Manager/ Task Leader |
| Kevin Ewsuk<br>kgewsuk@sandia.gov<br>505-844-6958 | Sandia<br>DOE Lab | Manger |

# Advanced Packaging/Board-Level Life Prediction and Reliability

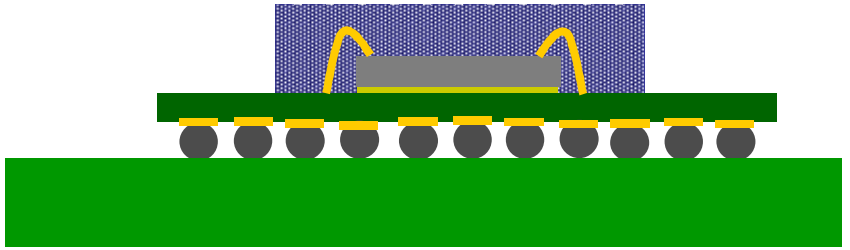
**This has been started as a New Area Of Focus starting with Seed funding from JMP in FY10 because of considerable interest in high I/O density, low cost Area Array COTS Packages.**

## What are we trying to do in this task?

- Develop assembly processes, array solder joint inspection techniques, reliability data and life prediction models for Plastic Ball Grid Array (PBGAs) and Chip scale Packages (CSPs).
- We are currently studying of 400 I/O PBGAs at component-level and at board-level.



PBGA
Component - level



PBGA
Board-level

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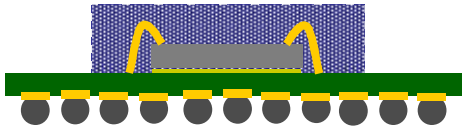
# Why Area Array Packaging Technology

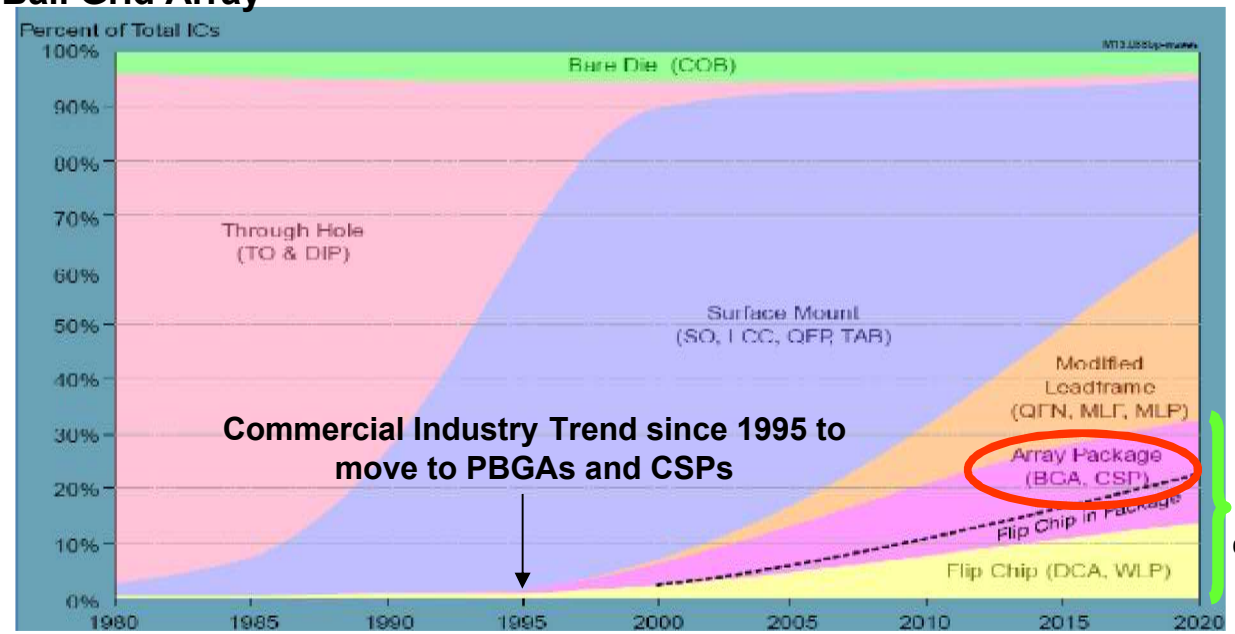
## It is inevitable that the technology will be used in the future DOD, DOE and Aerospace applications.



Ball Grid Array

Chip Scale package

Flip-Chip package




### Industry is moving towards Area array technologies because:

- I/Os in ICs are increasing at a fast rate. Periphery lengths cannot accommodate I/Os, thus area array are increasingly used.
- Smaller foot-print/height in X, Y, Z – dimension.
- Less materials used, lower weight
- In most cases lower cost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# Why Area Array Packaging Technology

## It is inevitable that the technology will be used in the future DOD, DOE and Aerospace applications.

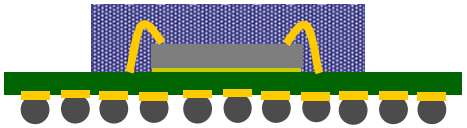
## Following the industry lead –

- **The time has come for advanced area array packaging technologies insertion in NW (DOE), DOD, and aerospace applications**

**An Example: Currently, Sandia is fabricating 400 I/O Via-array Stuctured ASICs for use in NW (B-61 Lifetime Extension Program).**

- **The insertion of the latest COTS technologies like PBGAs in these application will improve the circuit performance, and allow higher degree of integration and miniaturization at lower cost.**

In this project, our short Term Goal



**Plastic Ball Grid Array**

In this task, our Long Term Goal

**Chip Scale package**

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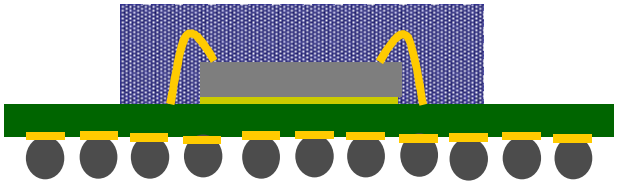
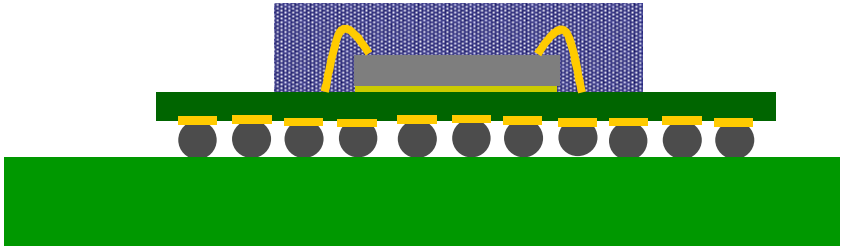
# Challenges involved in Area Array Technologies



PBGA Component



PBGA Component on a board

- We have selected Plastic Ball Grid Array Technology because it has a better thermal expansion match with Printed Circuit Boards.
- Ceramic BGA has higher thermal expansion mismatch will introduce another level of complexity involving the use Column Grid Array.
- Our work will address the following challenges:
  a. Component-level reliability validating life prediction models of PBGAs under HAST, temperature cycling and Moisture sensitivity level tests.
  b. Robust assembly Processes at Honeywell, KC (Honeywell, KC is trusted production site for DOE and DOD)
  c. Critical - Solder joint inspection technique or method to assure acceptance criteria.
  d. Solder joint reliability and life prediction models.

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# Advanced Packaging/Board-Level Reliability - Background

## FY2010 Goals

1) Identify the initial components and the Board or MCM technologies for the study.
2) Literature search the reliability studies done on relevant Board-level Reliability.
3) Plan the tasks for FY 2011 and beyond.
4) Preliminary reliability testing of PBGAs components and board-level with Plastic BGAs which has been started for DOE use.

## Component/Packaging Identified for the initial Study

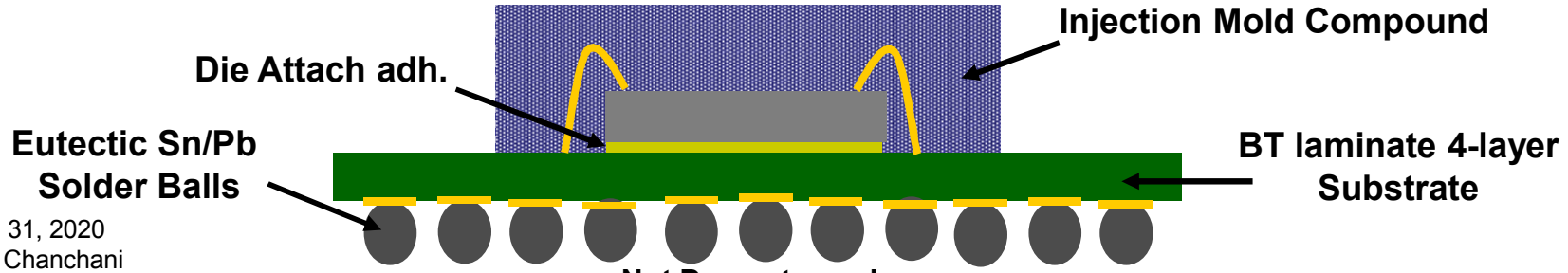
**Component:** Structured ASIC (Via Array) IC Fabricated in SNL.

**Packaging:** Plastic Ball Grid Array packaged by injection Molding at i2A Technologies, CA

**Package Size:** 27 mm x 27 mm x 1.53 mm (without solder ball height)

**# of I/Os:** 400

**Eutectic Sn/Pb Solder balls:** 0.76 mm diameter on 1.27 mm pitch

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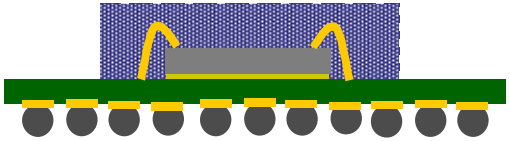
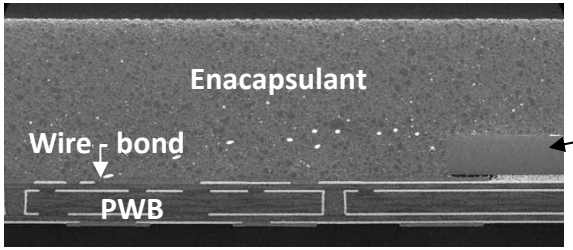
# Component-Level Packaging and Testing

## 1. Component Packaging production at i2a Technologies – we have done 3 production lots



Front

Back




Cross-Section view of Plastic Ball Grid Array Package

## 2. Component level Reliability

**JEDEC Standard Tests:**

1. Temperature Cycling
2. HAST
3. Moisture sensitivity
4. DPA

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# Preliminary Report on the Qualification plan in Other Enterprises

| Standard | Source | Moisture Sensitivity Test | Temp Cycling | Unbiased HAST | Comments |
|---|---|---|---|---|---|
| JEDEC | Internet | Moisture Sensitivity Level, level 3IPC/JEDEC J-STD-020 | -55 to +125°C, 700 cycles | 130°C/85%R.H., 96 Hours | Industry Standard |
| Current SNL Qualification | | Moisture Sensitivity Level, level 3IPC/JEDEC J-STD-020 | -55 to +125°C, 1000 cycles | 130°C/85%R.H., 350 Hours | |
| Endicott Interconnect | Internet | Not shown | -55 to +125°C, 1000 cycles | 130°C/85%R.H., 96 Hours | |
| STAT ChipPAC | Internet | Moisture Sensitivity Level, level 3IPC/JEDEC J-STD-020 | -65 to +150°C, 1000 cycles | 130°C/85%R.H., 96 Hours | |
| Amkor | Internet | Moisture Sensitivity Level, level 3IPC/JEDEC J-STD-020 | -55 to +125°C, 1000 cycles | 130°C/85%R.H., 96 Hours | Monitoring Key Indices |

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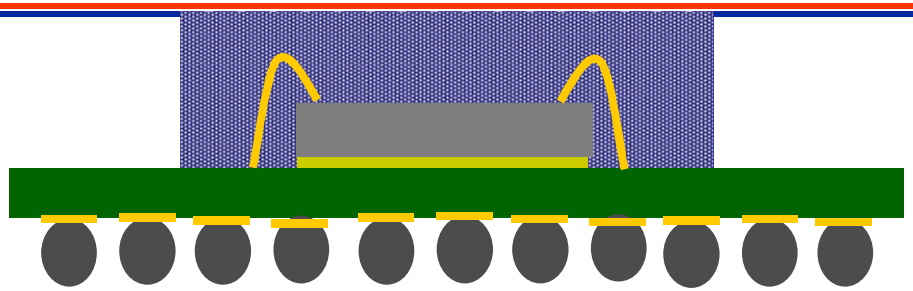
# Component – Level Evaluation

## Preliminary Qualification Data



| | Test Type | Batch 1 | | Batch 2 | |
|---|---|---|---|---|---|
| | | Sample Size | Results | Sample Size | Results |
| 1 | Initial Electrical Test | 453 | 8 Failed (1.8%) | 353 | 29 Failed (8.2%) |
| 2 | Temperature Cycling -55 +125 oC | 77 | Passed 1000 Cycles | 77 | Passed 1000 Cycles |
| 3 | HAST 130oC, 85% R.H. | 77 | Passed 350 Hours | 77 | Passed 168 Hours, failed 350 hours |
| 5 | MSL Level 3 | 11 | Passed | 11 | 3 Failed (27.2%) |
| 6 | DPA | 5 | Passed | 10 | Passed |

**No Smoking Gun yet Identified for batch 2 Failures**

**Work in progress**

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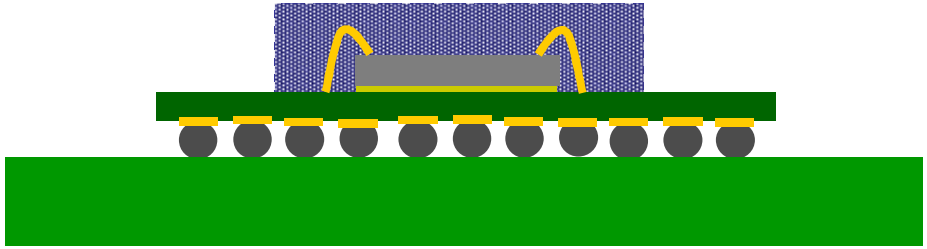
# Board – Level Evaluation

## Preliminary Plan



**Three main goals:**

1. Assure robust assembly process
2. Solder joint inspection and acceptance criteria
3. Solder joint reliability testing

**To Address these Issues, we are initiating work to:**

1. Design and fabricate the daisy Chain version of IC and package (Already started)
2. Use these Test dies to develop robust assembly processes at honeywell, KC.
3. Investigate different techniques and criteria to assure 'GOOD' solder joints after assembly. Develop an acceptance criteria.
4. Develop reliability data and predictive lifetime models.

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# Advanced Packaging/Board-level Reliability– Major Results To Date

**FY10:**

## Component – Level Reliability Testing

- **Milestone 1: Identified and developed the package and technology for initial study**

  **Accomplishment:**

  - **Identified Plastic Ball Grid array for structured ASICs for use in DOE (NW). We have obtained three production lot batches of these parts**

- **Milestone 2: Initiated preliminary qualification of the PBGA technology**

  **Accomplishments:**

  - **Have completed JEDEC testing on two production batches.**

## Board-Level Reliability Testing

- **Milestone 3: Identified the component and Board technology for the initial study**

  **Accomplishment:**

  - **Identified the PBGA and Polyimide-Glass Technologies for the first phase Studies**

- **Milestone 4: Design Test ICs and the Test packages**

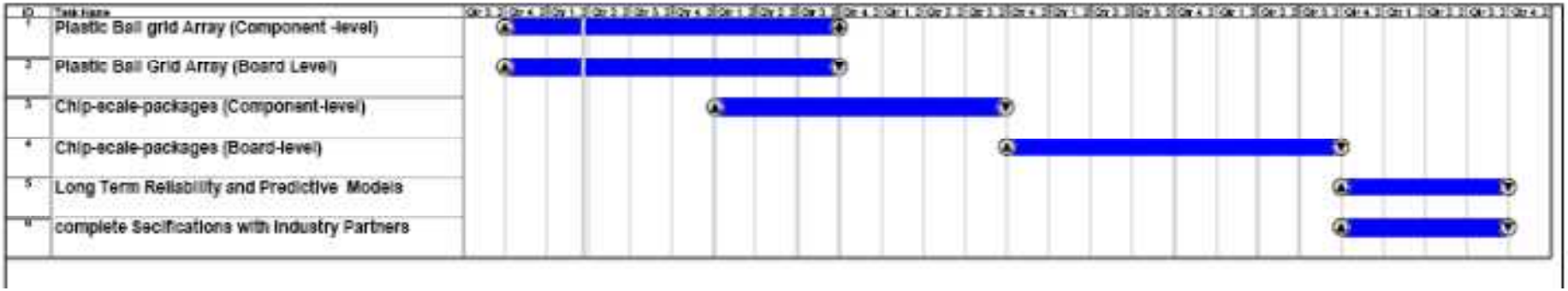
  **Accomplishment:**

  - **Completed the IC daisy chain and currently designing the package.**

# Milestones/Deliverables for FY11-15

| Task # | Milestones/Deliverables | Date | Metrics or Exit Criteria | DoD / DOE Linkage |
|---|---|---|---|---|
| 1 | a. Complete JEDEC reliability testing of three production lots of PBGA packages.<br>b. Complete Design and fabrication of Test PBGA packages for board-level reliability<br>c. Identify other adv.packaging components (e.g. CSP) for insertion in DOE/DOD systems | *1Q11* | Report | *AMRDEC/SNL* |
| *2* | a. Complete Component-level reliability testing of PBGA packages.<br>b. Complete the development of the assembly processes for PBGAs on Polyimide-glass boards.<br>c. Procure components for component-level testing of CSPs. | *3Q11* | Report | *AMRDEC/SNL* |
| *3* | a. Complete the documentation and specification for solder acceptance criteria for board-level assembly of PBGAs.<br>b. Initiate the reliability testing of CSPs. | *4Q11* | Report | *AMRDEC/SNL* |
| *4* | *a. Complete the PBGA board-level reliability testing and predictive life-time models*<br>*b. Complete the component-level testing of CSPs.* | 4Q12 | Report | *AMRDEC/SNL* |
| *5* | *a. Complete the CSP board-level assembly and reliability testing*<br>*b. Complete the predictive life-time models for CSP assemblies* | *1Q13-4* | Report | *AMRDEC/SNL* |
| *6* | *a. Complete the long-term reliability testing and predictive life-time models for PBGAs and CSPs.*<br>*b. Complete the development of the specifications for PBGAs and CSPs with industry partners* | *3Q15* | Report | *AMRDEC/SNL* |

# Advanced Packaging/Board-level Project Plan FY11-15

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