SAND2013-8542P

Surface Electrode – Triangle – Ion Trap Technology Overview

Matthew Blain
Daniel Stick

6 August 2013
NIST Boulder

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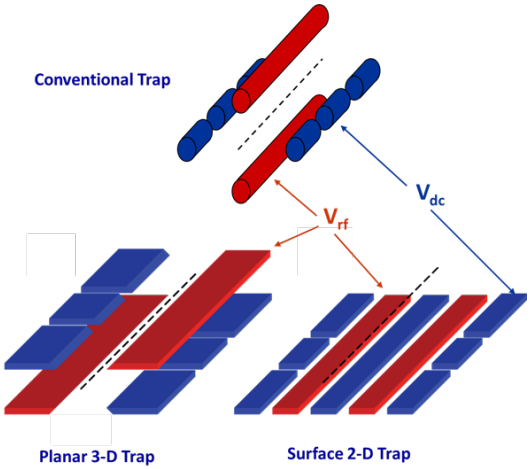
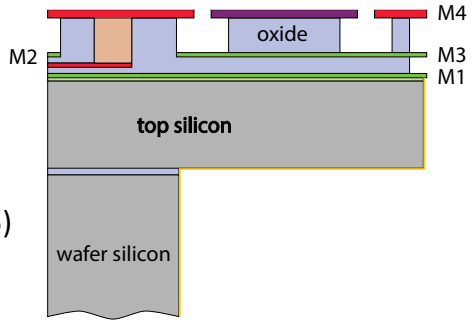
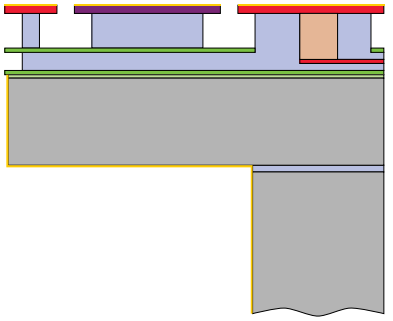
Surface Electrode Ion Trap Fabrication

4-metal-layer process modified from Sandia 0.35 µm Al/SiO_2 CMOS Process

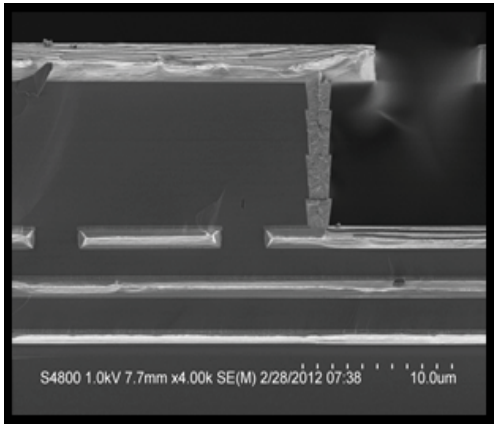


J. Chiaverini, *et al.,* Quant. Inf. Comp. 5, 419 (2005)





- **1.2/2.5 µm Al 4LM technology**
- **Trap flow: ~300 ops, 11 mask levels used 17x**
- **Interposer flow: ~320 ops, 15 mask levels used 21x**
- **10 µm oxide separating RF(M4), ground (M3)**
- **Precision Chip thru-holes**
- **Release singulation**
- **Precisely recessed oxide**
- **Routing on M2**
- **Gold coating from front and back side**



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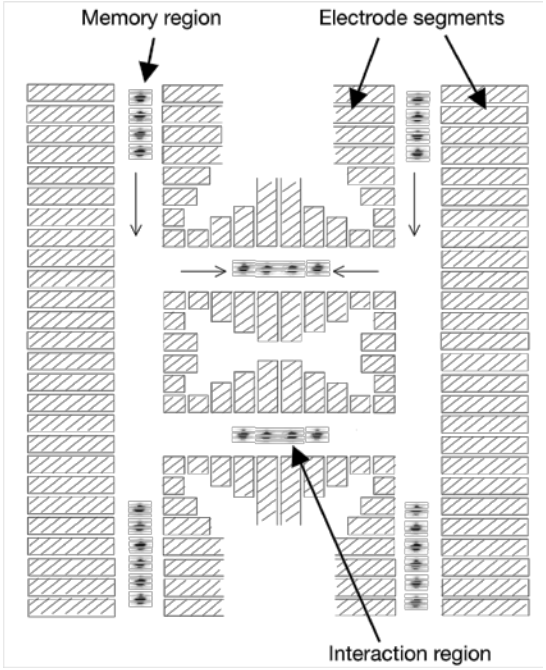
Possible geometries

multi-layer technology advantages

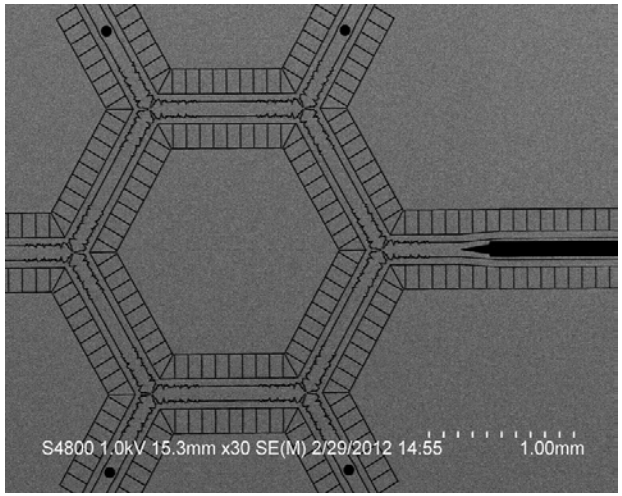


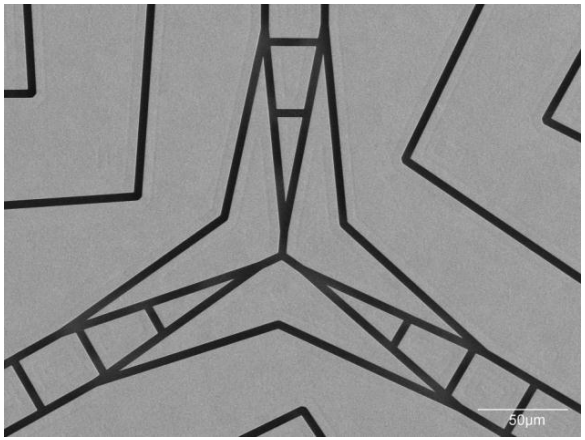
D. Kielpinski, *et al.* Nature 417, 209 (2002).

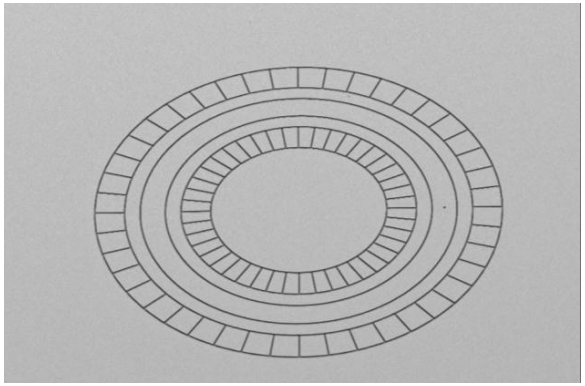
4-level-metal devices allow for:

- No exposed routing
- Islanded electrodes
- New topologies
- 5th layer for μ-wave delivery

Imagine your trap geometry:
it can be realized





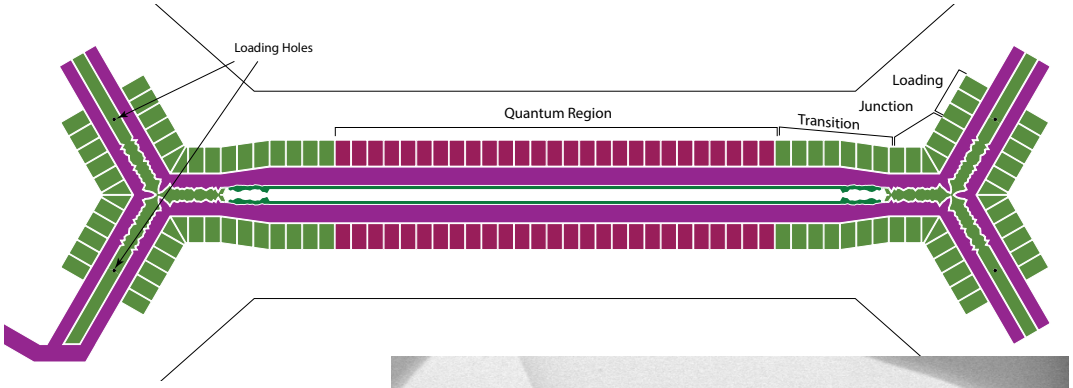


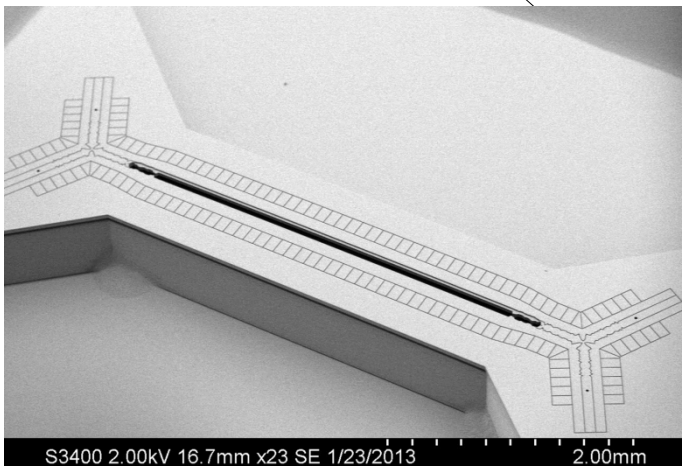
Sandia National Laboratories

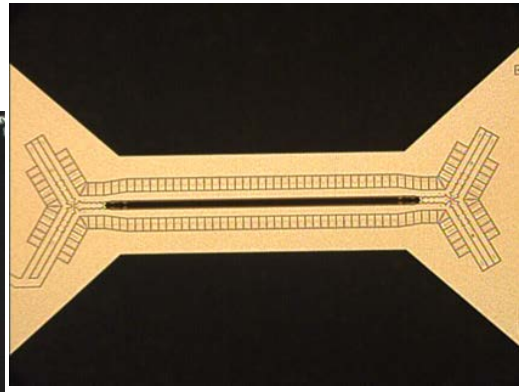
HOA trap platform
high optical access trap

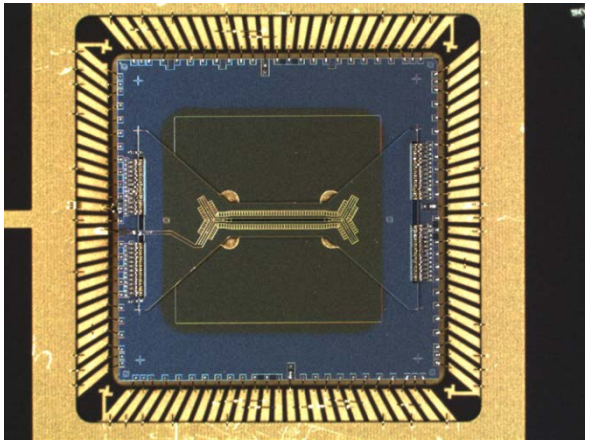
Optimized surface electrode trap platform for QIP

- Release singulation
- Unique shape
- Greatly improved optical access:
  - Larger trap depth
  - Higher trap frequencies
  - Less optical scatter



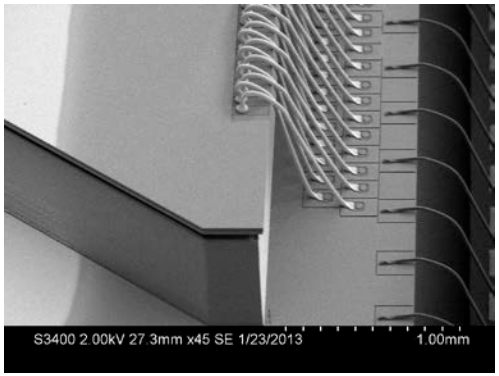


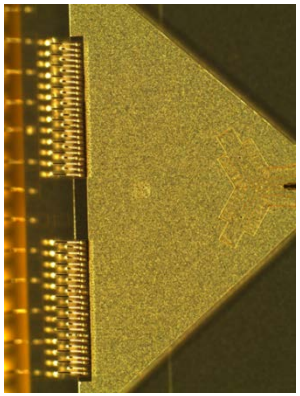


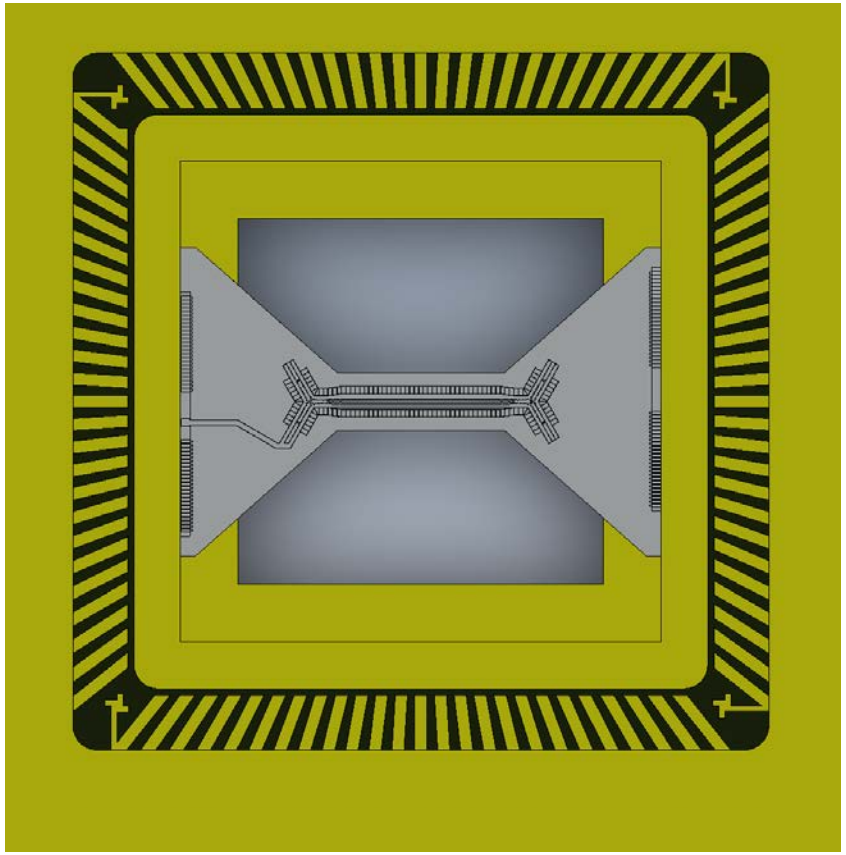


Interposers for Surface Traps

- Chip-to-interposer wires give unobstructed laser access to trapping region
- Redistribution layer (RDL) routes trap I/O (2-sides) to package (4-sides)

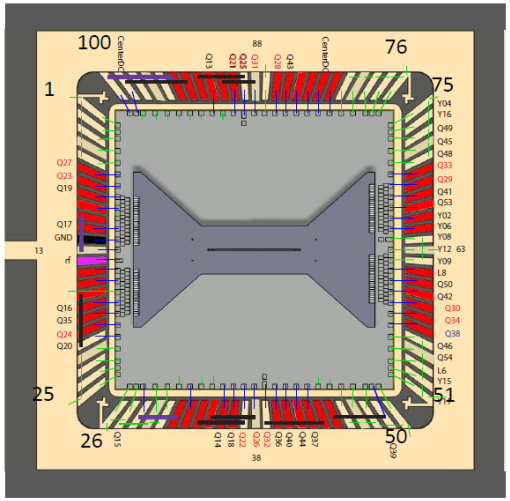






Sandia 48-pin chambers

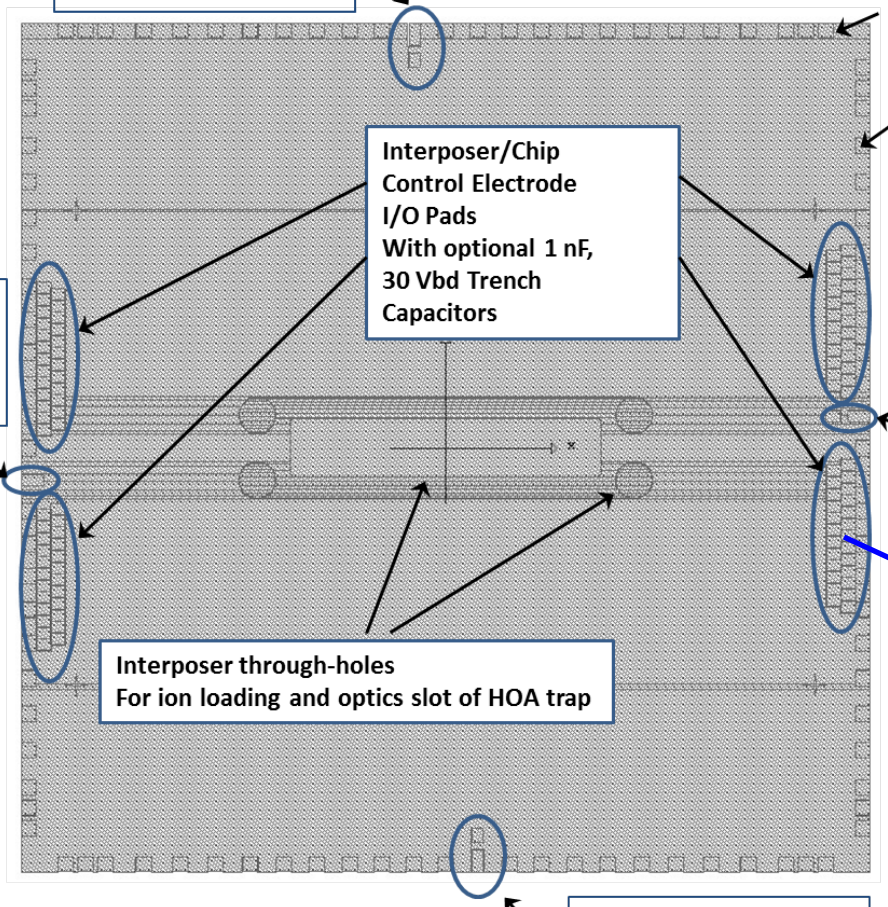
Version 5

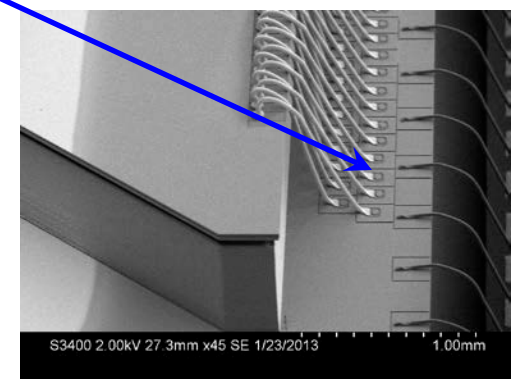


rf gnd
rf
Control
GND
Not used. The trap may short these pins to ground or to control pins.

- Interposer can support:
  - Passive and active electronics
  - Future and (some) existing traps

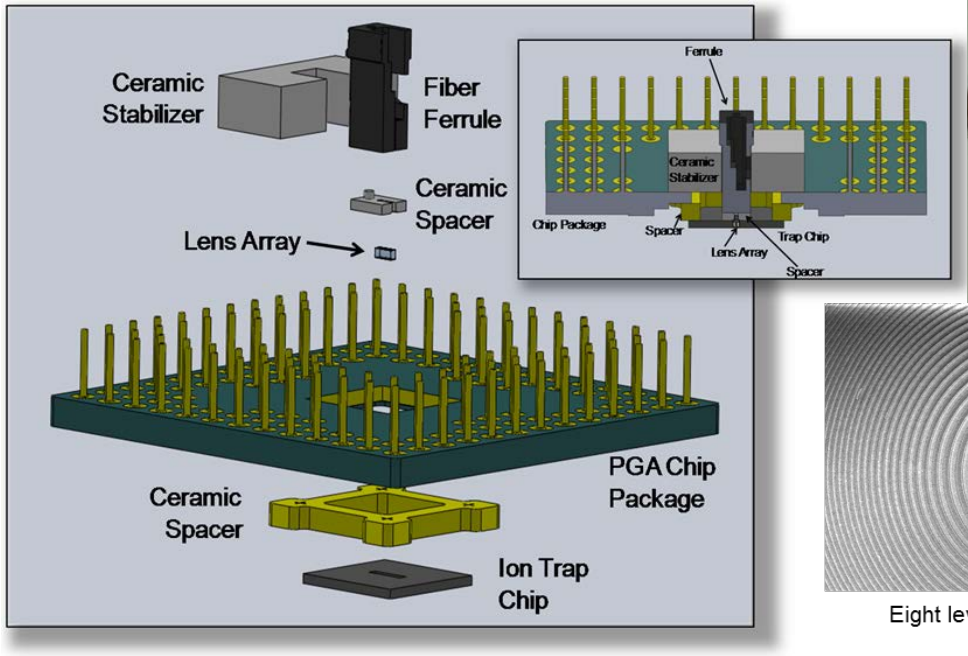
Interposers for Surface Traps

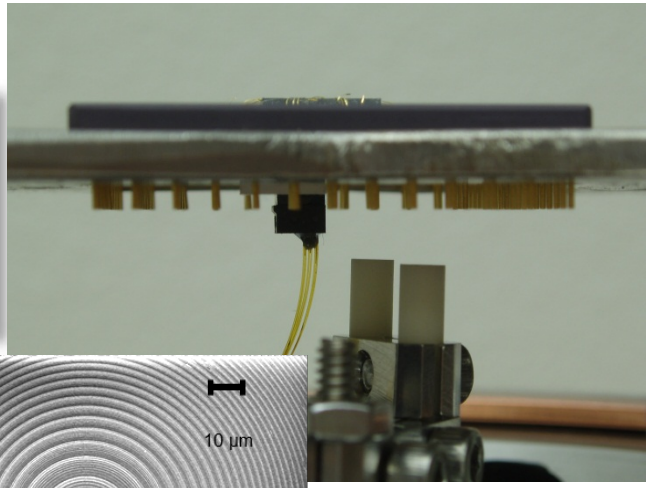


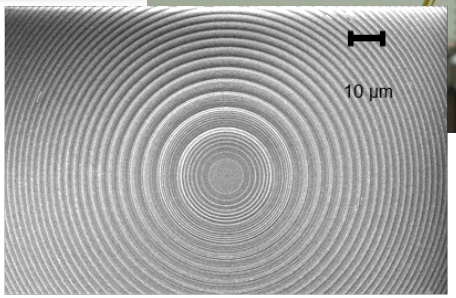


SNL Surface Ion Trap Interposer Chip

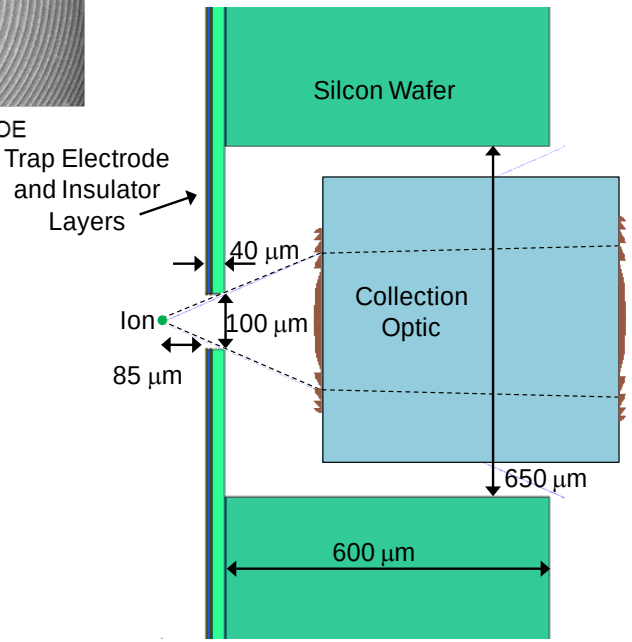
Integrated Optics







Eight level F/1 fused silica DOE



- **Optics have been integrated into linear surface ion trap.**
- **No detrimental effects to ultra-high vacuum.**
- **Successful shuttling with same voltage solutions as linear trap without integrated optics.**
- **Compensated any charging on dielectric lenses.**
- **Dielectric lenses ~150 microns away from ion.**

G. R. Brady, *et al.* Appl. Phys. B: Lasers and Optics 103, 801-808 (2011).

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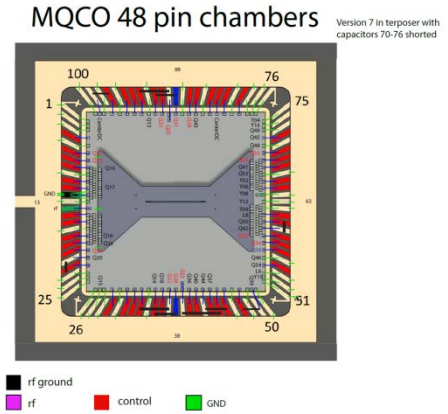
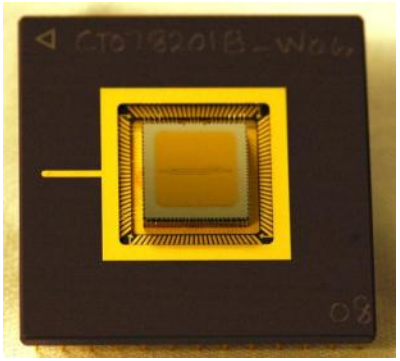
Packaging and testing

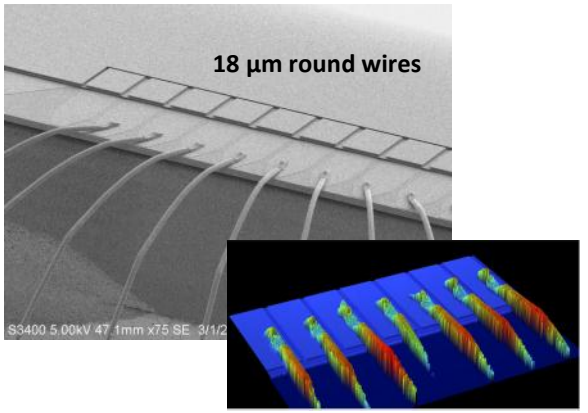
Sandia National Laboratories

Plug-and-trap design





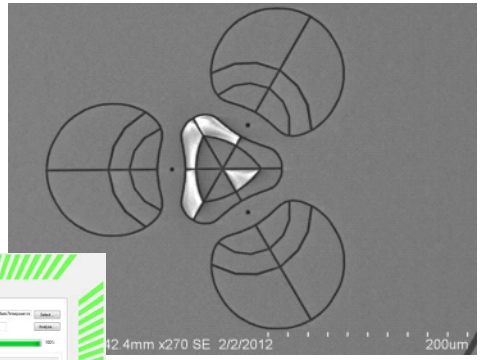
Low profile wirebonding

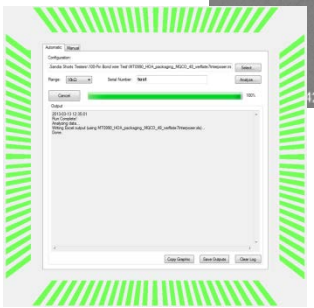


Plug-and-trap design

- Standard package part for chip ion traps
- Most trapping groups can accommodate the package
- Low profile wirebonds: good optical access
- Checks for opens and shorts > 40 MΩ

Parametric verification





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Trap operational testing

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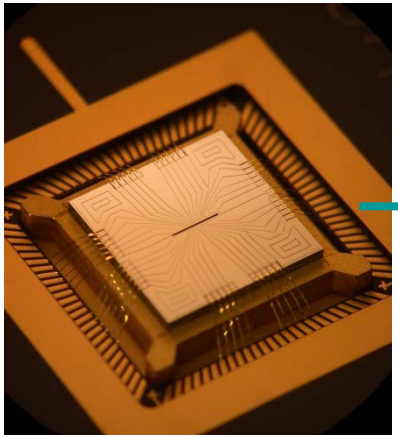

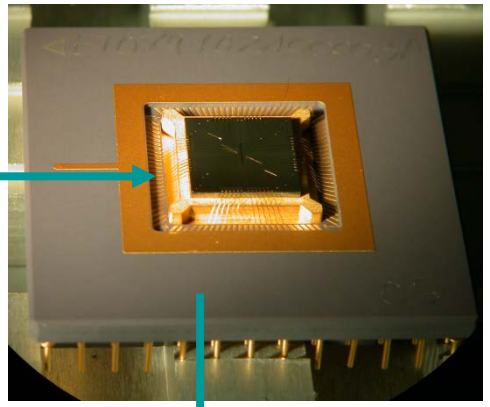

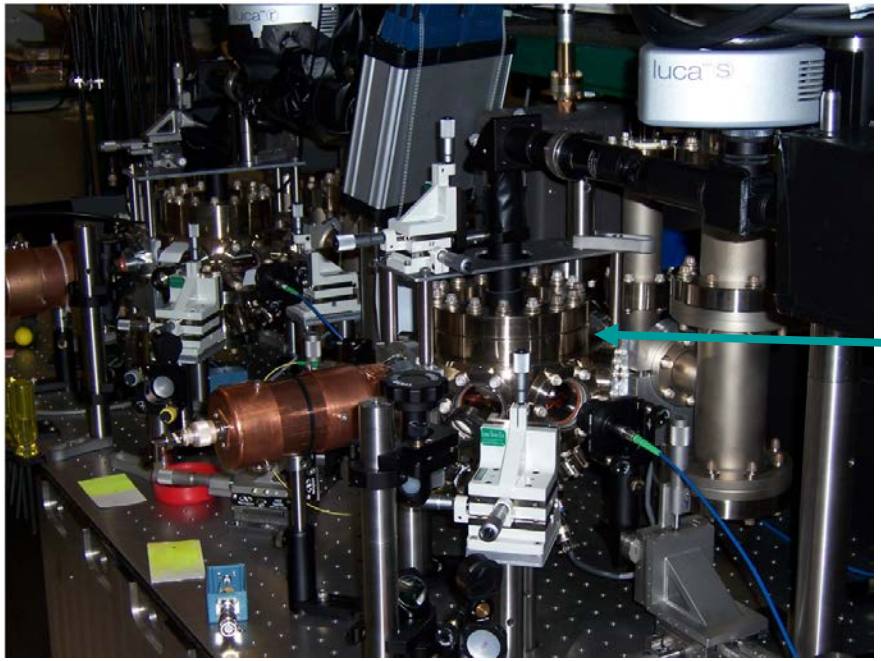

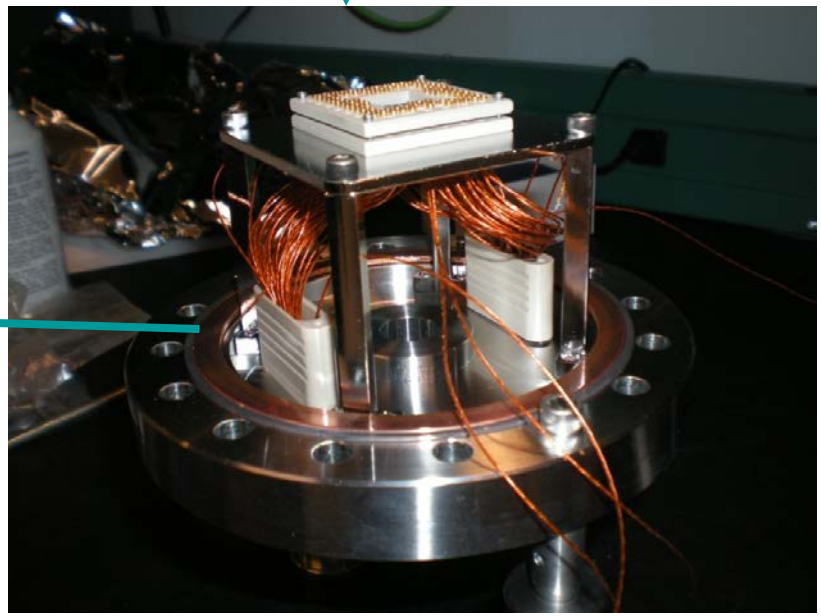

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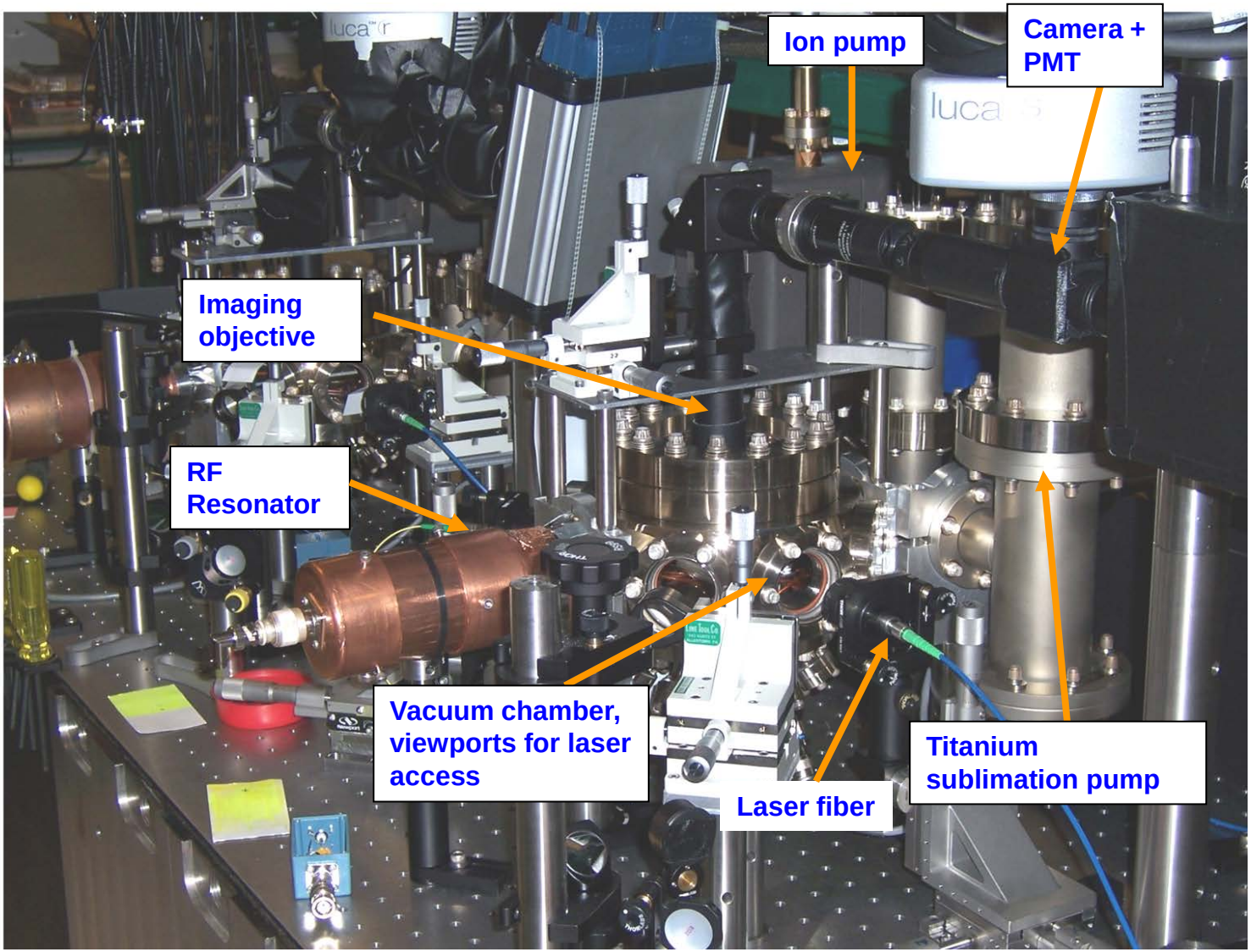
Trap operational testing



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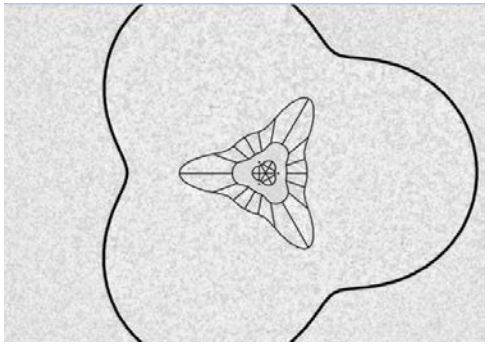
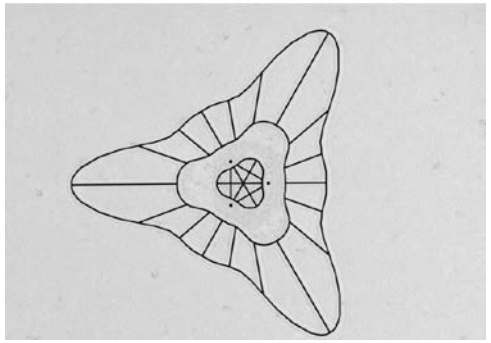
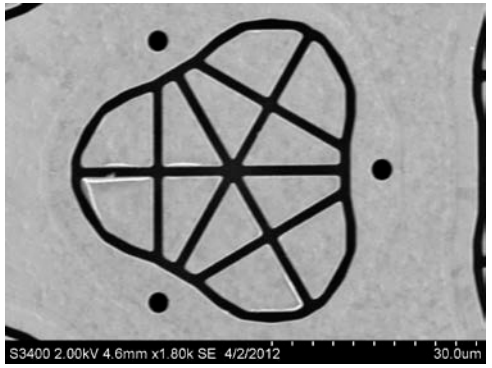
Triangle Trap Rev. 0 – 80 µm, 40 µm triangles

Sandia National Laboratories

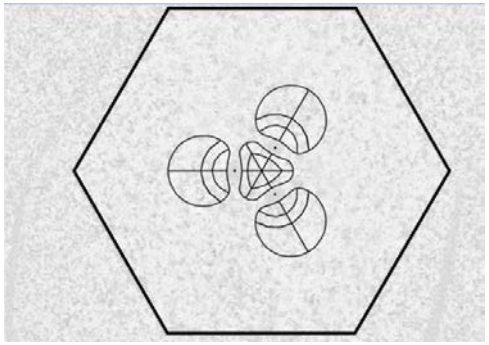
40 µm triangles

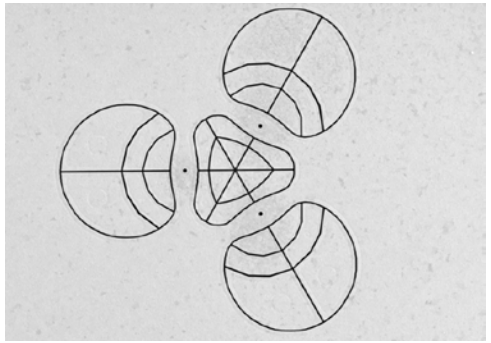


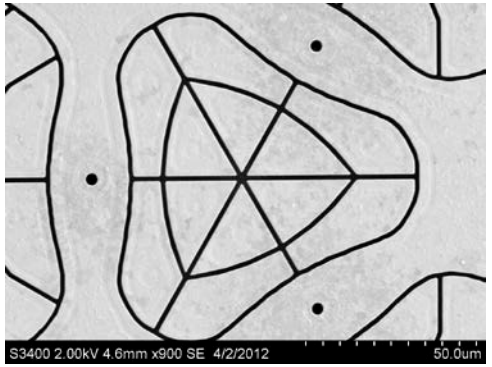




80 µm triangles







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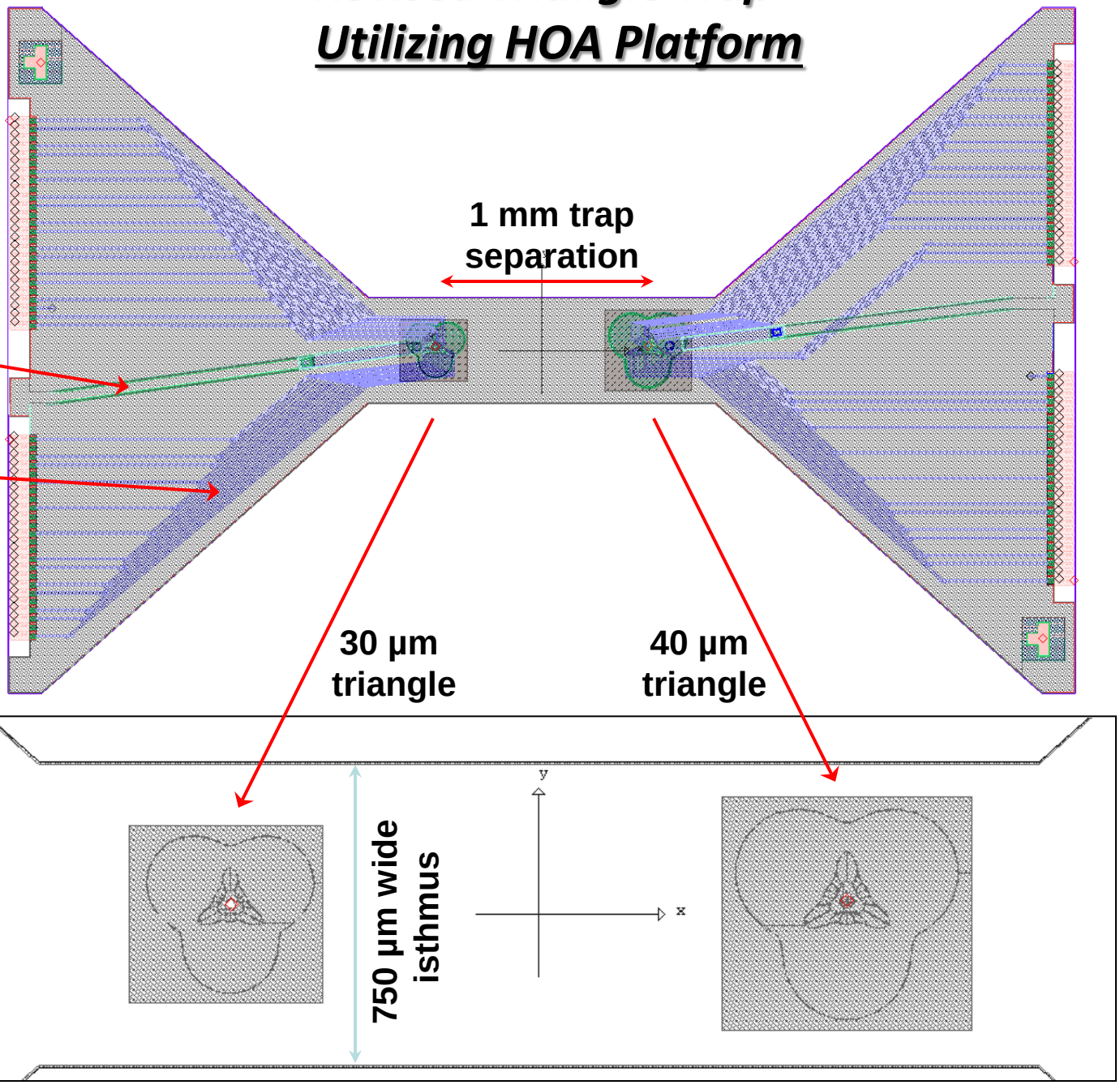
Sandia National Laboratories

Revised Triangle Trap Utilizing HOA Platform

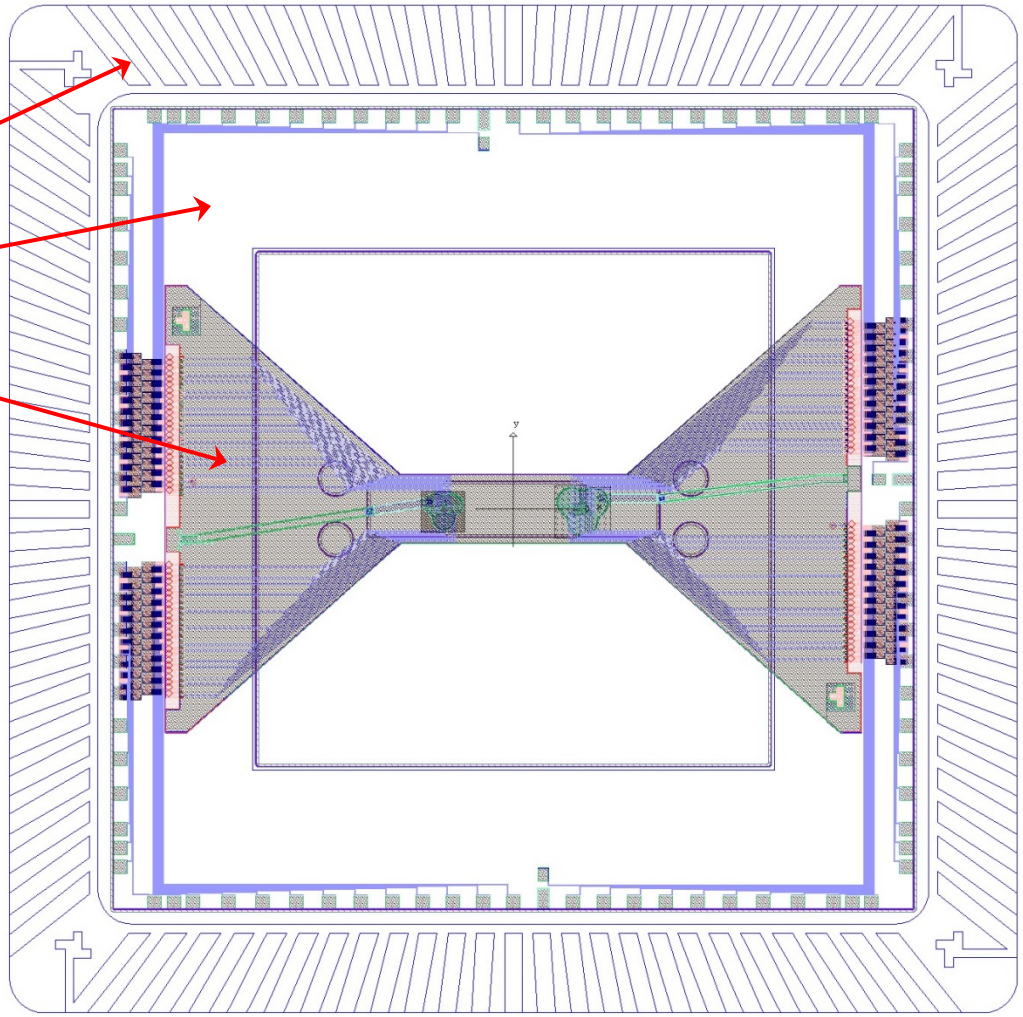
- Independent RF leads
- Independent DC controls



Sandia National Laboratories

Revised Triangle Trap Packaging Design

- Package
- Interposer
- Trap Chip



Trap Status

Triangle Trap

- Utilize existing 40 µm triangle design
- Add scaled 30 µm triangle design
- Layout complete August 2013
- Photomasks ordered, lot start September 2013
- Device fabrication/packaging completed March 2014

Hex + 1 Trap

- Simulate/design Hex + 1 4LM surface electrode trap utilizing concepts of hexagonal Kitaev trap array (Didi to discuss)

- Perform device layout for Hex + 1 ion trap
  - Independent control for 4 ions in Y configuration

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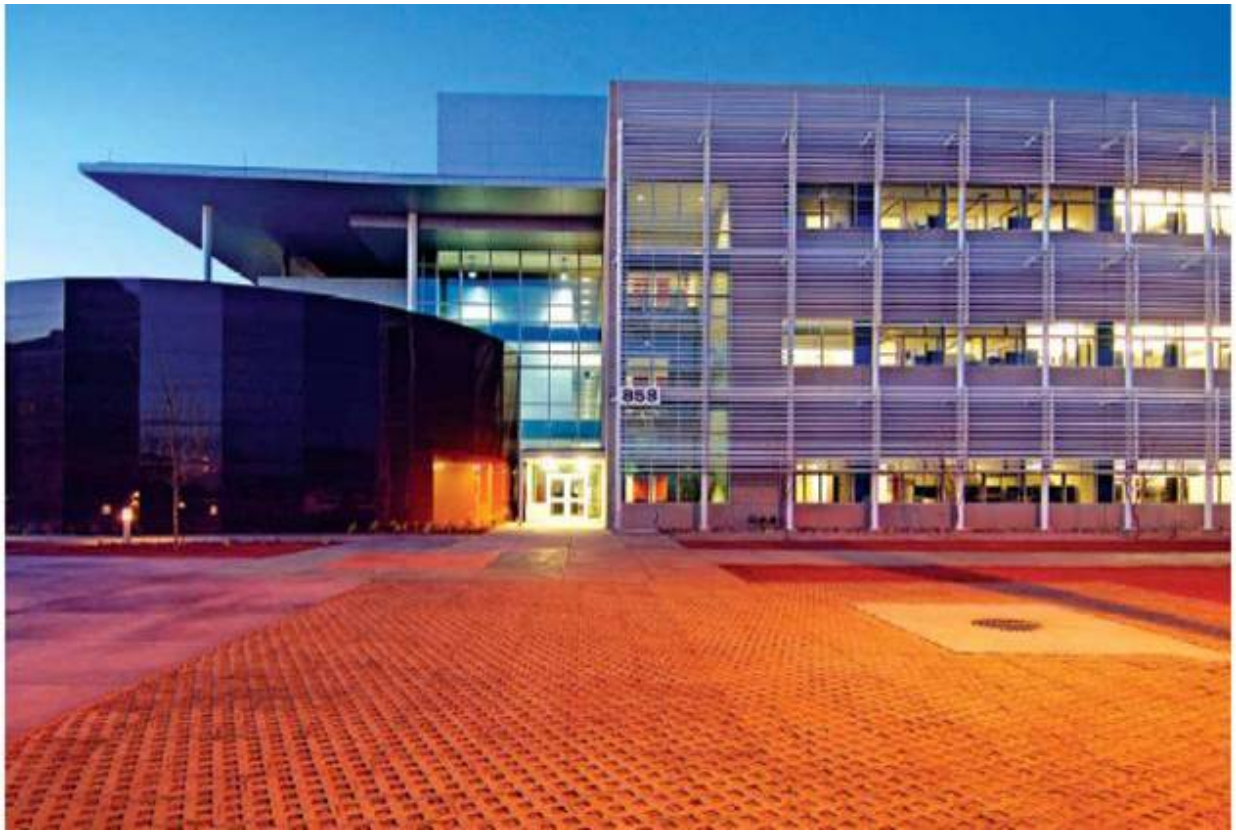
Surface Electrode Ion Trap Technology Overview

Matthew Blain – Org. 1725

6 August 2013

Laboratory Directed Research & Development



Experimental
D. Stick
P. Maunz
K. Fortier
D. Sterk
C. Tigges
B. Tabakov
F. Benito
T. Barrick
C. Johnson

Ion Traps
M. Blain
B. Loviza
A. Ortega
E. Heller
R. Haltli
D. Hollowell
L. Fang
J. Gallegos

Micro-Optics
S. Kemme
R. Ellis
R. Boye
A. Young
S. Samora

MESA Staff:
→SiFab/µFab

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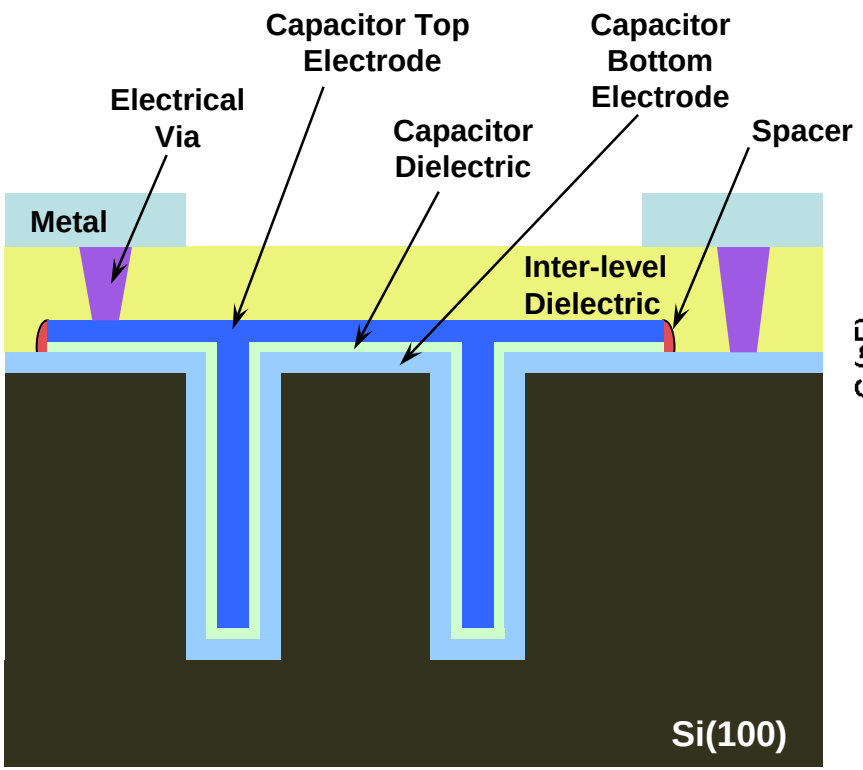
Integrated Trench Capacitors

Trench v. Surface Capacitors for Surface Ion Traps

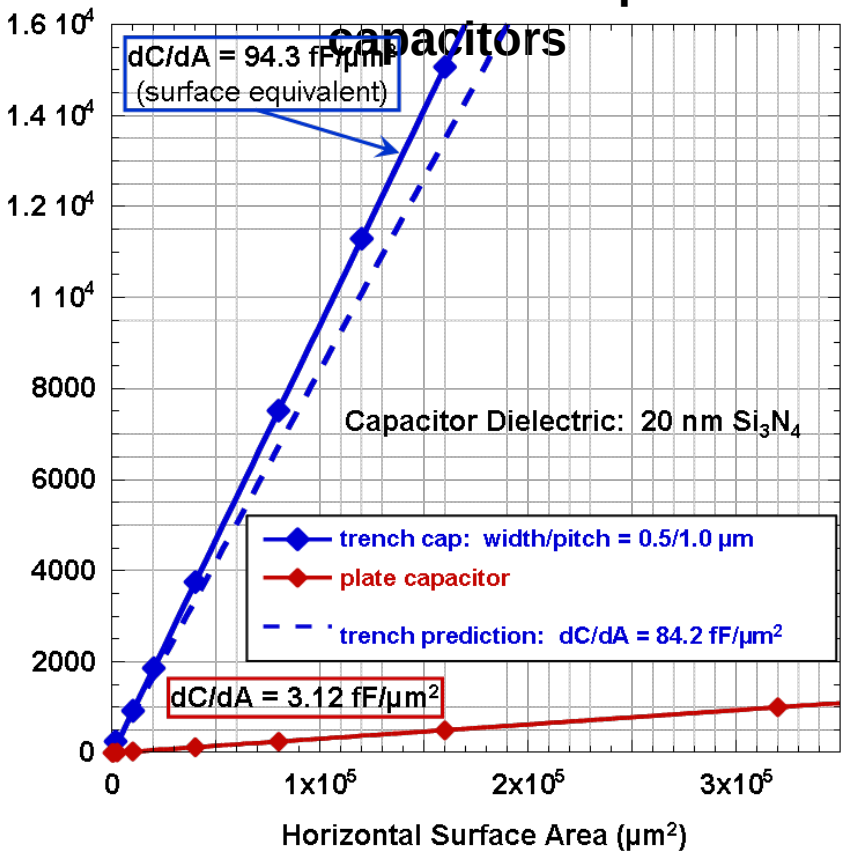
- High-k dielectric surface areas: still large
- Thin dielectric challenges: yield, reliability
- Vertical surfaces: more available area

ATC 116 Series Microcaps
Surface mount: 1.27 x 1.27 mm², 821±20% pF

Trench Capacitor Architecture



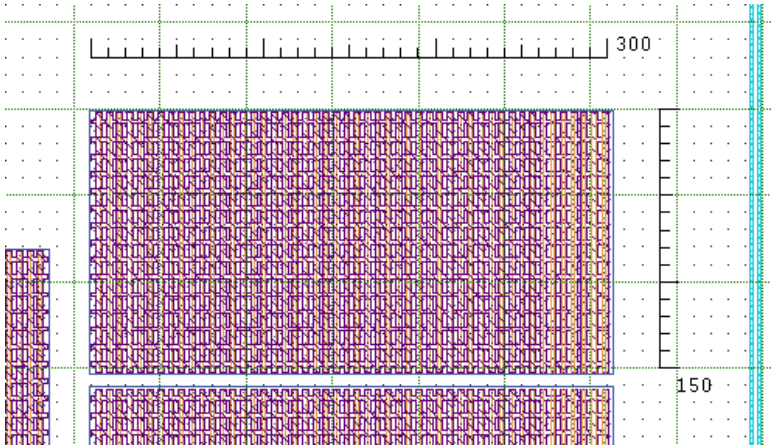
Area relationship for trench v. horizontal plate capacitors



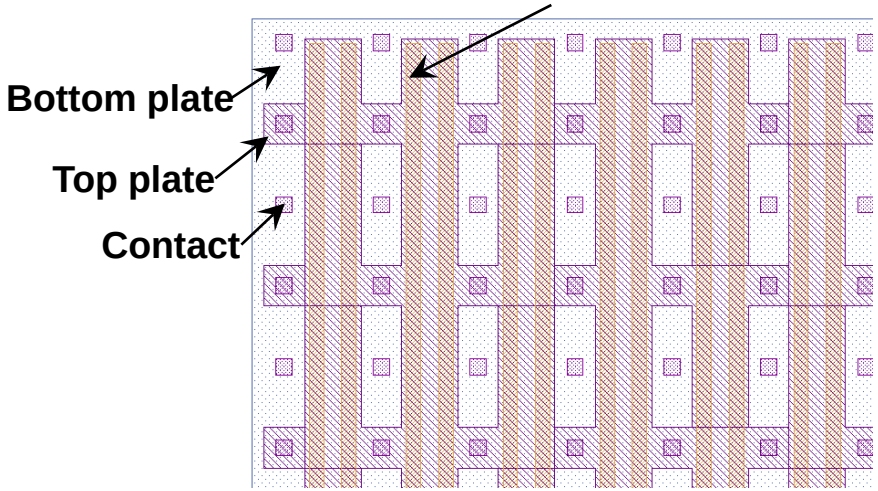
D.T.C. Allcock, *et al.*, Appl Phys B (2012) 107:913-919

Integrated Trench Capacitors

1.05 nF trench cap, 0.045 mm^2/cap



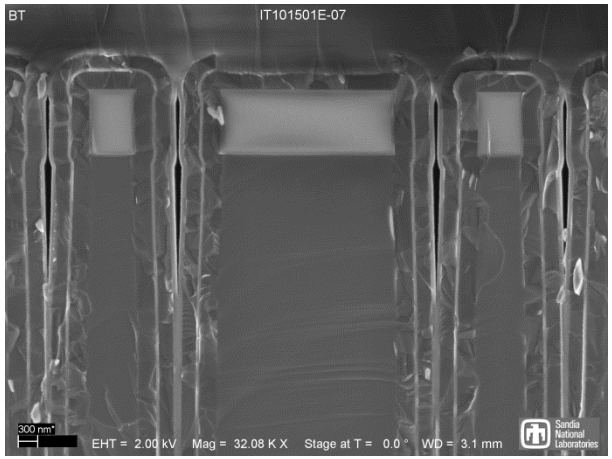
Trenches: 1 µm wide, 150 µm long, 19 µm deep



Top plate: 250 nm n-type a-Si

Dielectric: 40 nm Si_3N_4

Bottom plate: 300 nm n-type a-Si



19 µm