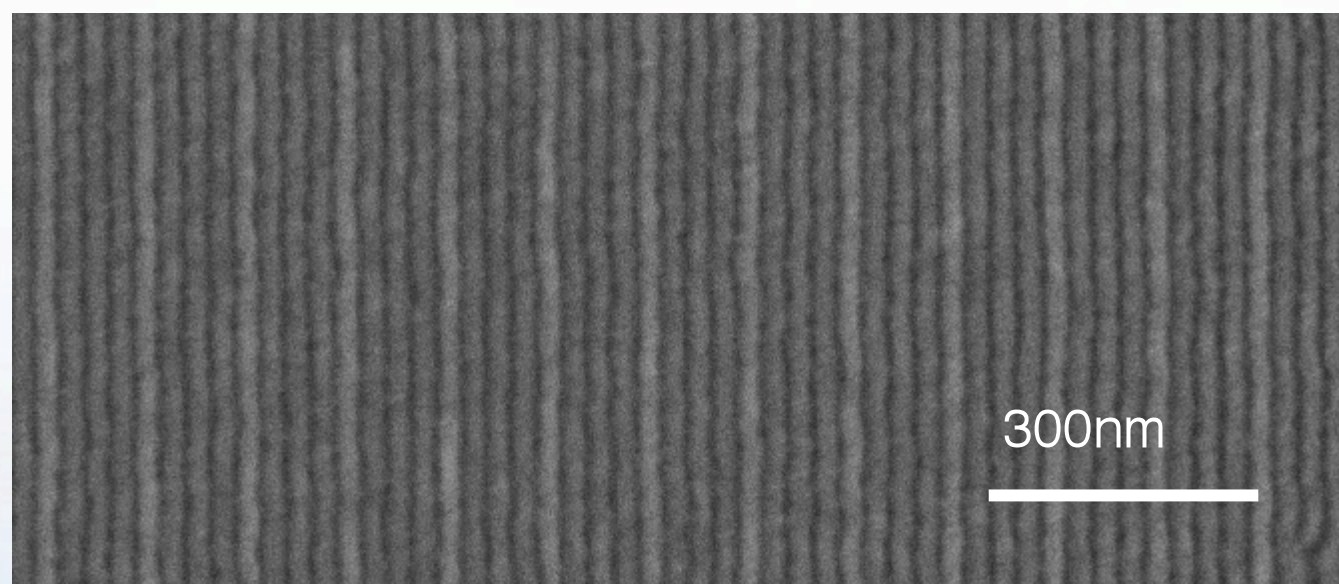
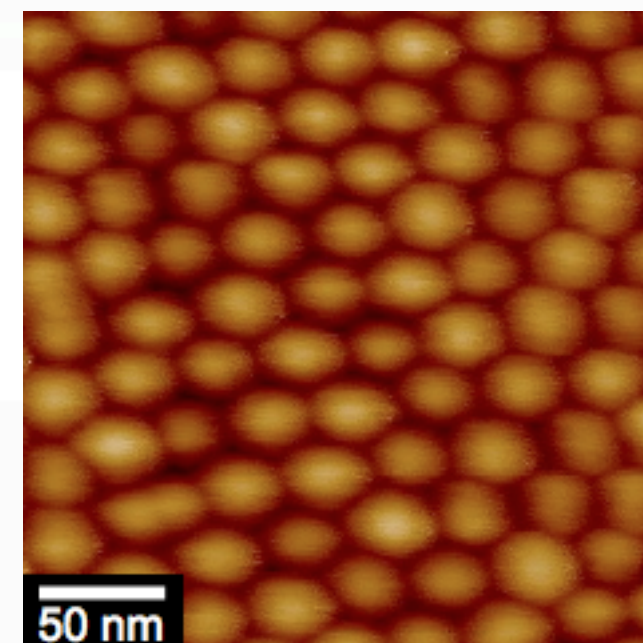
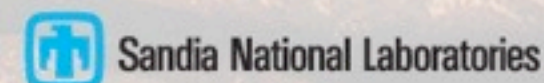


# Patterning and Integration of Ferroelectrics and other Functional Nanostructures



**Geoff Brennecka**  
Sandia National Laboratories



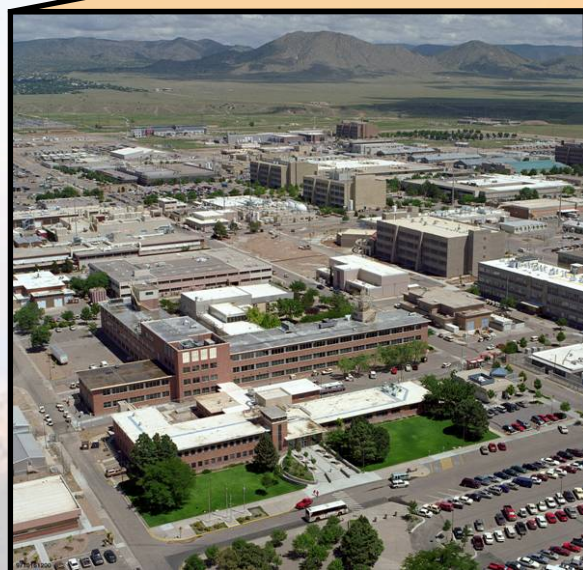
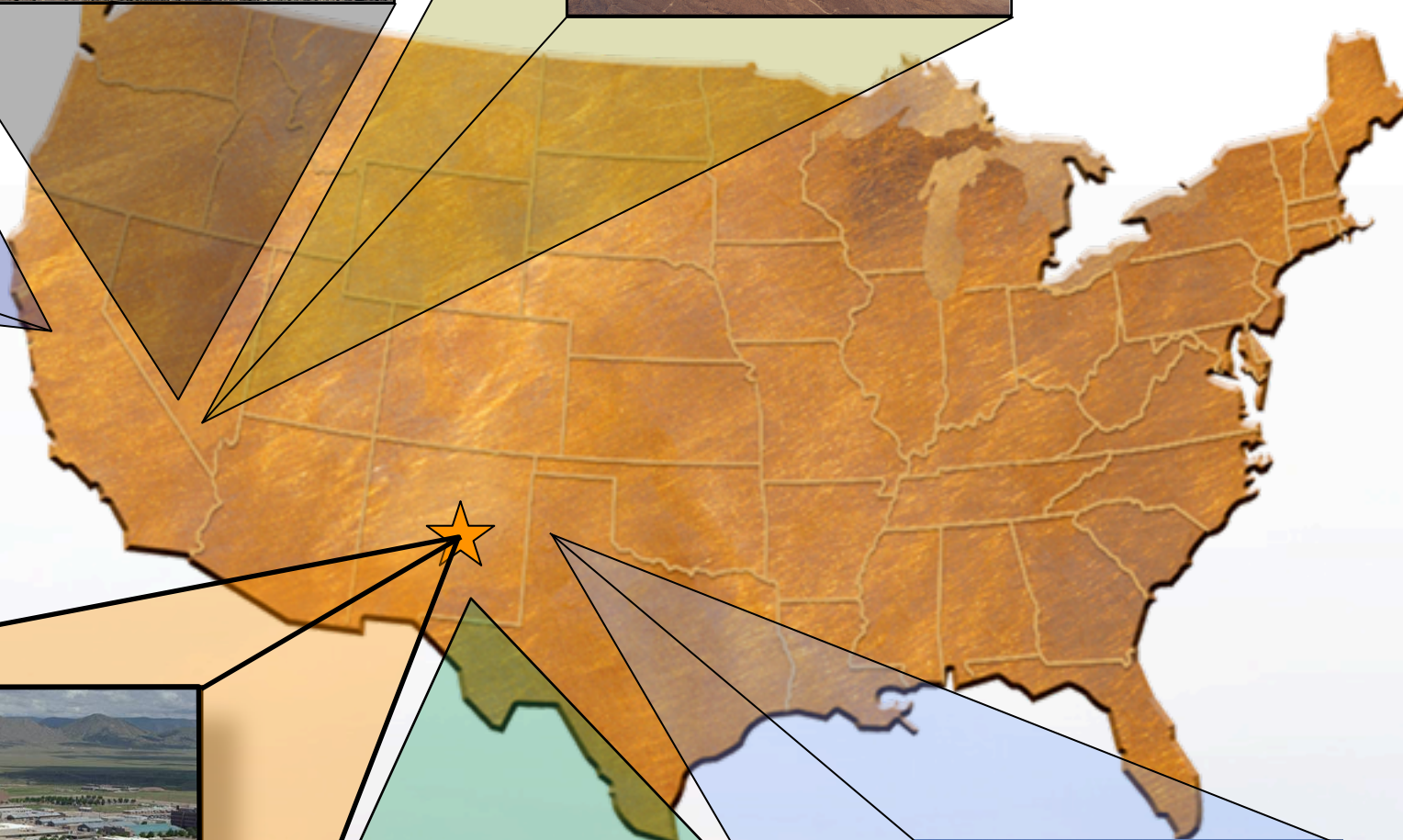
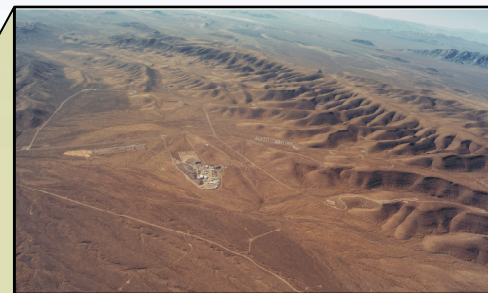


# National Laboratories and Production Sites





# Sandia National Laboratories





# Sandia National Laboratories: 60 Years of Exceptional Service in the National Interest



- National Security Laboratory
- Broad mission in developing science and technology applications to meet our rapidly changing, complex national security challenges
- Safety, security and reliability of our nation's nuclear weapon stockpile

Sandia is #1 in total citations of energy and fuels research and 3 in papers cited in photonics research.





# We're Hiring...

- ~8000 full time employees
- ~2500 retirements in FY09-11
- Average tenure ~23 years
- ~200 MatSE hires expected in 2011-2012

*US citizenship required for most (not all!) positions*

**SNL is the largest employer of Illini outside of the state of Illinois**





# Sandia's Work



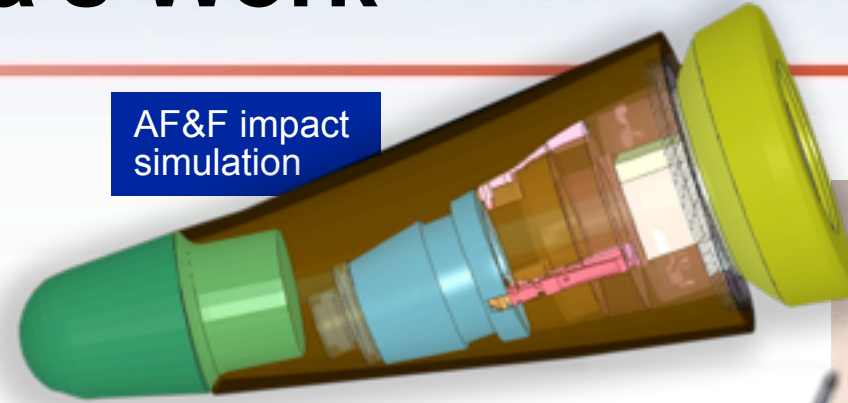
Shuttle Orbital  
Inspection System



## 4 Mission Areas

- Nuclear Weapons
- Defense Systems and Assessments
- Energy, Resources, and Nonproliferation
- Homeland Security and Defense

AF&F impact  
simulation



96% of total NW parts



Predator UAV  
with SAR

Small robotic  
vehicles



UGS

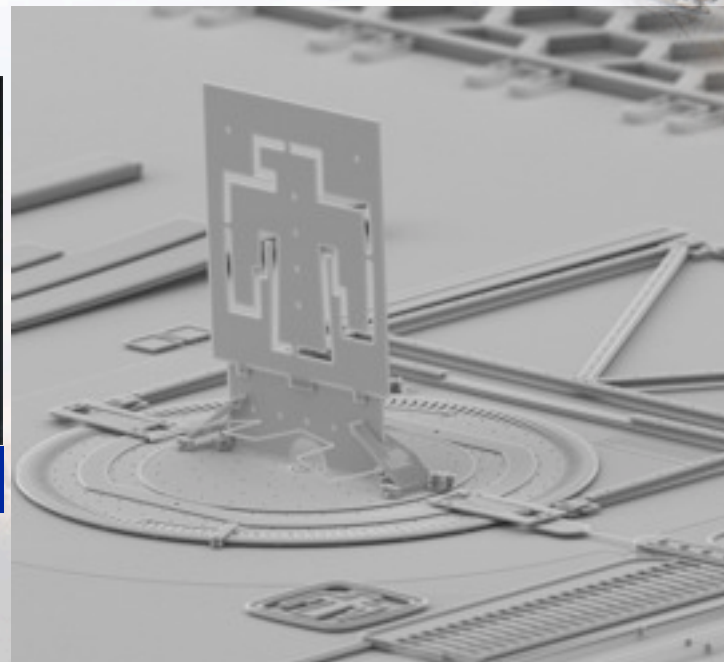


μChemLab

Renewable and  
alternative energy



Clean room invented at SNL in 1963

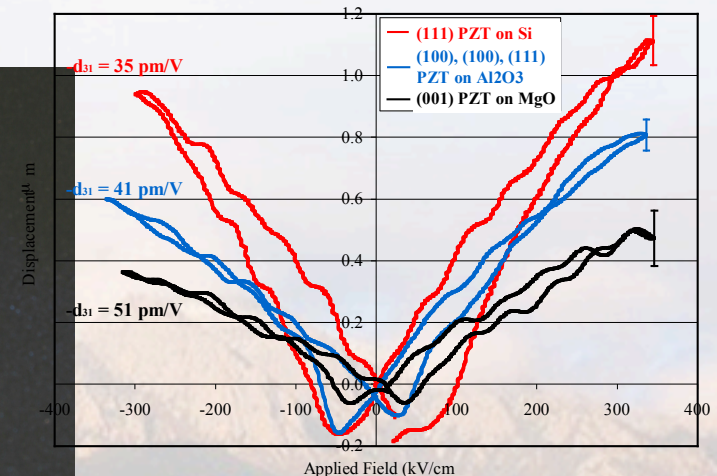
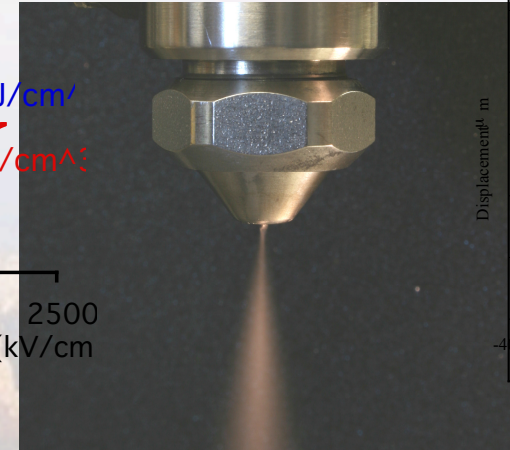
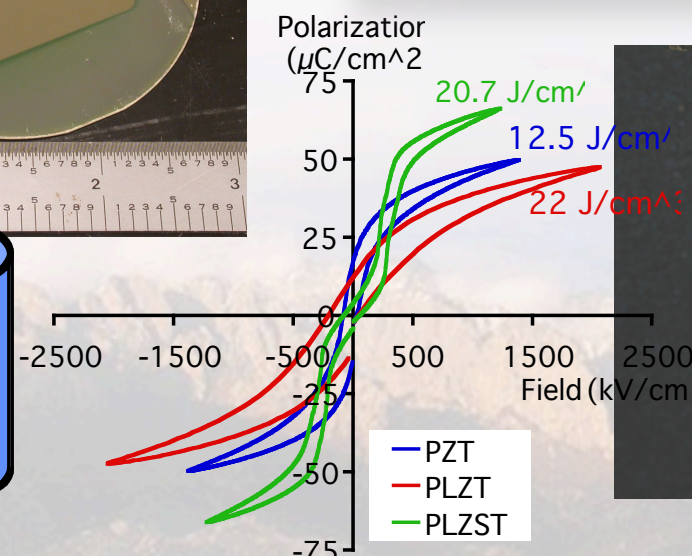
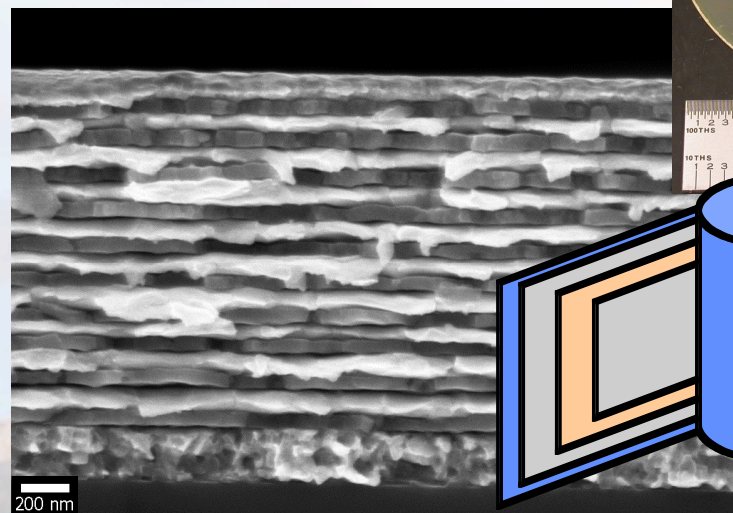
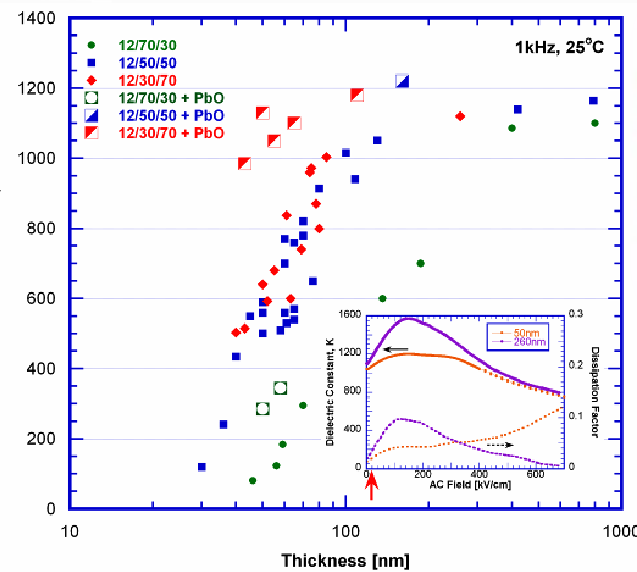
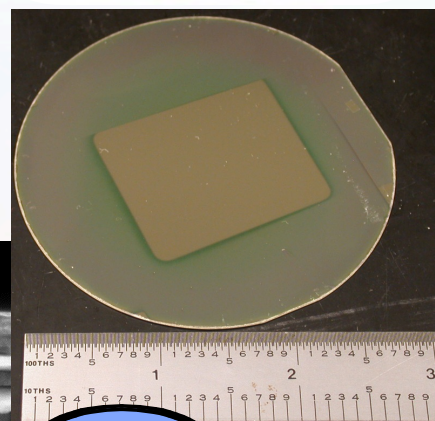
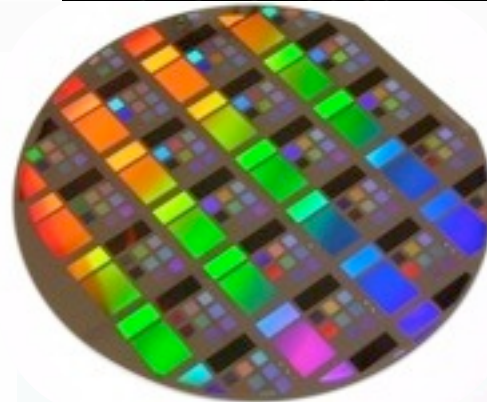
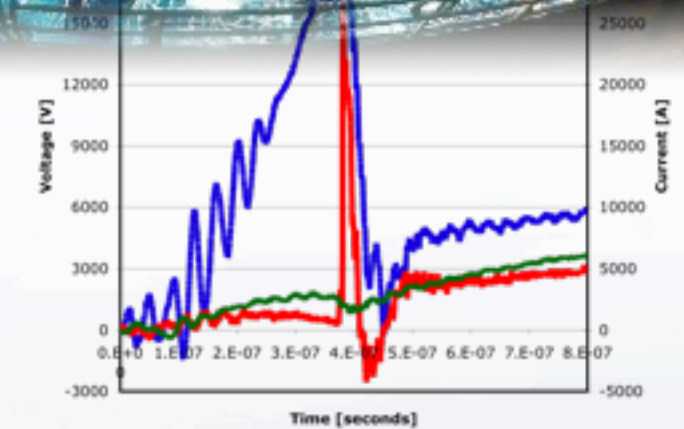
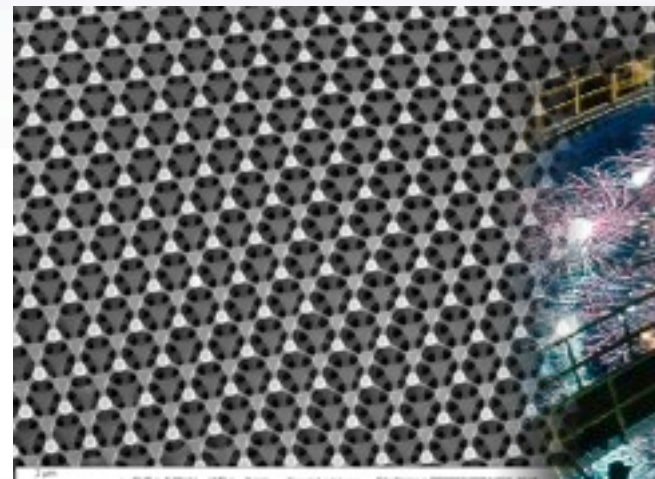
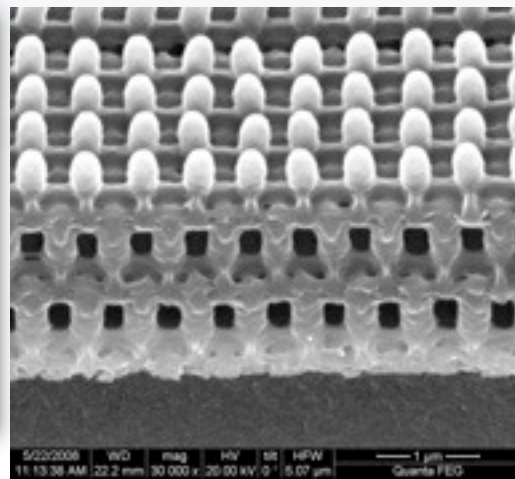
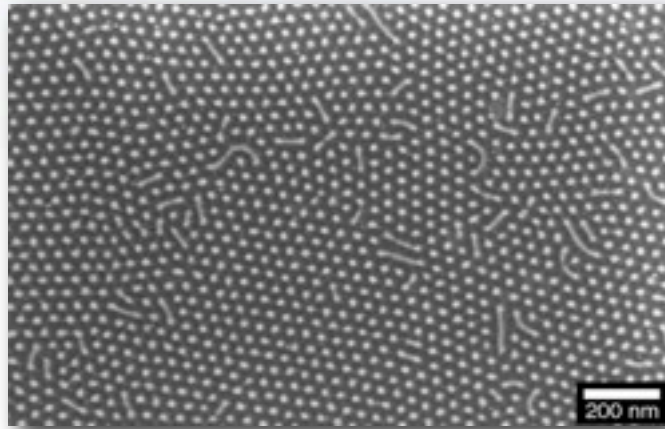


Z machine:  
the world's most powerful X-ray source



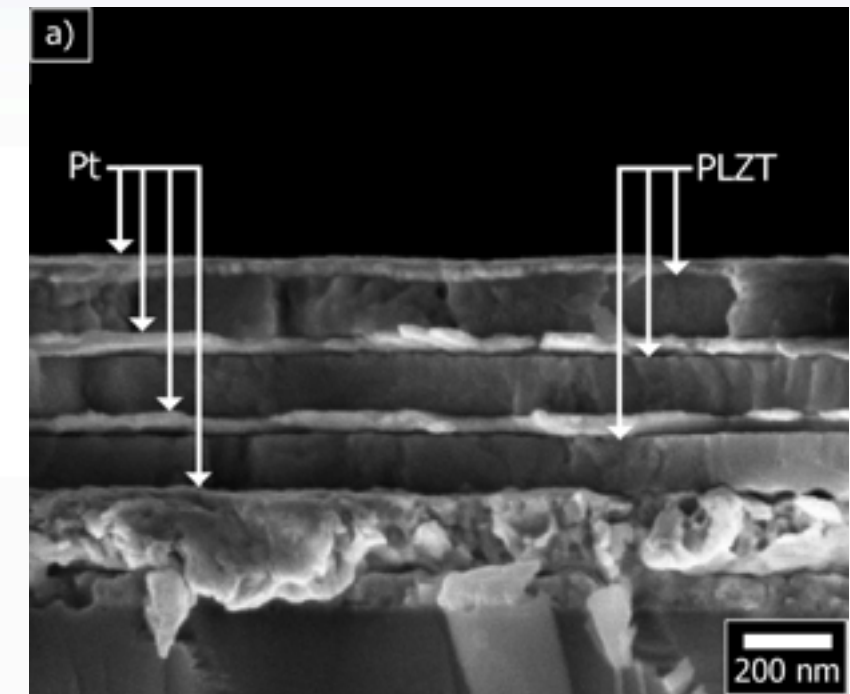
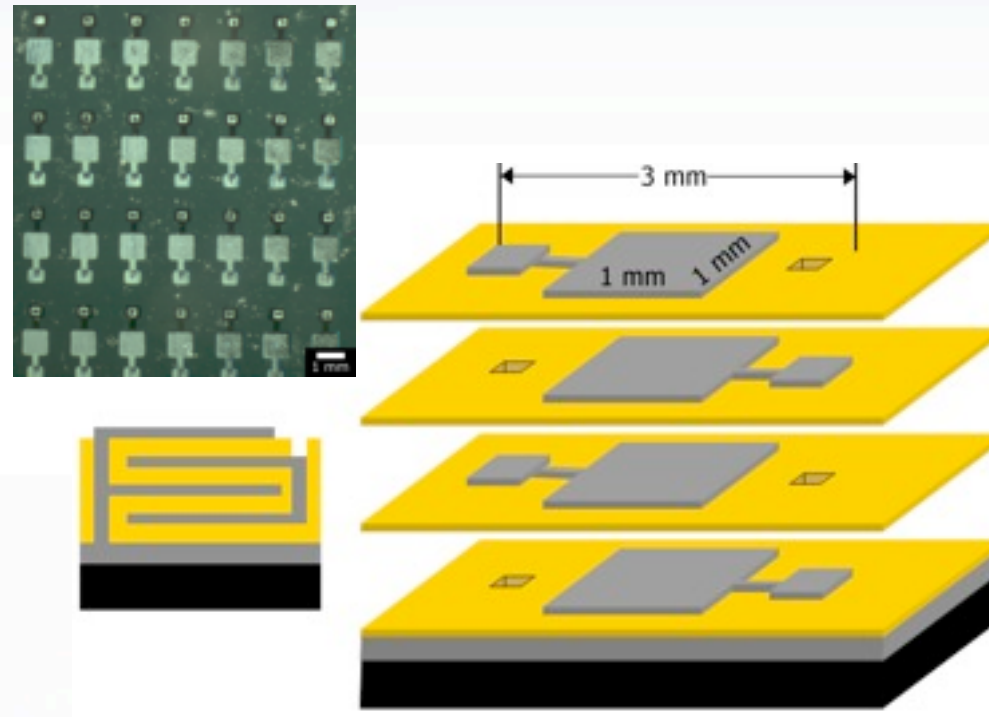
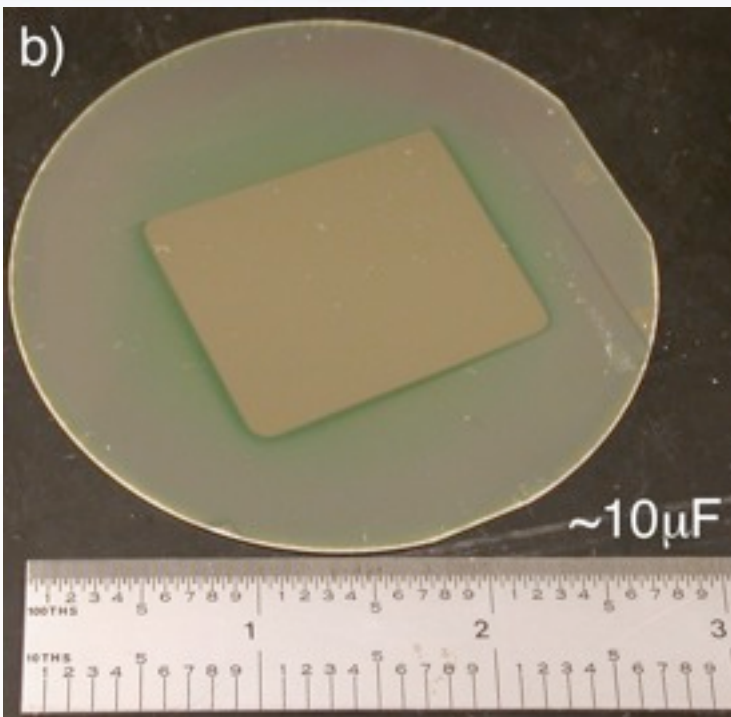


# Project Sampler

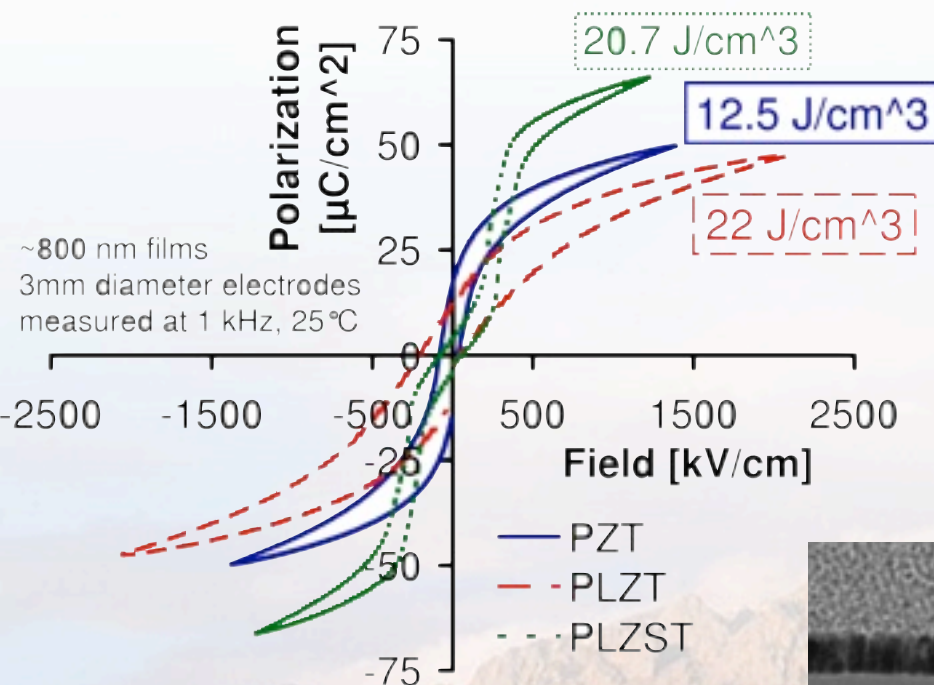




# Functional Ferroelectric Thin Films

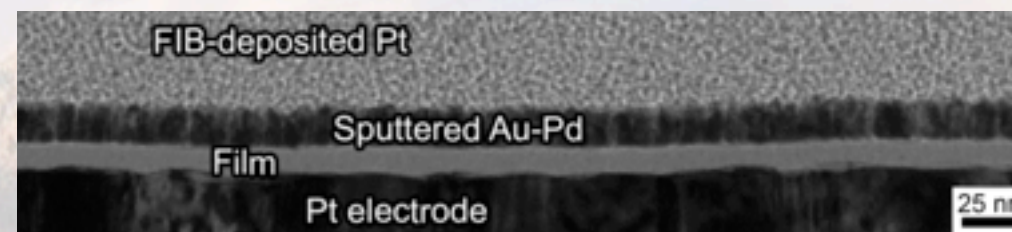


3 layers, ~120nm

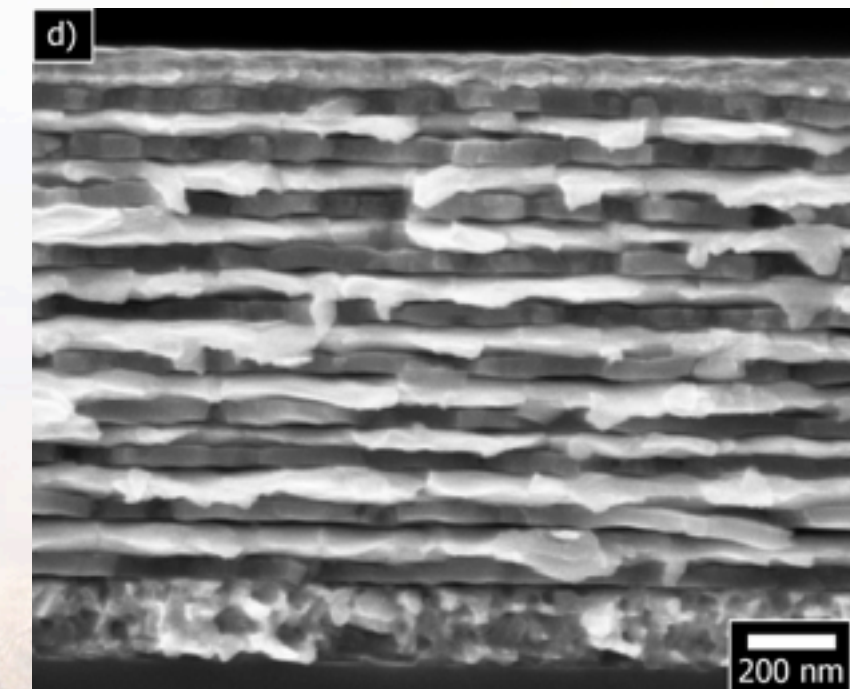


Brennecka, et al., *J. Mater. Res.* (2008),  
*J. Am. Ceram. Soc.* (2008, 2010)

*Ultimate thickness is limited  
 by wetting/islanding  
 behavior during deposition  
 and crystallization*



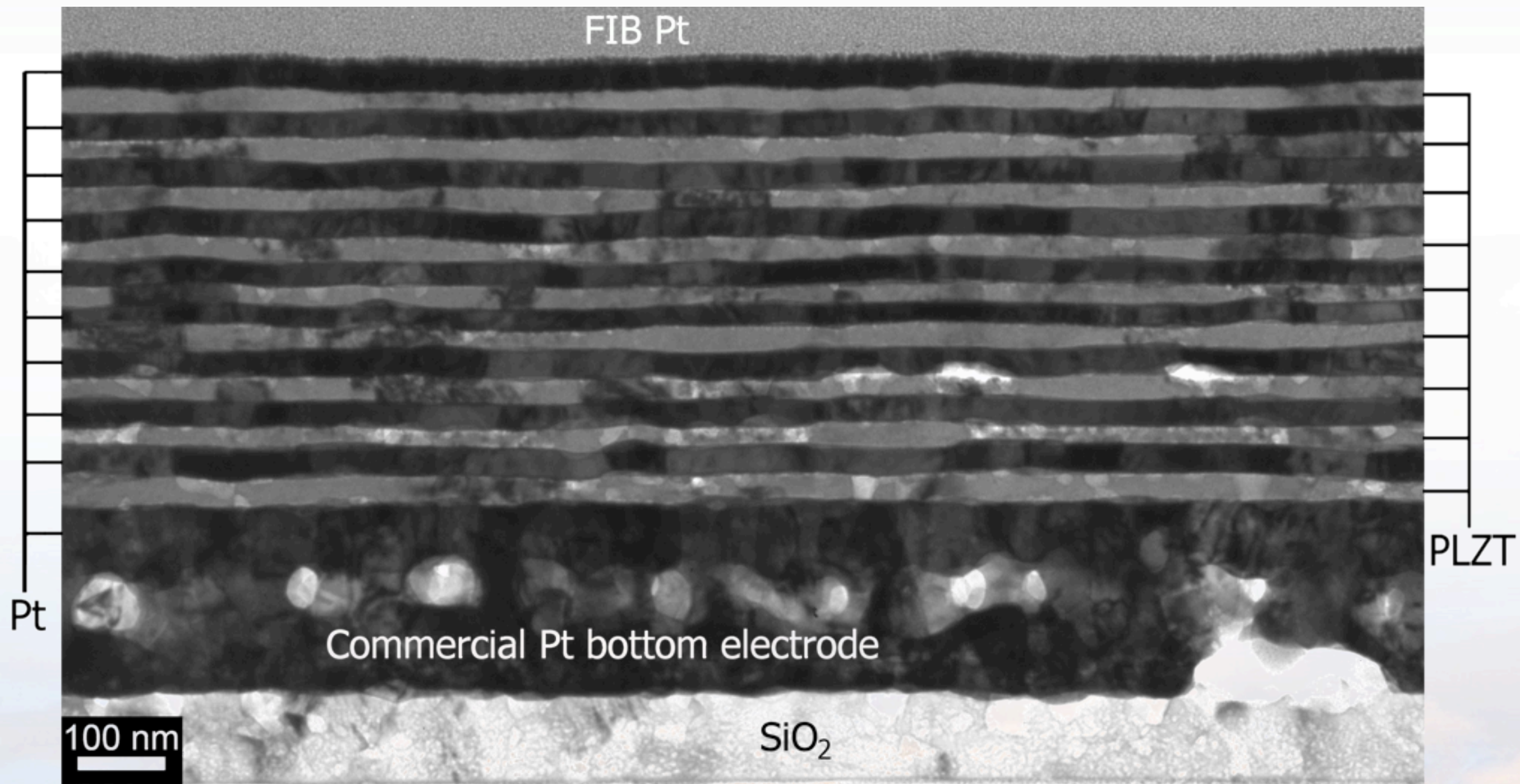
Continuous single-phase films as thin as 9nm



10 layers, ~50nm

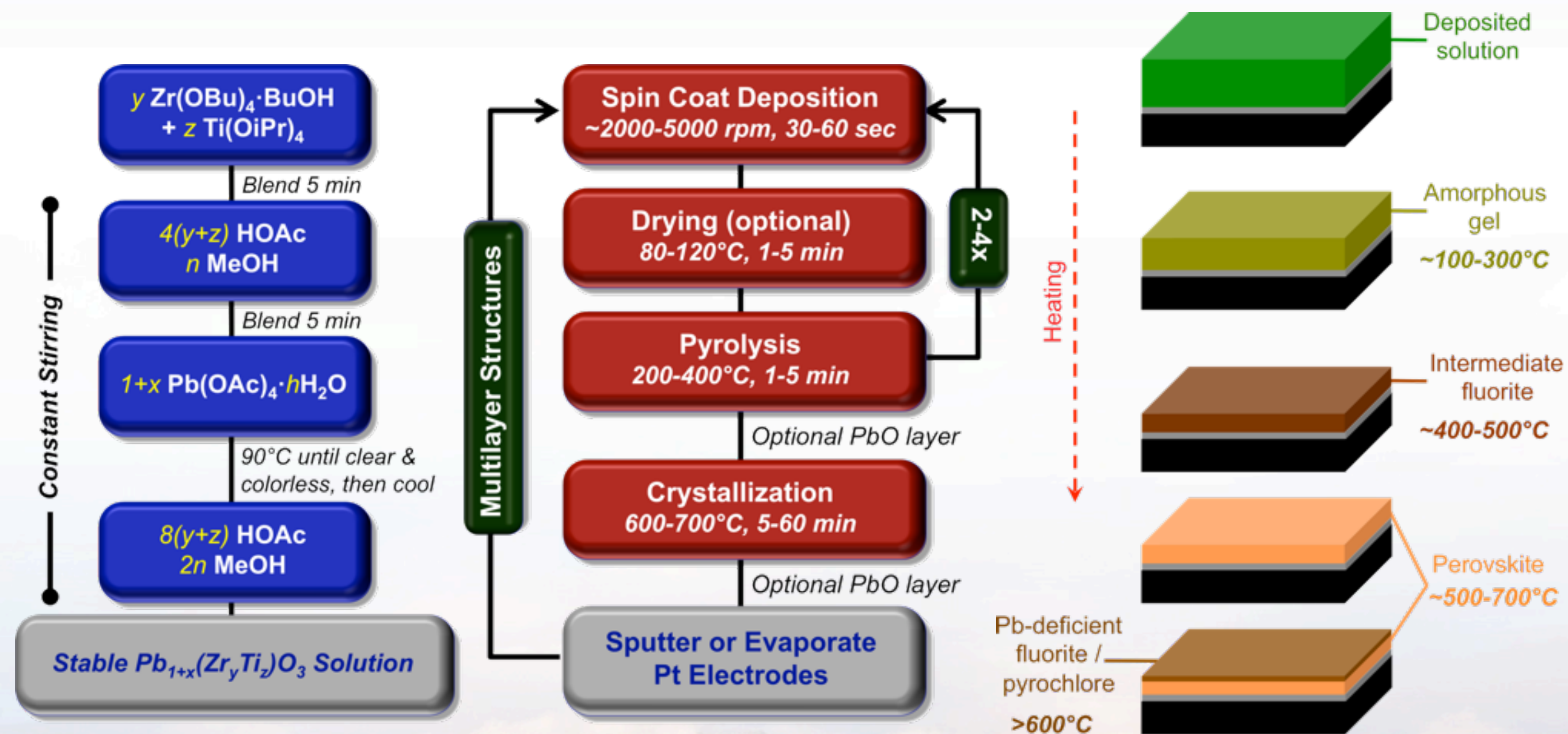


## 9 Dielectric Layers, ~20nm





# SNL IMO-based Solution Route



R.A. Assink and R.W. Schwartz; **Chem. Mater.** (1993)

G. Yi and M. Sayer; **J. Appl. Phys.** (1988)

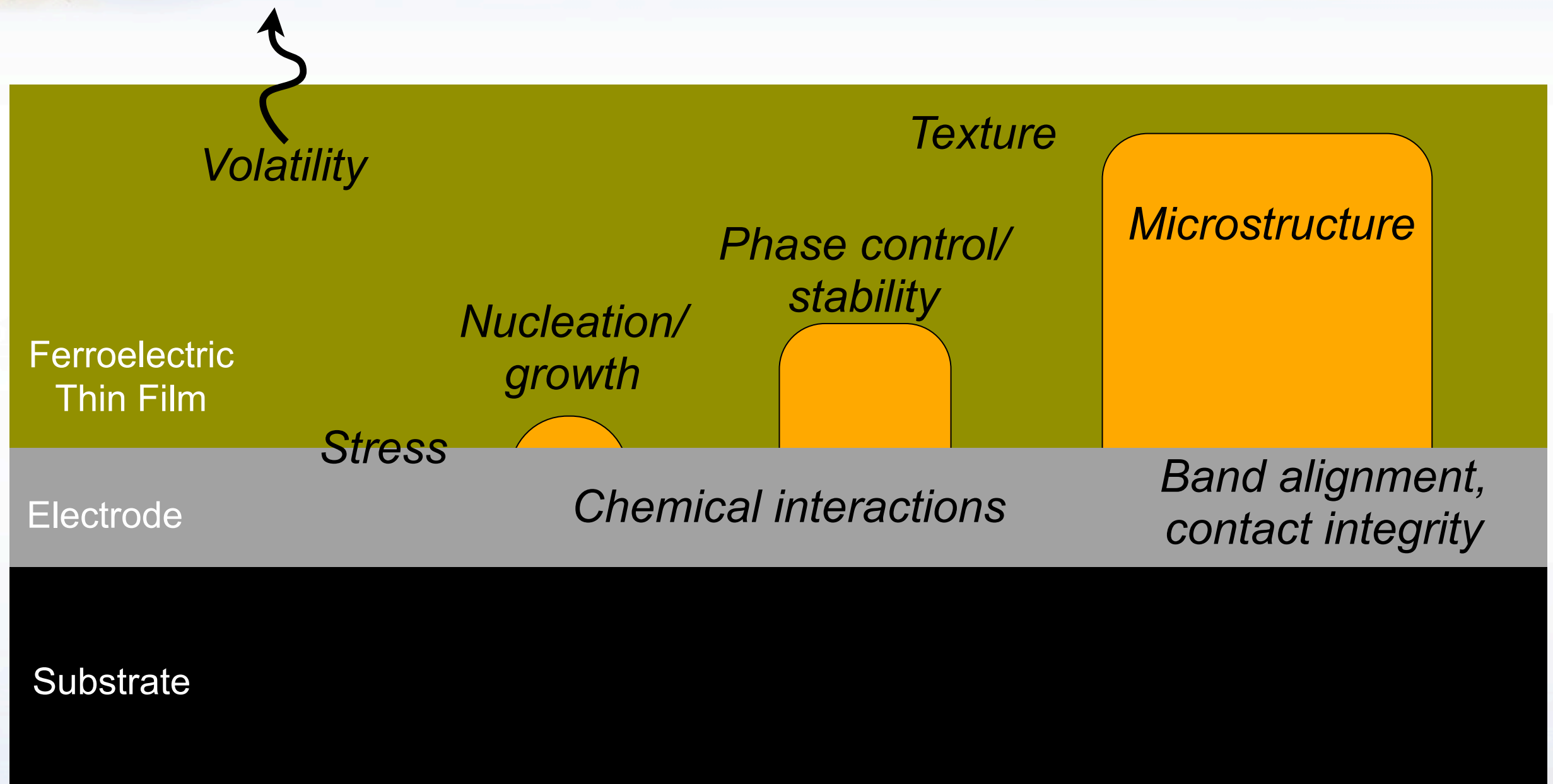
Brennecka et al., **J. Am. Ceram. Soc. feature article** (2010)



Sandia National Laboratories

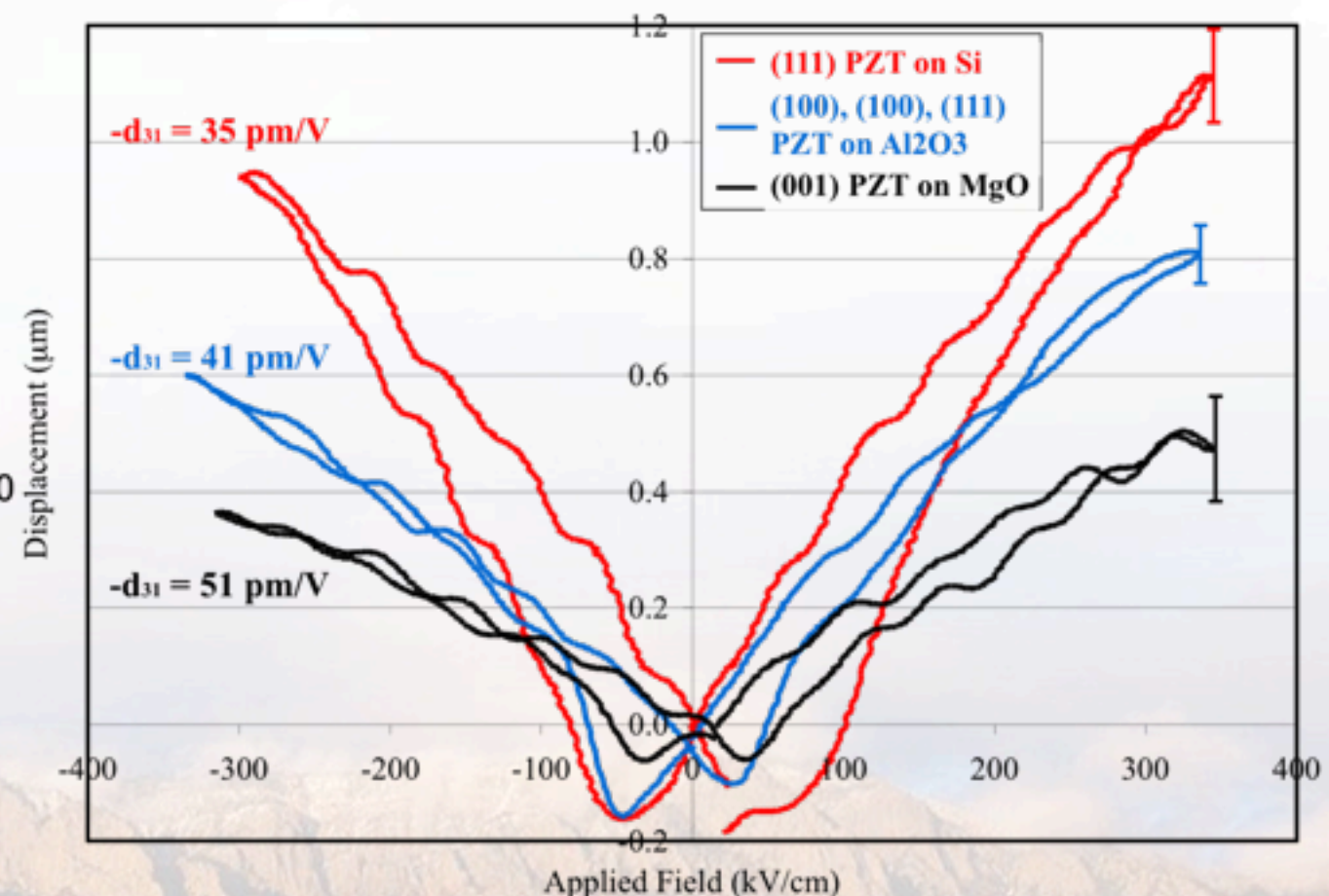
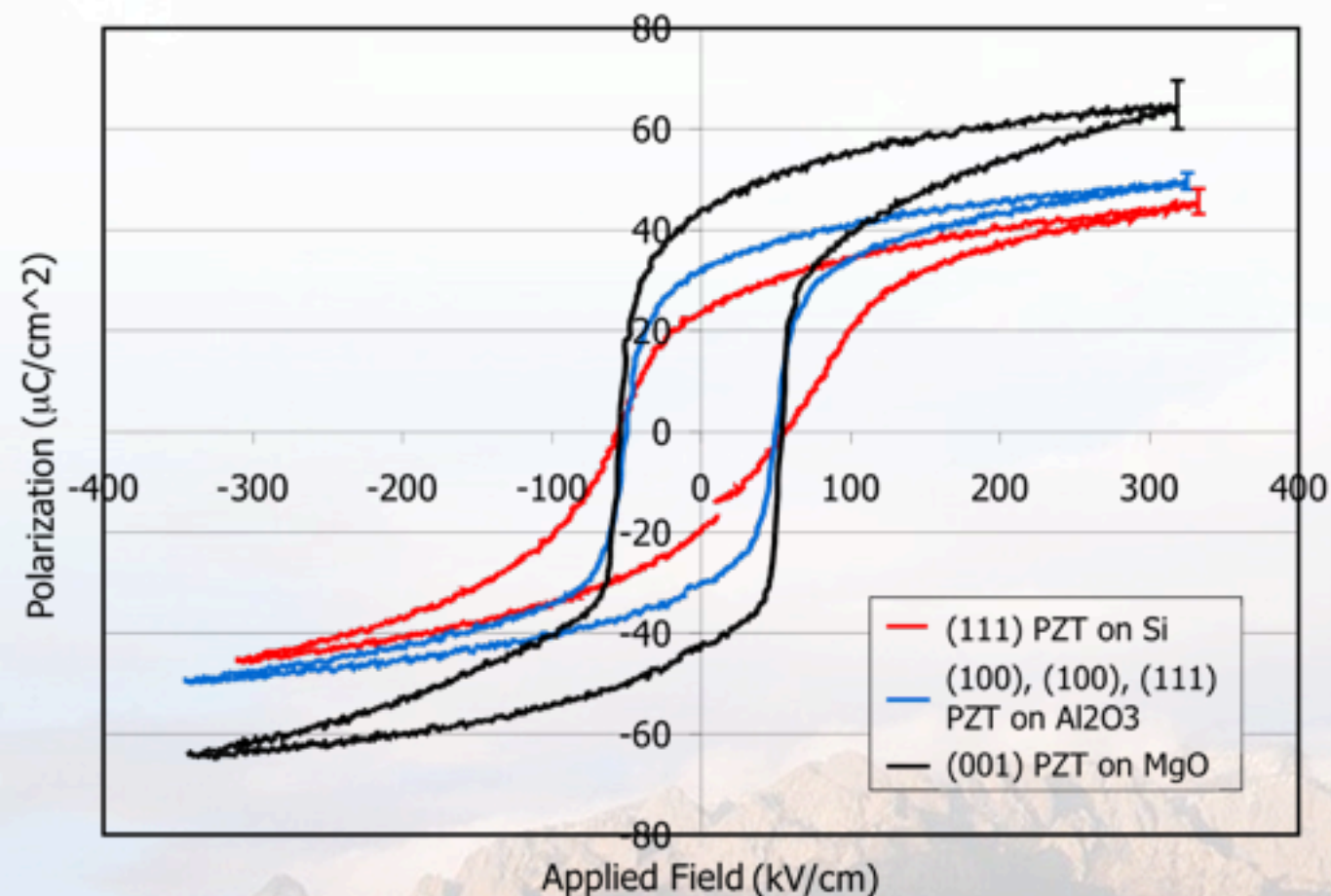
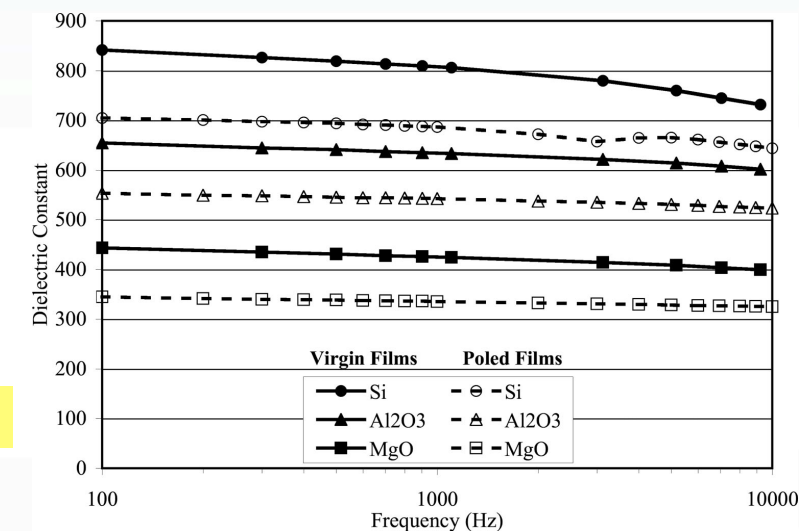
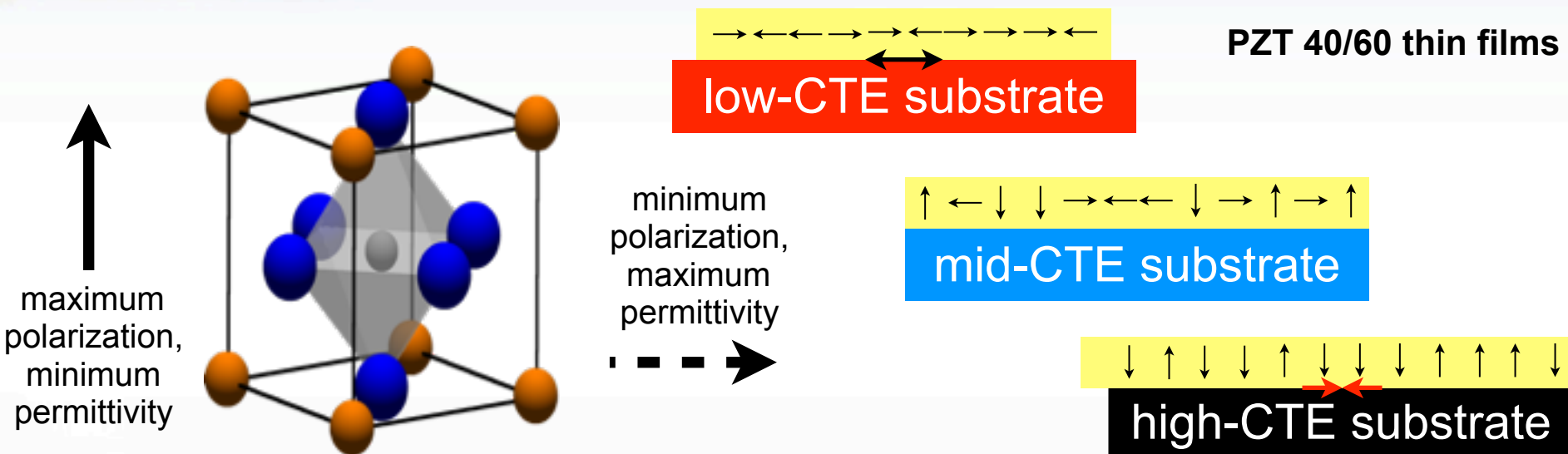


# Understanding (and Control) of Processing/ Structure/Property Relationships



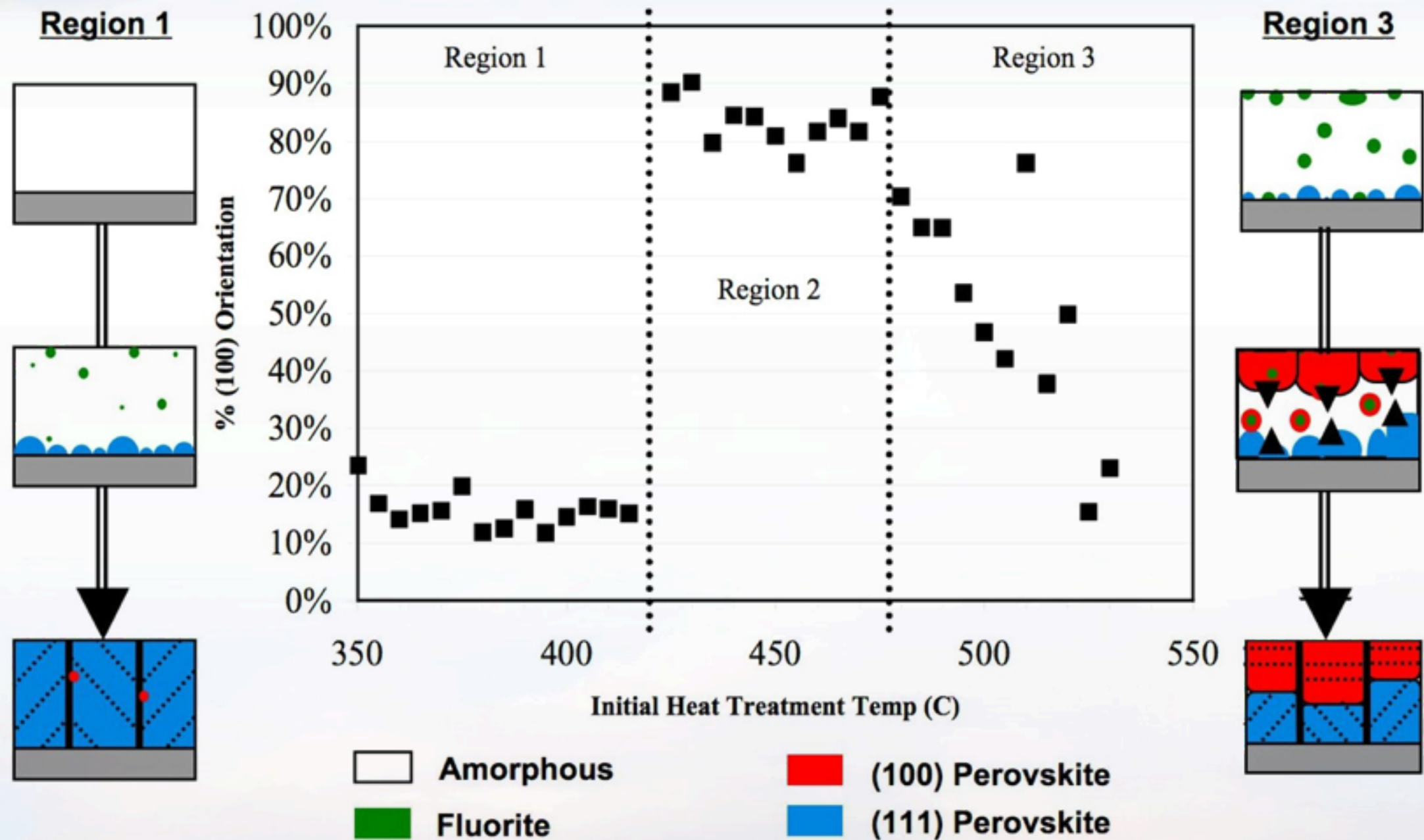


# Film Texture for Tailored Properties



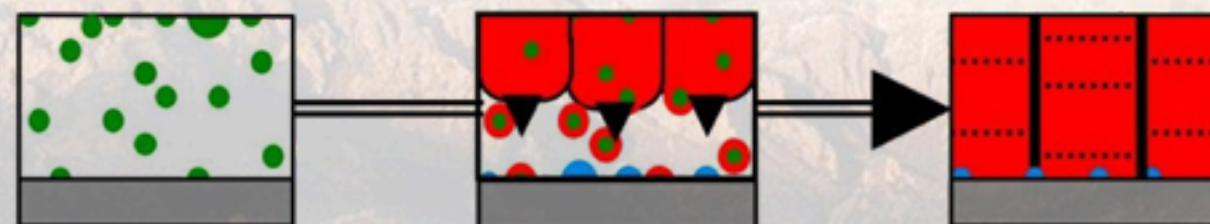


# Control of Texture via Nucleation and Growth



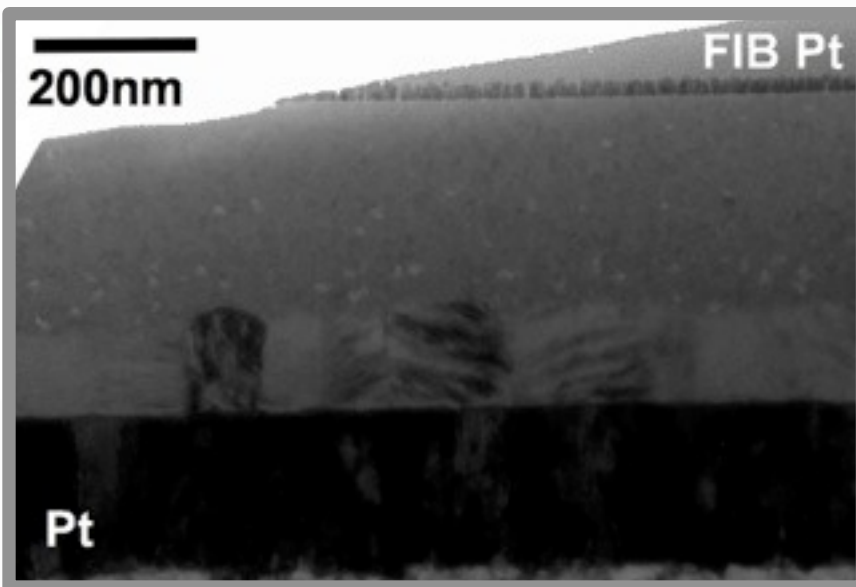
PZT 40/60 thin films

**Region 2**

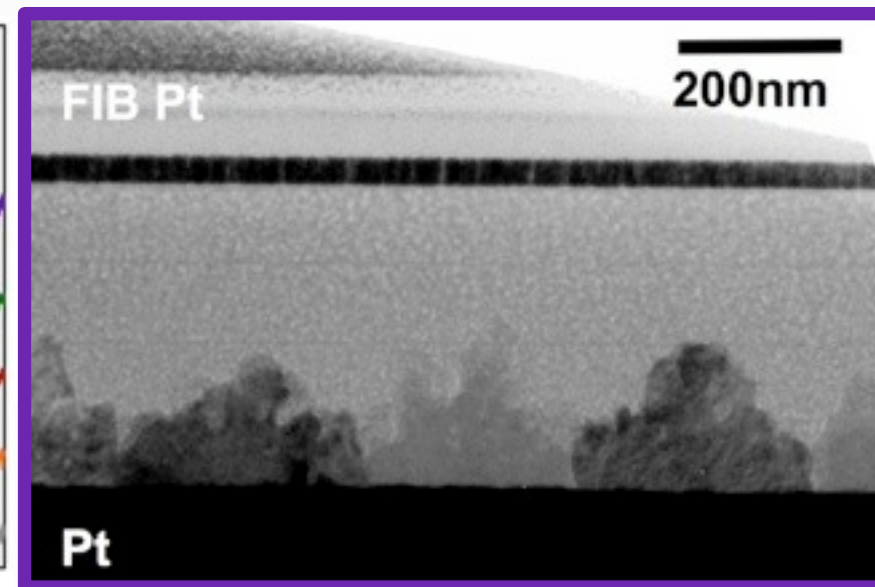
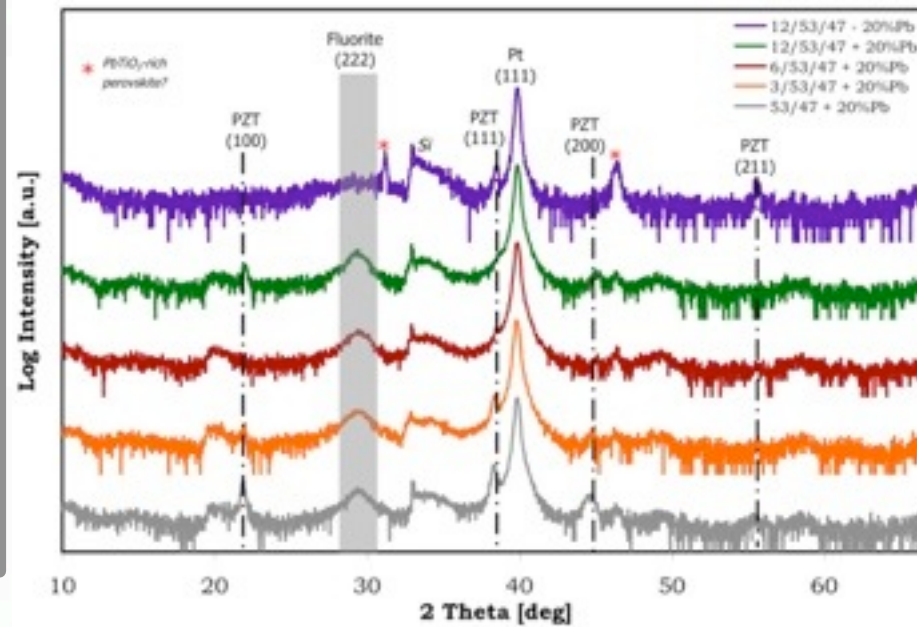




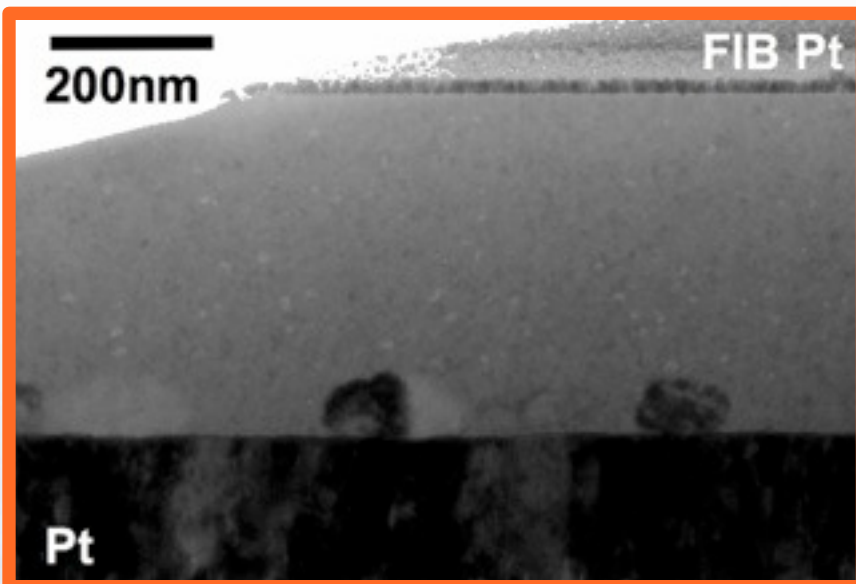
# A-site cation effects on nucleation



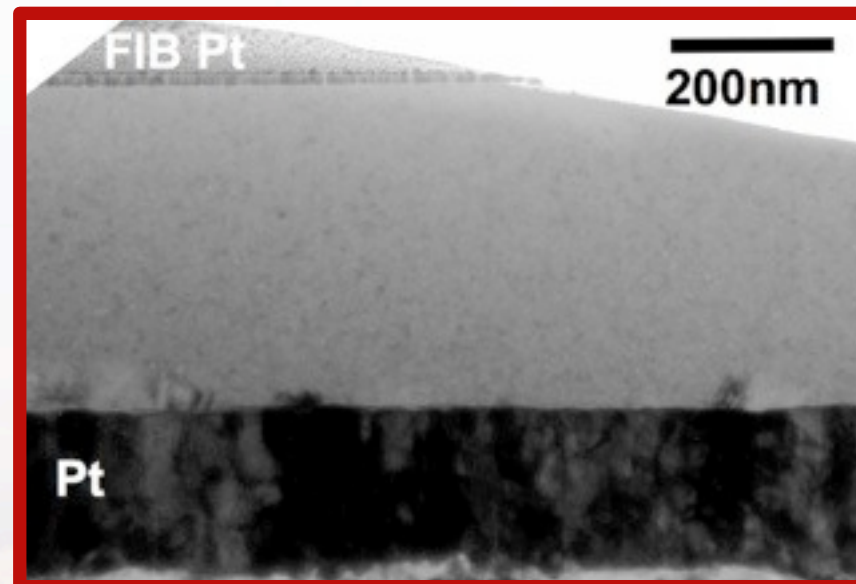
PZT 53/47, 20% excess Pb, 550C 1hr



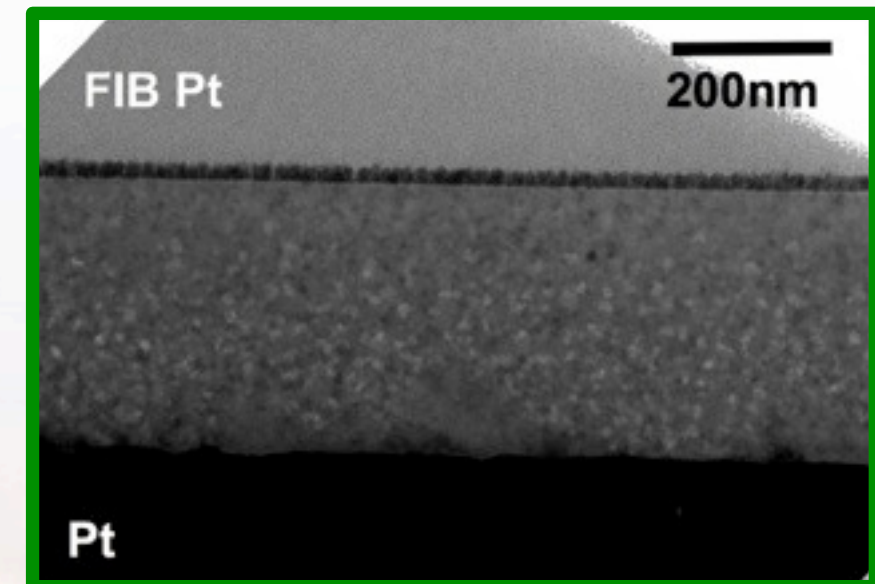
PLZT 12/53/47, 20% Pb deficient, 550C 1hr



PLZT 3/53/47, 20% excess Pb, 550C 1hr



PLZT 6/53/47, 20% excess Pb, 550C 1hr



PLZT 12/53/47, 20% excess Pb, 550C 1hr



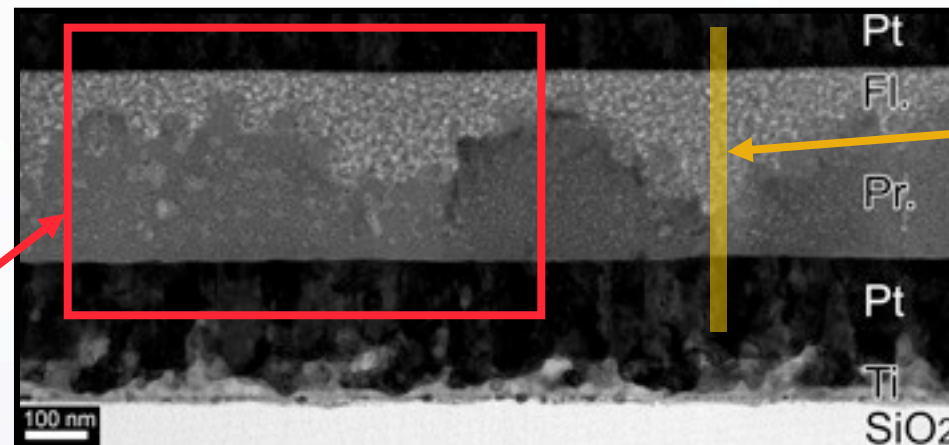
# Quantitative Cation Mapping in PLZT Films

SIMS, XPS, AES depth profiling  
~several 10s of microns  
≠ feature size



Feature size  
~hundreds of nms

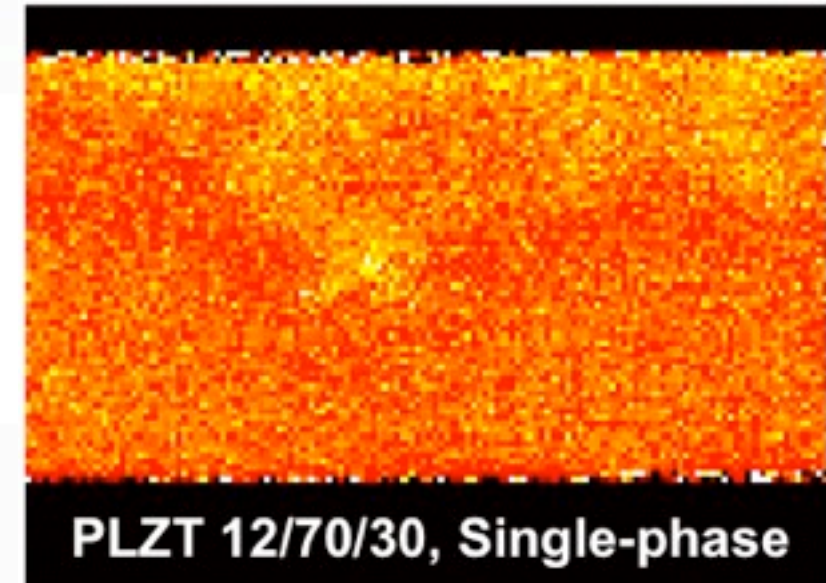
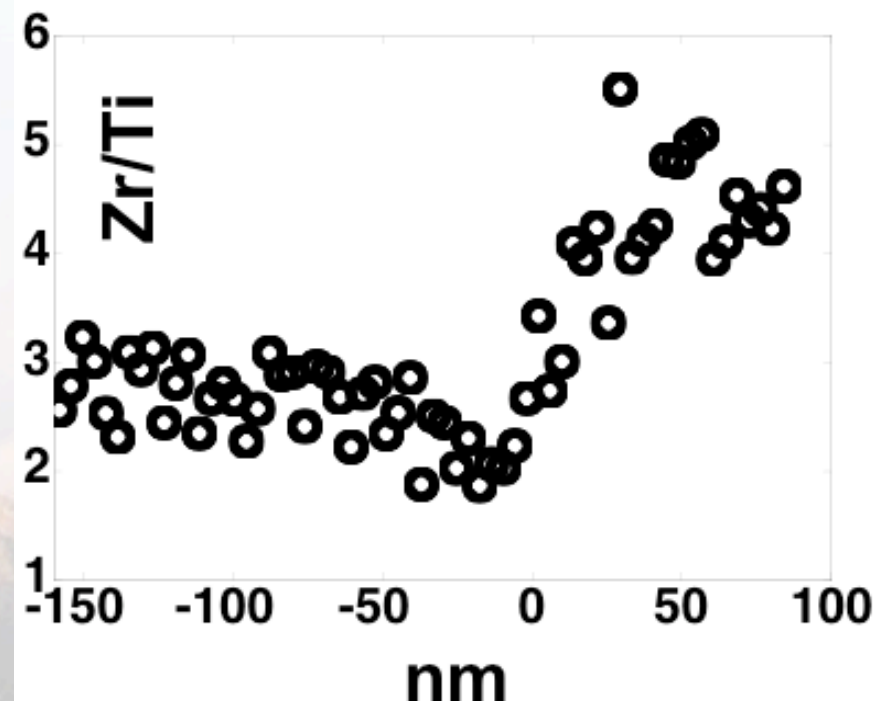
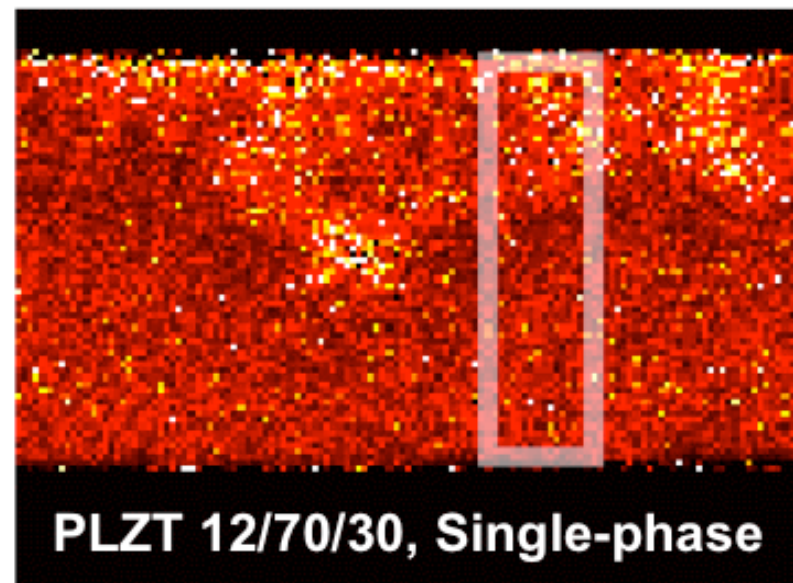
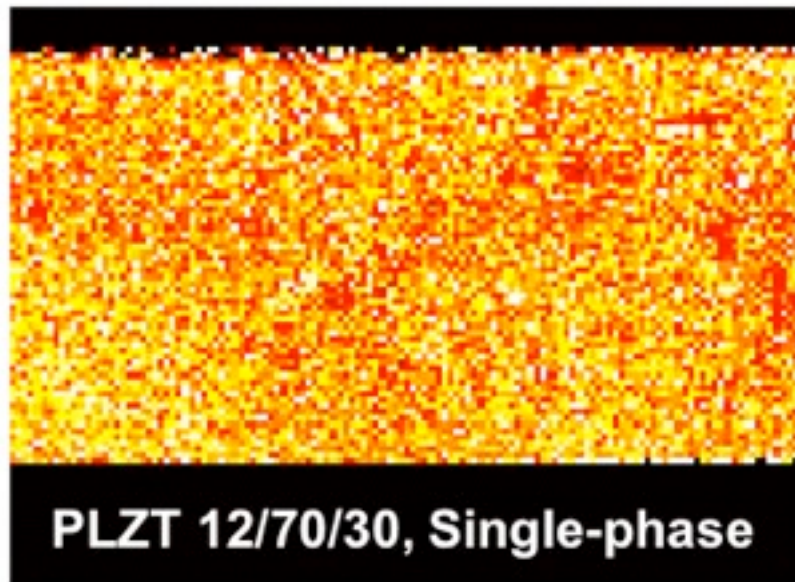
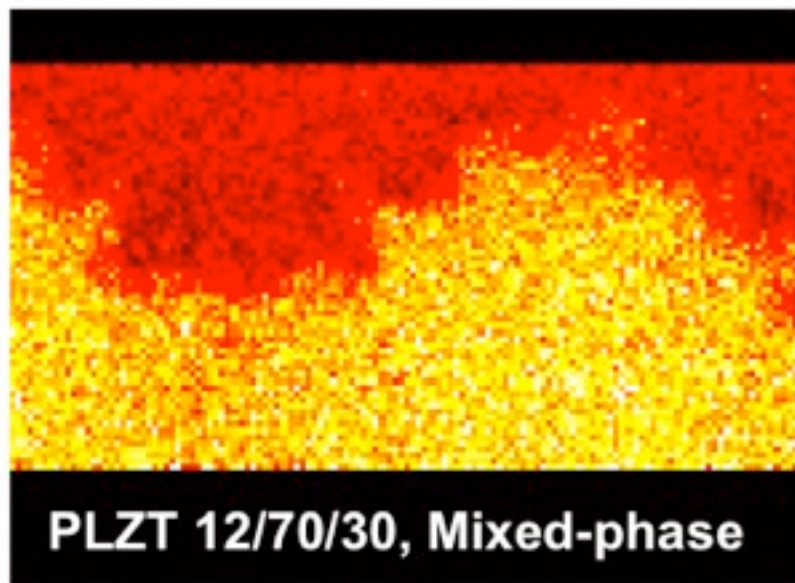
Used STEM-EDS SIs to  
sample this scale



EDS linescan sampling  
~several nanometers  
≠ feature size



# Quantitative Cation Mapping in PLZT Films

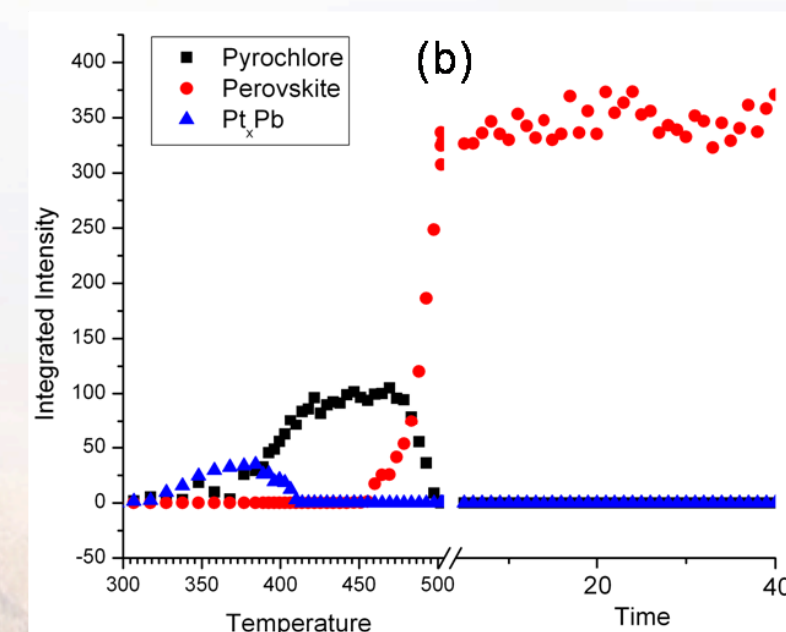
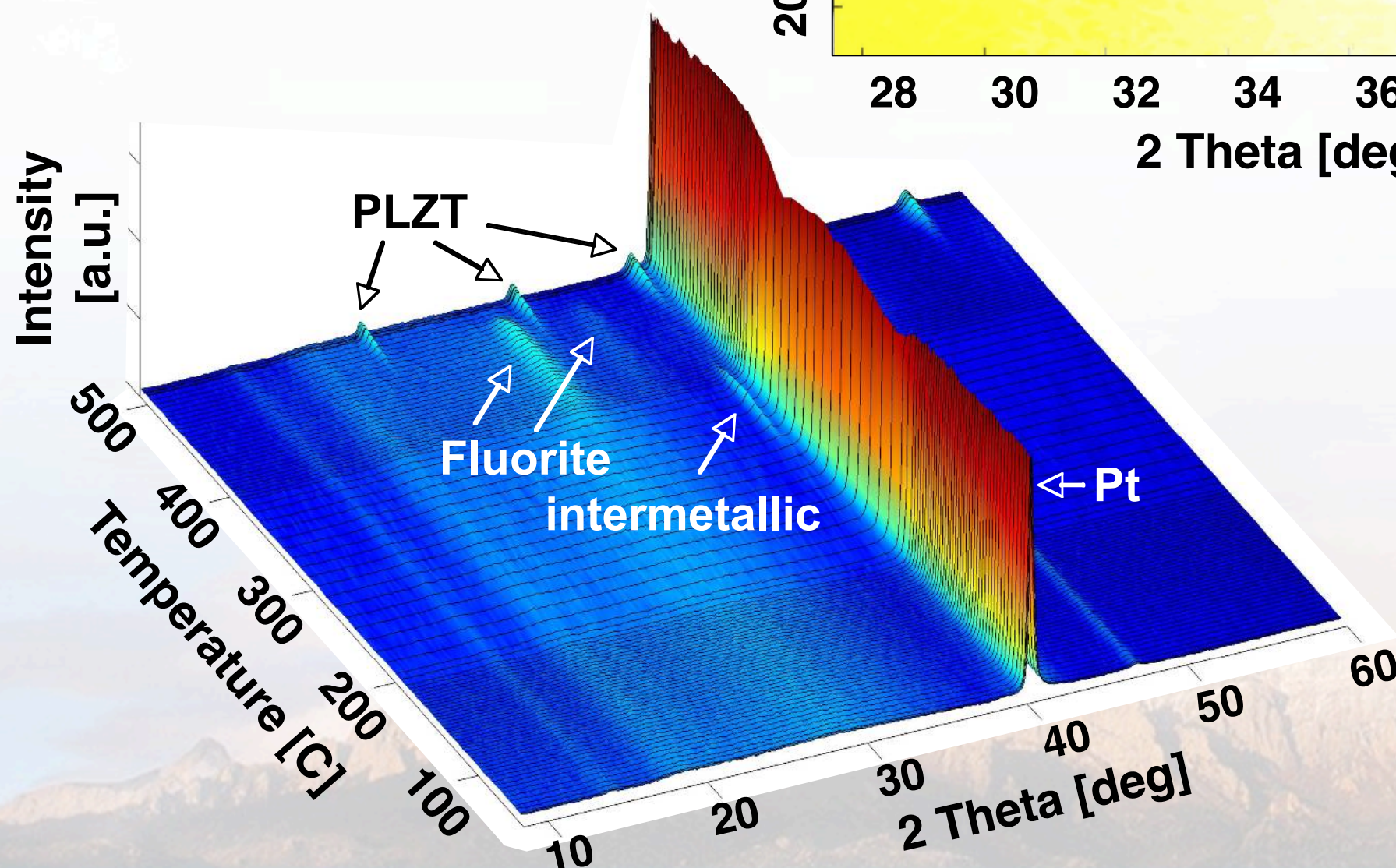
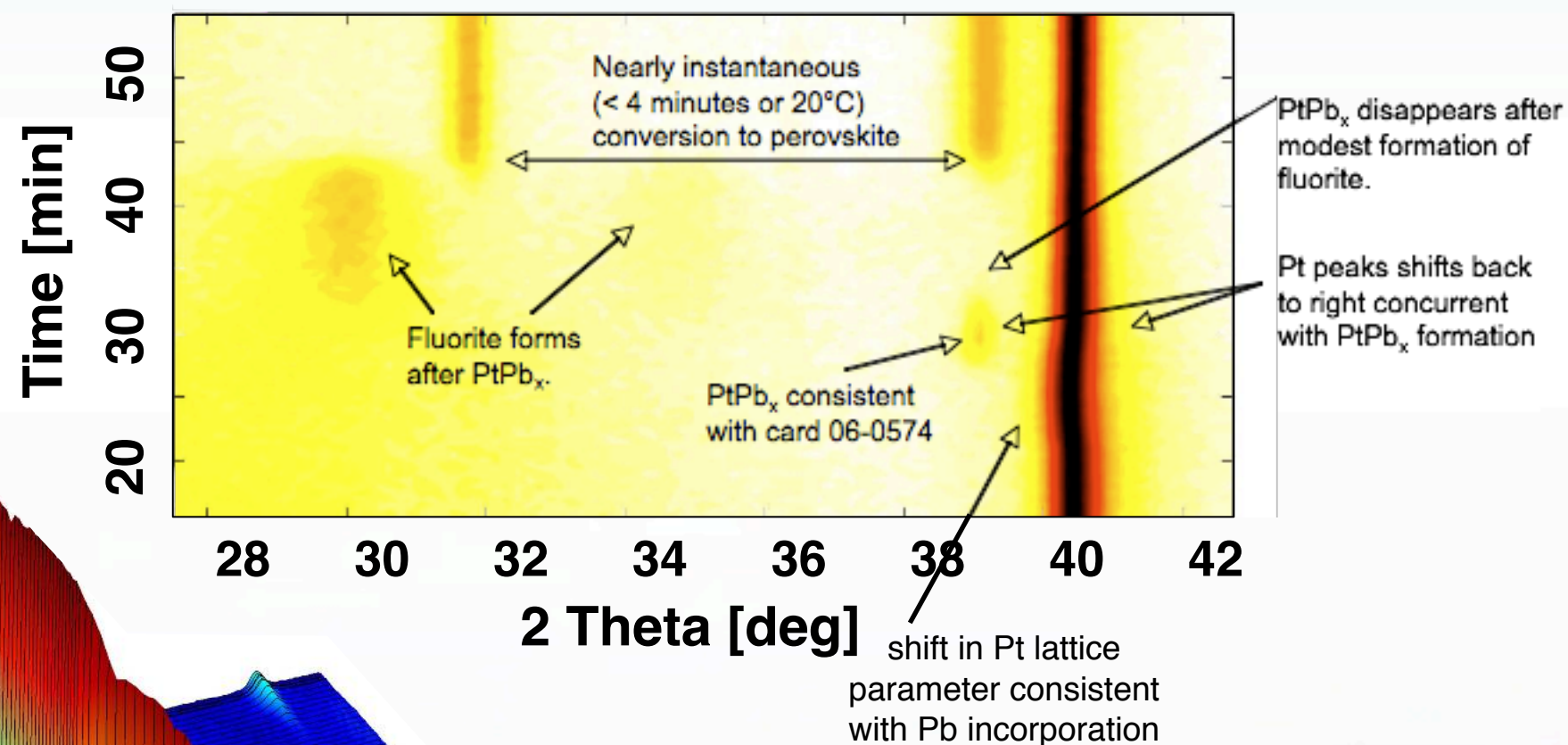


- Pb stoichiometry and homogeneity can be restored through Pb-rich annealing step
- B-site heterogeneities remain
- Evidence for co-segregation of La and Zr
- No Zr/Ti segregation observed for rapidly-crystallized PZT



# *in-situ* X-Ray Diffraction

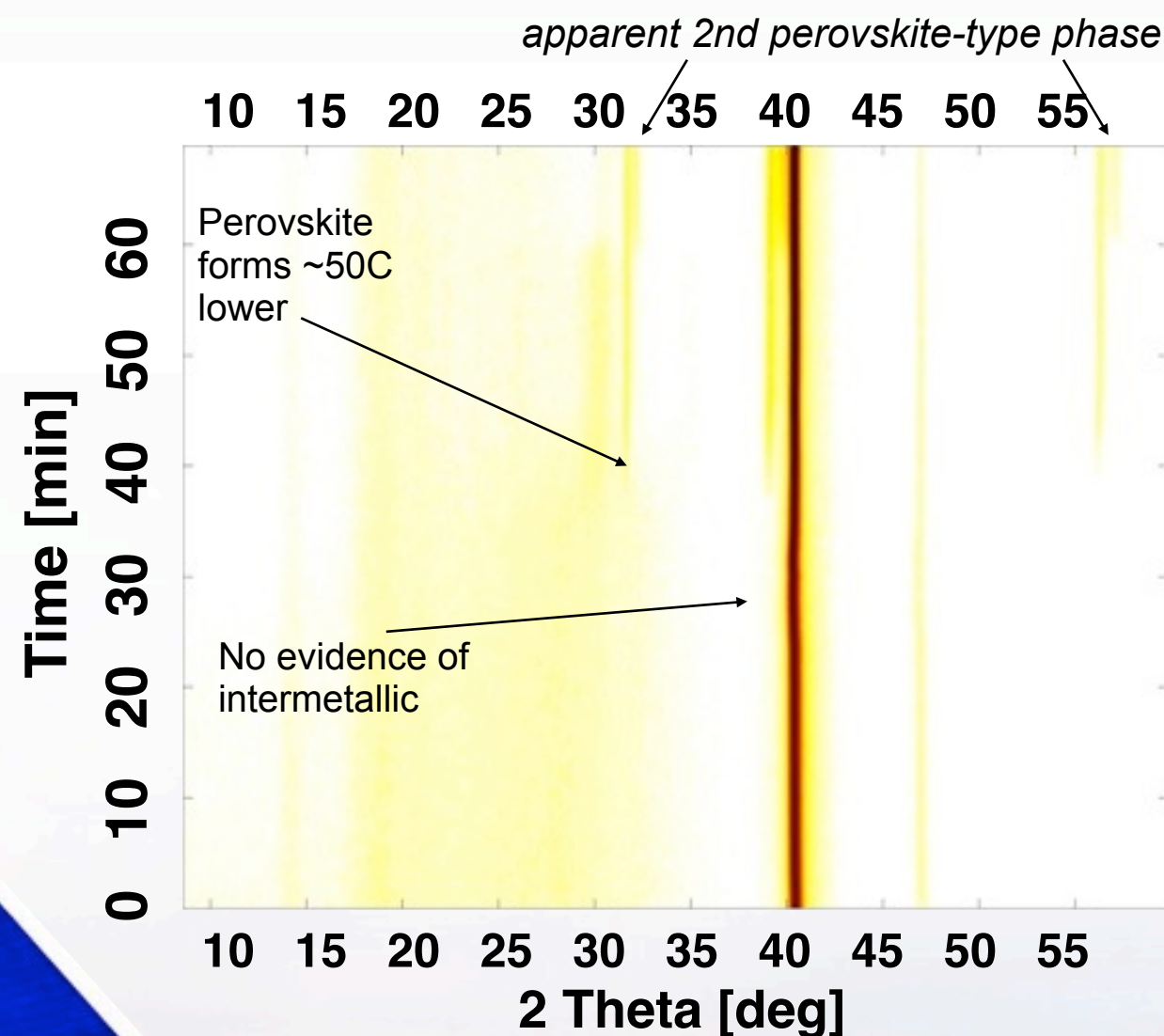
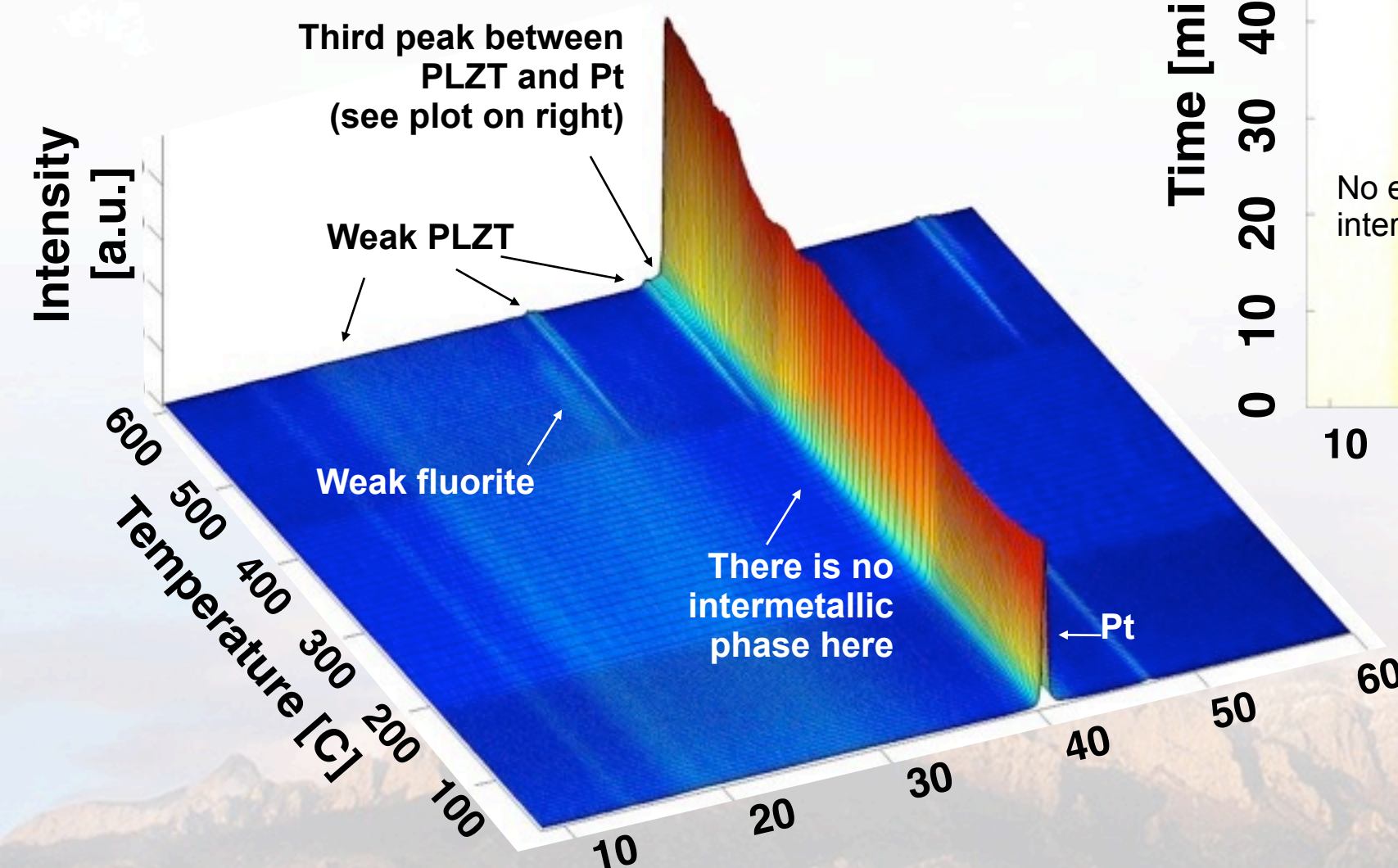
Crystallization of PLZT thin film from a solution containing 20% XS Pb





# *in-situ* X-Ray Diffraction

Crystallization of PLZT  
thin film from a solution  
containing 20% Pb  
deficiency

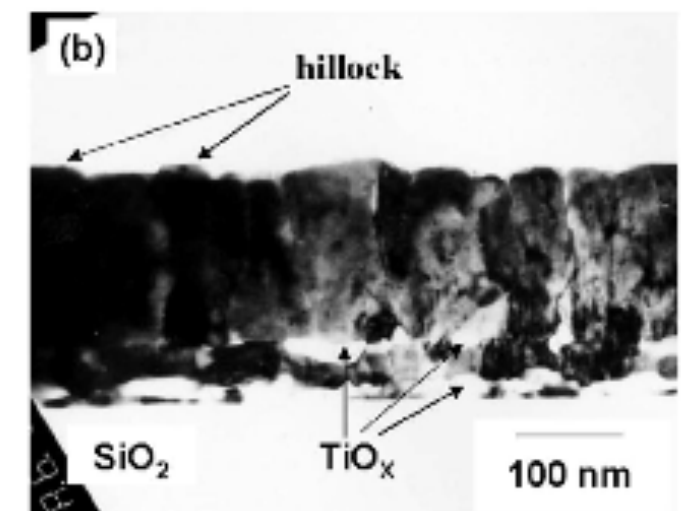
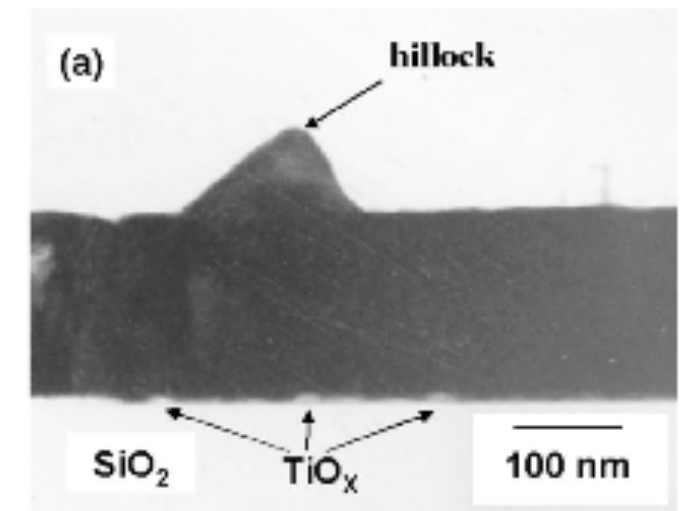
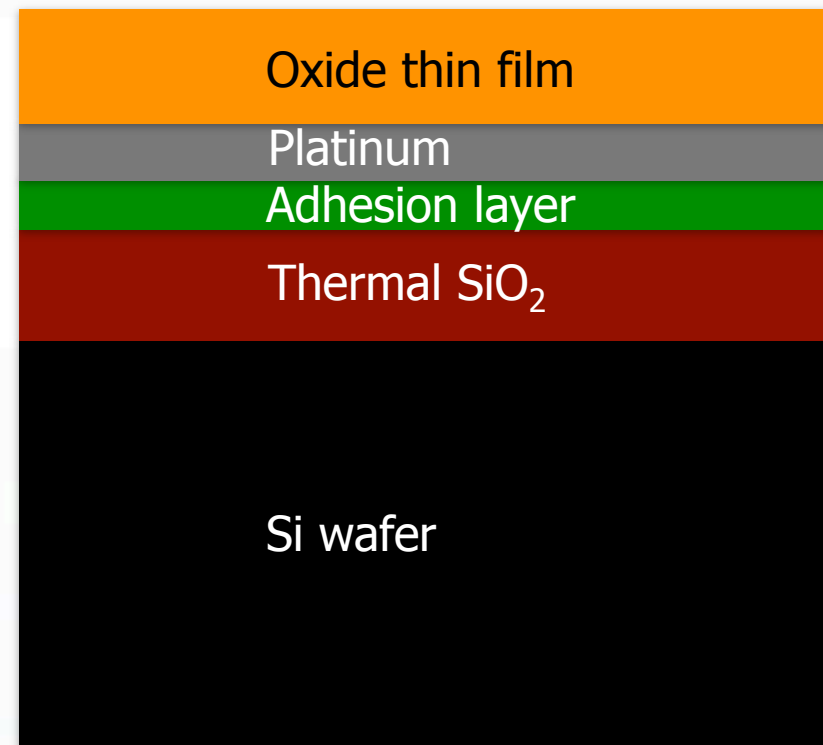




# Electrode Adhesion Layer

- Platinized Si is common substrate

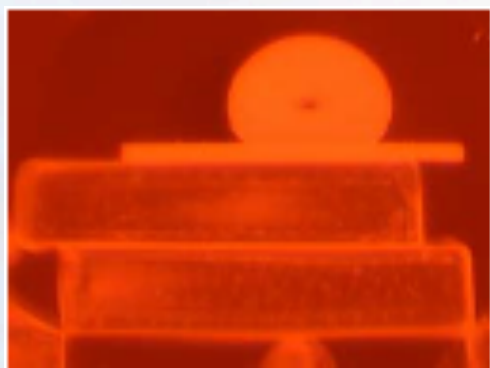
- 400 – 500 nm thermal SiO<sub>2</sub>
- 20 – 40 nm adhesion layer: typically Ti or TiO<sub>2</sub>
- 100 – 200 nm Pt



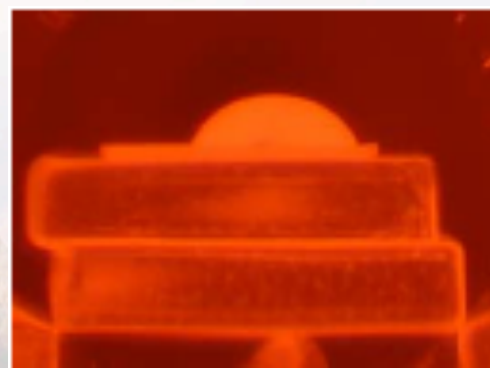
- Other adhesion layers:

- Zr, ZrO<sub>2</sub> (Al Shareef et al., 1997, Zohni et al., 2008)
- Ta (Kissurska et al., 1995)
- Al<sub>2</sub>O<sub>3</sub> (Halder et al., 2007)

- Previous work has shown Cu wets ZnO very well:



Molten Cu on Al<sub>2</sub>O<sub>3</sub>

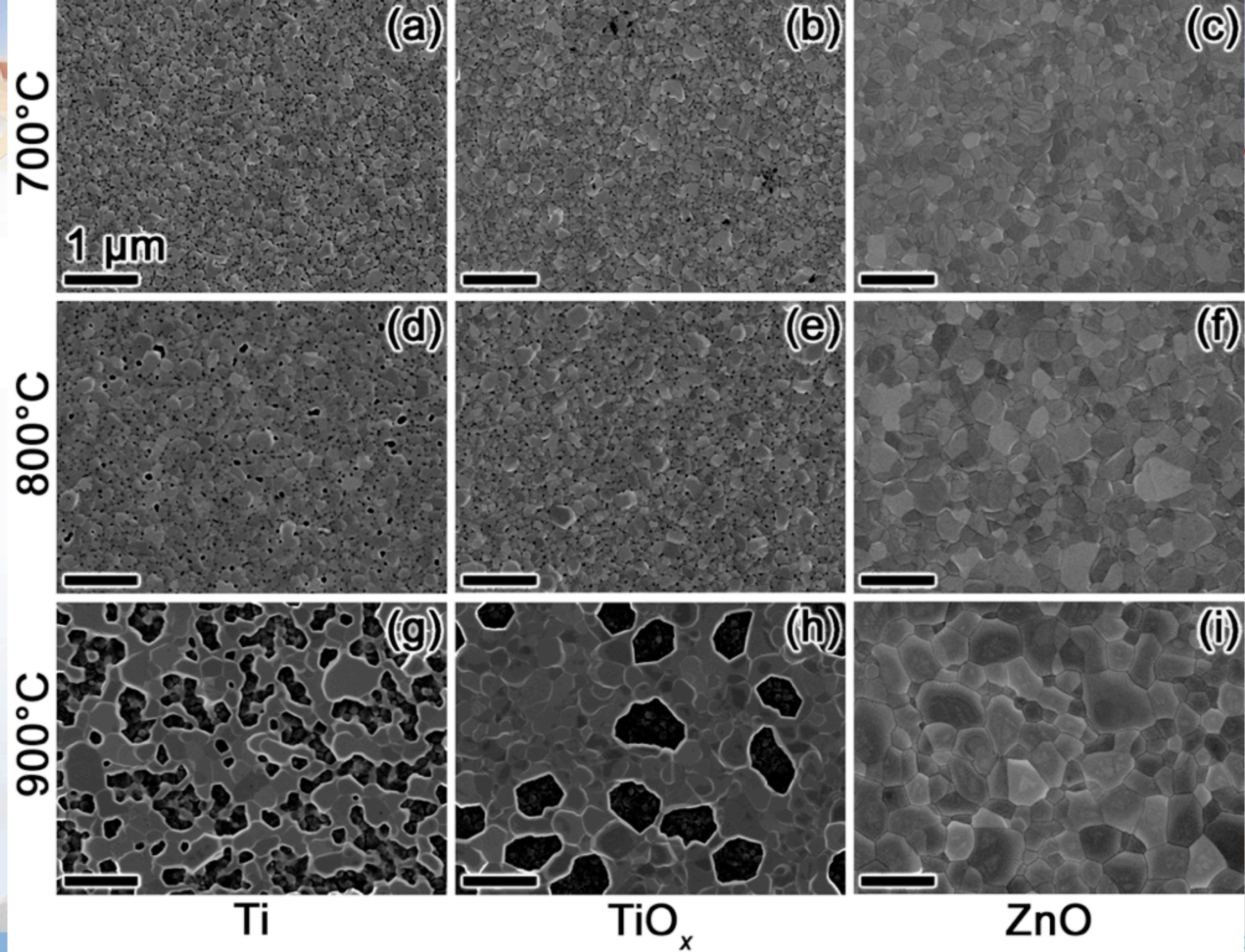


Molten Cu on ZnO

Substrate	Contact angle (°)	W <sub>a</sub> (J/m <sup>2</sup> )
Al <sub>2</sub> O <sub>3</sub>	133 ± 6	0.480 ± 0.142
ZnO	62 ± 5	2.012 ± 0.097

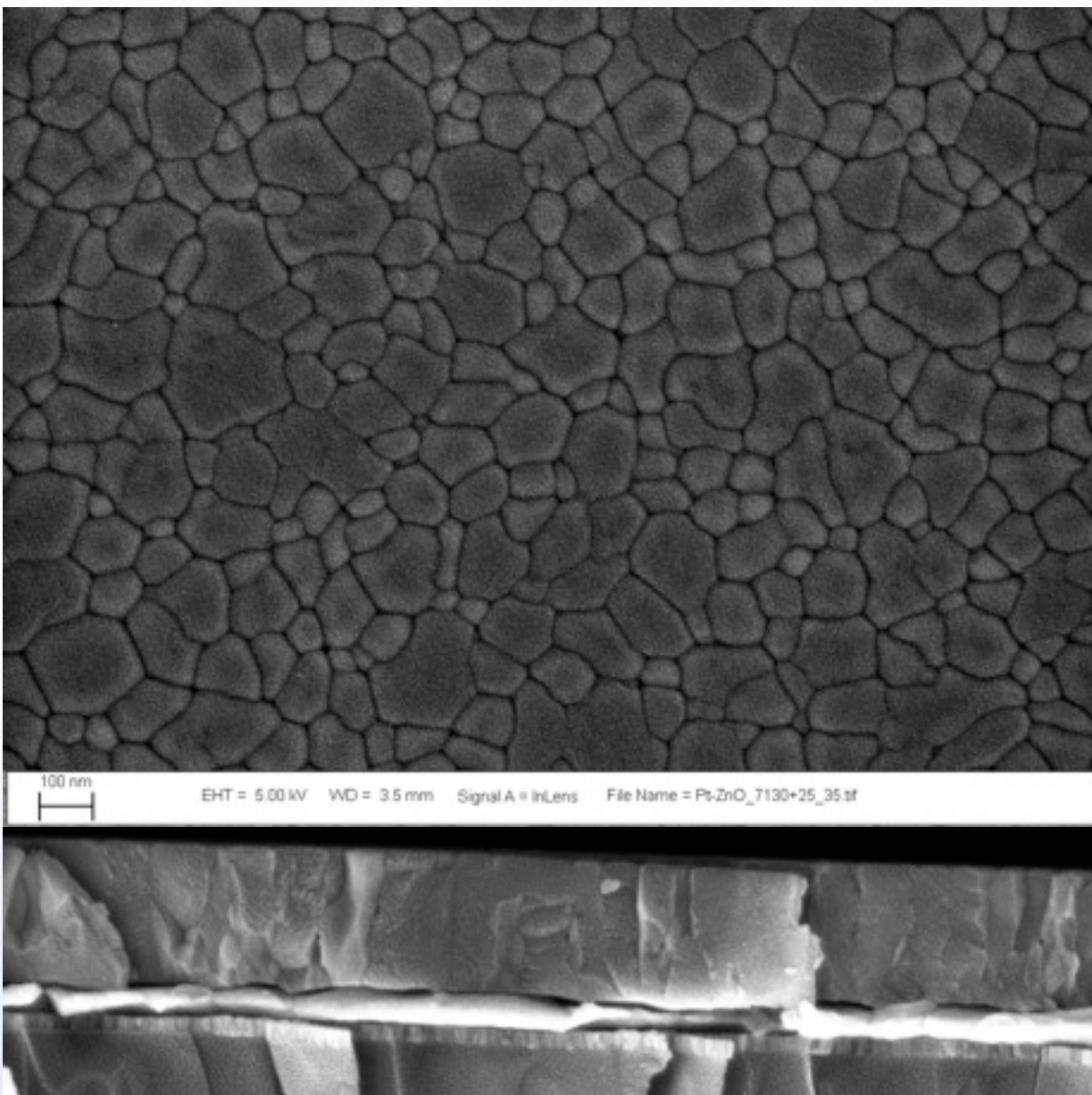
B. Laughlin, Ph.D. thesis, NCSU 2006





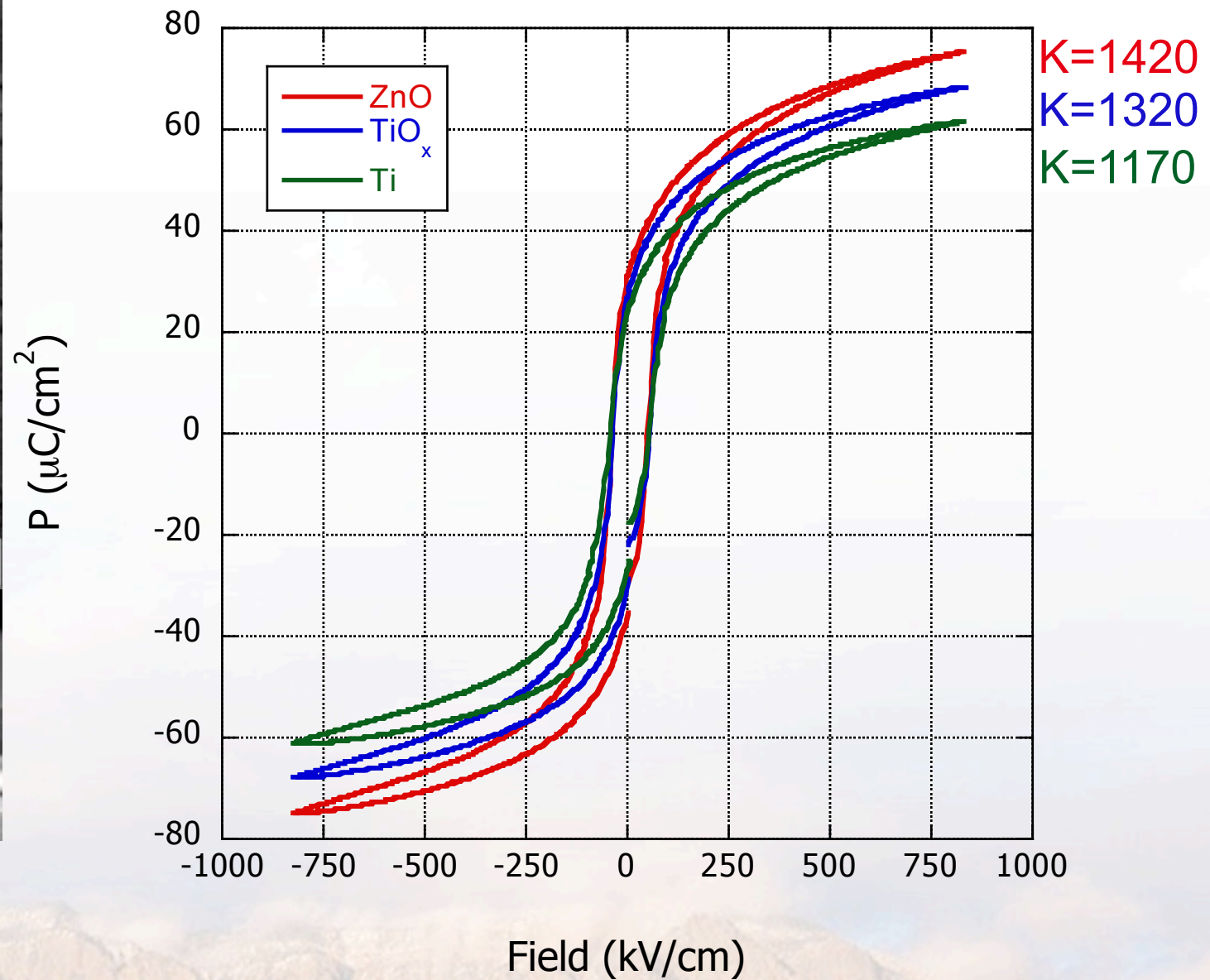


# Resulting Ferroelectric Films



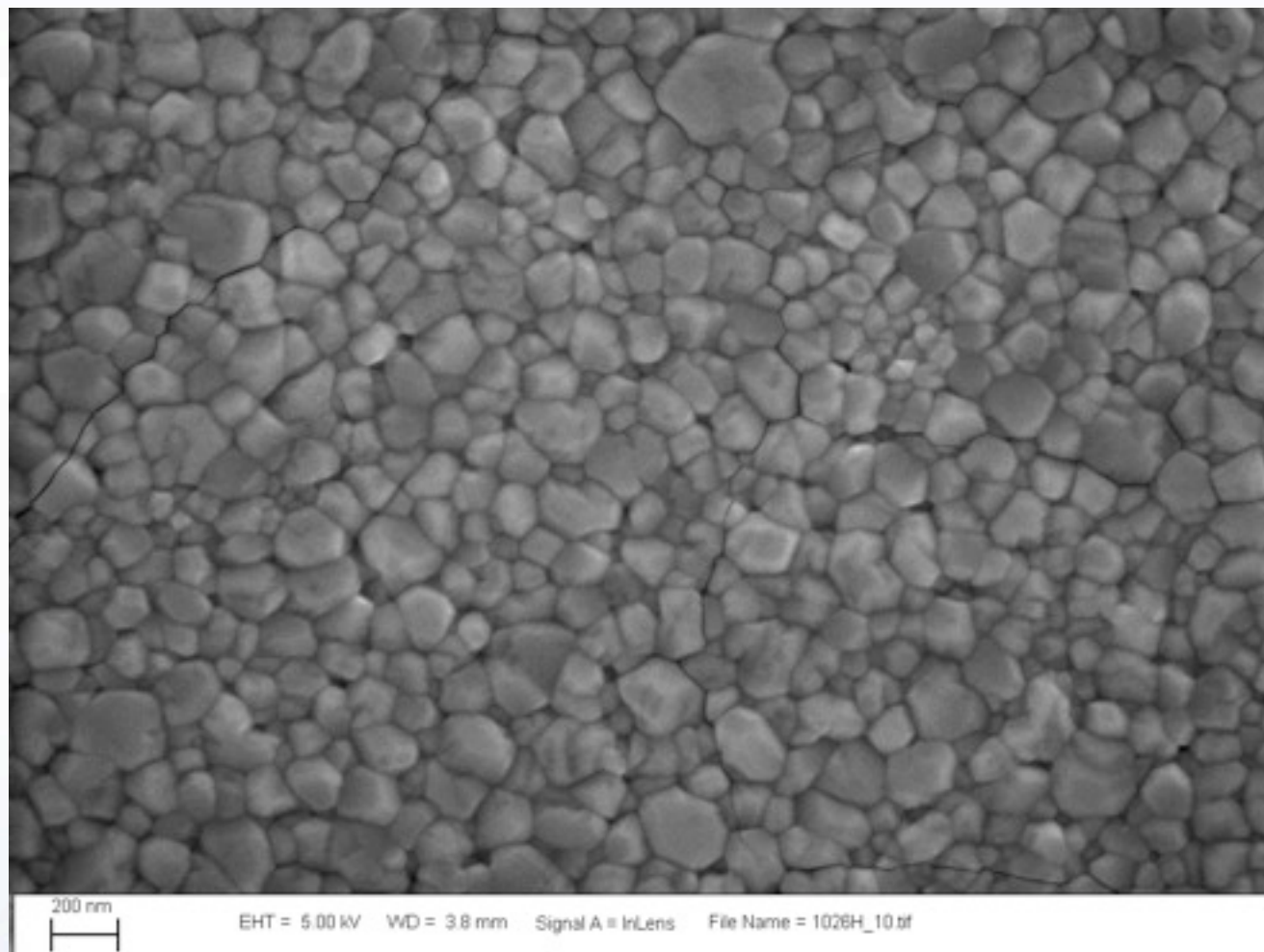
PZT on Pt//ZnO//SiO<sub>2</sub>//Si

PZT 52/48 on various adhesion layers

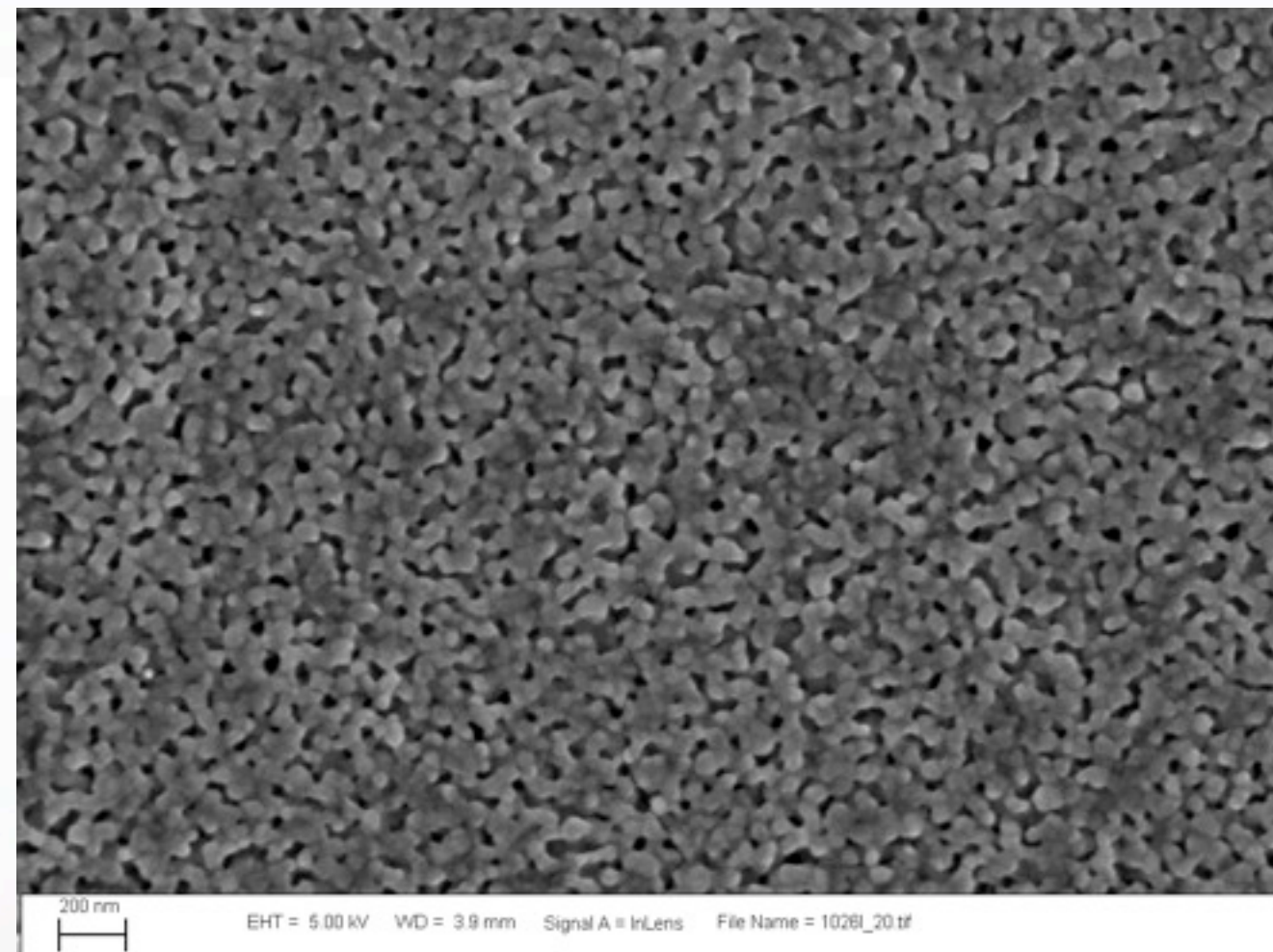




# BaTiO<sub>3</sub> on Platinized Silicon



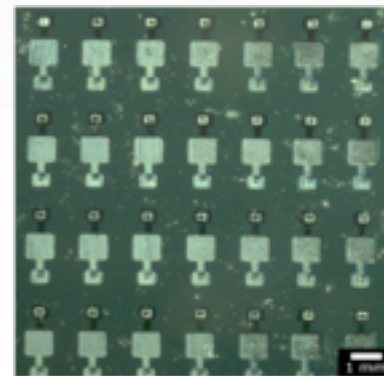
BaTiO<sub>3</sub> on Pt//ZnO//SiO<sub>2</sub>//Si  
K = 1800



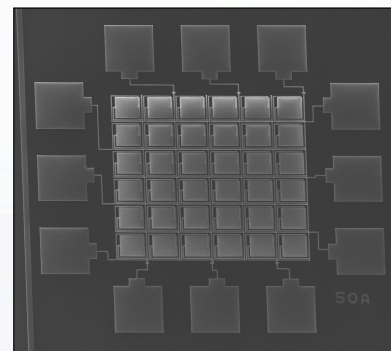
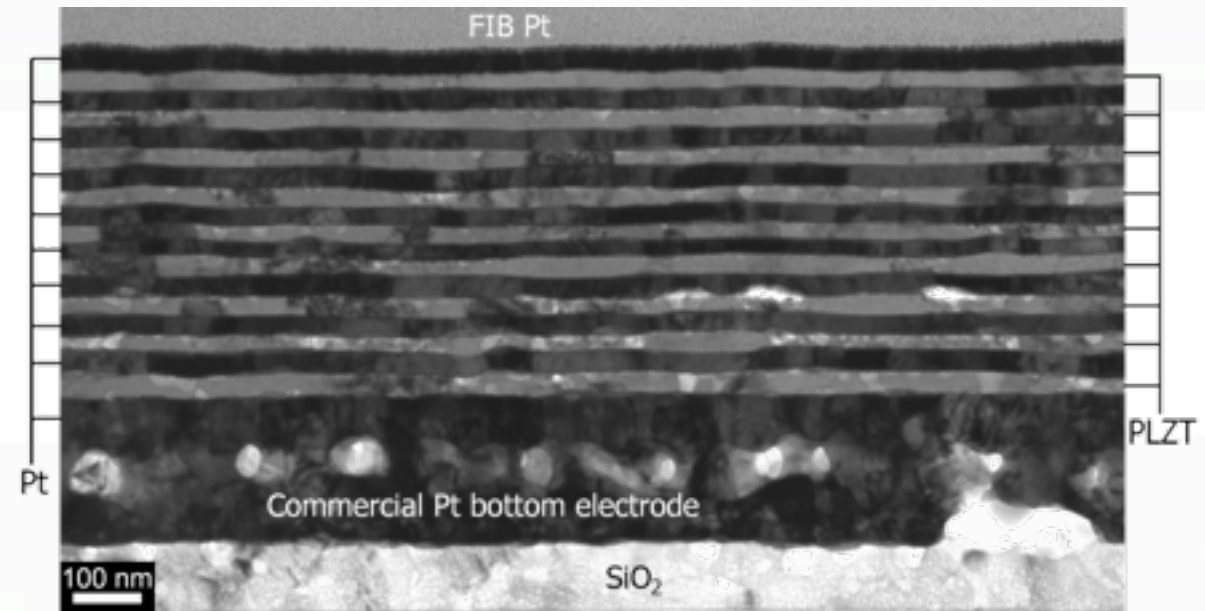
BaTiO<sub>3</sub> on Pt//TiO<sub>x</sub>//SiO<sub>2</sub>//Si  
K = 400



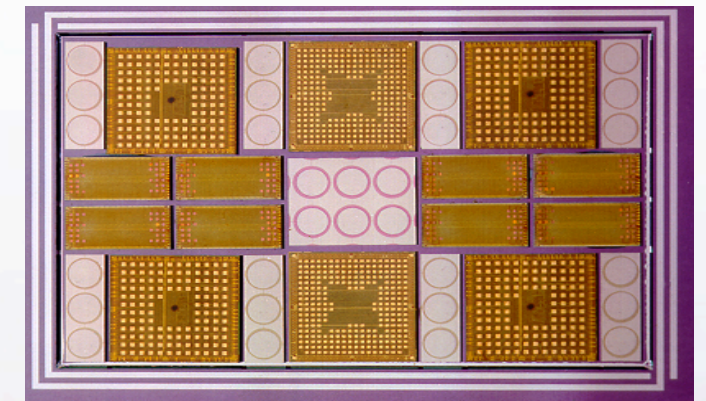
# From Blanket Film to Functional Structure



Functional PZT-based multilayer capacitor structures



Pyroelectric pixels w/aerogel insulation



Multichip module with PZT thin-film capacitor arrays



PZT-MEMs piezo cantilever beam for energy harvesting



# Doing More with the Same?

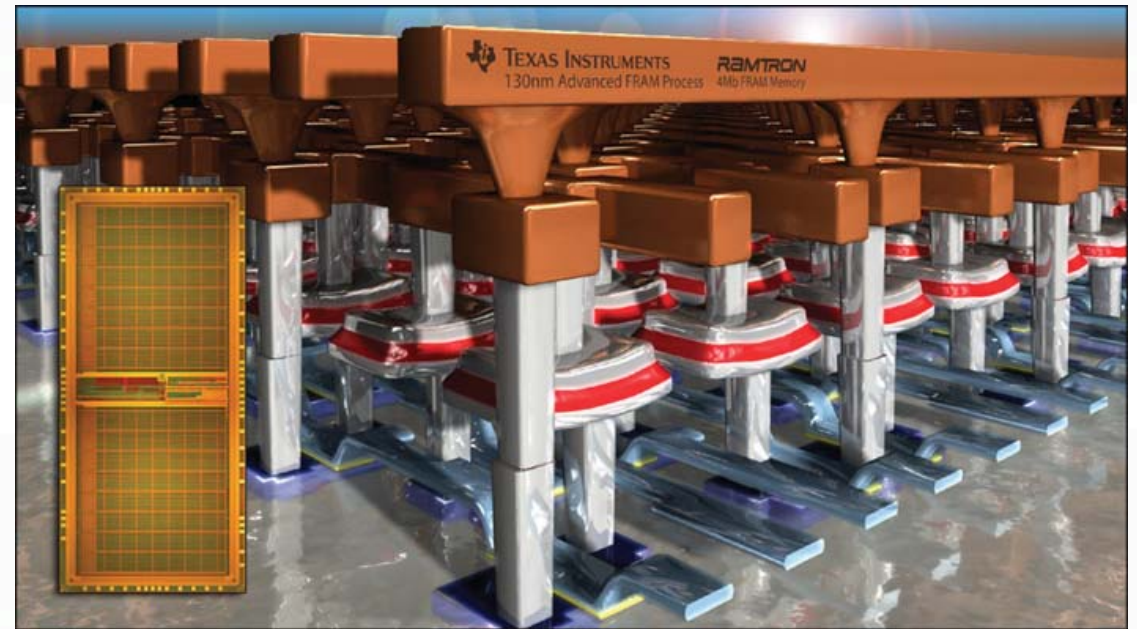
Integration of materials with new and/or increased functionality

## General Fabrication Technique for Controlled Nanopatterning

- Any material, any substrate
- Arbitrary, addressable features/patterns
- Platform for size/interface effects studies, device development, etc.

## Why Ferroelectrics?

- Demonstrate broad applicability
- Study fundamental lateral size and aspect ratio effects
- Ultrahigh density NVRAM



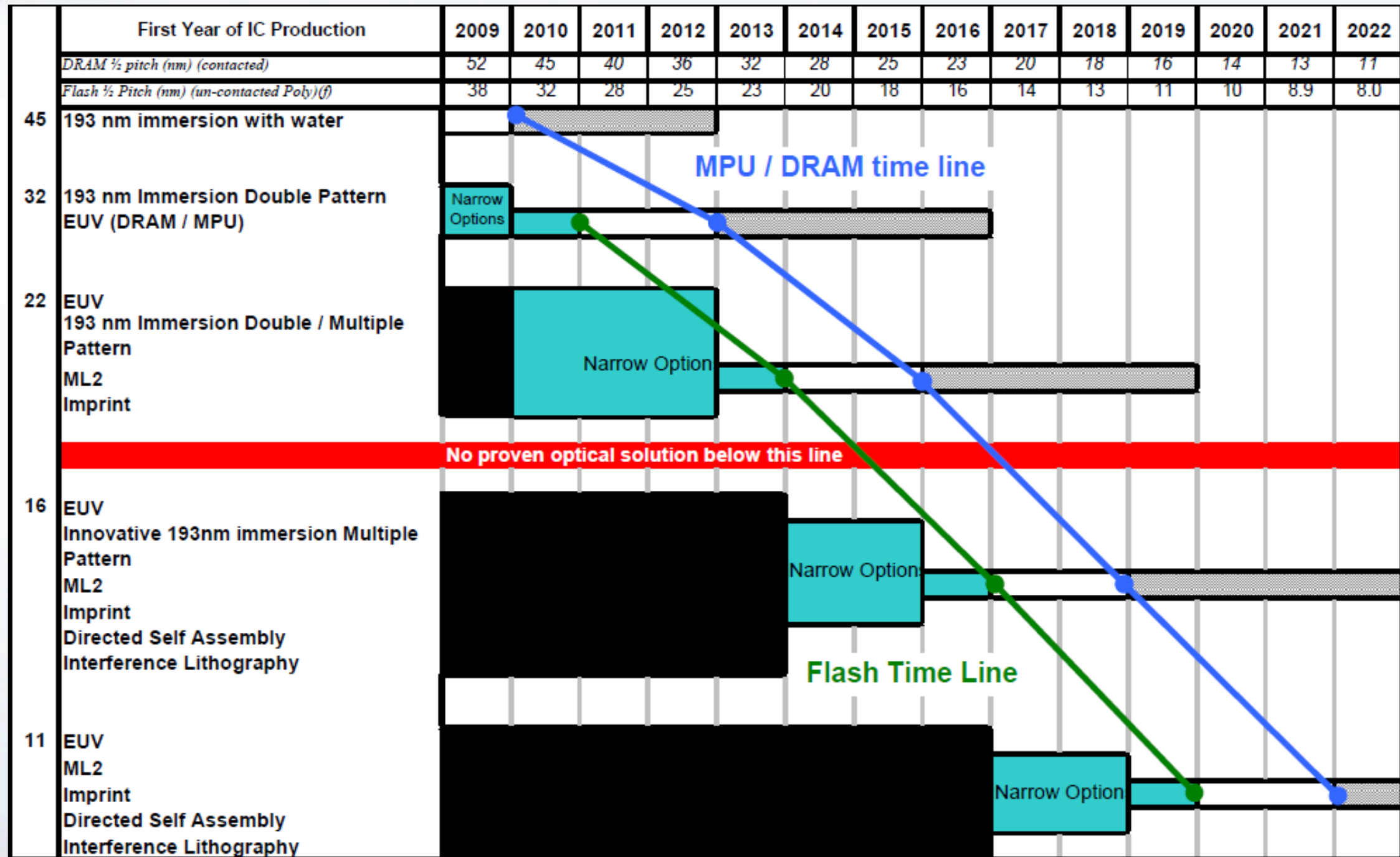
*From MRS Bulletin v33 (2008), originally from TI, Ramtron*

## Target Demo Application Information Storage (NVRAM)

- Reduce physical size
- Reduce power consumption
- Improve operation through interface control



# Doing Moore with the Same?



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution

Research Required

Development Underway

Qualification / Pre-Production

Continuous Improvement

ITRS 2009



Sandia National Laboratories



# Micro-, Nano-Patterning of Arbitrary Materials

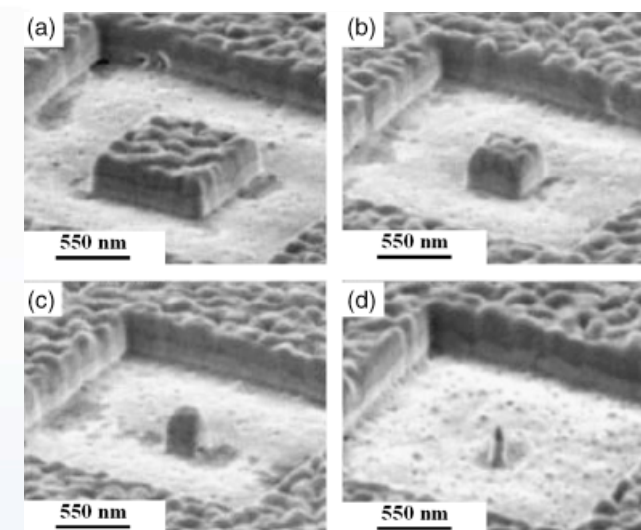
## ■ Challenges of expanding beyond 'standard' materials

Fabrication

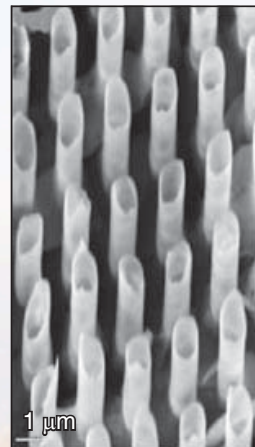
Patterning

Integration

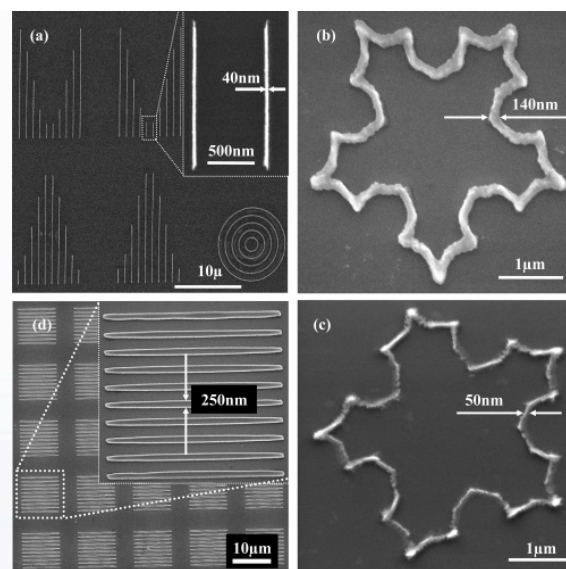
Performance



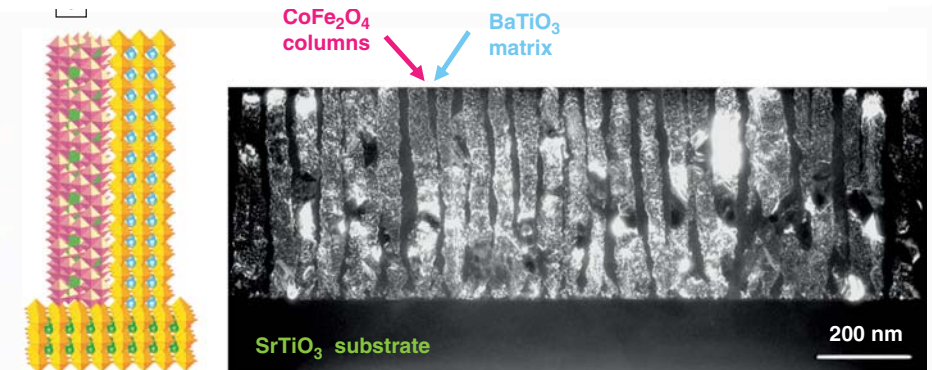
Ganpule et al., MRS Proc. (2001)



Scott et al.,  
Nano Lett. (2008)



Donthu et al., Nano Lett. (2005)



Zheng et al., Science (2004)

- Need functional crystalline nanostructures without needing to develop new etching / integration approaches for each new material(s)
- **Extreme limitations on use of fab tools**



# Overview of Our Approach

- Goal: Combine flexibility and functionality of chemical solution deposition with use of e-beam and BCP patterning capabilities

## Solution Deposition

Fabrication

Patterning

Integration

Performance

## DSA-BCP

Fabrication

Patterning

Integration

Performance

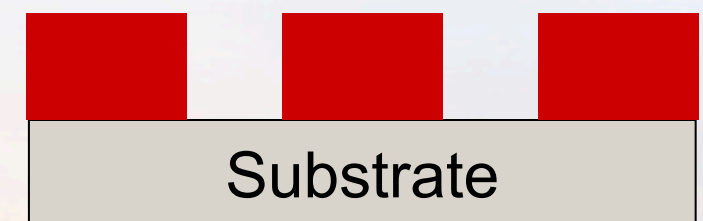
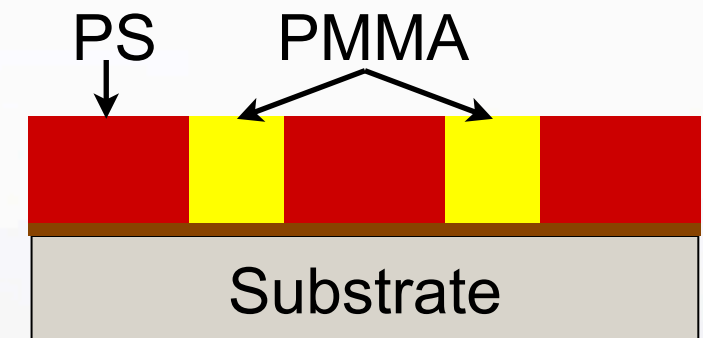
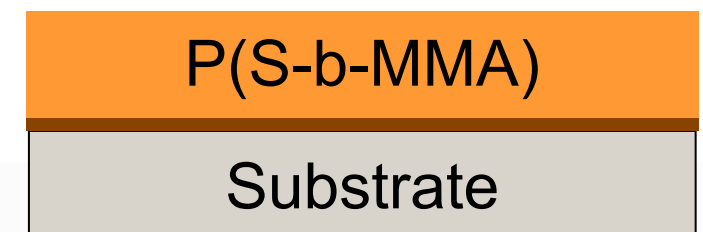
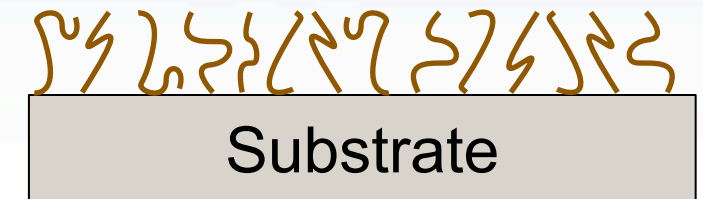
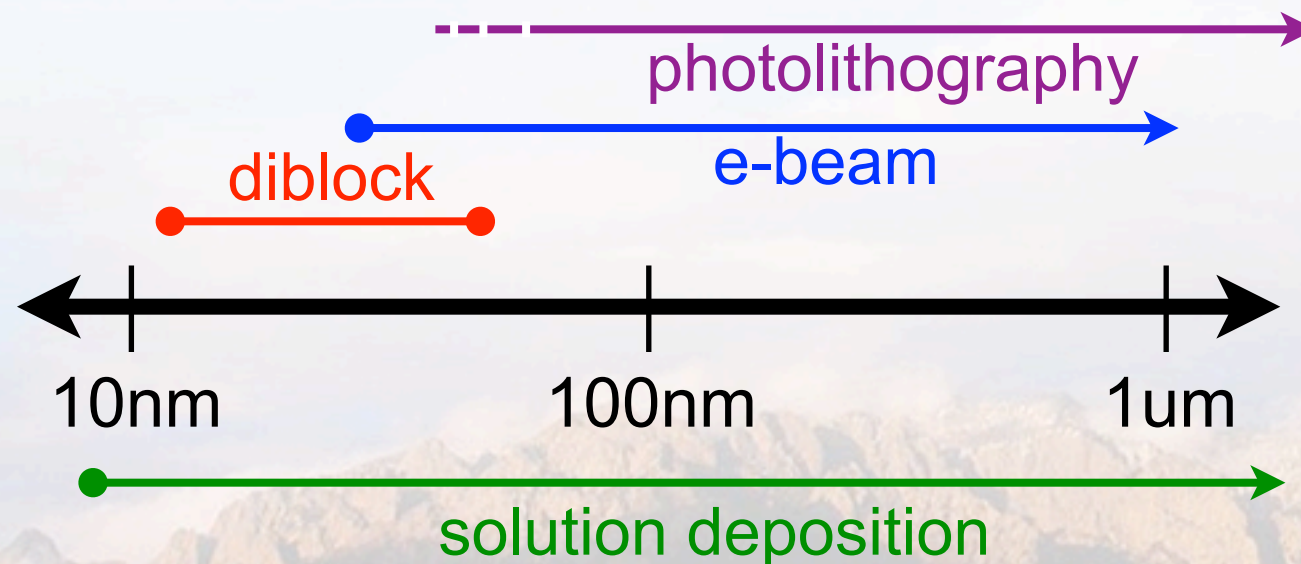
## Challenges:

- Avoid etching functional materials
- Avoid any fab-based processes during/ after deposition of functional materials
- Maintain feature integrity after thermal treatment(s)
- Retain function in nanoscale features



# Patterning

- Continuous films are very limited in function
- Difficulties of etching PZT-based films
  - Access to tools...
  - Property/reliability degradation
- Alternative approaches to patterning/integration
  - Direct write
  - Microcontact printing
  - Various transfer techniques
  - PZT-friendly lithography



Guarini, K W, et. al., *J. Vac. Sci. & Tech. B*, 2001, **19** (6), 2784-2788



# Sub-22nm Lithographic Options

## Extreme Ultraviolet Lithography (EUVL)

### 13.2 nm soft x-ray source power

- (+) high-resolution resist development
- (-) poor Line Edge Roughness (LER)
- (-) complex, **costly**

## Mask-less Lithography (ML2)

- (+) high resolution electron-beam, ion-beam
- (-) slow serial process, **costly, charge build-up**

## Interference Lithography (IL)

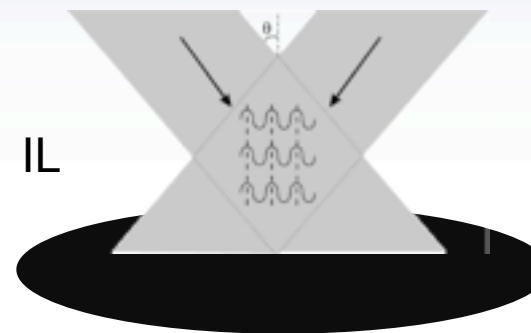
- (+) rapid, large area, parallel process
- (+) **low cost** (rapid, large area, maskless)
- (+) tunable symmetry, period, motif
- (-) layer alignment & spatial pattern variation difficult

## Directed Self-assembly (DSA)

- (+) alignment to pre-pattern gives long-range order
- periodicity set by size of blocks
- (+) pattern rectification and density multiplication
- (-) slow process with many steps

## Nano-Imprint Lithography (NIL)

- (+) long-range order set by master
- (-) overlay can be difficult
- (+) high resolution
- (+) **low cost**



IL pattern



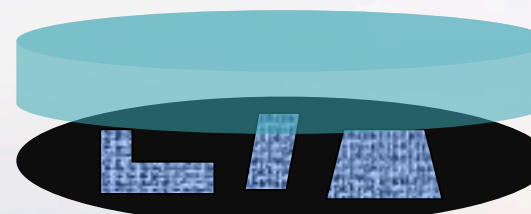
BCP DSA



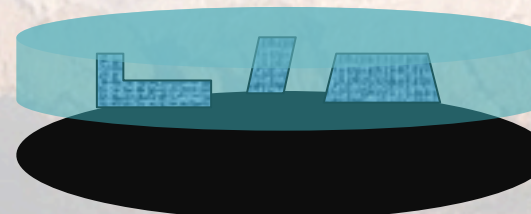
etch



transfer to NIL



NIL to die



### IL-defined chemical pre-patterns

- 60-90 nm pitch, ~4 cm<sup>2</sup> areas

### BCP Directed Self Assembly

- 20-30 nm pitch device patterns
- 10-50 nm CDs
- Half-pitch to ~11 nm over ~4 cm<sup>2</sup> areas

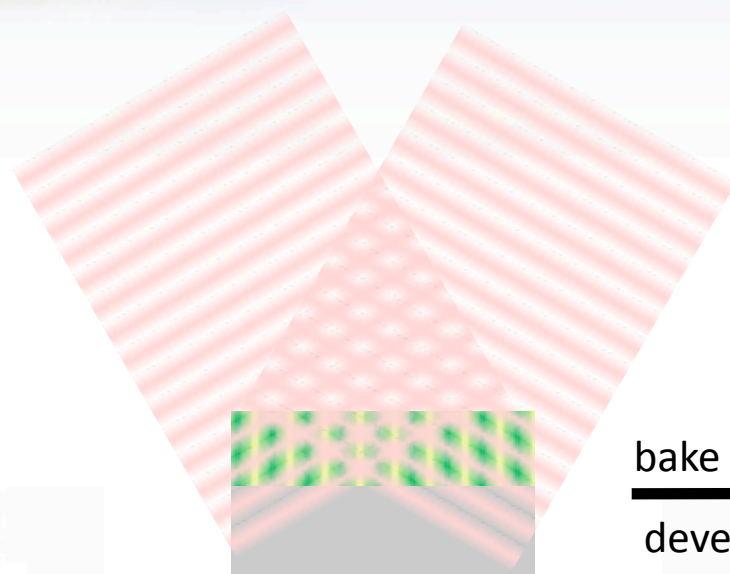
### Pattern transfer to create Nano-Imprint lithography (NIL) device masters



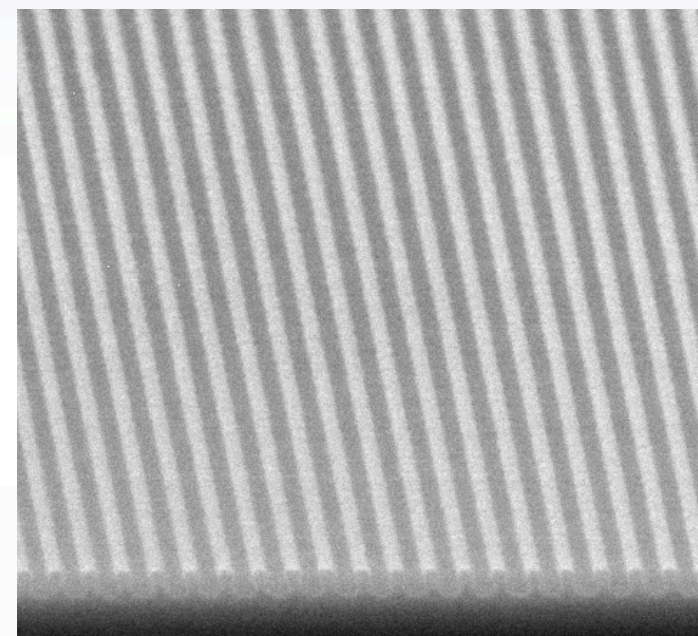
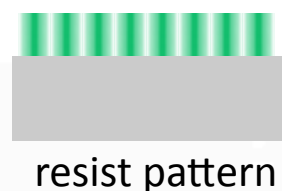
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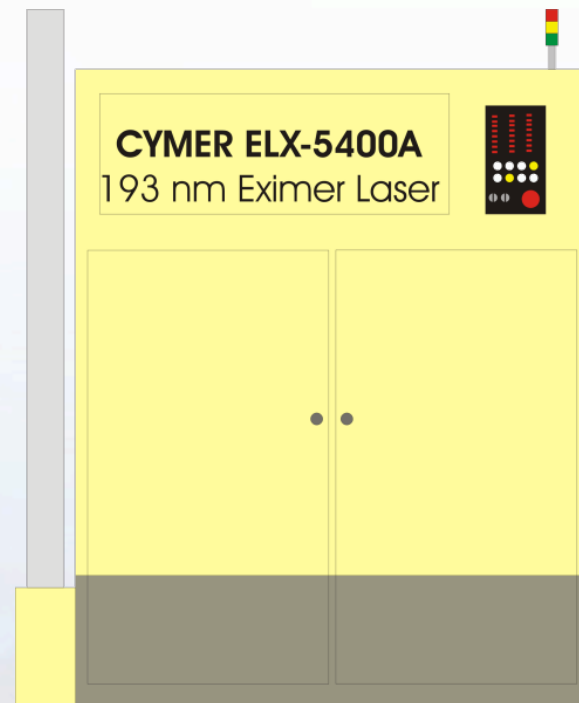
# Optical Interference Lithography



bake and  
develop



Critical dimensions  $\sim 70$  nm  
Patterned areas  $\sim 4\text{cm}^2$



dielectric  
mirror

BS = beam splitter

BS

Aperture

Beam  
Telescope

immersion prism

Water

Wafer

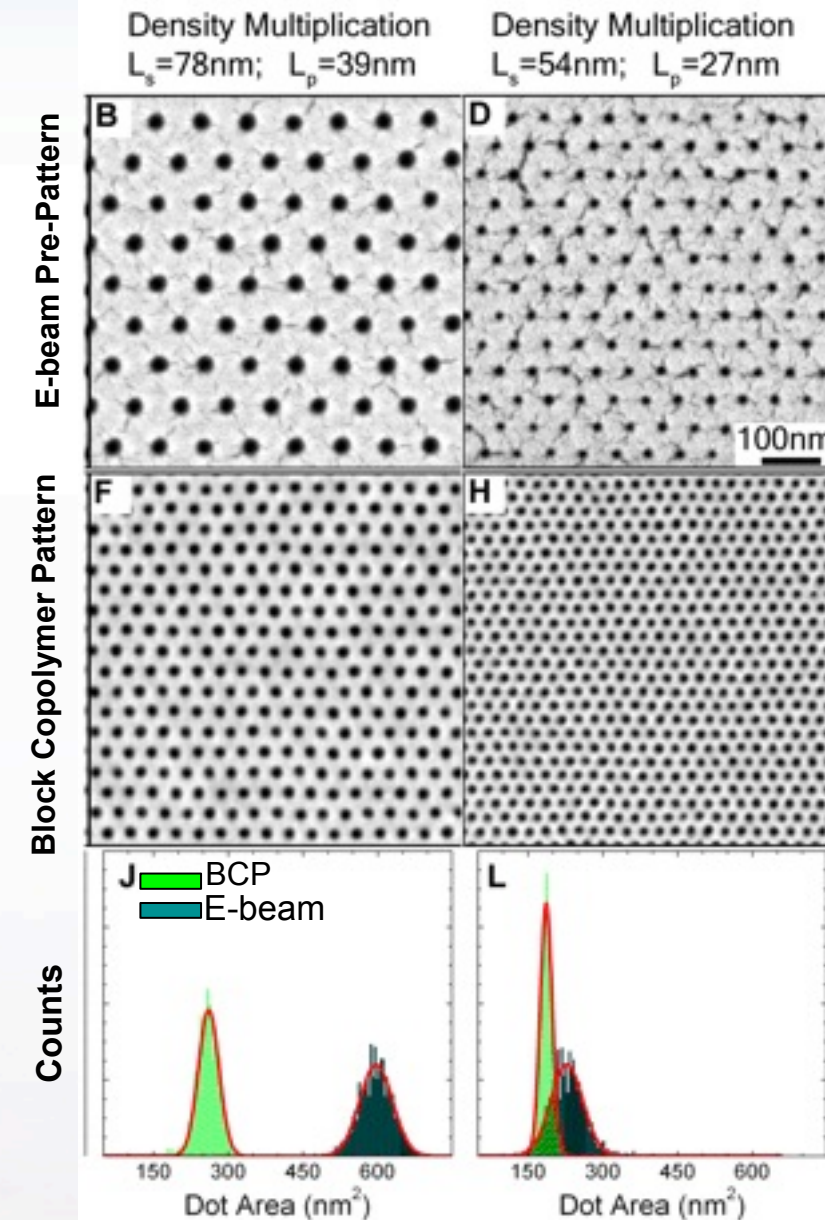
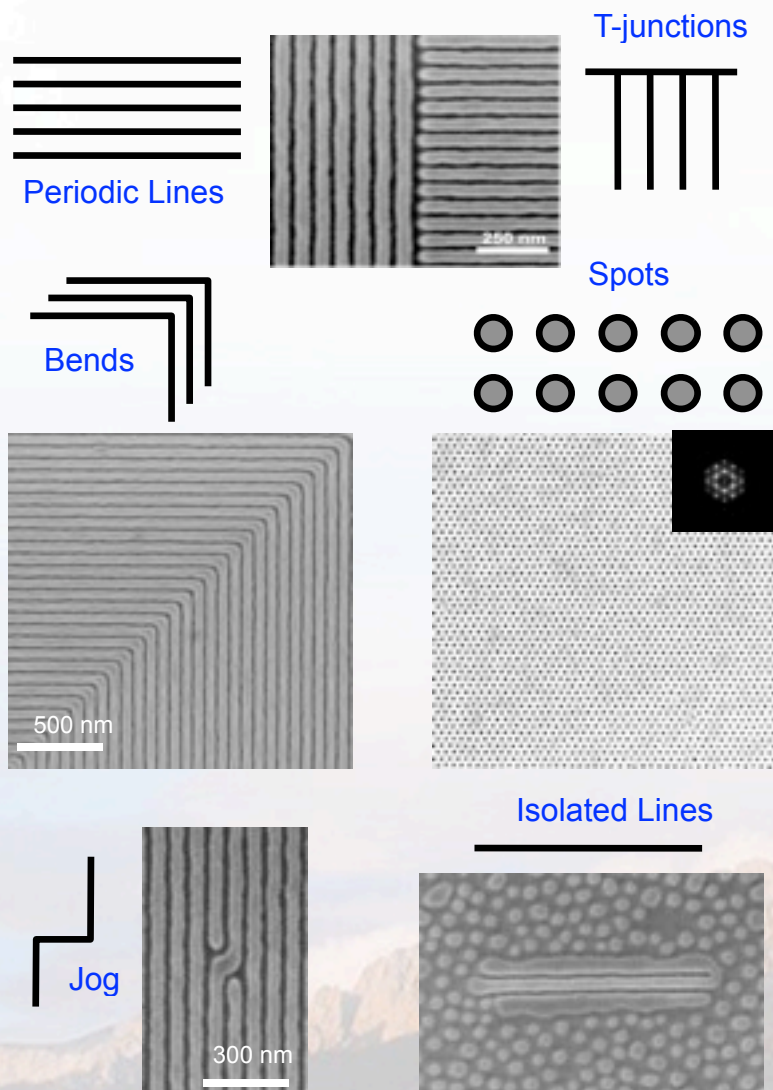
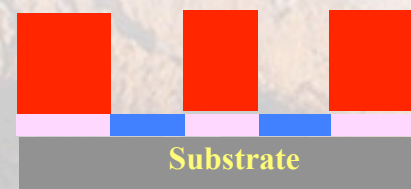
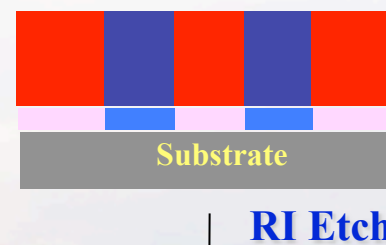
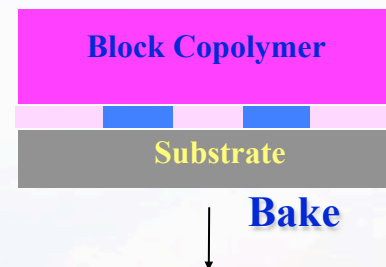
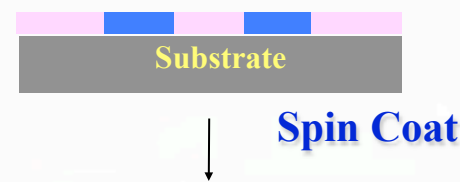
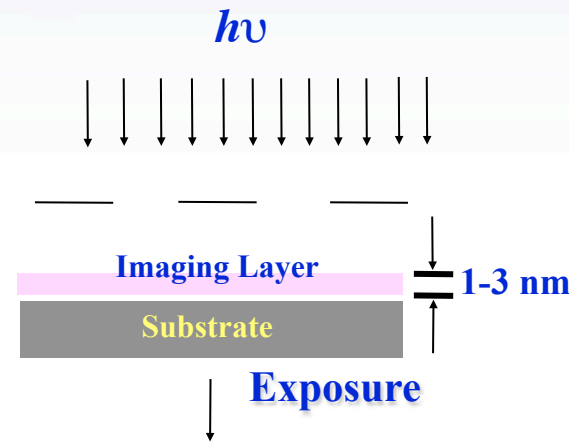
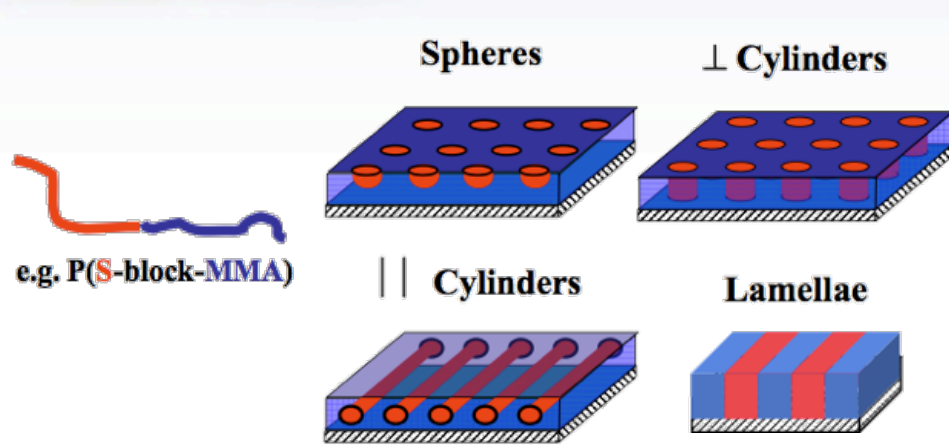


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# Block-Copolymer Directed Self Assembly

with Profs. Paul Nealey  
and Juan de Pablo



Ruiz, Nealey, de Pablo et al. *Science*, 2008

Daoulas et al., *Langmuir*, 2008

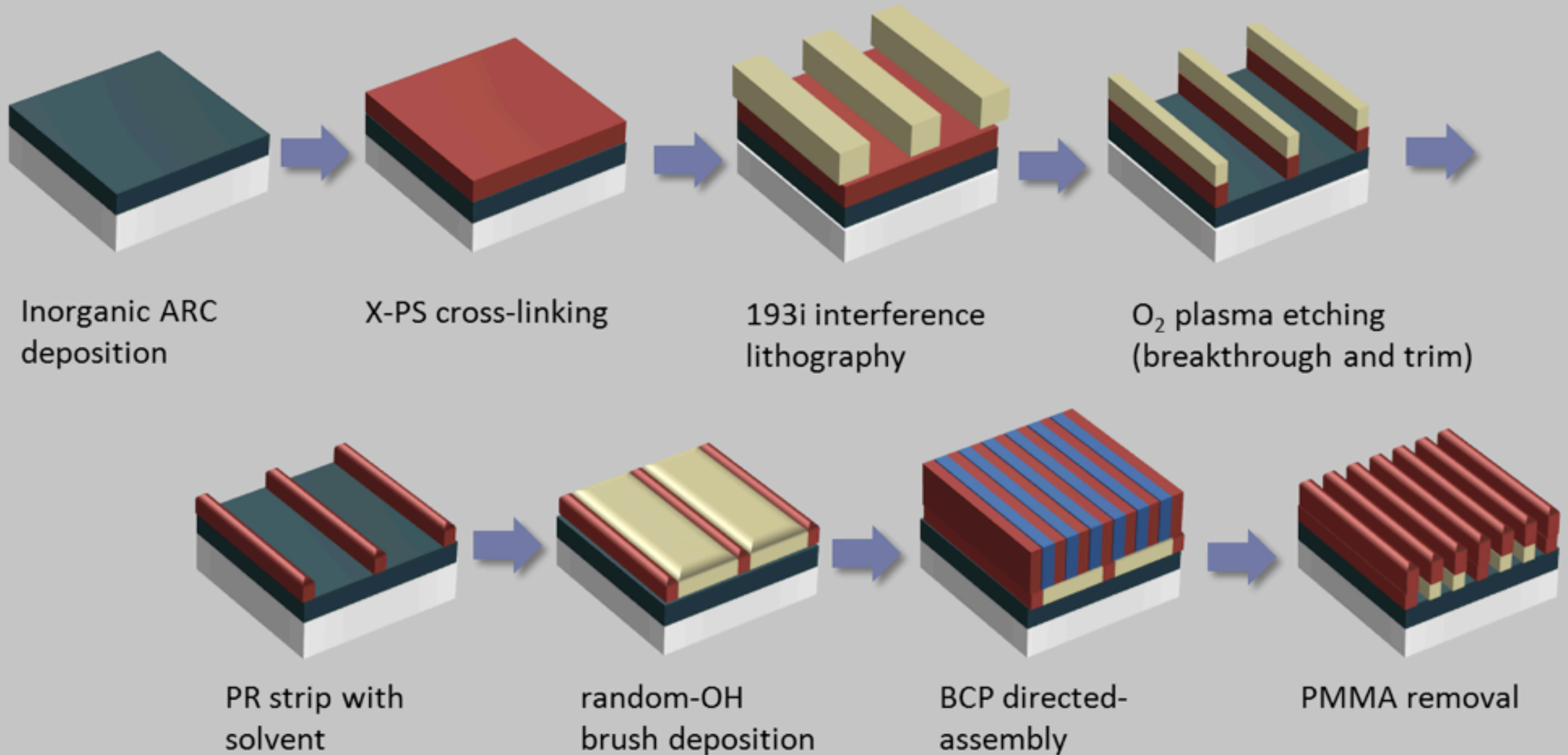
Sandia National Laboratories

Stoykovich et al. *ACS Nano*, 2007, *Science* 2005



# Density Multiplication

## Process flow with ARC and 193i





3x density multiplication  
30nm features in 90nm IL pattern  
over mm<sup>2</sup> areas



# Density Multiplication

22-22k on 100nm

300nm

18-18k on 110nm

300nm

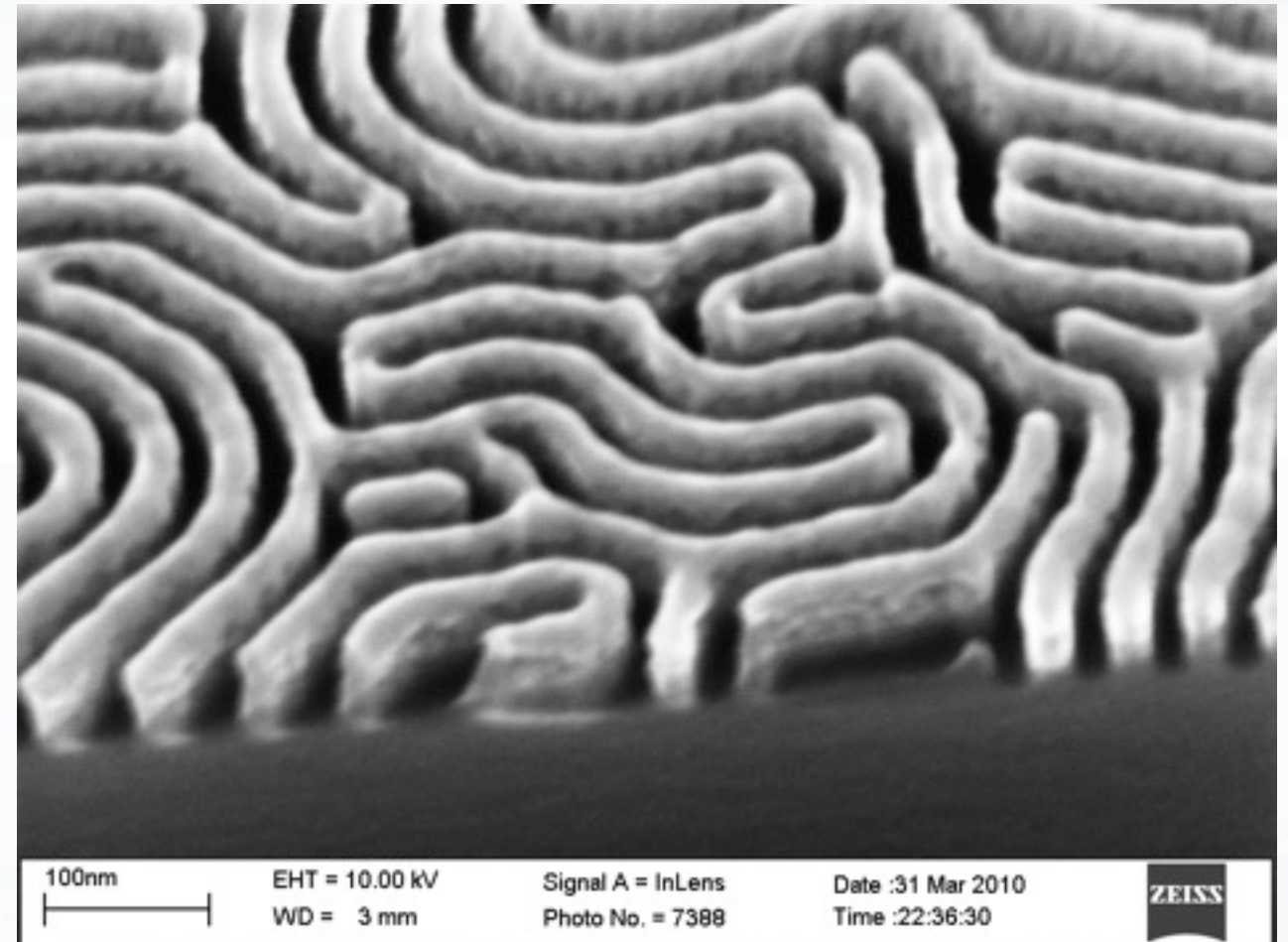
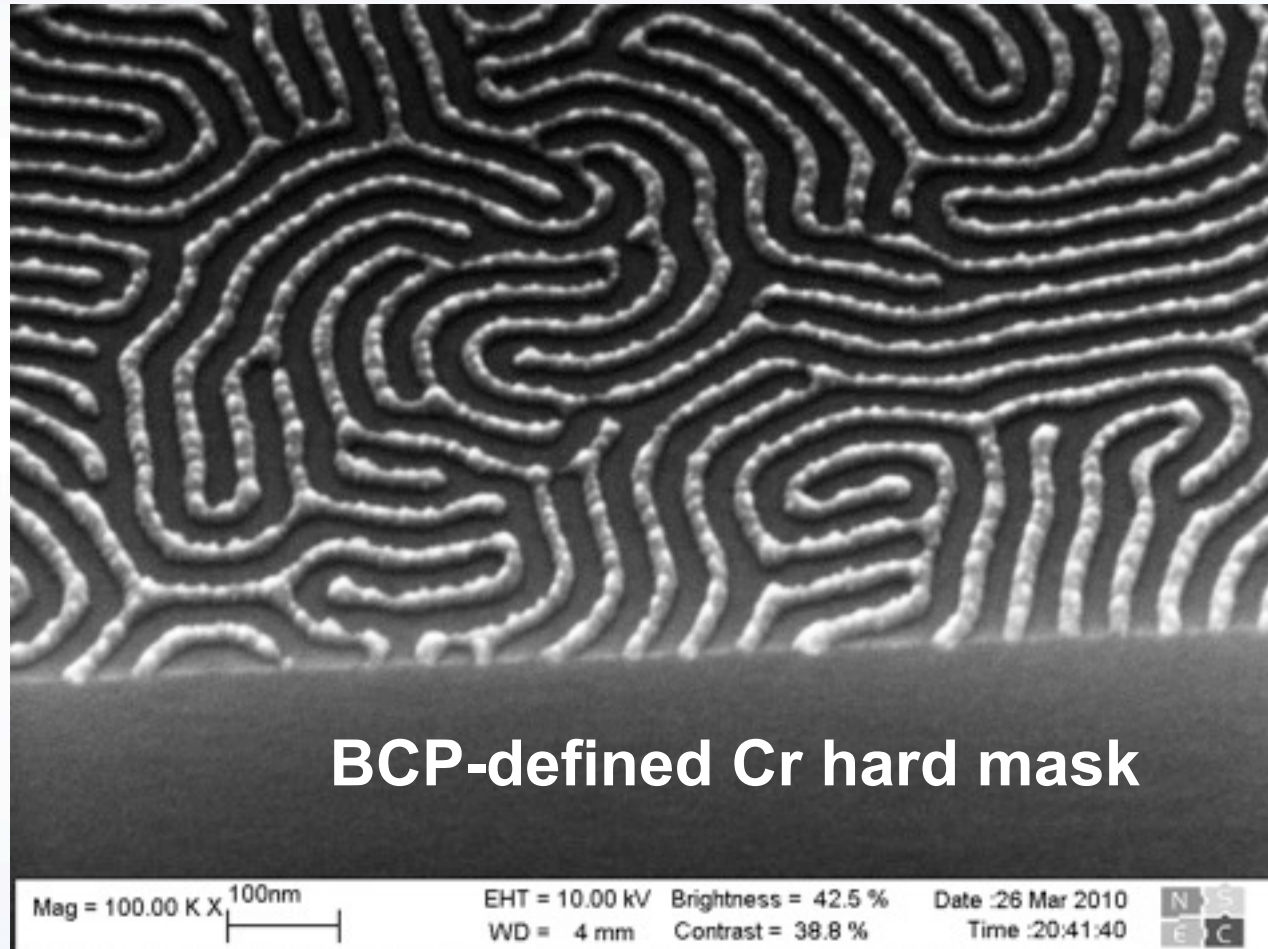
4X Multiplication

Molecular weight inaccuracies, inconsistencies, and distributions limit continued multiplication factors

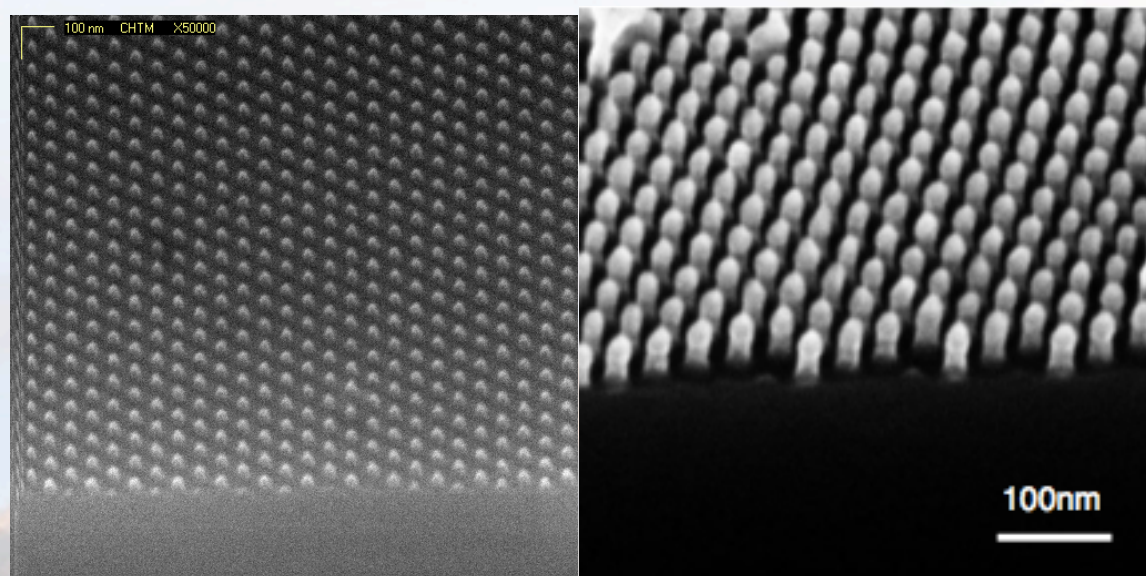
Surface interactions are crucial



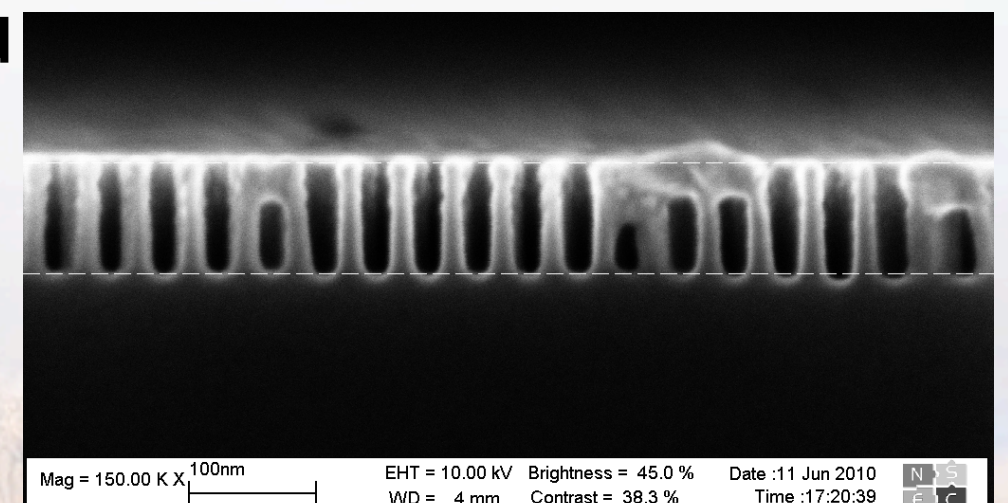
# Pattern Transfer



Si etched  
through  
Cr mask

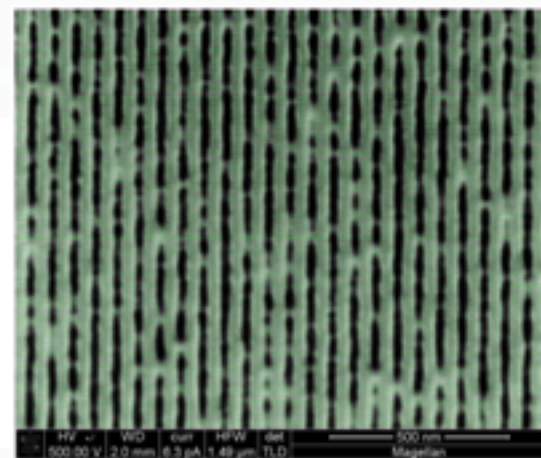
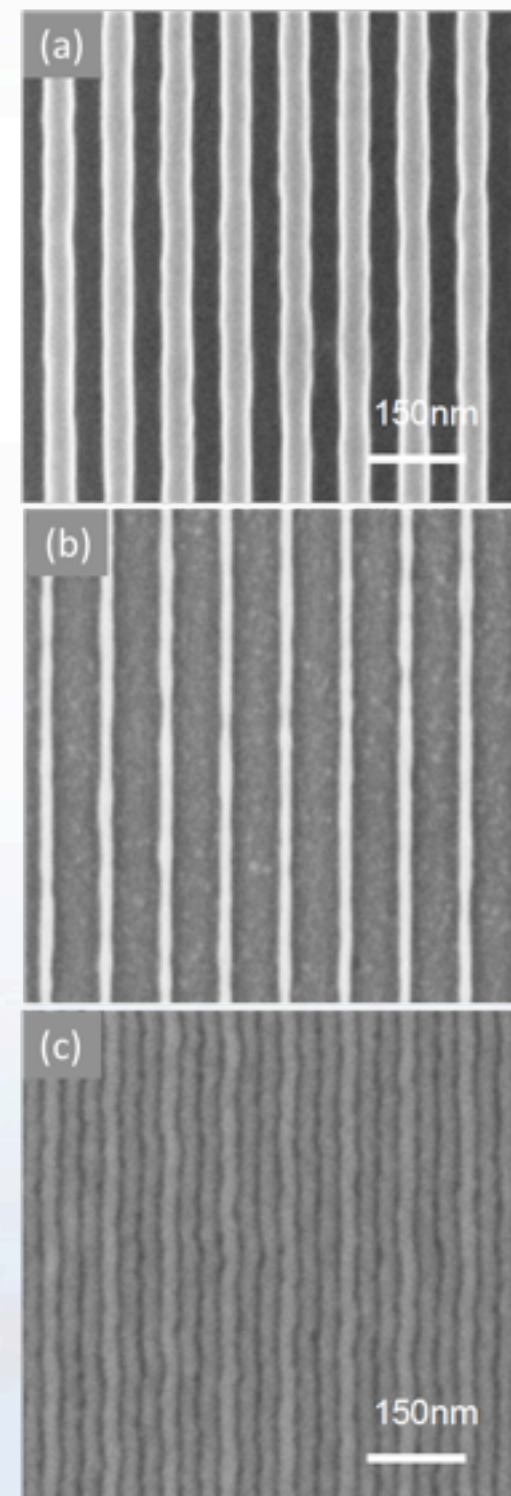


Si pillars  
defined  
by BCP  
for NIL  
master

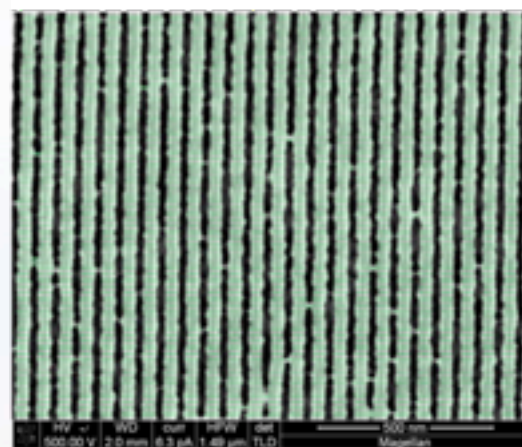




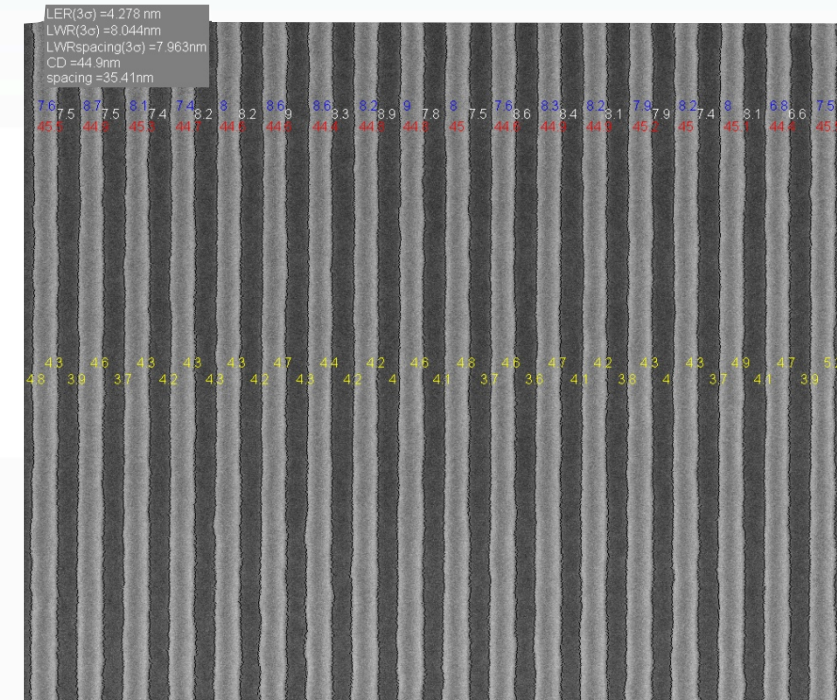
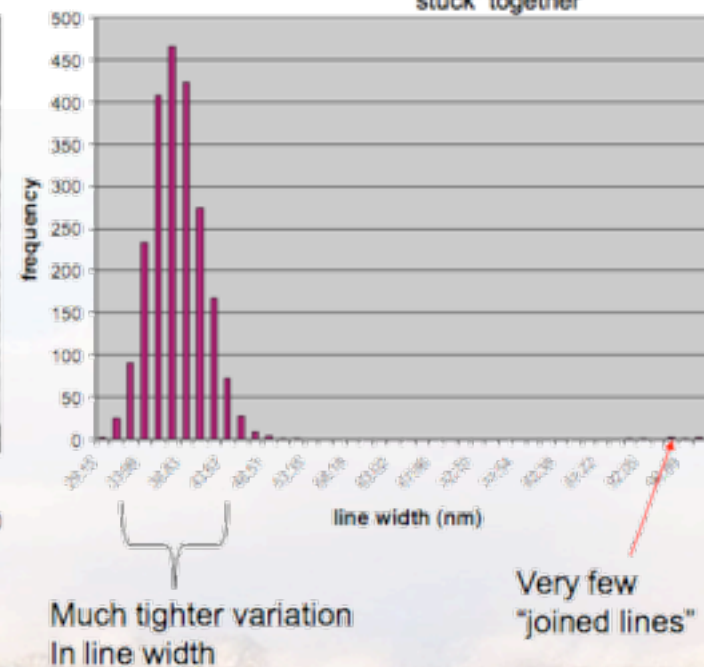
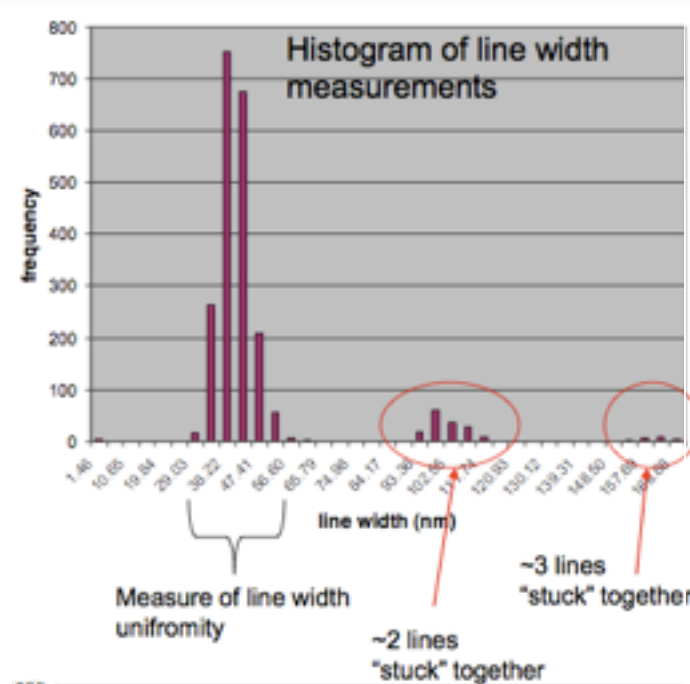
# Metrology



After insertion of 100 grid lines and  
BOOLEAN combination



Wafer090121-002\_30nm\_middle bo

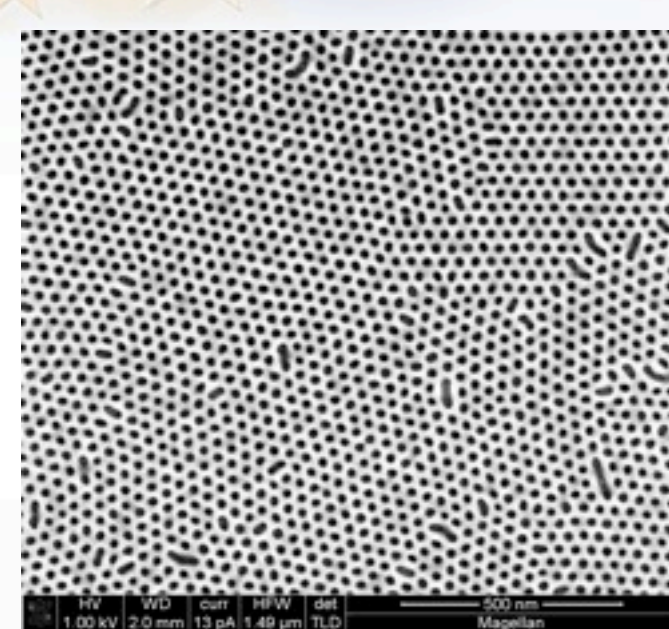


**Line Edge Roughness (LER)**  
3 $\sigma$  deviation of a line edge  
from best-fit straight line  
target LER < 5 %

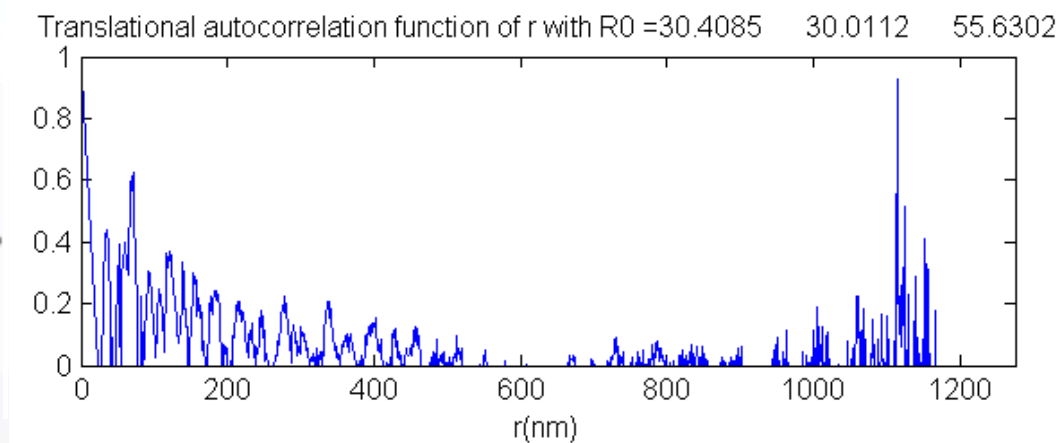
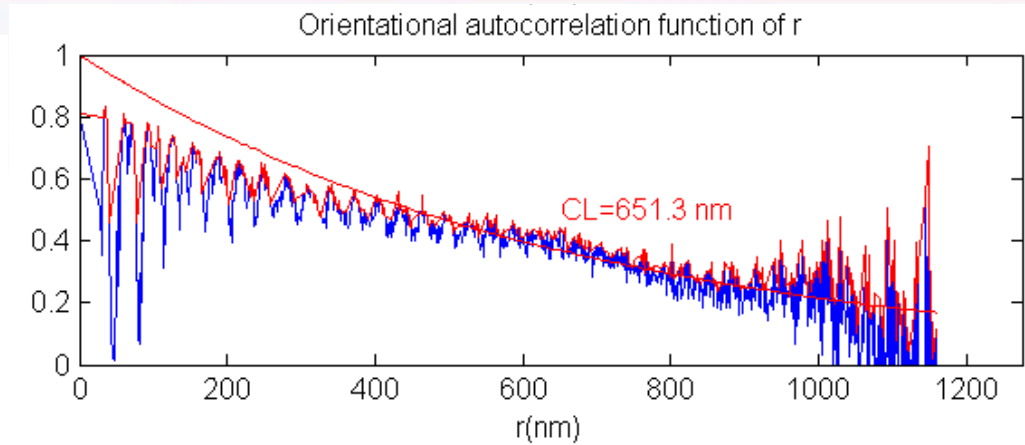
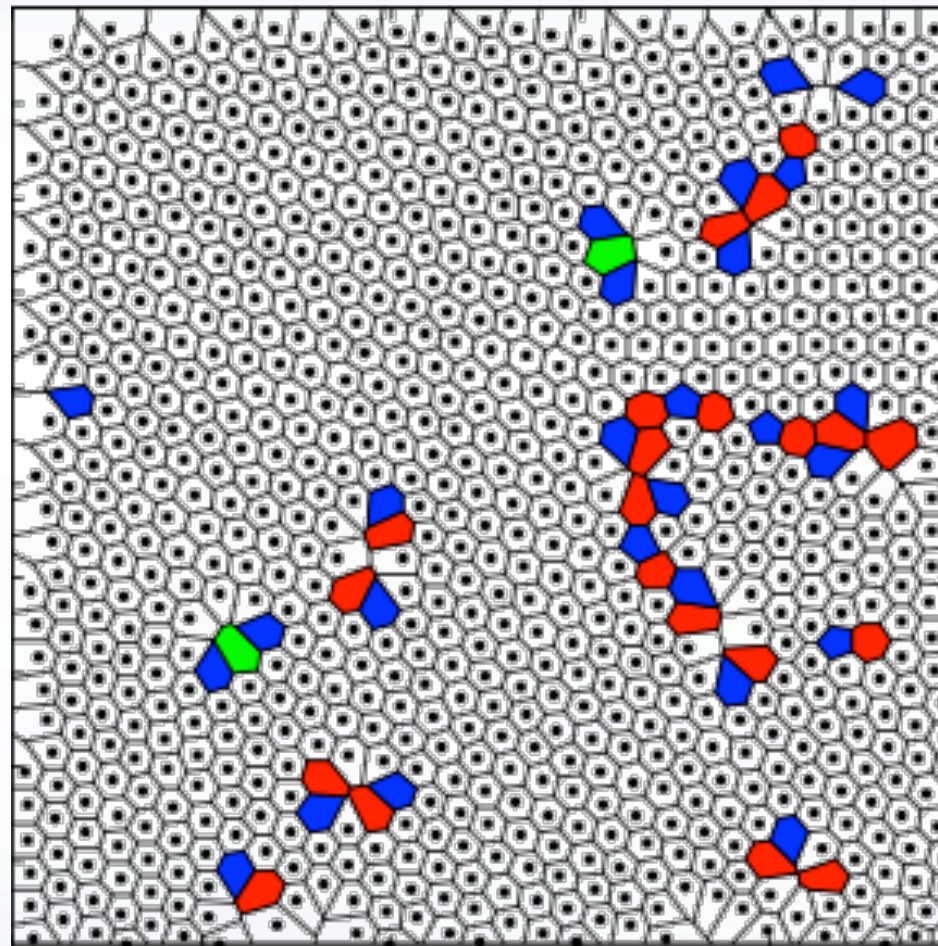
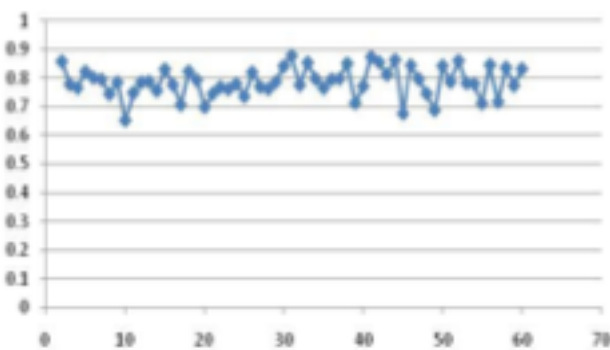
Intel-blessed standard, quantitative, non-destructive  
feature/defect analysis at each stage of process



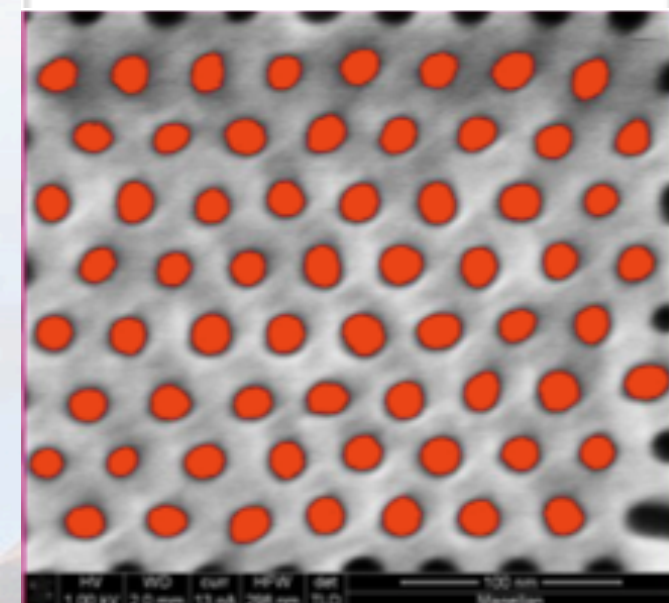
# Metrology



Roundness



All made possible by FEI Magellan SEM:  
quantitative sub-nm measurements from  
***uncoated*** samples

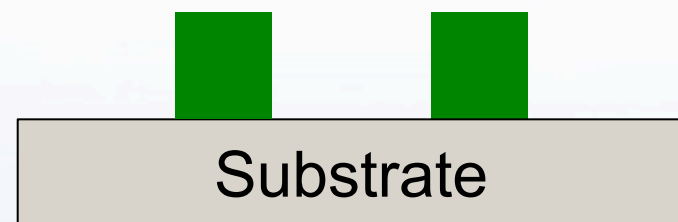




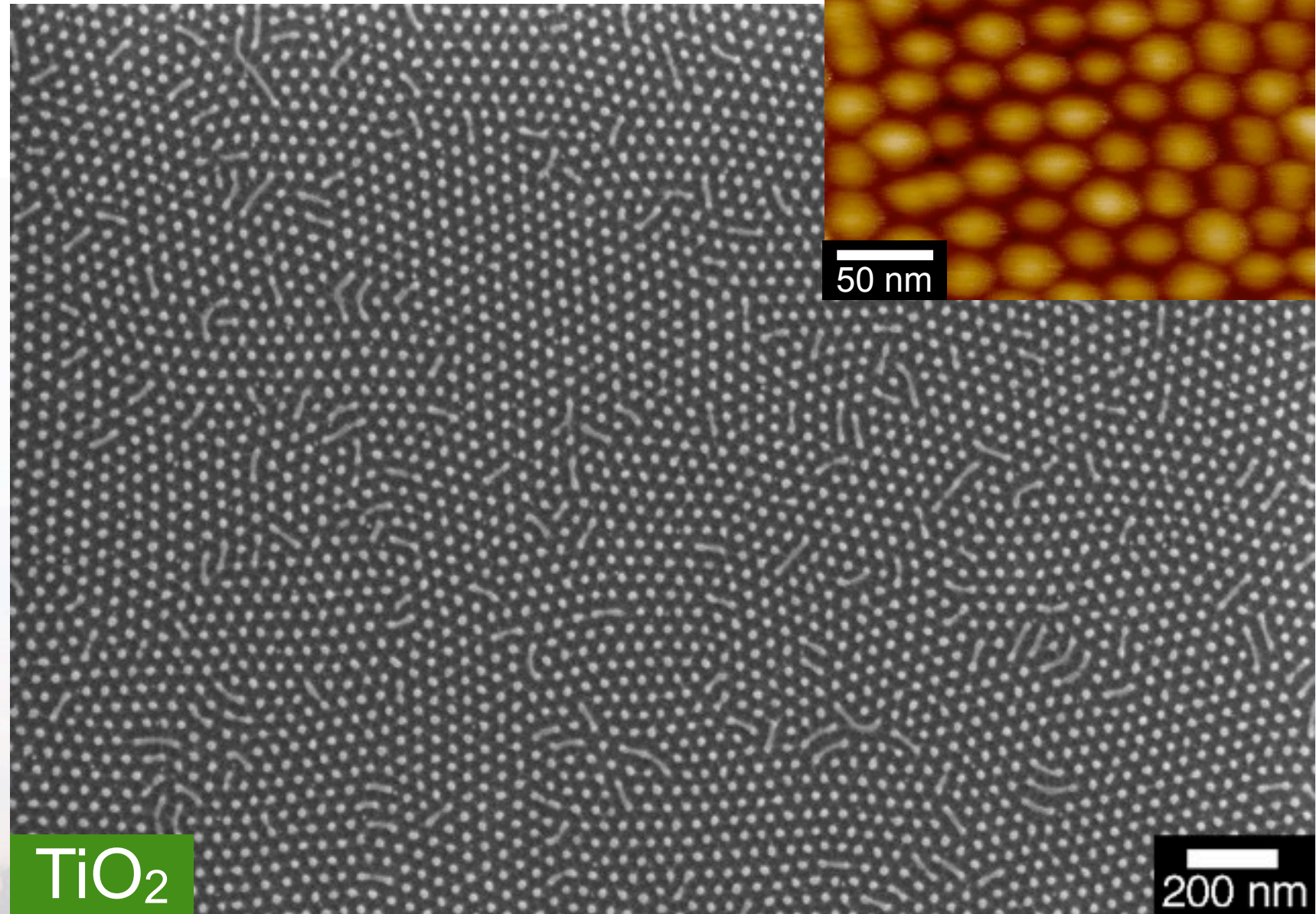
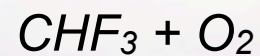
# Additive Fabrication of Patterned Electronic Oxides



Fill, Gel

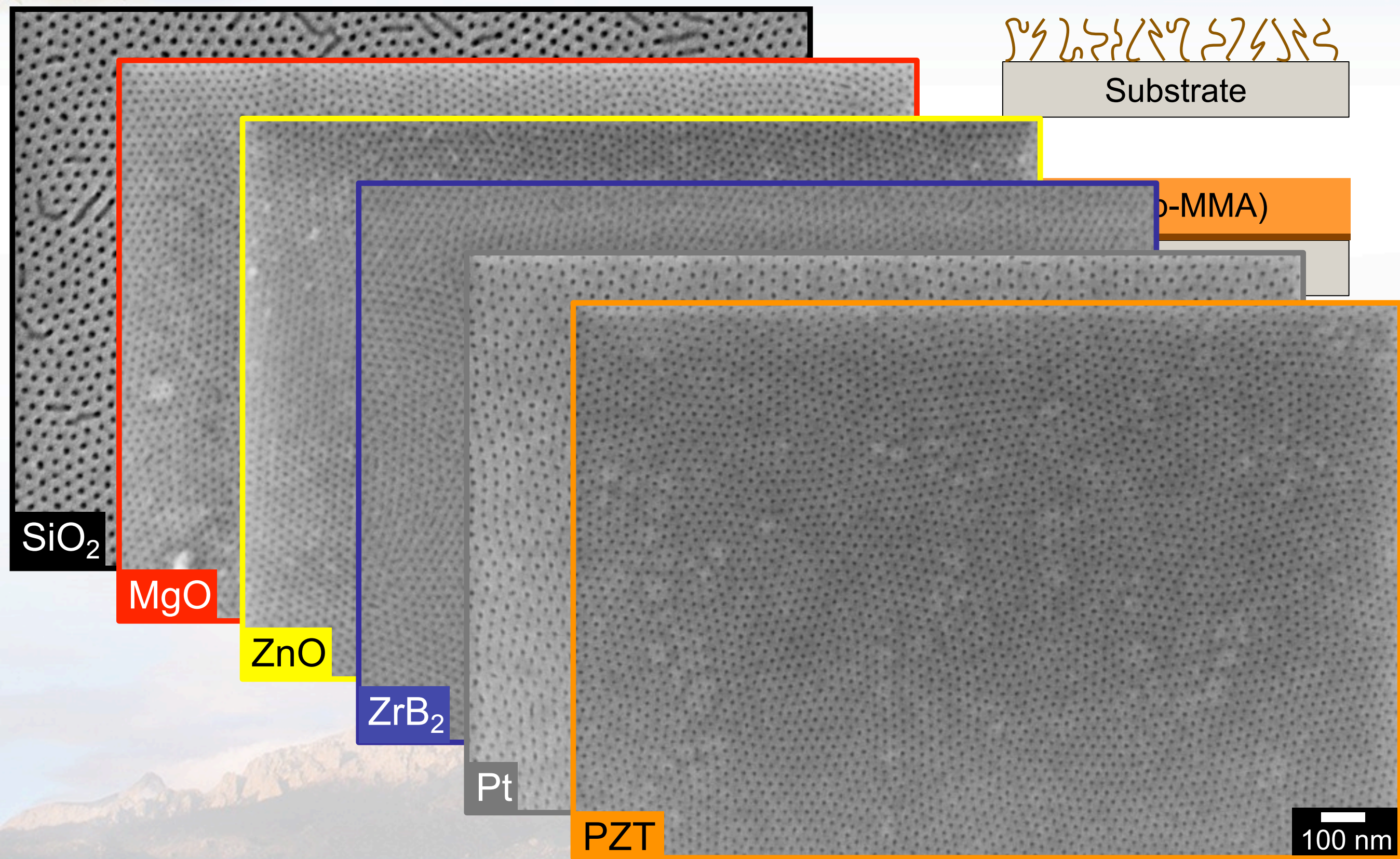


Remove Mask





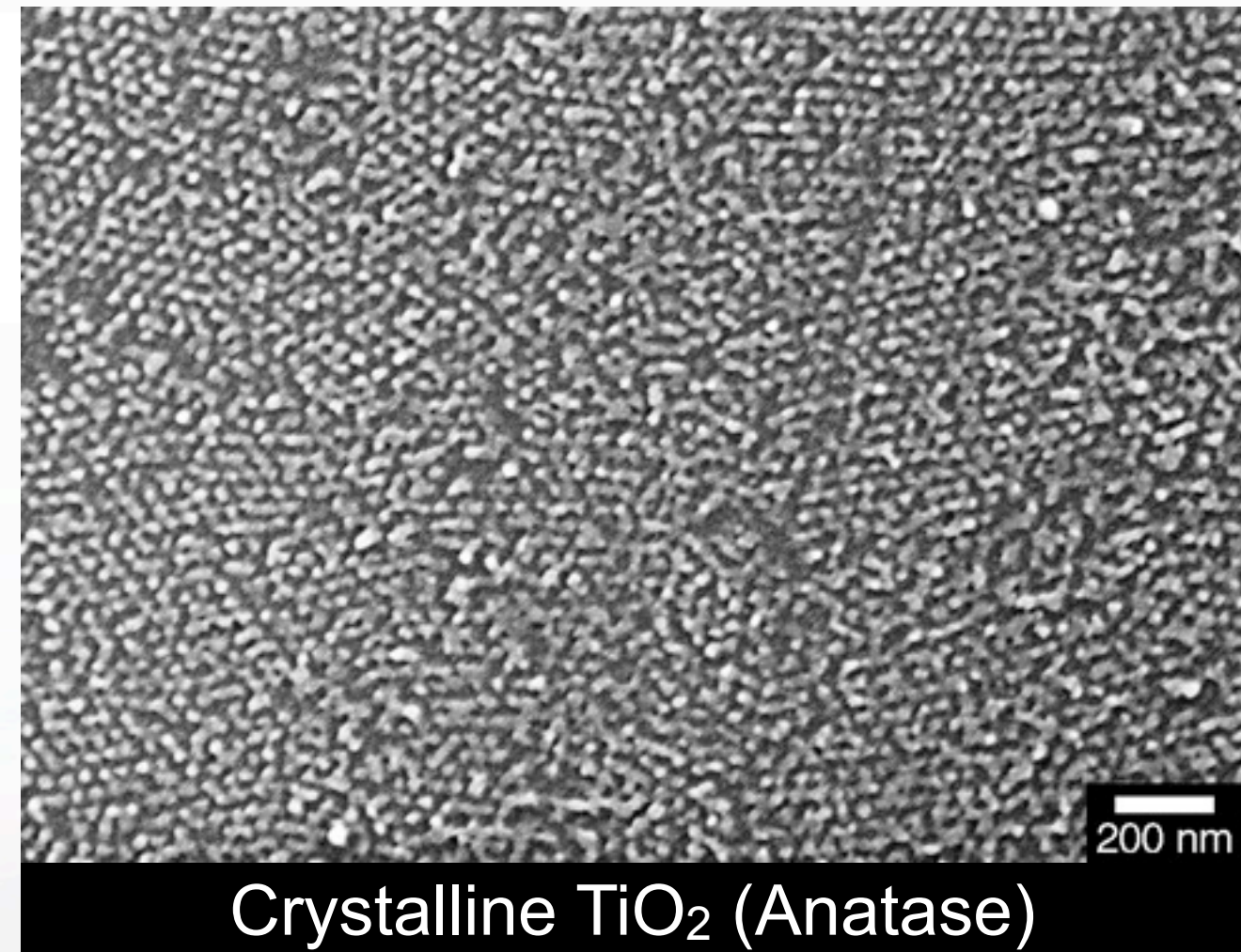
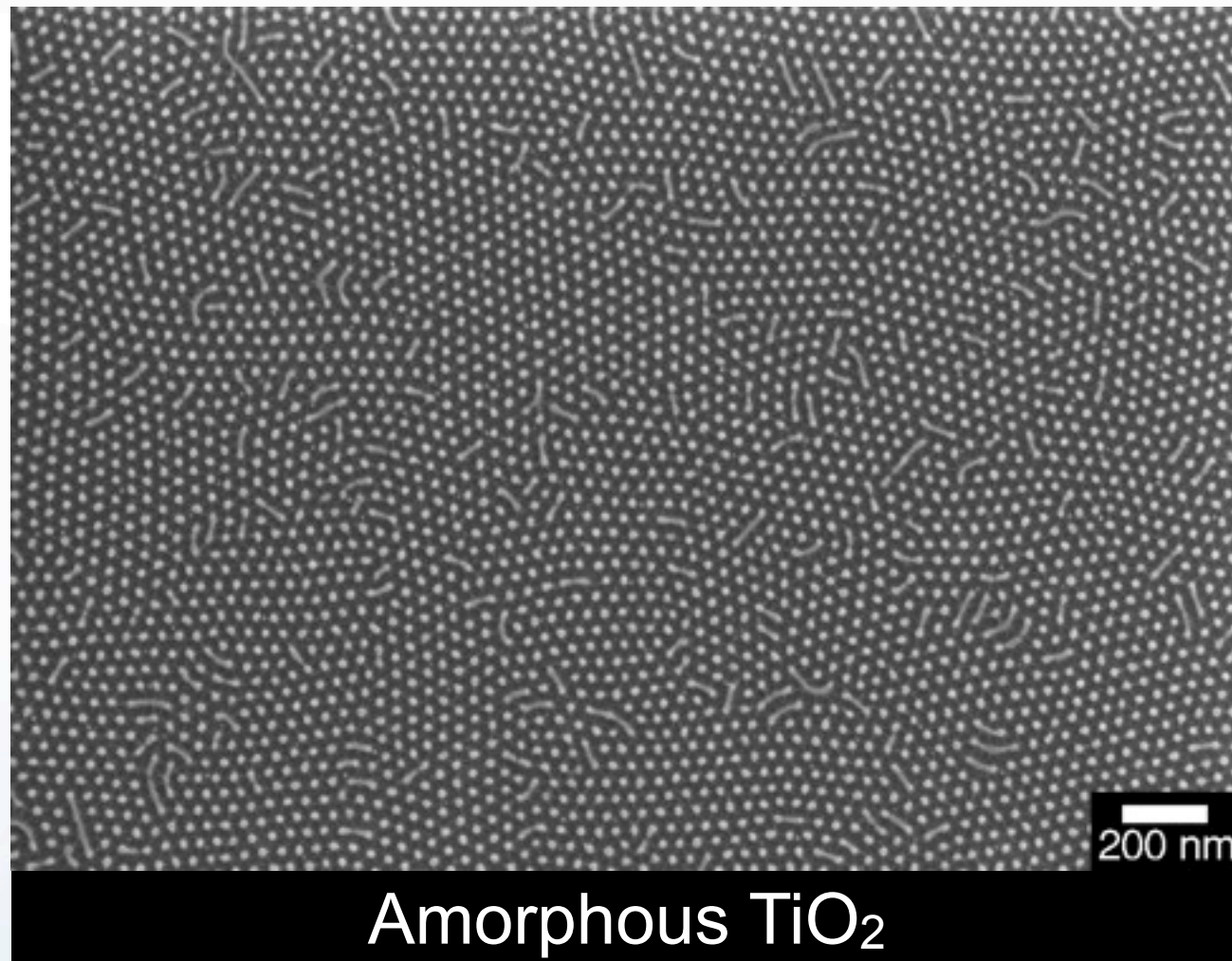
# Diblock Assembly on Various Substrates





# Crystallization Destroys Freestanding Nanofeatures

After removal of PS mask, TiO<sub>2</sub> nanopillars were heated to 550°C for 30min to crystallize

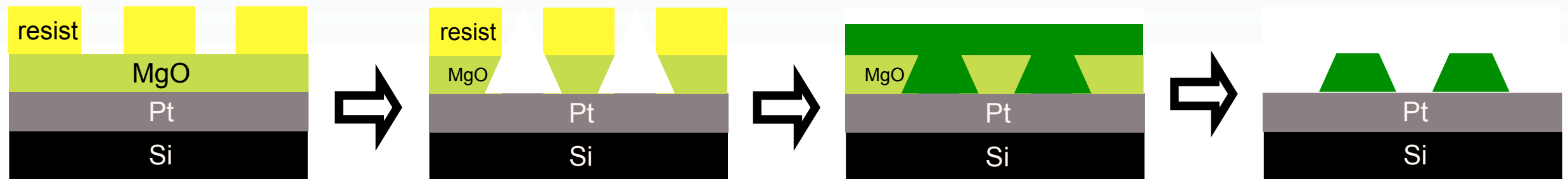


Still lacking:

- Controlled long-range order for addressability
- Crystallization before patterning or within inert and removable mask



# Maintaining Pattern Fidelity through Thermal Processing ( $>600^{\circ}\text{C}$ )





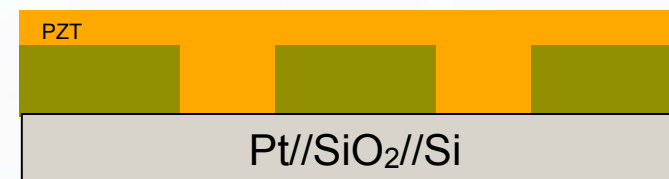
# Alternate Microscale Patterning



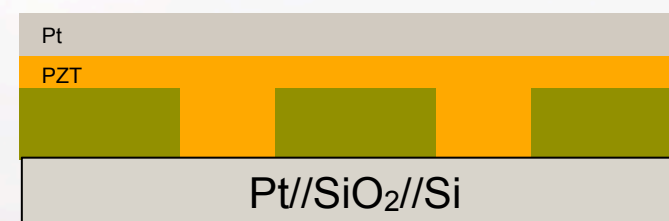
*etch*



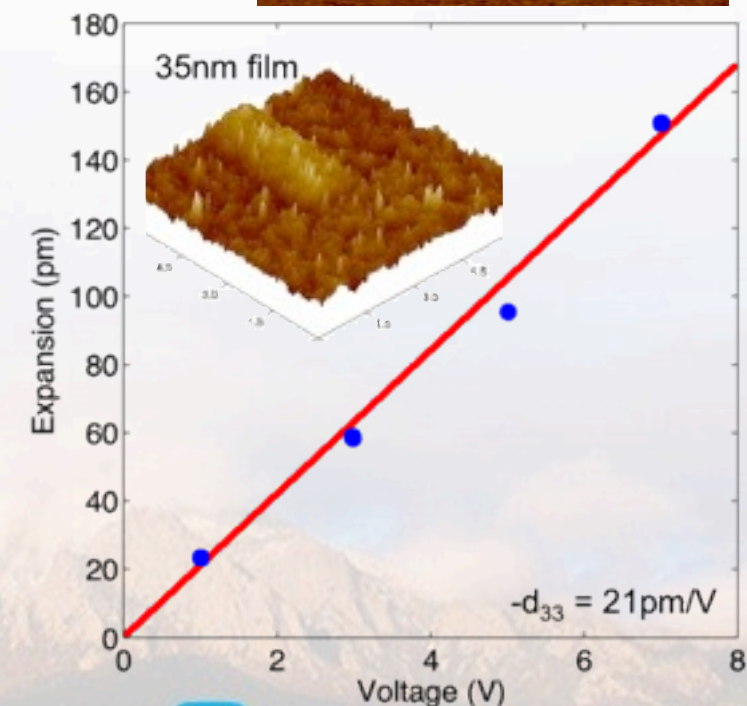
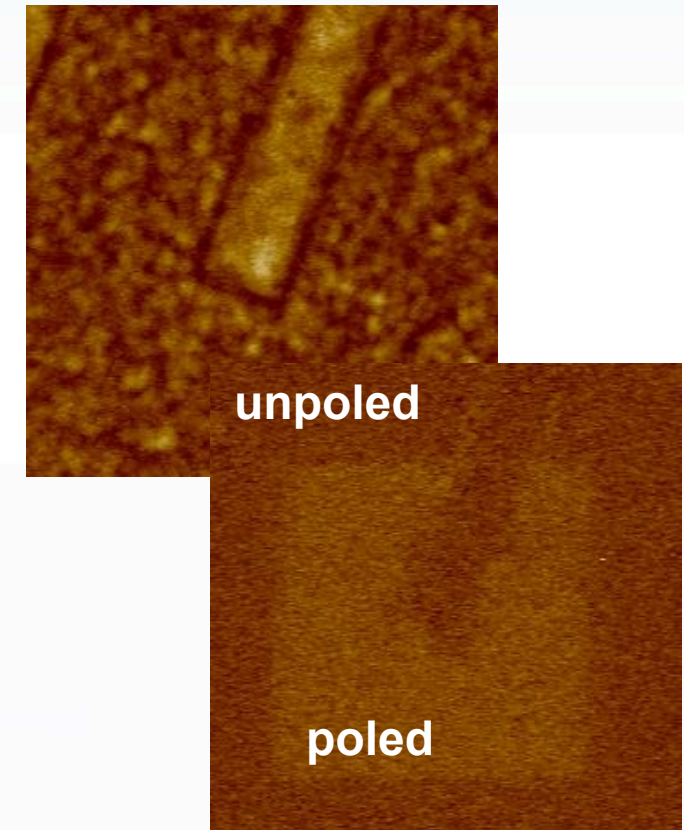
*deposit, crystallize*



*sputter Pt*



*liftoff*





# Maintaining Pattern Fidelity through Thermal Processing ( $>600^{\circ}\text{C}$ )

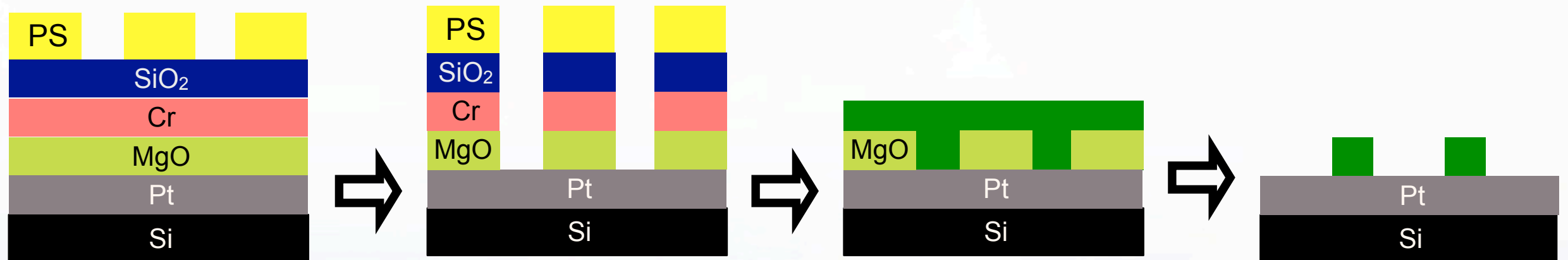
**Wet Etch Limits to Microscale**





# Maintaining Pattern Fidelity through Thermal Processing ( $>600^{\circ}\text{C}$ )

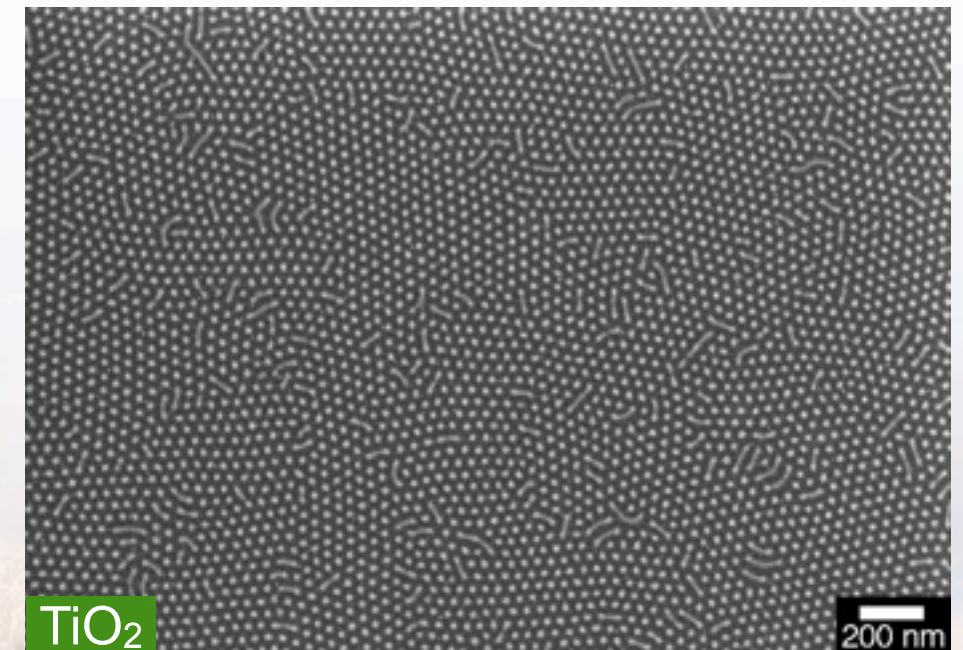
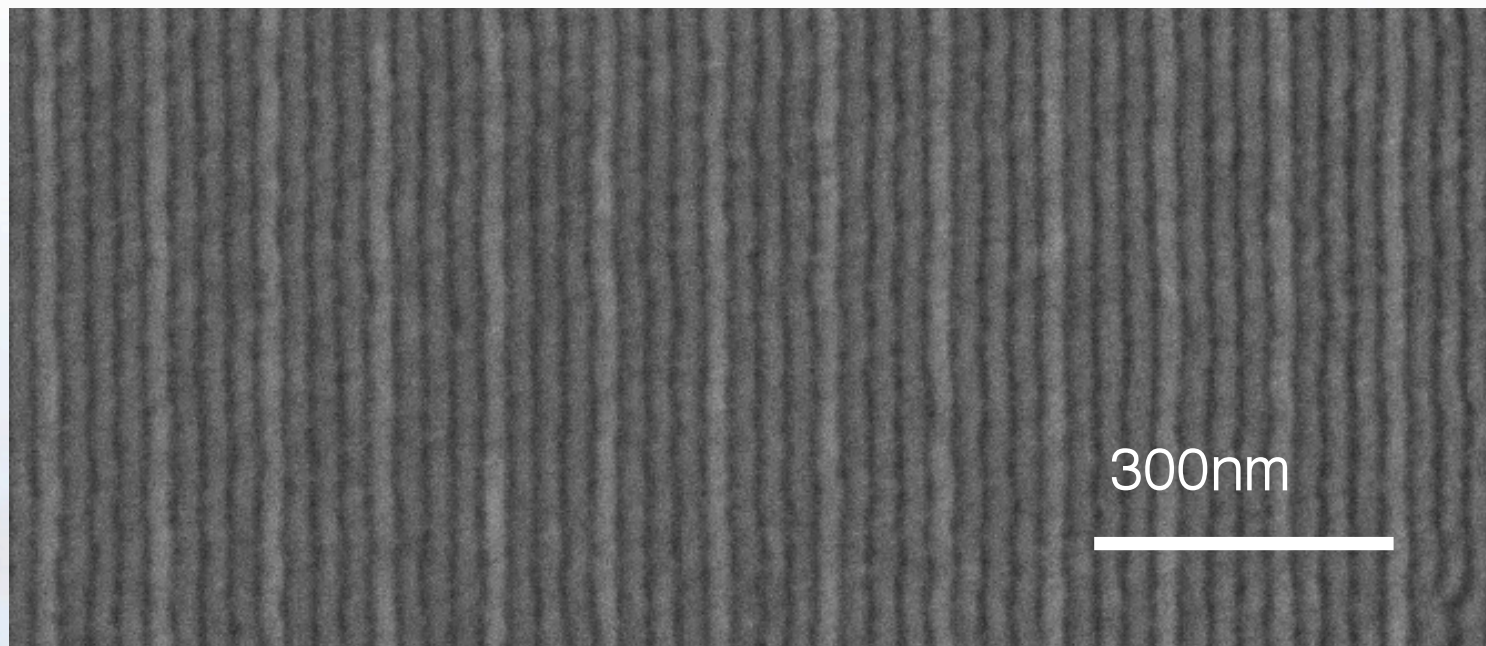
Wet Etch Limits to Microscale





# Summary

- Solution deposition of ferroelectrics is alive and well
- Up to 4x density multiplication with DSA-BCP over mm<sup>2</sup> areas
- Extended BCP-based patterning to wide variety of materials (substrates and solution-derived features)
- Initial work on extending functional solution-derived ferroelectrics to etch-free 2+ dimensions





# Acknowledgments

## Sandia

- Jon Ihlefeld
- Matt George
- Bruce Tuttle
- Chris Shelton
- Kelsey Meyer
- Mark Rodriguez
- Aaron Gin
- David Scrymgeour
- Bonnie McKenzie
- Dick Grant
- Michael Rye
- Jeff Stevens

## External Collaborators

- University of Wisconsin
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  - Charlie Liu
  - Lance Williamson
  - Brandon Peters
- University of Texas-Austin
  - Prof. John Ekerdt
  - Wes Ahearn
  - Wyatt Winkenwerder
  - Ryan Fitzpatrick
- University of Florida
  - Prof. Jacob Jones
  - Krishna Nittala
- Missouri S&T
  - Prof. Bill Fahrenholtz
  - Harlan Brown-Shaklee
- Intel
  - Todd Younkin
  - Mike Garner
  - David Shykind
  - Steve Putna
- ExxonMobil
  - Mark Disko
  - Amy Herhold

