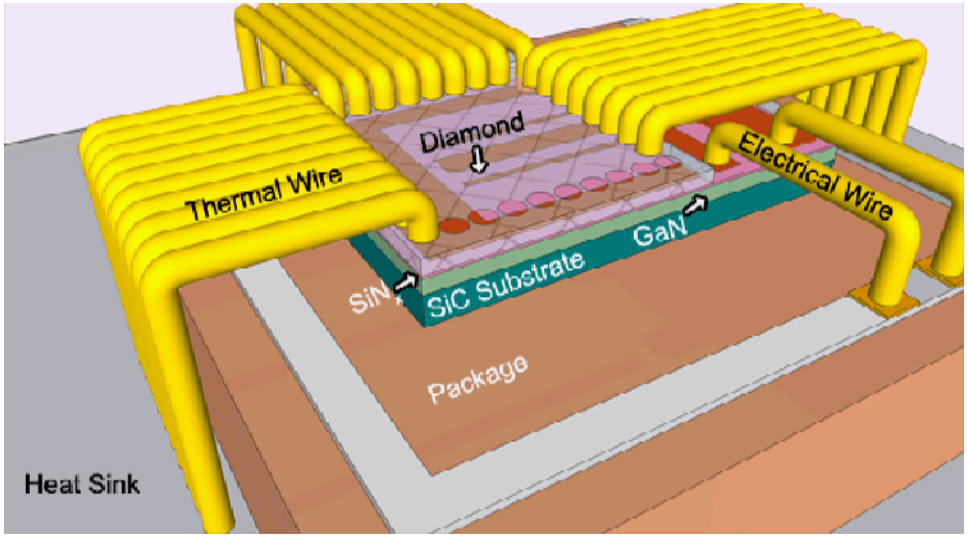
SAND2011-1300P

Top Side Cooling Via Integrated Thermal Circuits

Why wire bonds should be thermal connections too



Thomas Beechem

Embedded Thermal Management Workshop

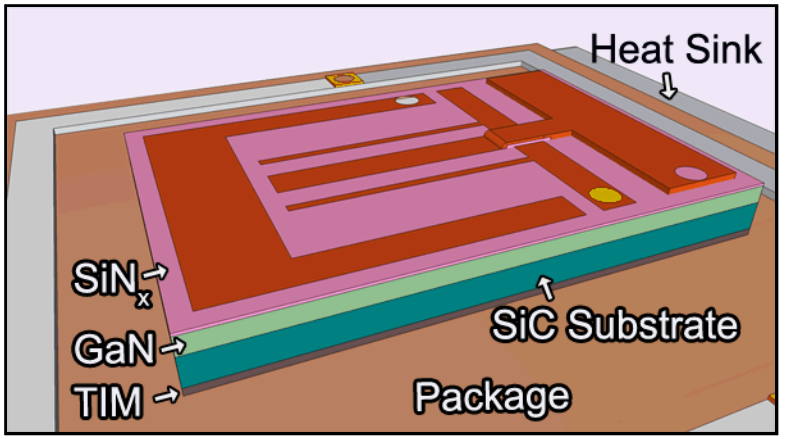
March 2, 2011

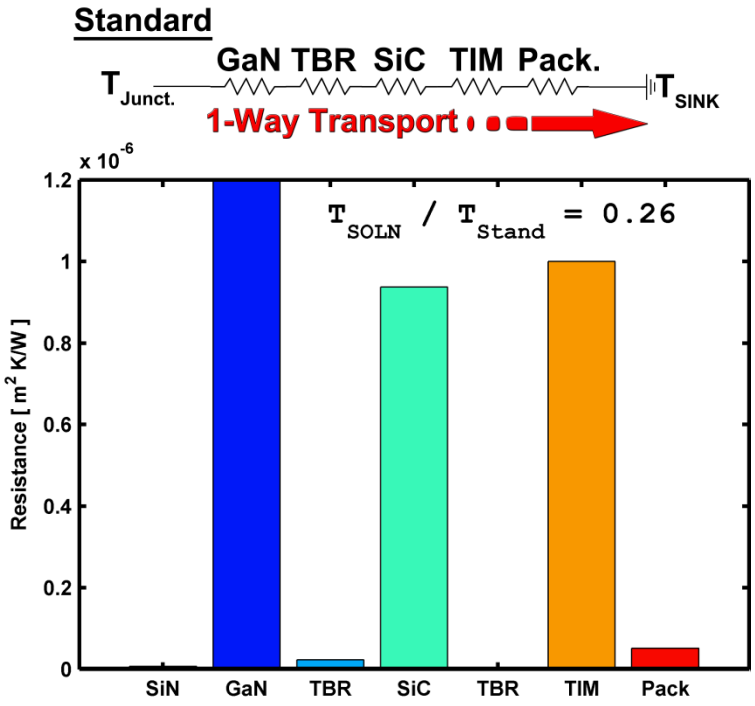
Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Problems with 1-Way Roads

- **Thermal resistance scales with length.**
- **To reach thermal ground, heat must travel through:**
  - **GaN, Substrate, TIM, Package, Sink**
- **Most effective thermal solutions will be placed closest to heat source.**
- ***Problem:*** **All solutions are "far away" from source and in one direction.**

Takeaway: New lane needed on thermal roadway.



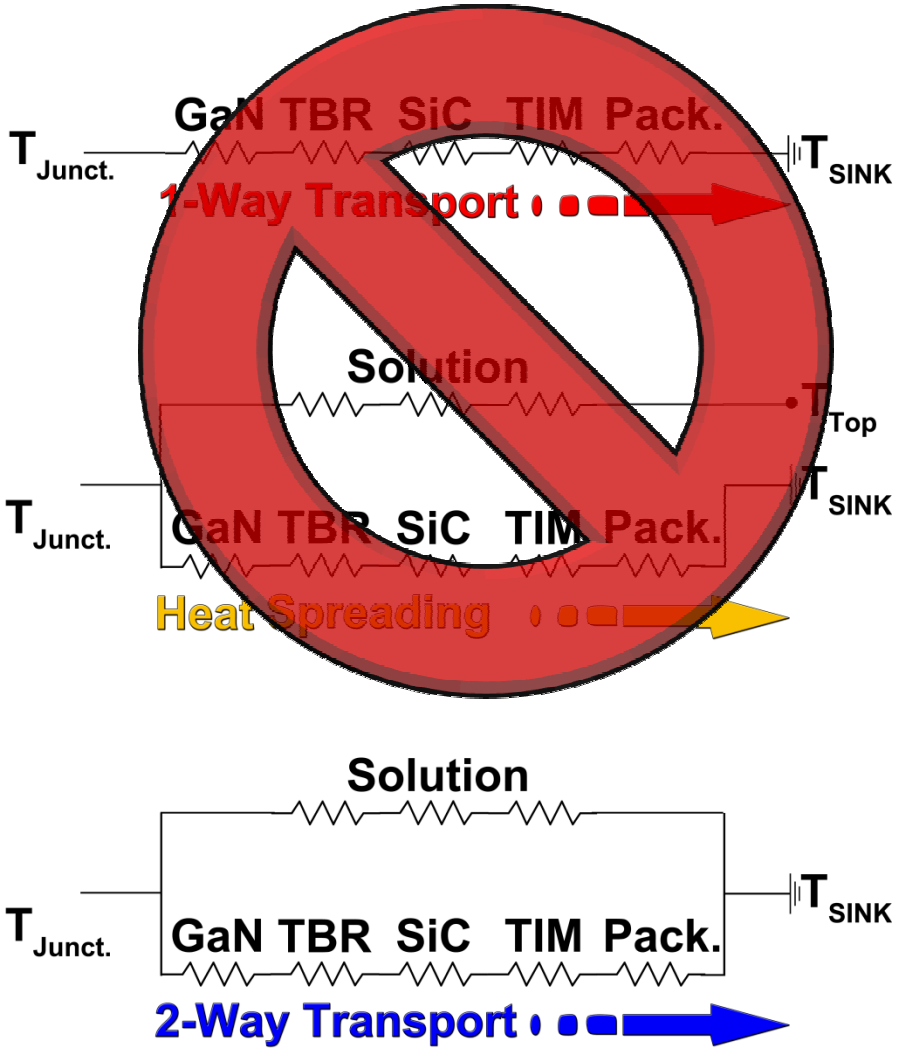


Sandia National Laboratories

New Lane Via Thermal "Skyscraper"

- ***Question:*** **Can a 3X improvement be achieved in 1-step?**
- **Only 1-direction to go…up**
- ***Solution:*** **Top side cooling having a resistance ½ that of the bottom channel.**

Takeaway: Top sided solution that sinks rather than spreads heat



Sandia National Laboratories

Task List

Goal: **Create top side thermal lane with ½ resistance of standard backside solution.**

TASKS:

1. **Place thermal conductor on top of device.**
2. **Sink conductor to thermal ground.**

What material for the conductor?

How do we "sink" it to the thermal ground?

How do we "stick" it on device?

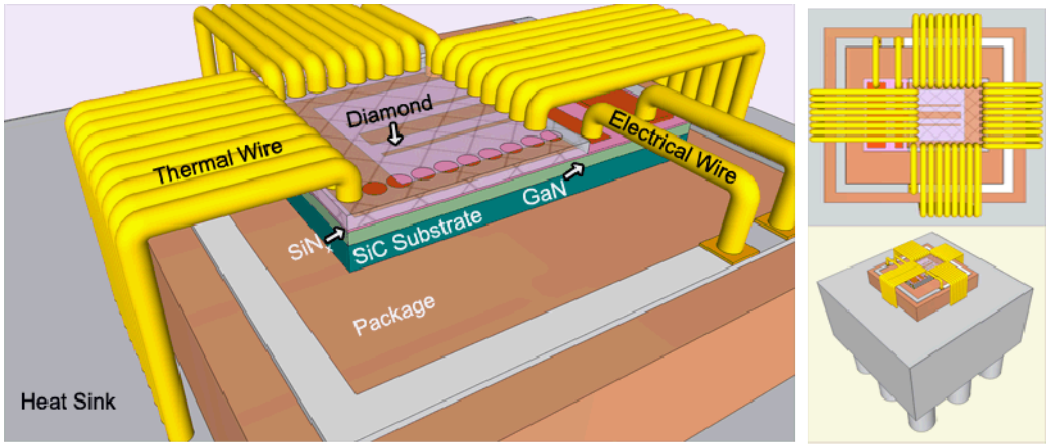
How do we minimize the thermal resistances?

How do we quantify the effectiveness?

Sandia National Laboratories

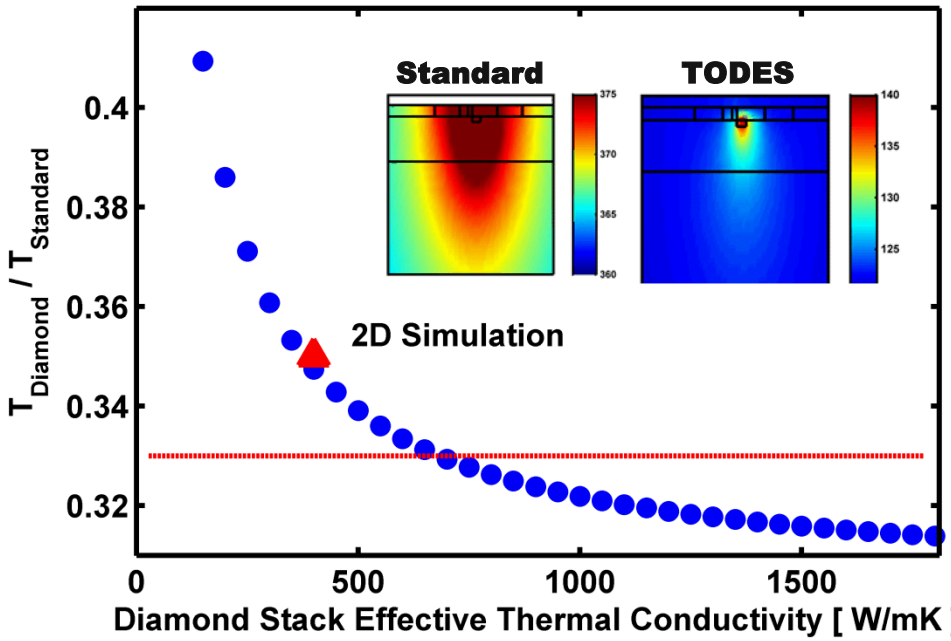
TOp-side Diamond Enabled Sinks (TODES)

- ***Approach:***
  - Utilize printing transfer techniques to place diamond on top of the device
  - Sink diamond to thermal ground using wire bonds



- ***Advantages:***
  - Low temp processing
  - Synthesis of existing technologies
  - Retrofit possibility
  - Margin in material properties

- This is ***NOT***:
  - GaN on diamond
  - Diamond growth on device



Sandia National Laboratories

Why Diamond?

- ***Margin:***
  - Commercial CVD makes it easier
  - 1800 W/mK >> everything else
- ***Problems:***
  - Not smooth
  - CTE mismatch with GaN
- ***Mitigation:***
  - Planarization
  - Thin, compliant, adhesive layers

Takeaway: Go with diamond but open to alternatives.

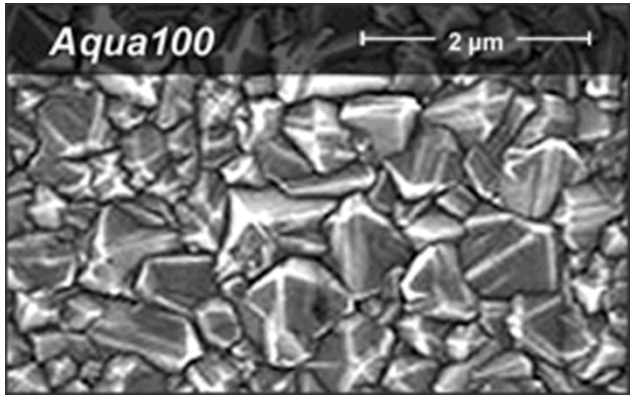
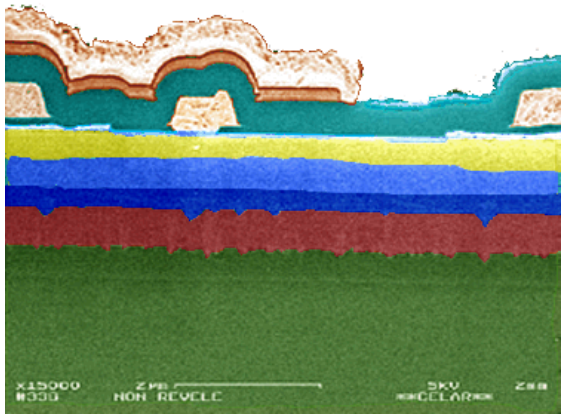
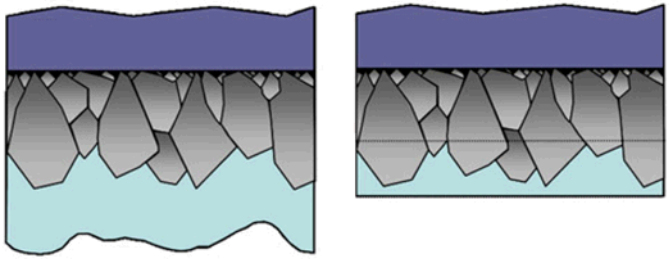


Image courtesy of Adv. Dia. Tech. (ADT)



Adapted from Burgaud et al. Micro. Rel. 2007.



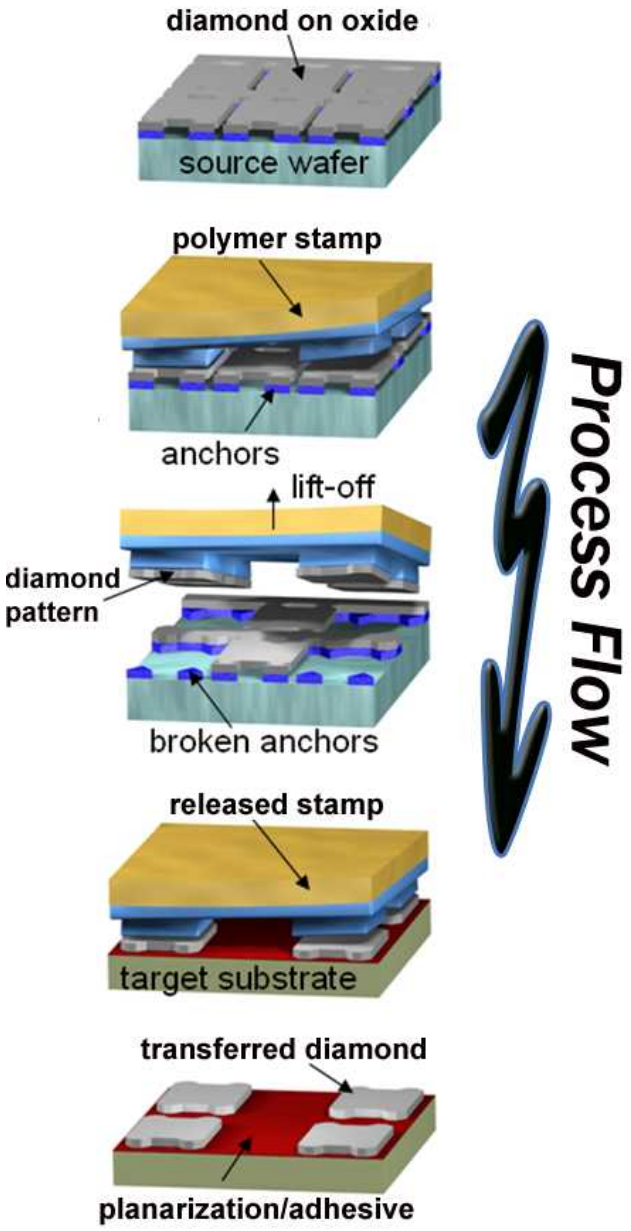
Rabarot et al. Dia. & Rel. Mat. 2010

Sandia National Laboratories

Sticking Diamonds to Devices

- ***Candidates:***
  - Gluing: epoxy/solder
  - Bonding
  - Printing transfer

- ***Printing Transfer Method***
  - Allows for placement of thin layers of material upon another
  - Established technology for diamond and GaN*
  - Strain minimization with flexibility?



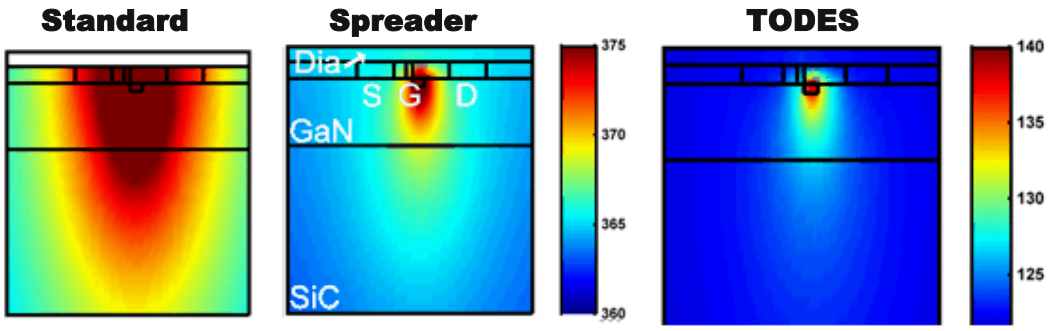
*DARPA Seedling led by Semprius with support from M. Rosker

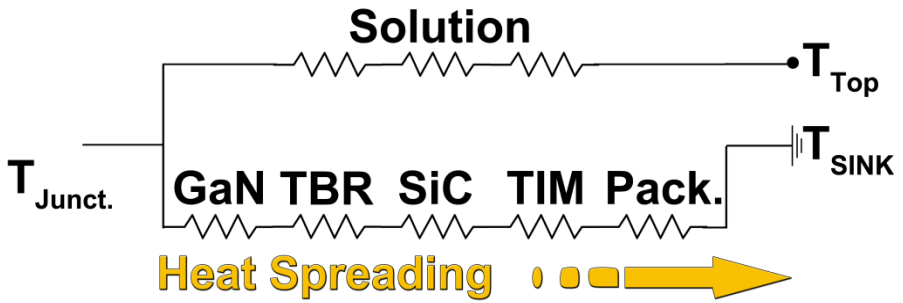
Adapted from Rogers et al. Science 2006.

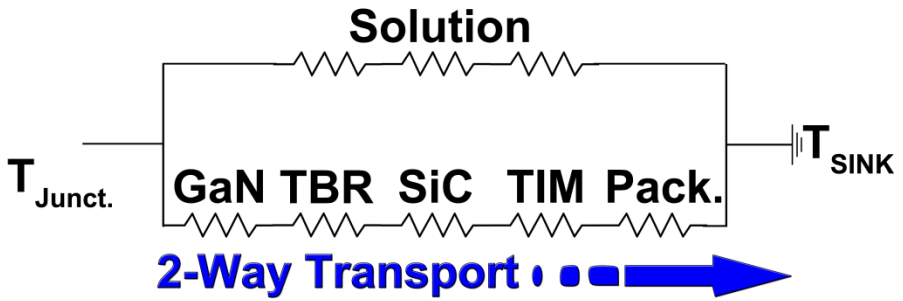
Sandia National Laboratories

Thermal Interconnects for Sinking

- Diamond on top is just a heat spreader.
- ***Key Question:***
  - How do we integrate the top thermal circuit?
- **Options:**
  - Shaping diamond
  - Top side heat sink (DirectFet/I.R. & Dual Cool/Fairchild)
  - Thermal interconnects
- ***Interconnect Advantages:***
  - Standard processing techniques
  - Only 1 heat sink
  - Need only ~30% coverage of the diamond with interconnect



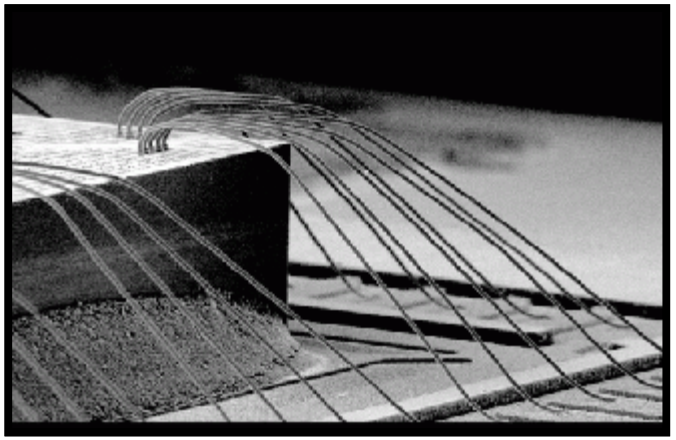


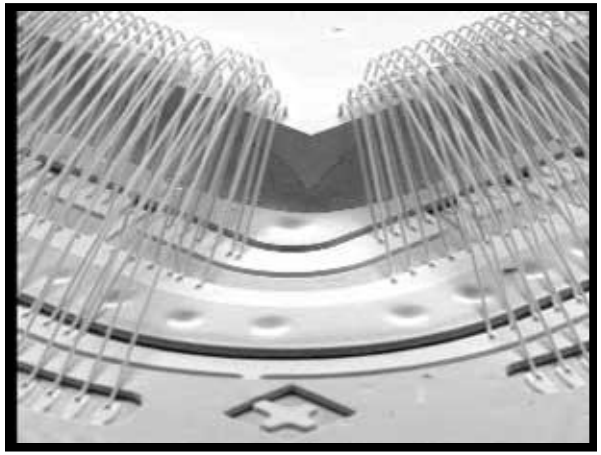


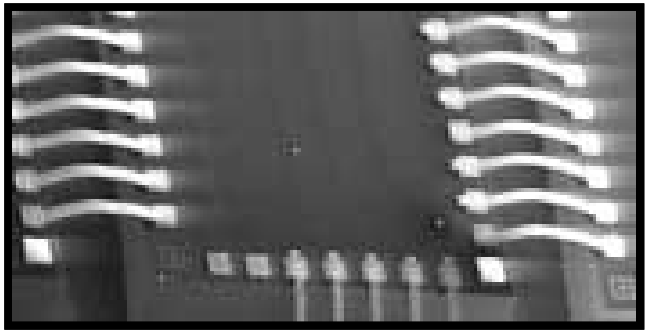
Sandia National Laboratories

Thermal Interconnects for Sinking

- Diamond on top is just a heat spreader.
- ***Key Question:***
  - How do we integrate the top thermal circuit?
- **Options:**
  - Shaping diamond
  - Top side heat sink (DirectFet/I.R. & Dual Cool/Fairchild)
  - Thermal interconnects
- ***Interconnect Advantages:***
  - Standard processing techniques
  - Only 1 heat sink
  - Need only ~30% coverage of the diamond with interconnects







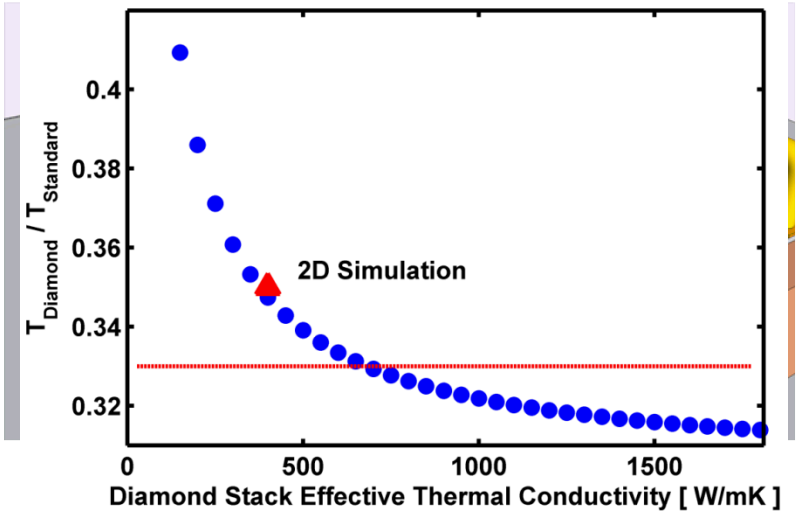
Images courtesy of Palomar Technologies

Thermal Resistance Minimization

- **Application of TODES creates at least 3 new interfaces.**
  - **GaN/Diamond**
  - **Diamond/Interconnect**
  - **Interconnect/Sink**

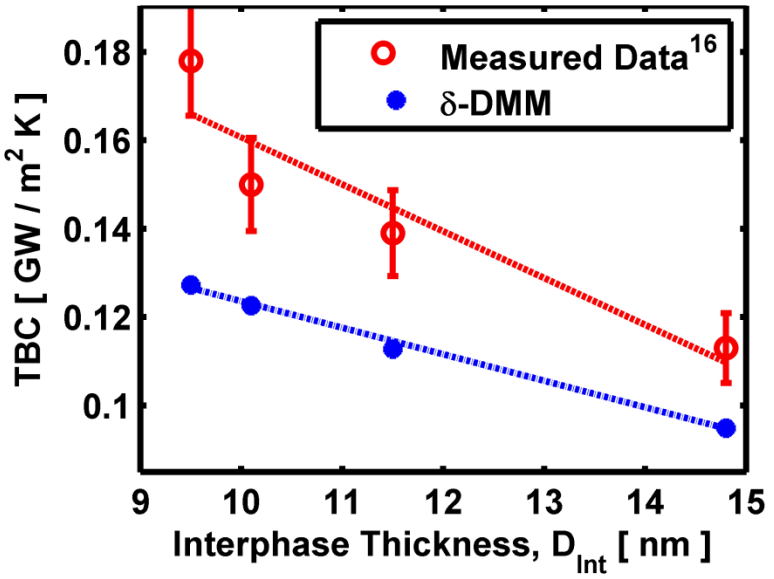
- **Interfacial conductance can span 3 orders of magnitude.**
  - **Minimum: 6 MW/m²K**
  - **Maximum: 600 MW/m²K**

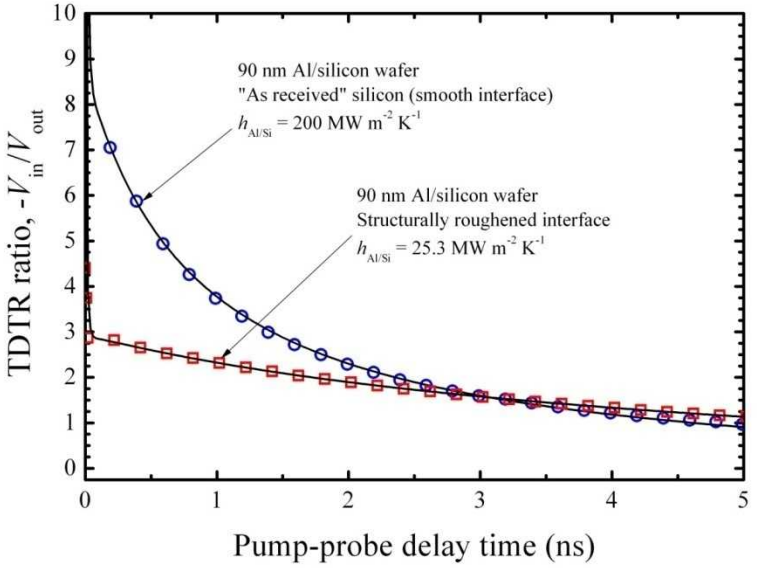
Takeaway: Minimizing these resistances can make or break this approach.



Thermal Resistance Minimization

- **Thermal boundary conductance follows process/property relationship.***
- **Fabrication procedures must me optimized for this conductance.**
- **Thermoreflectance measurements offer a means to measure the TBC.**





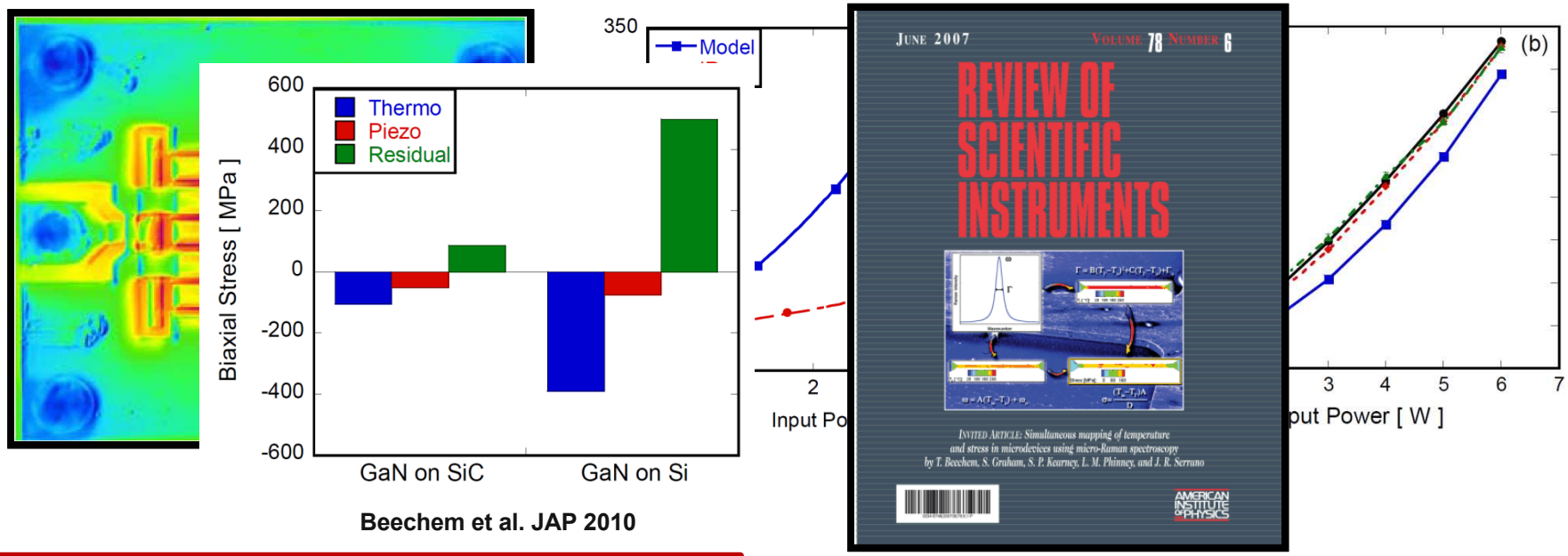
Takeaway: Combine measurements, thermal models, and fabrication into an iterative loop to optimize TBC.

*See Beechem & Hopkins JAP, 2009 or Hopkins, Beechem et al. PRB 2010

Sandia National Laboratories

Quantifying the TODES Ability

- ***Key Question:***
  - Does it work?
- ***Needs:***
  - Electrical
  - Temperature
  - Stress
- ***Thermal:***
  - Electrical
  - IR
  - Raman
- ***Stress:***
  - Raman



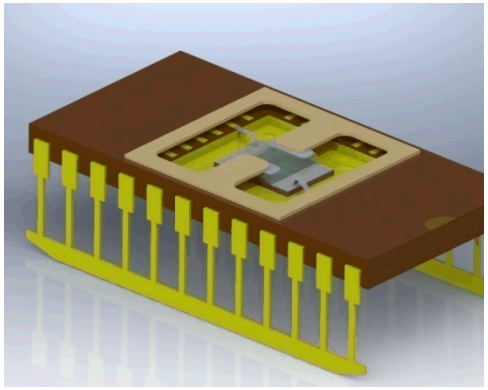
Beechem et al. JAP 2010

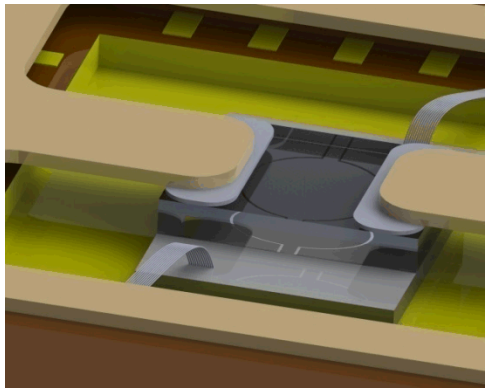
Takeaway: Combining IR and Raman allows for full quantification of temperature and stress.

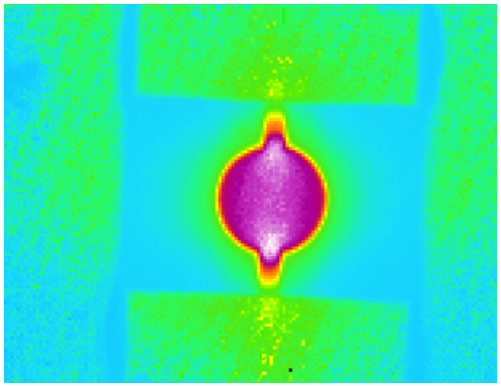
Sandia National Laboratories

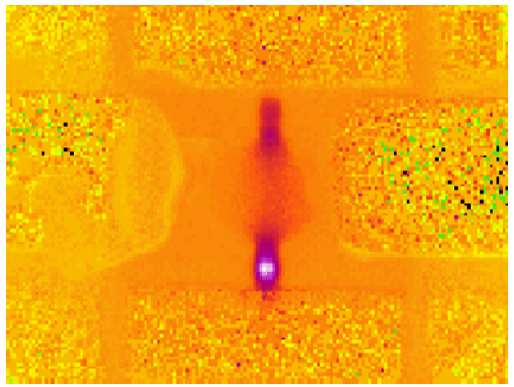
Viability of TODES

- TODES* were placed atop a silicon microheater.
- IR measurements show nearly ***3X*** temperature reduction.
- Crude experiment without any optimization.

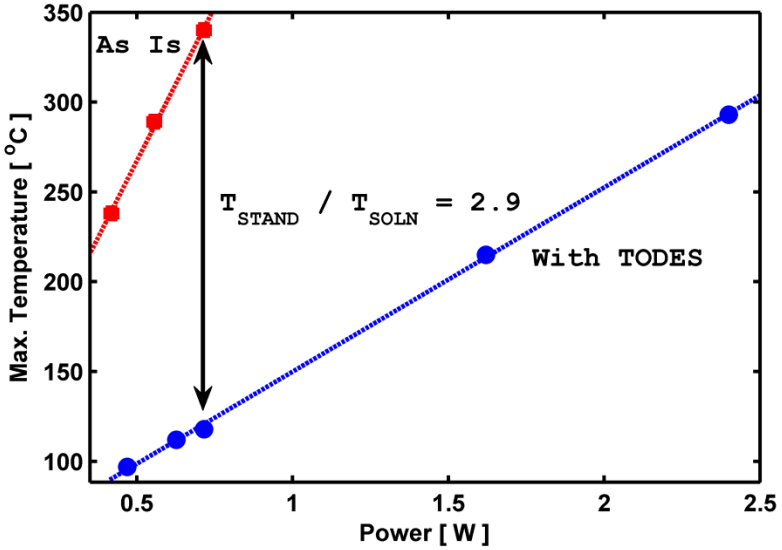








Standard **TODES**



Takeaway: TODES can do it!

*Patent Caution

Sandia National Laboratories

Collaborators

Sandia National Laboratories

- Patrick Hopkins
- Jay Johnson
- Nathan Young
- Seethambal Mani

ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

- John Rogers

ADVANCED DIAMOND TECHNOLOGIES, INC.

- John Carlisle

RFMD

- Rama Vetury

THE UNIVERSITY of WISCONSIN MADISON

- Zhenqian (Jack) Ma

The University of New Mexico

- Ganesh Balakrishnan

This work was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories.

LDRD LABORATORY DIRECTED RESEARCH & DEVELOPMENT

Sandia National Laboratories