SAND2020-10417X

LDRD PROJECT NUMBER: 218971
LDRD PROJECT TITLE:
Noise Erasure in Quantum-Limited Current Amplifiers
PROJECT TEAM MEMBERS: Tom Harris (1882), Tzu-Ming Lu (1879), Sueli Skinner (1882), Don Bethke (1879), and Rupert Lewis (1879)

ABSTRACT:

Superconducting quantum interference devices (SQUIDs) are extraordinarily sensitive to magnetic flux and thus make excellent current amplifiers for cryogenic applications. One such application of high interest to Sandia is the set-up and state read-out of quantum dot based qubits, where a qubit state is read out from a short current pulse (microseconds to milliseconds long) of approximately 100 pA, a signal that is easily corrupted by noise in the environment. A Parametric SQUID Amplifier can be high bandwidth (in the GHz range), low power dissipation (less than 1pW), and can be easily incorporated into multi-qubit systems. In this SAIL LDRD, we will characterize the noise performance of the parametric amplifier front end -- the SQUID -- in an architecture specific to current readout for spin qubits. Noise is a key metric in amplification, and identifying noise sources will allow us to optimize the system to reduce its effects, resulting in higher fidelity readout. This effort represents a critical step in creating the building blocks of a high speed, low power, parametric SQUID current amplifier that will be needed in the near term as quantum systems with many qubits begin to come on line in the next few years.

INTRODUCTION AND EXECUTIVE SUMMARY OF RESULTS:

Quantum computing using silicon quantum dot qubits is a topic that Sandia Labs is actively pursuing. The spin state readout of these qubits is based on a tunneling measurement of a single charge. The current readout signals are very low-level, being 10 – 100pA in magnitude and are short in time duration, e.g., ~10μs. Because this low-level signal is quite weak, it can be easily corrupted by noise from the environment. To maintain the readout signal integrity, a close-proximity amplifier is required next to the qubit device that is located on the mixing chamber of a dilution refrigerator, where the base temperature is ~10mK and the cooling power ~100μW. Contemporary efforts rely on either a heterojunction bipolar transistor (HBT) or a high electron mobility transistor (HEMT) to amplify the readout signal from a single qubit [1, 2]. Although these types of amplifiers work well for single qubits, HBTs and HEMTs are not ideal for a large number qubit system (100-1000 qubits) because of their power requirements, which can reach 10μW of dissipated power. Such a large number of HBT or HEMT amplifiers would result in a required cooling capacity much greater than the dilution refrigerator could handle.

An alternative to HBTs and HEMTs are superconducting parametric amplifiers, which have the potential to be much lower power for an equivalent amplifier gain and with a substantially increased bandwidth [3]. For a typical superconducting parametric amplifier, the input power for the para-amp will be ~1pW per channel. Furthermore, if we can improve the amplifier's

bandwidth, we could extend the operational range of the qubits to higher frequencies—reducing other challenges, and perhaps provide a route to learning new physics.

In this LDRD project, we developed single Josephson junction devices and SQUIDs to examine the noise sources present in these structures. By identifying the noise sources in these devices, we can potentially mitigate them, and if possible, completely remove them. By removing noise sources in the SQUID, which is the front-end of a parametric amplifier, one can improve the overall noise performance of the amplifier system.

DETAILED DESCRIPTION OF RESEARCH AND DEVELOPMENT AND METHODOLOGY:

One of the most challenging portions of this project was the fabrication of the Dolan bridges for Al-based Josephson junctions [4, 5]. The suspended Dolan bridge (see Addendum slides) creates a gap during the double-angle evaporation process that one uses to form Al-based Josephson junctions. Without a viable Dolan bridge, the electrodes on the two sides of the AlOx tunnel barrier are shorted, and the device will not work. Dolan bridges were fabricated with electron beam lithography using a special combination of bilayer resist consisting of PMMA 950A3 as the top layer and MMA EL13 as the bottom (sacrificial/undercut) layer. To form Al/AlOx/Al tunnel junctions, we performed a double angle evaporation of Al at 0° and 30°, while including an intermediate step of oxidation carried out at ~1 Torr for 10 minutes.

To understand how both junction size and tunnel barrier thickness affect Josephson junction performance, a series of single junction testers were fabricated (see Addendum), where the areas of the junctions varied. These single junction testers were given a prescribed, static oxidation condition during the device fabrication process. Each tunnel barrier oxidation was conducted for 10 minutes, with the oxidation pressure varying over a series of 0.2, 0.5, 1, and 2 Torr, where is pressure represents a separate fabrication process and a separate batch of devices. Higher values of pressure result in a thicker tunnel barrier. These testers ultimately provide information as to how the critical current of the junction is limited the junction cross sectional area and the tunnel barrier thickness.

For noise measurements in SQUIDs, we developed a device layout consisting of 2 SQUIDs, with each SQUID having its own flux bias line. This device consisted of 12 electrical leads, which we could readily accommodate in a helium-3 refrigerator. (This is also shown in the Addendum.). The 2 SQUIDs on the chip consisted of a SQUID with the smallest junctions and a SQUID with the largest junctions fabricated, i.e., the min and max areas of the single junction tester series.

RESULTS AND DISCUSSION:

The greatest labor investment in this project was in the development of sub-100nm Josephson junctions. For applications in numerous areas of quantum information science, Josephson junctions in the range of $(50nm)^2$ to $(200nm)^2$ are highly desirable. Thus considerable effort was made to produce junctions in those ranges of areas. The size of these junctions required the use of electron beam lithography. The specifics of this resist layer stack were given in the previous section. A series of electron beam fluence dose tests revealed that the optimum dose was $400\mu C/cm^2$. Doses above that range resulted in features excessive in size, where as doses below that range resulted in the bottom layer of MMA not fully clearing-out. Our biggest challenge with this fabrication process was overcoming the failure of Dolan bridges. When using the optimized dose, the Dolan bridge would nearly always fracture (see Addendum), presumably due to stress across the bridge. Thicker PMMA resists were implemented, but none of these thicker resists could withstand the applied stress either. We developed a method of incorporating strain relief along the sides of the Josephson junctions (see Addendum). This strain-relief method worked quite well, with essentially all of the junctions fabricated in this way being viable. Once metallized the strain relief channels leave small metal islands on both sides of the junctions. For high-frequency applications, these metallic islands could become a parasitic capacitance. To eliminate the stress relief channel's contribution as a parasitic capacitance, the channels were integrated into the junction electrodes. Two versions of this integrated stress-relief design are shown in the Addendum. This integrated design places the strain-relief channels at the same electrical potential as the junction electrodes, such that no parasitic capacitance exists.

The single junction testers are shown in the Addendum. These devices consisted of 5 single junctions with the following areas: 100nmx100nm, 100nmx200nm, 100nmx300nm, 100nmx400nm, and 100nmx500nm. We processed these devices using a single, prescribed static oxidation value. These testers allowed us to evaluate the critical current density as a function of junction size.

Using the aforementioned strain-relief technique, we developed devices with SQUIDs. Each SQUID device is accompanied by a flux bias line, for flux tuning the SQUID and for modulating the SQUIDs critical current. For our helium-3 refrigerator we have a maximum of 15 leads available. Thus, for a 4-wire electrical measurement on a SQUID, plus 2 leads for flux biasing, we were able to accommodate two SQUID devices, which total 12 electrical leads.

ANTICIPATED OUTCOMES AND IMPACTS:

The device fabrication for Josephson junctions that was developed in this project provides Sandia and the CINT user community with a new method for fabricating sub-100nm junctions. Due to the COVID-19 pandemic, our efforts for noise measurements were stalled. The next immediate steps for this research are to test the SQUID devices that we fabricated and to develop a low-frequency noise measurement, to evaluate the noise in the single junctions and to evaluate the flux noise in a SQUID. Additional next steps, in terms of measurement improvements for this superconducting work, would be to design a μ-metal sample package to protect the SQUID from any spurious magnetic fields. This anticipated type of enclosure could have an approximate 1"-square footprint and be an 8-port device (2 current and 2 voltage lines for the

SQUID, 2 current leads for the flux bias line, and 2 current leads for the device under test). As an alternative lower-cost approach, we could also (potentially) line the insides of the refrigerators (in the vacuum space) with μ-metal film, which would provide a modest level of shielding and would not prohibit any type of electrical connections with the samples.

As a successful demonstration of fabricating SQUIDs, this work has been included into the new Quantum Systems Accelerator (QSA) program (UC Berkeley/Sandia). Because of the seedling funding granted towards this effort, we were able to show promise in this area of research, and this team will work with the QSA effort to develop superconducting qubits.

An anticipated outcome from this work is the publication of a high-impact journal article. After implementing the device and the measurement refinements listed at the beginning of this section, we foresee the demonstration of this device and its capabilities being published in a high-quality, peer-reviewed journal. A demonstration of this device's sensing and amplification capabilities when coupled to a simple resistor will be the first manuscript.

CONCLUSION:

In this LDRD project, we developed the Josephson junctions and SQUIDs for the evaluation of noise performance in a SQUID-based cryogenic amplifier, as a first step towards a wide-bandwidth (DC-GHz), parametric amplifier that will ultimately enable enhanced performance in multi-qubit systems due to ultra-low power consumption and vastly improved speed, while maintaining the same noise performance as an HBT or HEMT. Never before have these metrics been demonstrated in a parametric amplifier for spin qubit current readout. A key accomplishment of this project was the successful development of sub-100nm, self-aligning Josephson junctions with integrated strain-relief. A critical component of that success was formulating a working microfabrication process flow. For the process flow to be successful, we overcame several technical issues. Various resist compositions were tried along with multiple dosing tests and CAD design biasing to dial-in the optimal junction geometry. For our process the optimum dosing was 400μC/cm^2 using a resist bilayer of PMMA 950A3 spun at 4000rpm and a base layer of MMA EL13 spun at 3000rpm. The thicknesses of the resists were 140nm and 760nm, respectively, for the foregoing spin speeds. Several leading research groups have struggled with the successful fabrication of self-aligning junctions. Prior to this work, resist layers were used that required multiple types of developers, including cold development processes. To our knowledge, this is the first successful implementation of self-aligning junctions using a combination of PMMA/MMA and a single developer compound. The integrated junction strain-relief method that we've developed will be useful for superconducting qubit work as it removes any parasitic capacitance that could be caused by the strain-relief.

Using our new junction fabrication technique, we were able to successfully fabricate arrays single junction devices. These devices were oxidized at a pressure 0.5Torr for 10minutes and then tested at room temperature. These devices showed junction resistances in the range of 4kΩ to 10kΩ (inversely scaling with junction cross-sectional area), which is approximately our target value for fabricating SQUIDs with critical currents desirable for both amplifiers and qubits.

Our final efforts were to then use our junction design to develop a platform for studying the noise in SQUIDs. We constructed a chip layout that harbored 2 SQUIDs, with each SQUID having its own flux bias line. The choice to produce a chip with only 2 SQUIDs was a limitation of our helium-3 cryogenic system, which has a maximum number of 15 leads. The 2 SQUIDs fabricated on the device were composed of the min and max areas of junctions that were fabricated, i.e., 100nmx100nm and 100nmx500nm. Again, we tested these devices at room temperature and they showed an equivalent resistance comprised of two parallel junctions as anticipated from the single junction tests.

REFERENCES:

1. L. Tracy, D. Luhman, S. Carr, N. Bishop, G. Ten Eyck, T. Pluym, J. Wendt, M. Lilly, and M. Carroll. Single shot sping readout using a cryogenic high-electron-mobility transistor amplifier at sub-Kelvin temperatures, *Appl. Phys. Lett*, **108**, 063101 (2016).

2. M. Curry, T. England, N. Bishop, G. Ten-Eyck, J. Wendt, T. Pluym, M. Lilly, S. Carr, and M. Carroll, Cryogenic preamplification of a single-electron-transistor using a silicon-germanium heterojunction-bipolar-transistor, *Appl. Phys. Lett*, **106**, 203505 (2015).

3. M. Castellanos-Beltran and K. Lehnert, Widely tunable amplifier based on a superconducting quantum interference device array resonator, *Appl. Phys. Lett*, **91**, 083509 (2007).

4. A. Dayem, and J. Wiegand, Behavior of Thin-Film Superconducting Bridges in a Microwave Field. *Phys. Rev.* **155**, 419–428 (1967).

5. G. Dolan, *Appl. Phys. Lett.* **31**, 337 (1977).

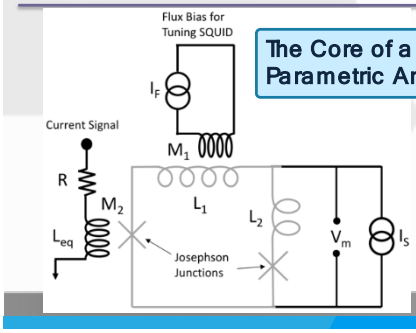
ADDENDUM:

Noise Erasure in Quantum-Limited Current Amplifiers

PI: Tom Harris (1882), Sueli Skinner (1882), Tzu-Ming Lu (1879), Don Bethke (1879), Rupert Lewis (1879)

Purpose, Approach, and Goal

- **Motivation:** Of high interest to Sandia is the read-out of quantum-dot-based qubits (quantum bits), which is vital for quantum computation and relevant to preserving national security.
- **Technical Approach:** Characterize the noise in the "front-end" of a parametric superconducting quantum interference device (SQUID) current amplifier, which includes the device under test and the flux tuning circuit.
- **Goal:** Identify noise sources and eliminate them if possible and if not possible, mitigate their effects.



The Core of a SQUID Parametric Amplifier

Key R&D Results and Significance

- **R&D Summary**
  We designed, fabricated, and tested single Josephson junctions (JJ) and SQUIDs using a new fabrication process flow involving electron beam lithography at Sandia.
- **Our Key Accomplishment:**
  Development of a new type of self-aligning, sub-100nm Josephson junction that can be used for precision superconducting qubit devices.
- **Lessons Learned**
  The device fabrication took much longer than expected, as unforeseen stress issues in the electron beam resist presented a significant challenge in the fabrication process. However, we developed new stress mitigation techniques along the way that will be useful for the scientific community.
- **Follow-on plans/activities**
  The Josephson junctions and SQUIDs developed in this project will be used in the new Quantum Systems Accelerator Program (UC Berkeley/Sandia). I will also be using the results from this project to pursue a full NSP LDRD (FY22) and towards an AFRL BAA (FY22).
- **Staff Development: New Postdoc, Sueli Skinner**
  She learned cryogenics, microfabrication, measurements.
- **IP** We're submitting a TA on the new JJ fab process.

R&D Summary

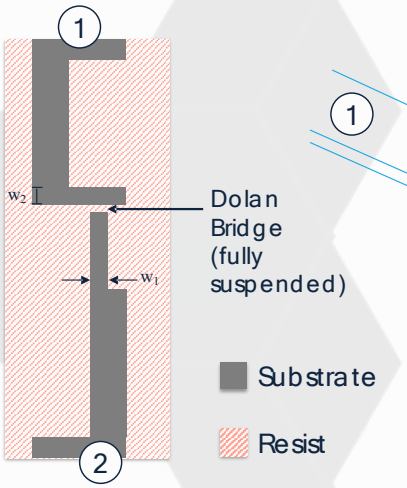
What are the key aspects of this research you would want your colleagues to take away? What are you most proud of? Did anything not work as expected?

The junction fabrication did not work as expected, initially. (shown on the next slides) However, this fabrication challenge forced us to develop a new type of self-aligning Josephson junction. This was quite a satisfying achievement and ***this result will have an impact in both the superconducting circuit and quantum computing communities.***

- What was the current practice/state-of-the-art before you started? What contributions did you make? What risks were you able to buy down for future programs?
  - Our work is the first demonstration of an Al/AlOx/Al self-aligning junction with integrated strain relief, permitting the fabrication of sub-100nm aligned Josephson junctions.
  - For future Quantum Information Science programs that rely on Josephson-based electronic devices, we've bought-down the fab risk associated with making these.
- Provide some details about your R&D. Did you help move across TRL or tech maturation boundaries?
  - The research conducted in this program provides an advancement in state-of-the-art Josephson junction fabrication.
- Important lessons learned, good or bad - What have you learned from any "failure"?
  - Overcoming fabrication obstacles took longer than expected. There were no real failures in the project, only severe delays due to COVID-19.

R&D Summary

Creation of a new type of Dolan bridge that facilitates self-alignment for sub-100nm Josephson junctions.



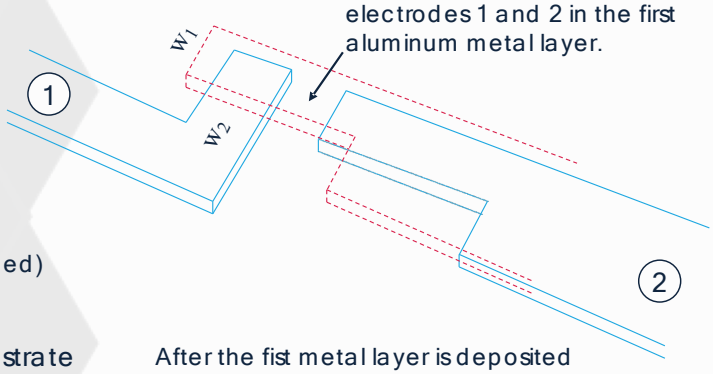
Dolan Bridge (fully suspended)

Substrate

Resist

Top view of junction resist (stencil) mask

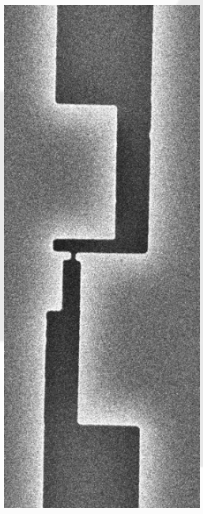
The suspended Dolan bridge creates a gap between electrodes 1 and 2 in the first aluminum metal layer.



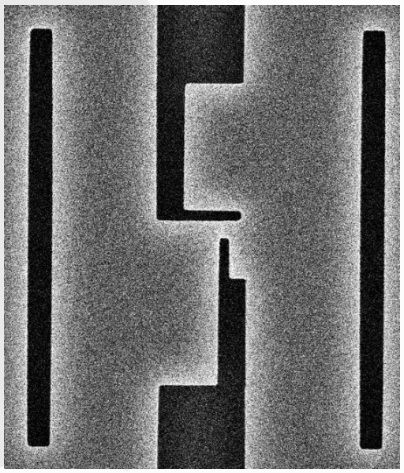
After the fist metal layer is deposited (blue lines) it is partially oxidized, then the sample stage is tilted, and a second metal layer is deposited (red lines), forming a self-aligning Al/AlOx/Al Josephson junction with area $w_1 \times w_2$.

R&D Summary

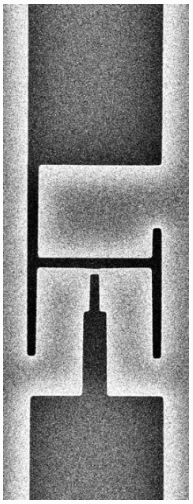
We developed a fabrication technique that uses strain relief to mitigate stress and permits sub-100nm Josephson junction fabrication. We also created a design that incorporates the stress relief into the working junction electrodes.

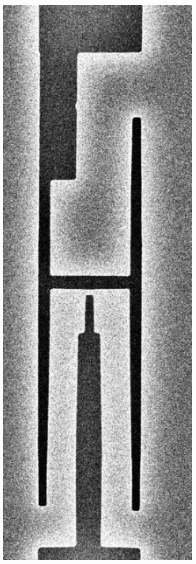


Broken bridge



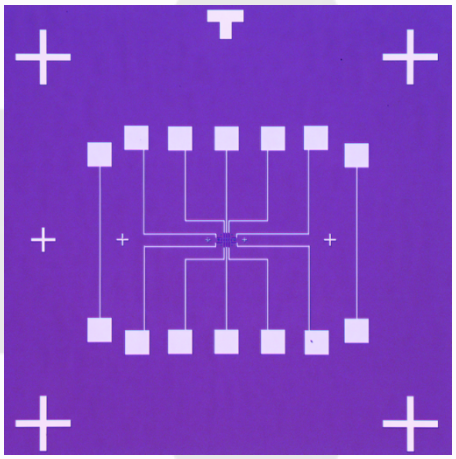
Functional bridge with strain-relief channel



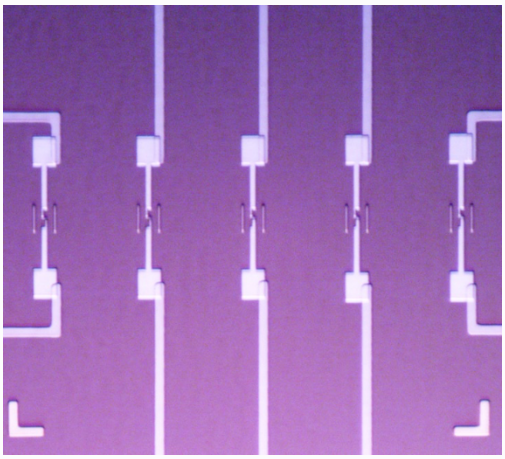


Bridges with integrated strain-relief channel

Single Junction Testers

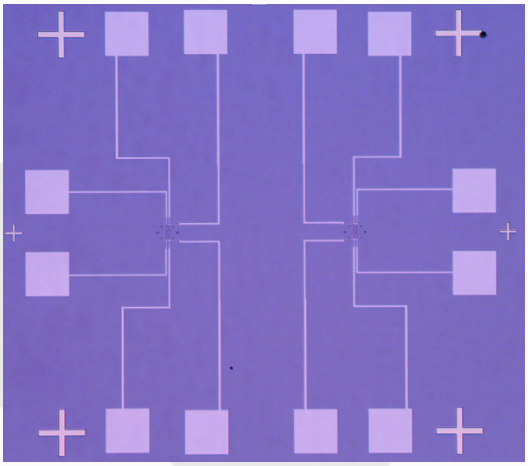


Single Junction Tester Chip

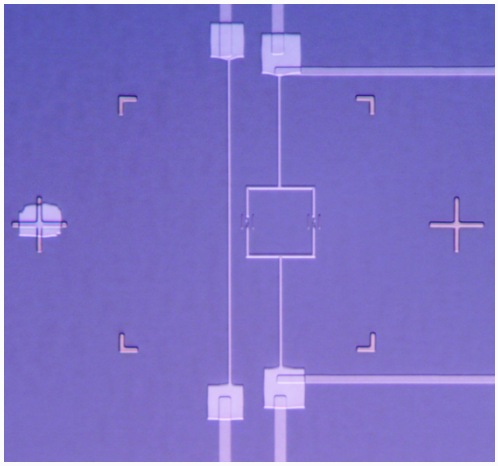


Center region of the single junction testers

2-SQUID Devices



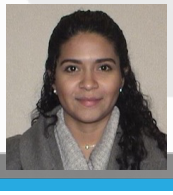
2-SQUID Chip



Left device of the 2-SQUID chip

Project Metrics

- Presentations and Publications
  - We anticipate publishing a high-impact journal article on our new self-aligning Josephson Junction fab technique. (~6 mo.)
  - We will be presenting this information at the APS March Meeting 2021. (in 6 mo.)
- IP
  - We are pursuing a patent on our new Junction fab technique and have drafted a Technical Advance that we are currently preparing.
- Tools and Capabilities
  - These SQUIDs will become a new CINT user capability, available to both Sandians and to external users.
- Staff development, Sueli Skinner (Early Career)



This project supported a recently-hired postdoc and provided her with new skills related to cryogenics, device fabrication, low-level electronic measurements, and quantum device physics.

Project Legacy

Key technical accomplishment

- We developed a new type of self-aligning, sub-100nm Josephson junction that can be used for superconducting qubit devices requiring precise geometry.

How does this engage Sandia missions?

- The results from this project are already being leveraged by a new ASCR program at Sandia on quantum transduction (M. Eichenfield, Org 5219).
- Our results on superconducting device development from this project have strengthened our foundation in quantum information science (QIS) at Sandia, which is vital for quantum computation and relevant to preserving national security.
- Which customers have you talked to about your results?
  - I have spoken with potential customers in both center 2000 and 5000 about funding opportunities to continue this work. I plan to submit a full NSP LDRD on this topic for FY22. I will also be submitting a full proposal on quantum-limited amplifiers to an AFRL BAA on hybrid quantum systems (FY22).

Plans for follow-on and partnerships?

- *NSP LDRD, AFRL BAA, Continuing a portion of this work in the new UC Berkeley/Sandia Quantum Systems Accelerator NQI hub.*

What do you wished you could have done but didn't?

I wish we could have spent more time on developing noise measurements, but COVID-19 stalled our efforts.