SAND2011-3359P

UNM | Electrical & Computer Engineering

CHTM | Center for High Technology Materials

Design and Integration of Discrete Components for Low Energy WDM Silicon Photonics on CMOS Systems

May 12, 2011

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rle AT MIT RESEARCH LABORATORY OF ELECTRONICS AT MIT

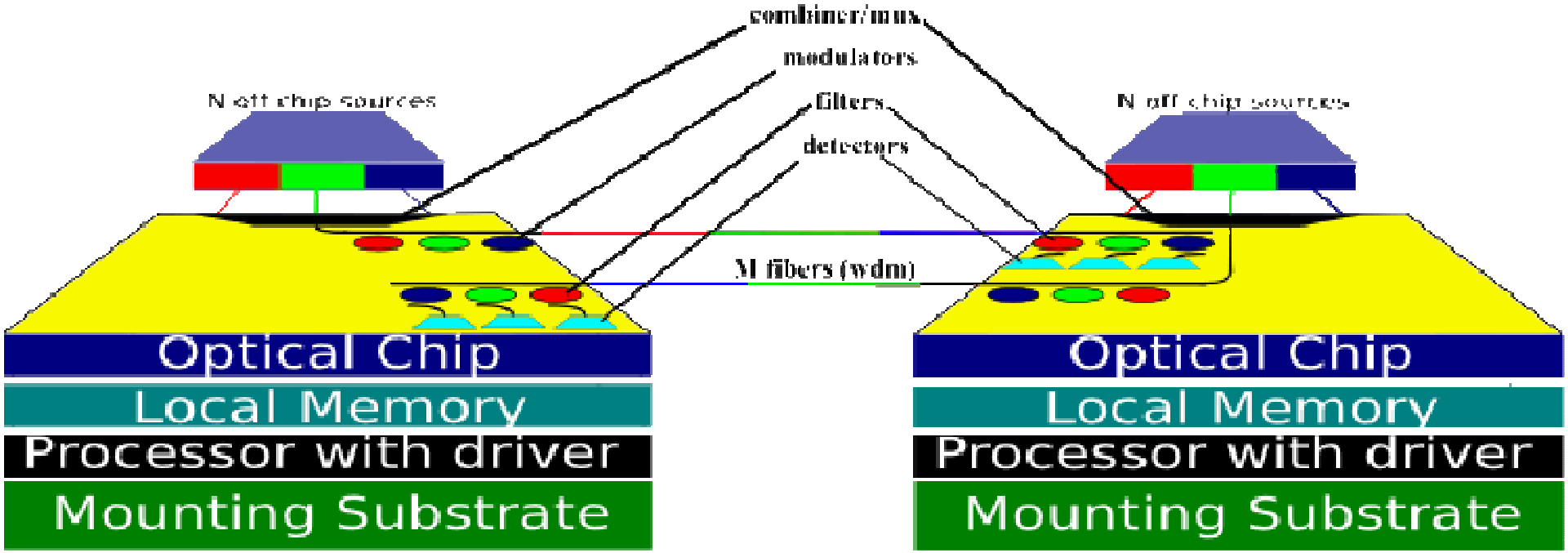
MIT

Sandia National Laboratories

DARPA

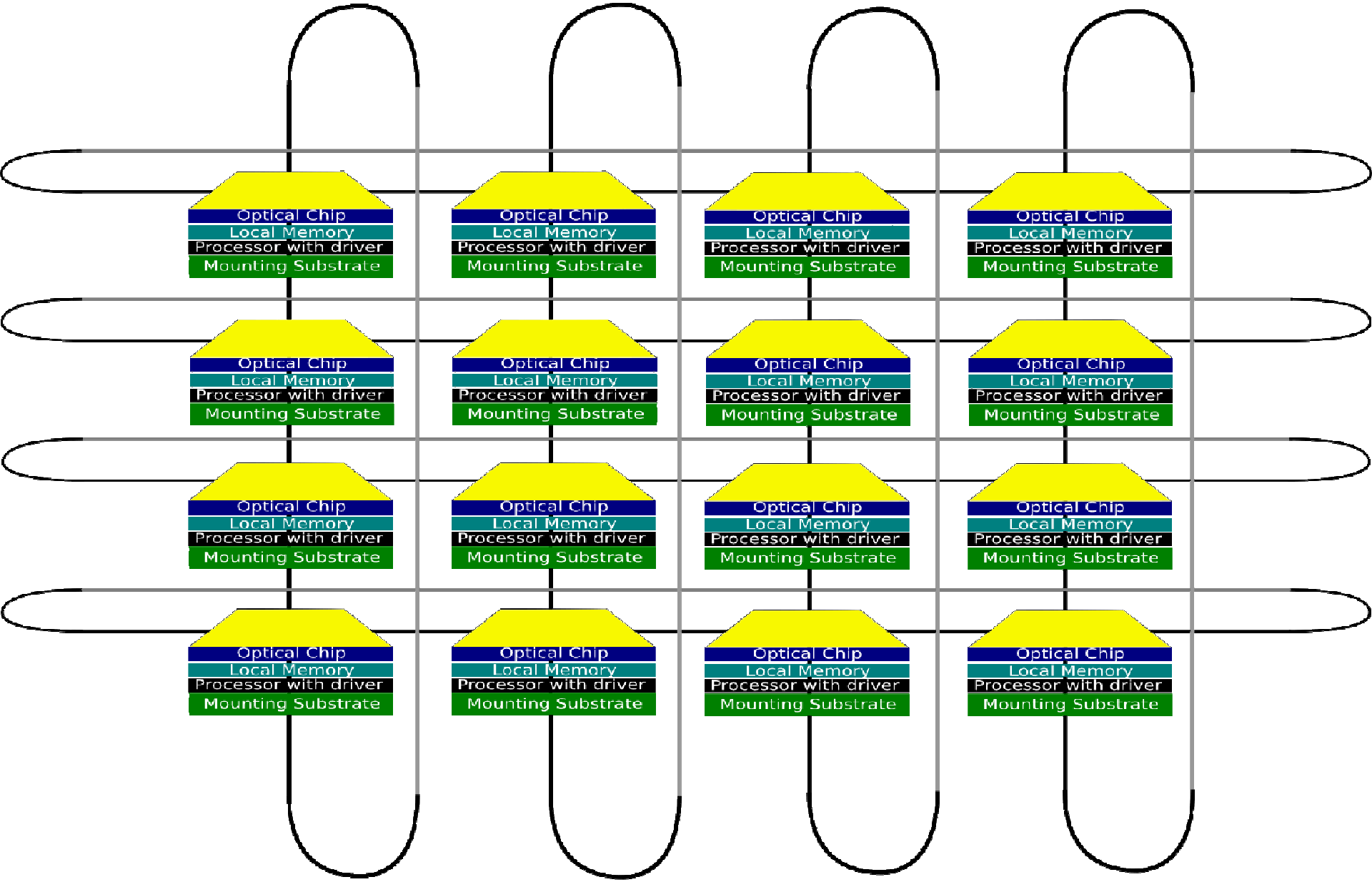
NNSA National Nuclear Security Administration

LORD

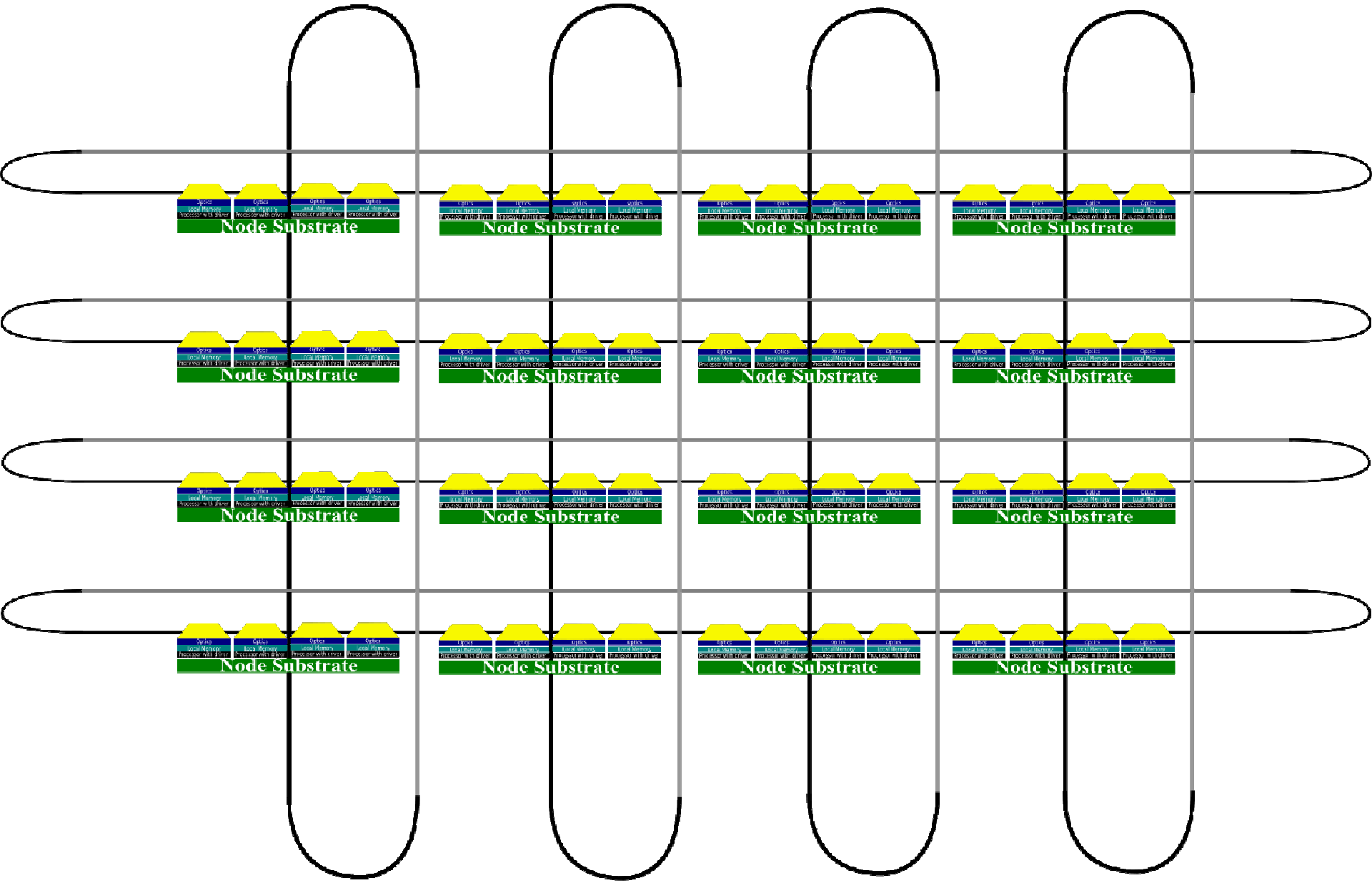


N X M Channels Between Two Chips

The framework for today is a multichip system connected by a WDM optical system.



The chips can be thought of as existing in an optically connected mesh network.



... which may in fact be a network of nodes each of which contain a number of chips

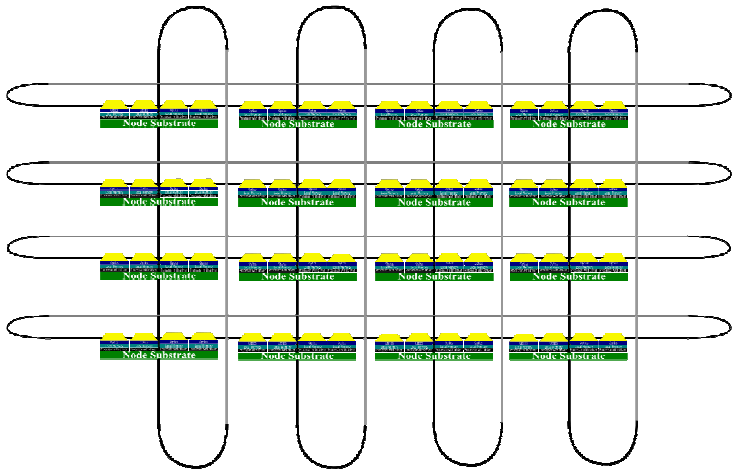
Supercomputer inter-chip BW

IBM / U of Illinois
Blue Waters,
http://www.ncsa.illinois.edu/BlueWaters

Data Center Energy Consumption

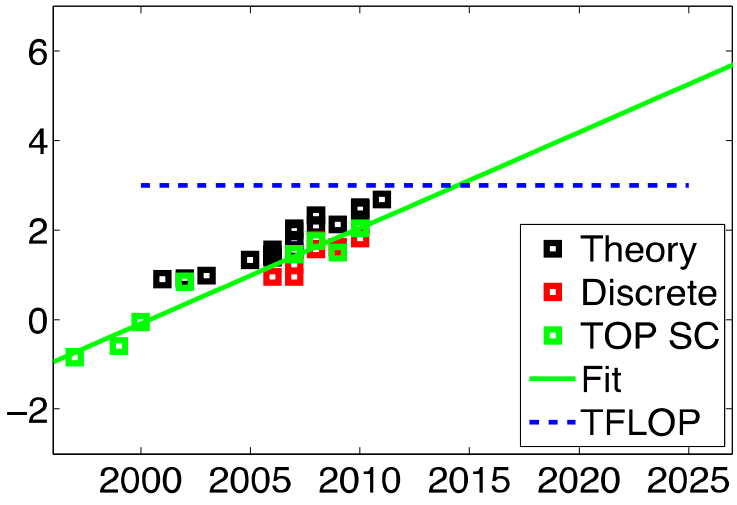
Google Dalles, Or
http://www.nytimes.com

http://scienceblogs.com



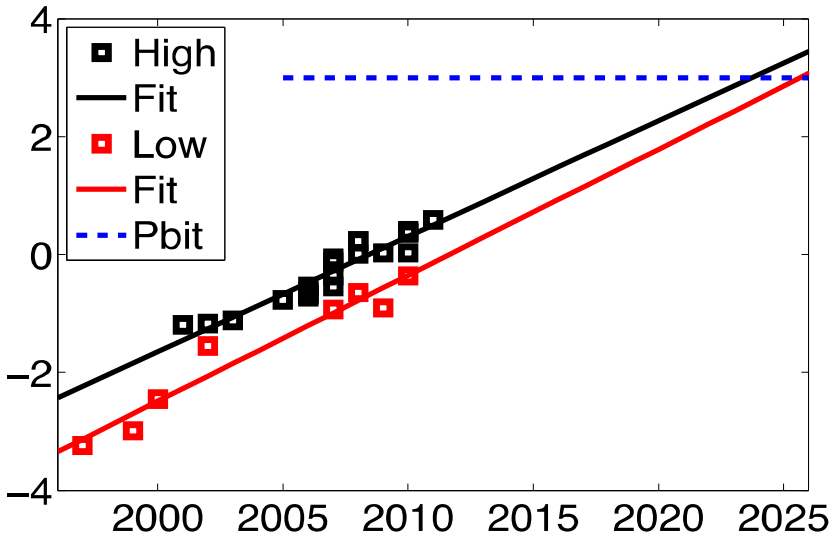
A network like the one considered may serve as a large computer or data center

These networks improve as server chips get faster

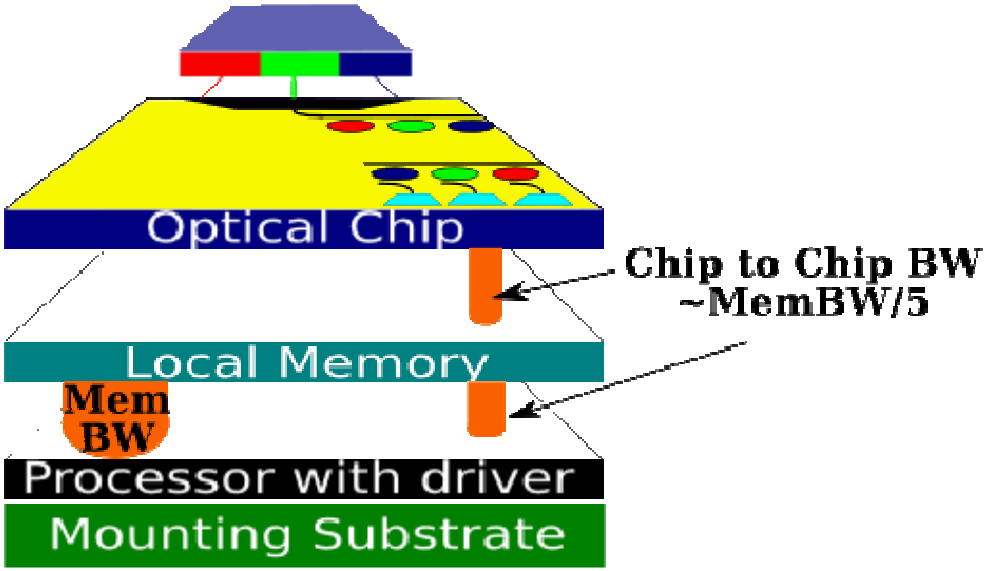


We talk about communications because of the memory and off chip data needs

Memory: 0.5-1Byte/FLOP
Off-Chip: 0.2Bytes/FLOP

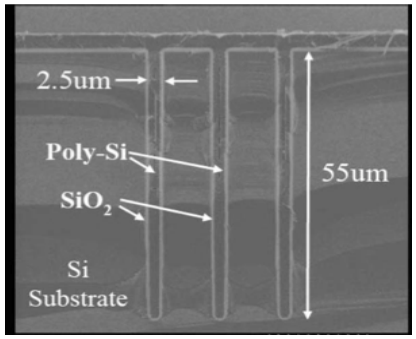


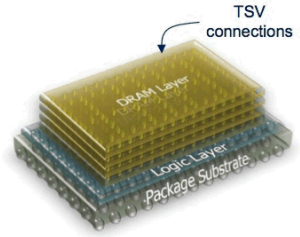
through silicon vias are a promising DRAM access technology with industry support



$$\frac{1pbps - Mem_{BW}}{Chip \cdot to \cdot Chip_{BW}}$$

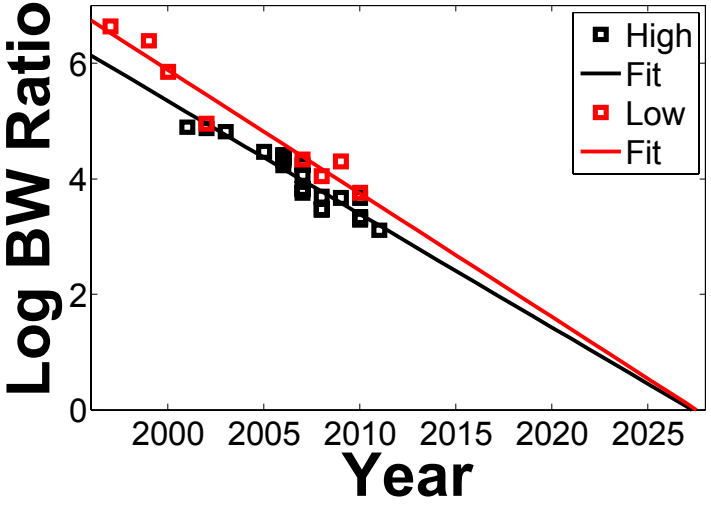
TSV BW Limit





Functioning prototypes in silicon TODAY

Micron inc.



Key finding: optics is not necessary on chip for chip-to-chip interconnect or memory
Implication: crystalline lattice silicon photonics can enable exascale interconnect

analysis on TSV's assumed only 1-3% of the chip for I/O and 1Gbps BW per TSV yet 3Gbps TSV interconnect has been shown as have pitches below 10μm

➔TSV BW could increase by 5-10

➔Mem BW estimates may decline for multicore, large cache chips

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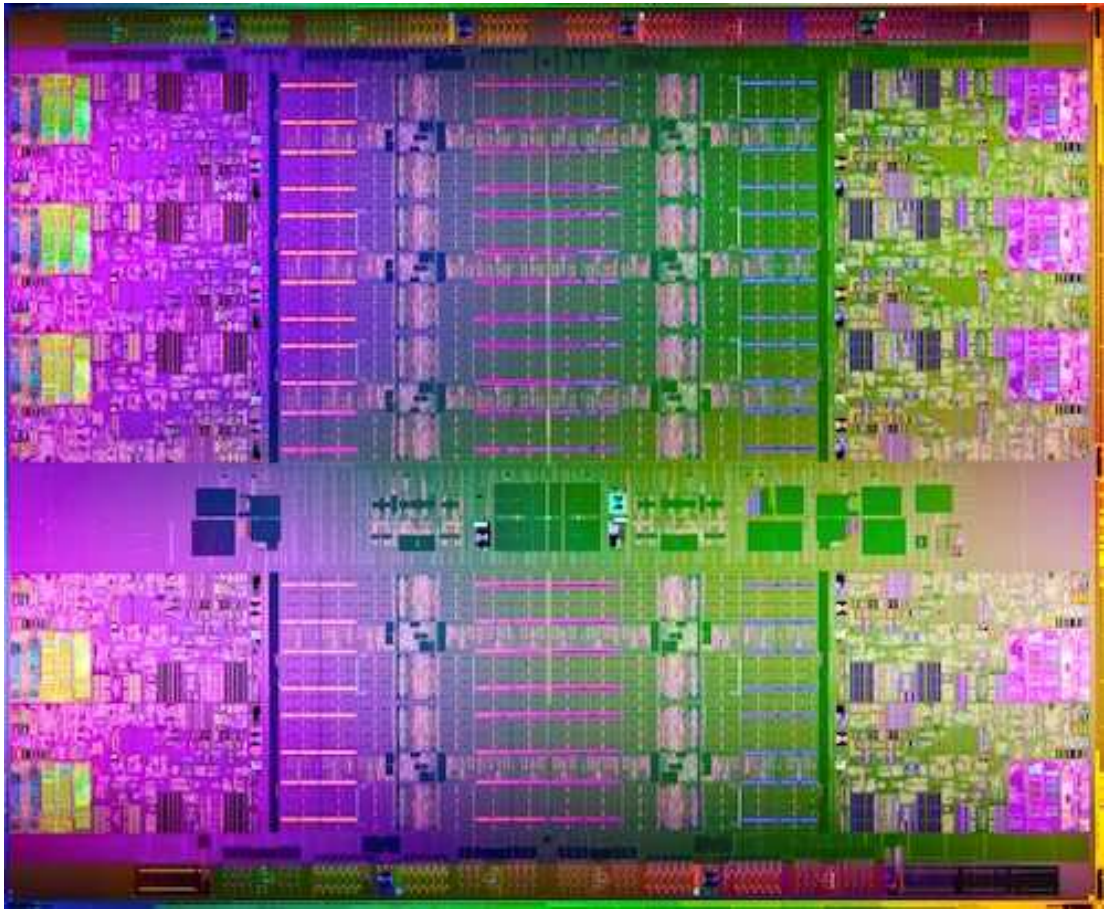


10 core Xeon from Intel

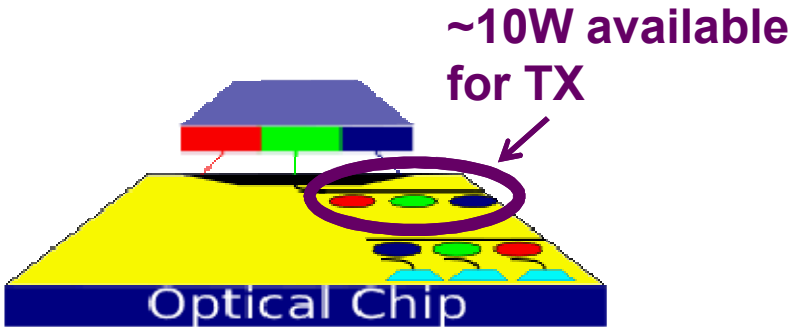
☐Optics for core and cache interconnect to reduce latency is another area of study

☐Application of optics to DRAM access seems less likely

2nd key requirement – power, scaled to bandwidth using energy/bit

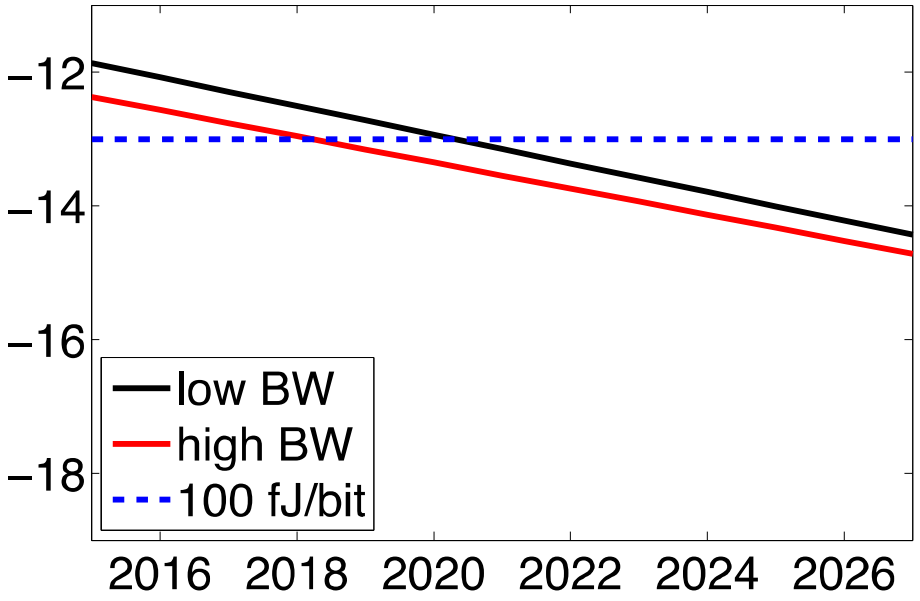
Basis:

- **100W available per chip**
- **allocate 10% to the transmitter** *(Miller, 2007)*



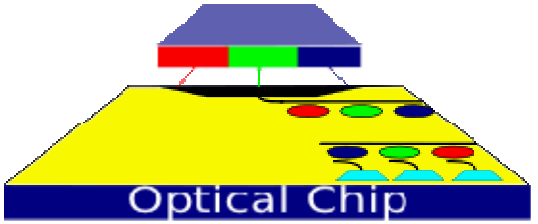
$$E_{bit,low} = \frac{10W}{FLOPS \times \frac{0.5B}{FLOP}}$$

$$E_{bit,high} = \frac{10W}{FLOPS \times \frac{1B}{FLOPS}}$$

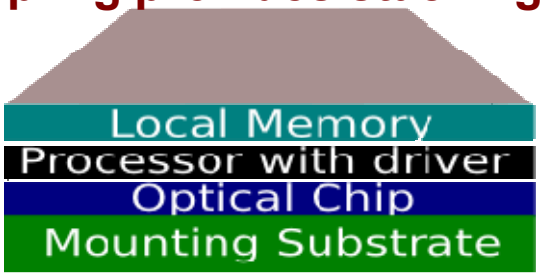


Reference Ebit levels – 100fJ/bit (2018)
10fJ/bit (2022)

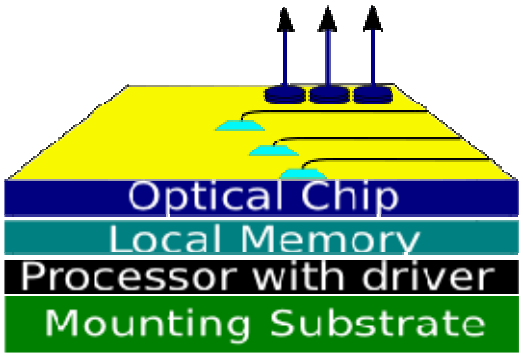
silicon photonics



side coupling provides stacking options



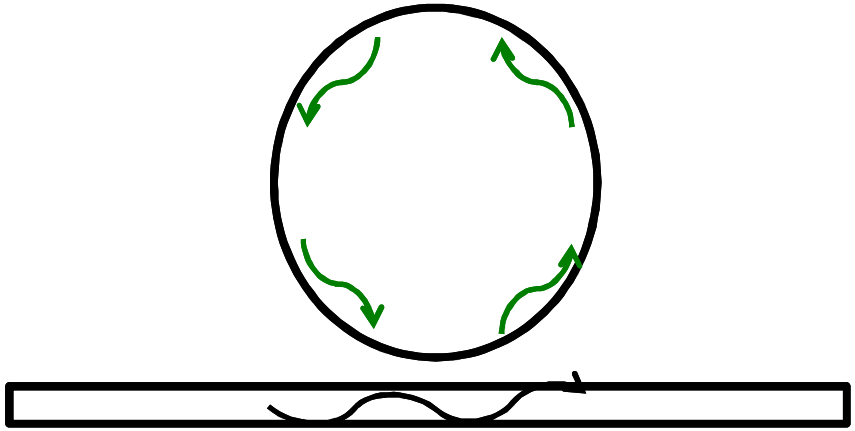
VCSELs



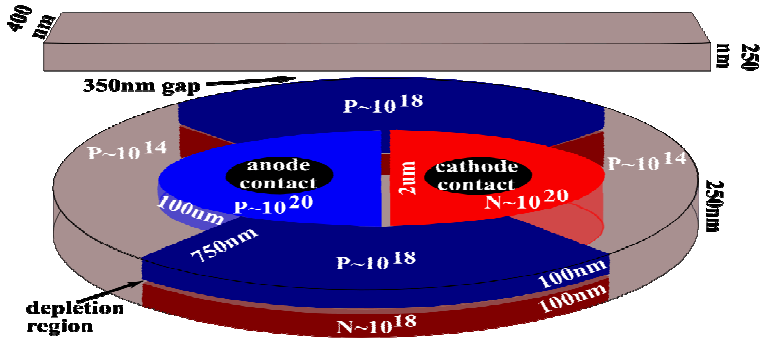
research device attributes for a 2018, 10 TFLOP chip	Dis	Si Photonics	VCSEL
Manufacturing volume to match server chips 1:1	✔	✔	✔
Energy/bit (on chip) (2018 ~100fJ/bit)	✔	**~100fJ/bit**	**~140fJ/bit**
Energy/bit (total)		~150fJ/bit	~140fJ/bit
Low Voltage Compatibility	✔	**(300mV) ✔**	**?**
Fibers per chip (assume 10Gbps SiP, 100 channels, 5THz)	✔	**2 (WDM)**	**457 (35Gbps)**
Fibers per exascale system	✔	**200 thous.**	**45.7 million**
Integration with TSV		✔	✔★
Monolithic with CMOS (electrical multiplexing)	✔	✔	**?**
Data center virtualization (long haul)	✔	✔	✔

The frequency selective modulator of the WDM transmitter solution

resonant silicon microdisk – optical properties

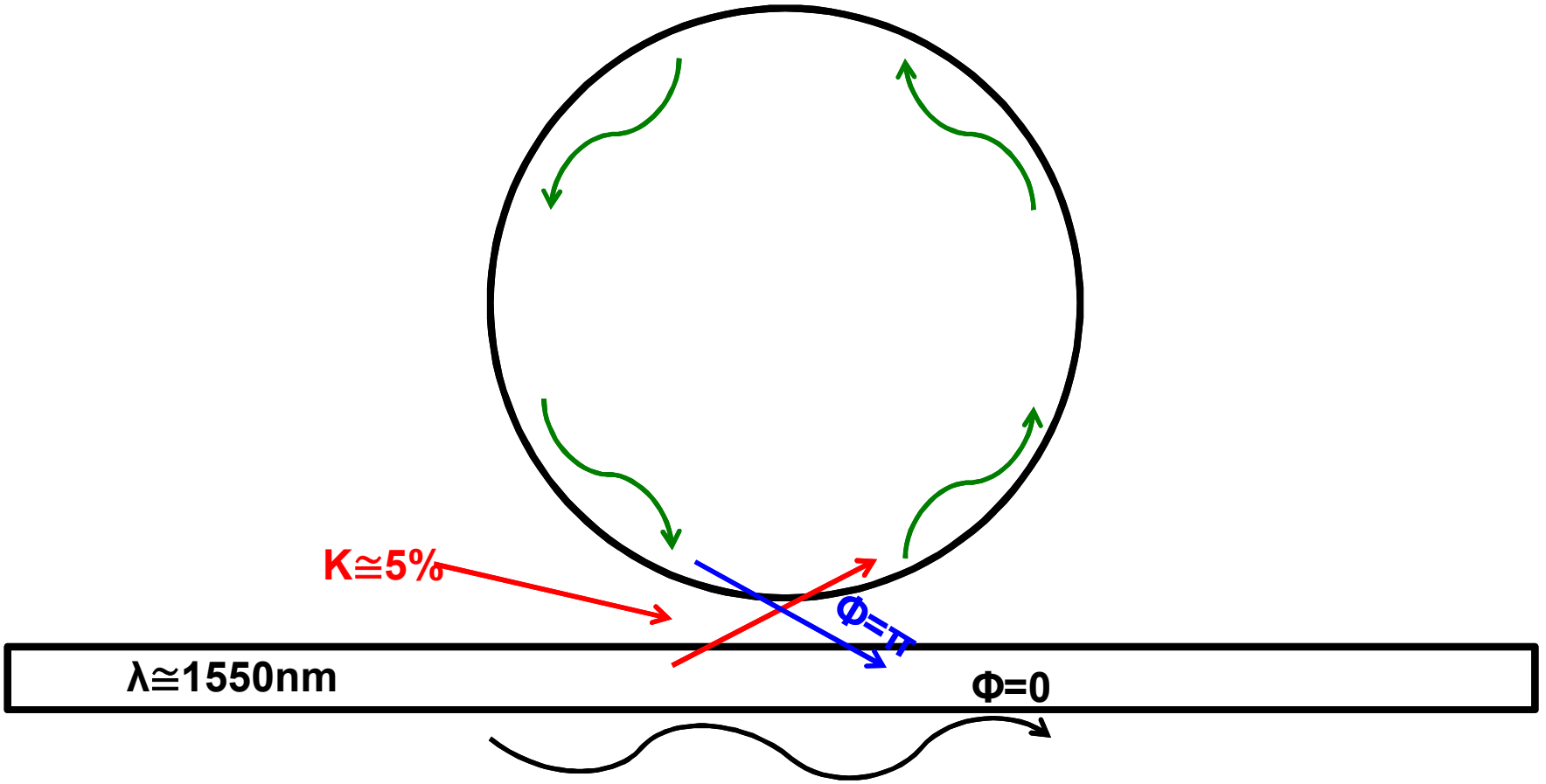


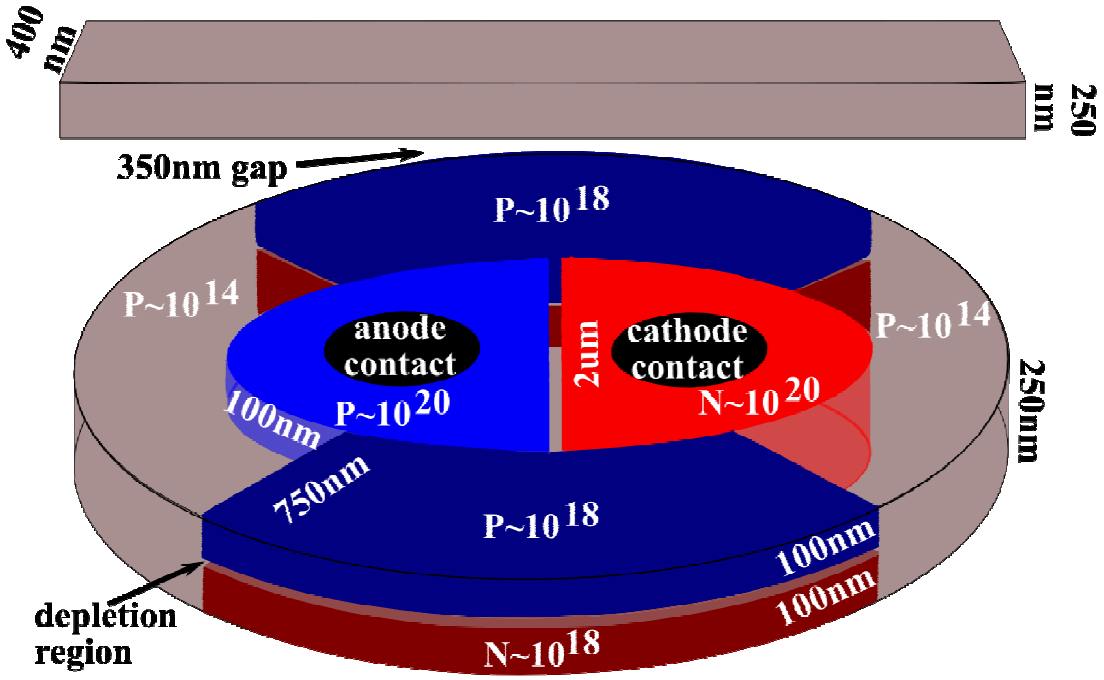
resonant silicon microdisk – electrical properties

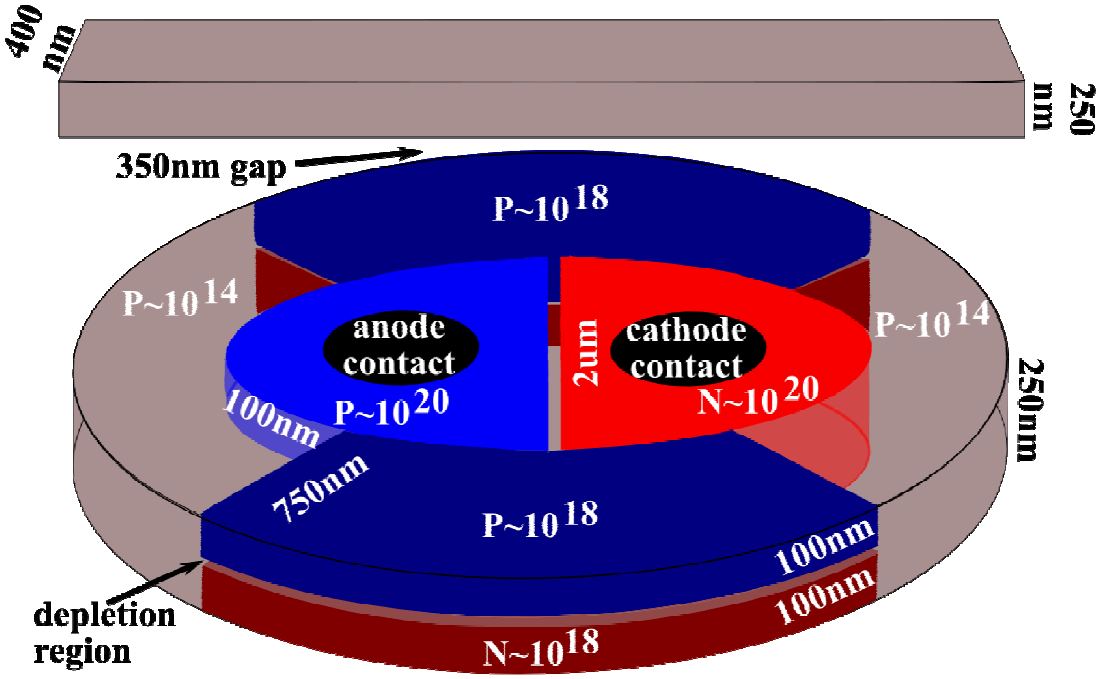


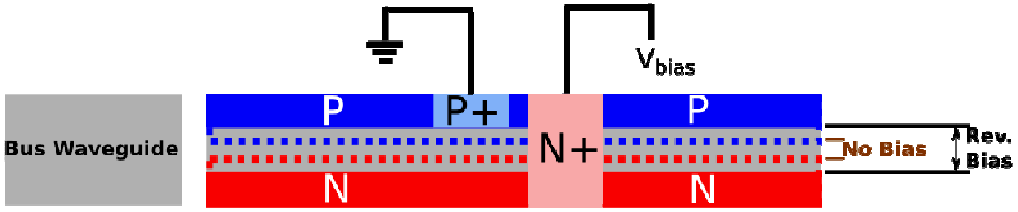
The frequency selective modulator portion of the WDM transmitter solution

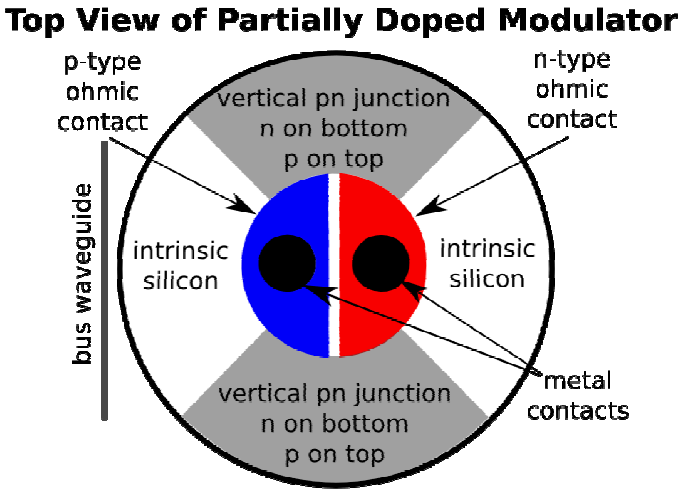
resonant silicon microdisk – optical properties




400 nm
250 nm
350nm gap
P~10 18
P~10 14
P~10 14
anode contact
cathode contact
2um
P~10 20
N~10 20
100nm
750nm
P~10 18
100nm
100nm
N~10 18
250nm
depletion region







3.5 micron diameter

Silicon on Insulator 250nm thick silicon on 3μm buried oxide

5μm deposited oxide over the device and waveguide

operates in reverse bias

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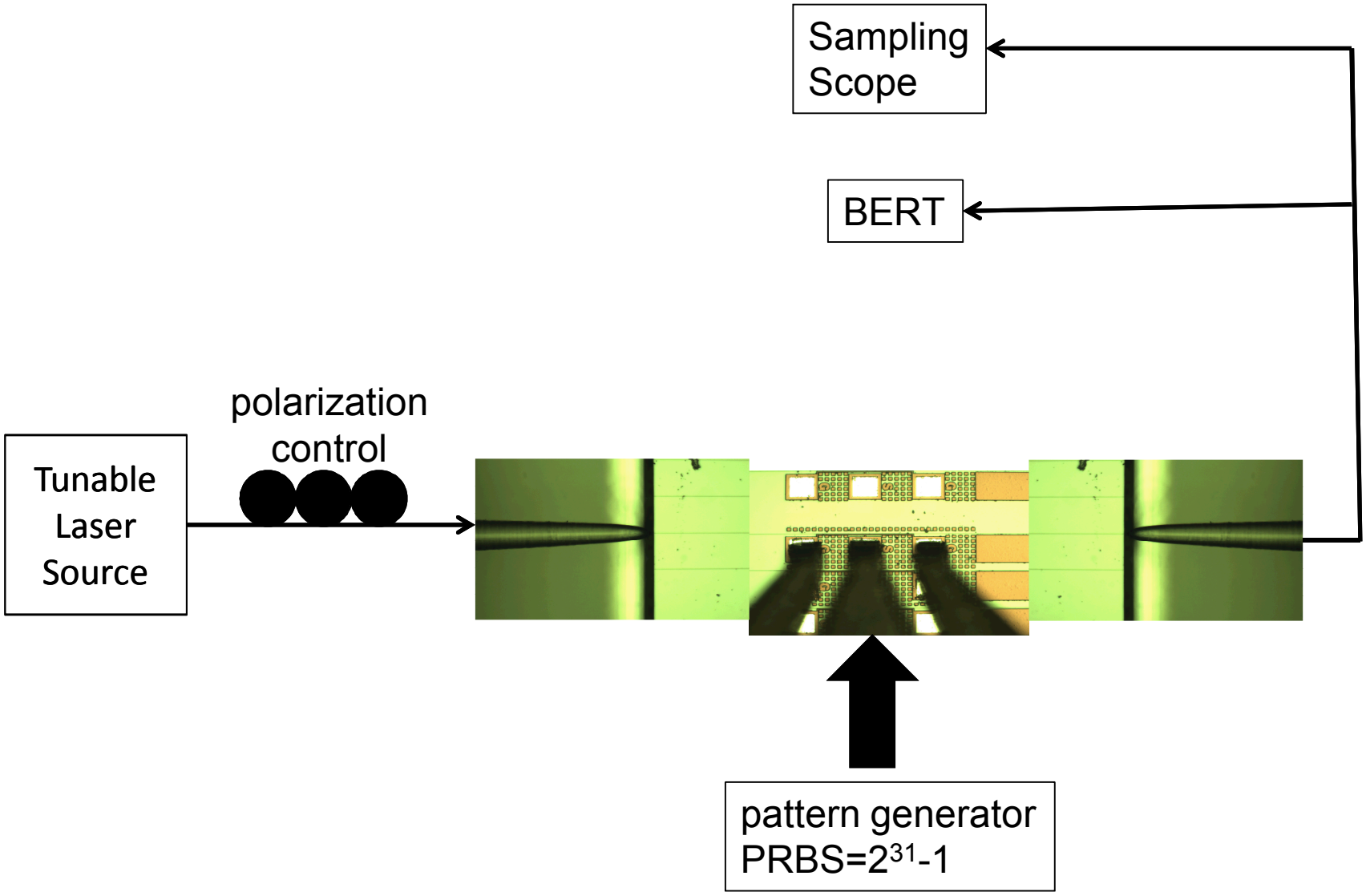
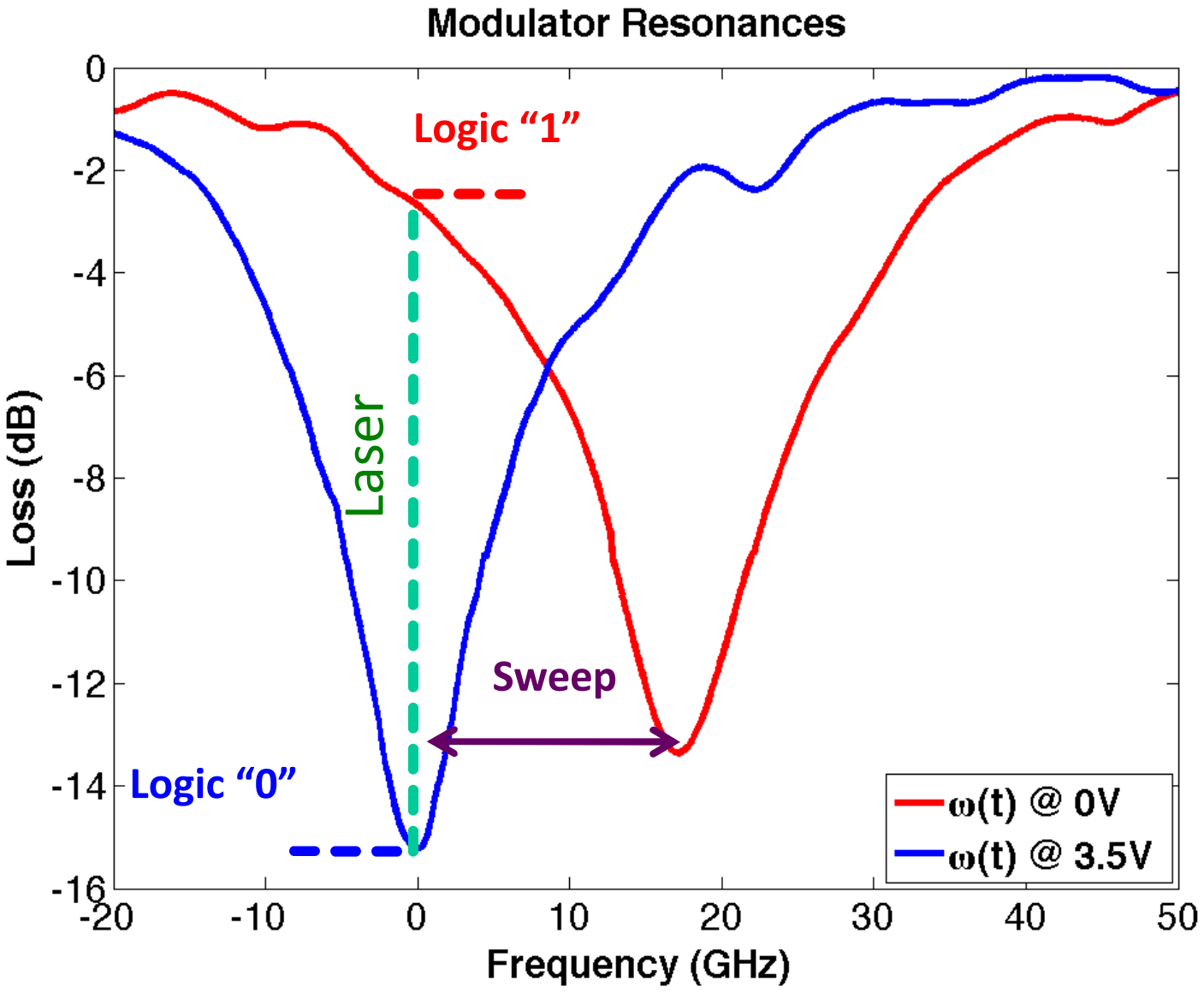

Sampling Scope
BERT
polarization control
Tunable Laser Source
pattern generator
PRBS=2^31-1

Reverse Bias Modulation Action



Sub-Threshold/Reverse Bias Modulation

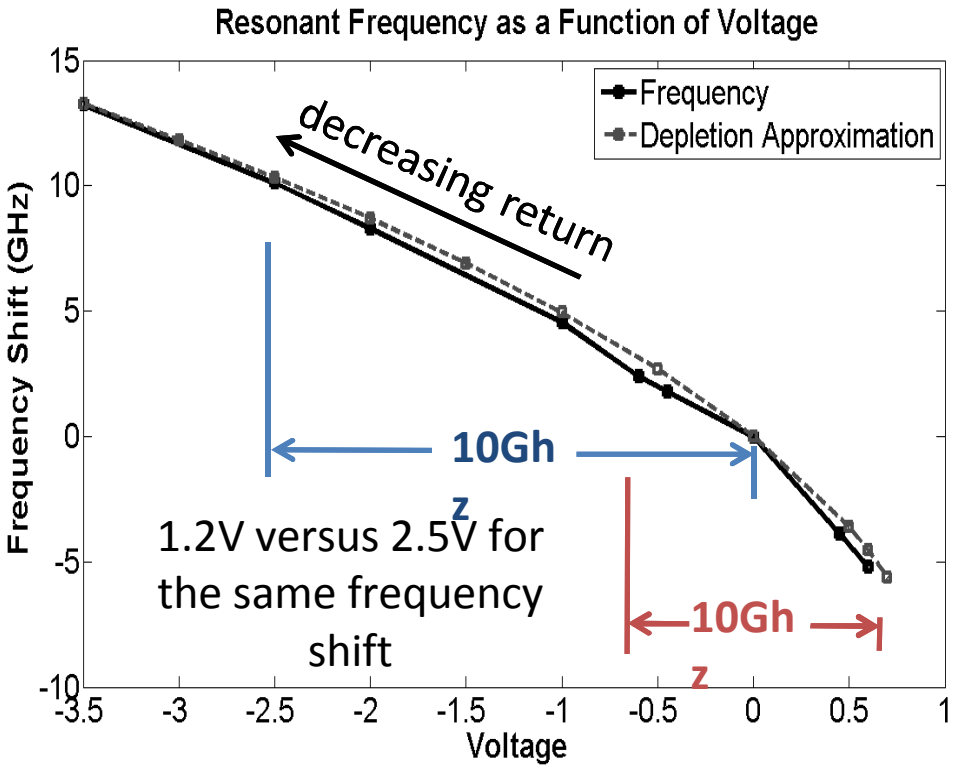
Frequency shift is a function of the square root of voltage:

$$W \propto \left(V_{bi} - V_a\right)^{\frac{1}{2}}$$

$$W = \sqrt{\frac{2\varepsilon_s\left(N_a + N_d\right)\left(V_{bi} - V_a\right)}{qN_aN_d}}$$

$$\Delta f \propto L\sqrt{\Delta V}$$

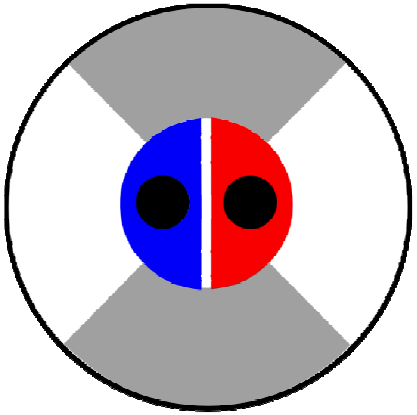
L is the interaction length

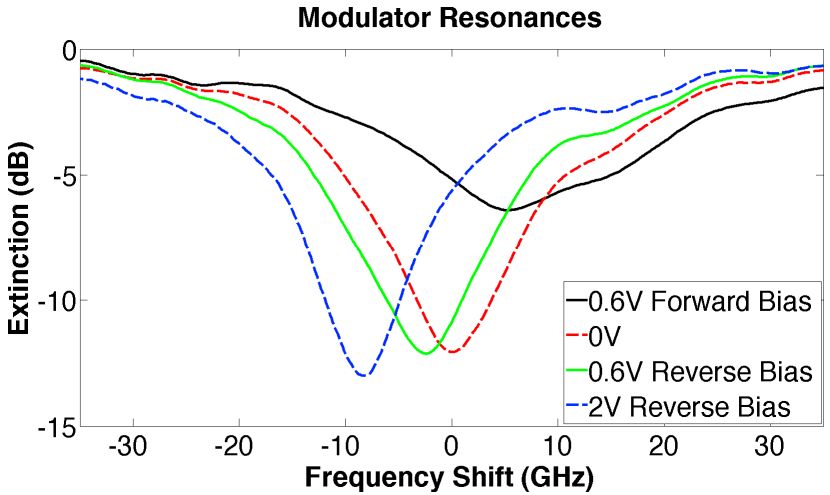


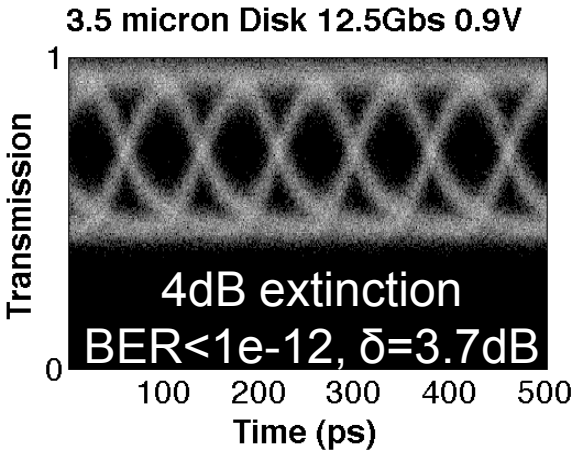
Working partly in the sub-threshold region maximizes the return on voltage

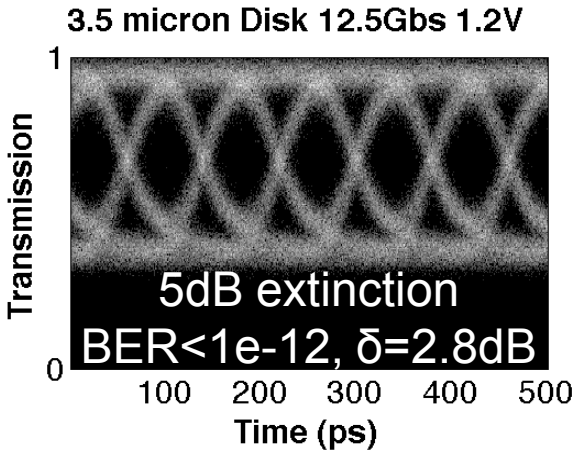
E=QV → **10GHz Energy savings is ~50%**
13GHz Energy savings is ~67%

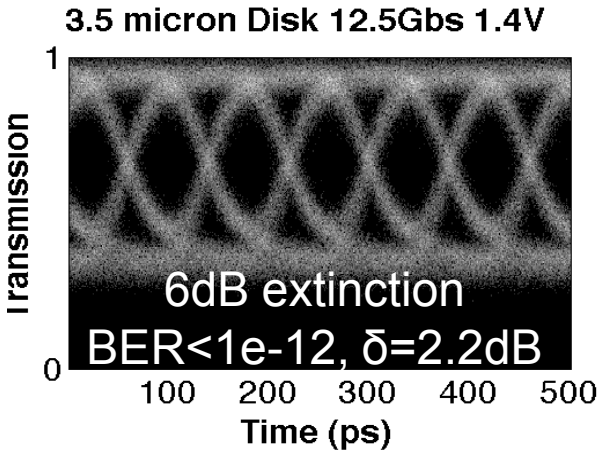
Sub-Threshold/Reverse Bias Modulation







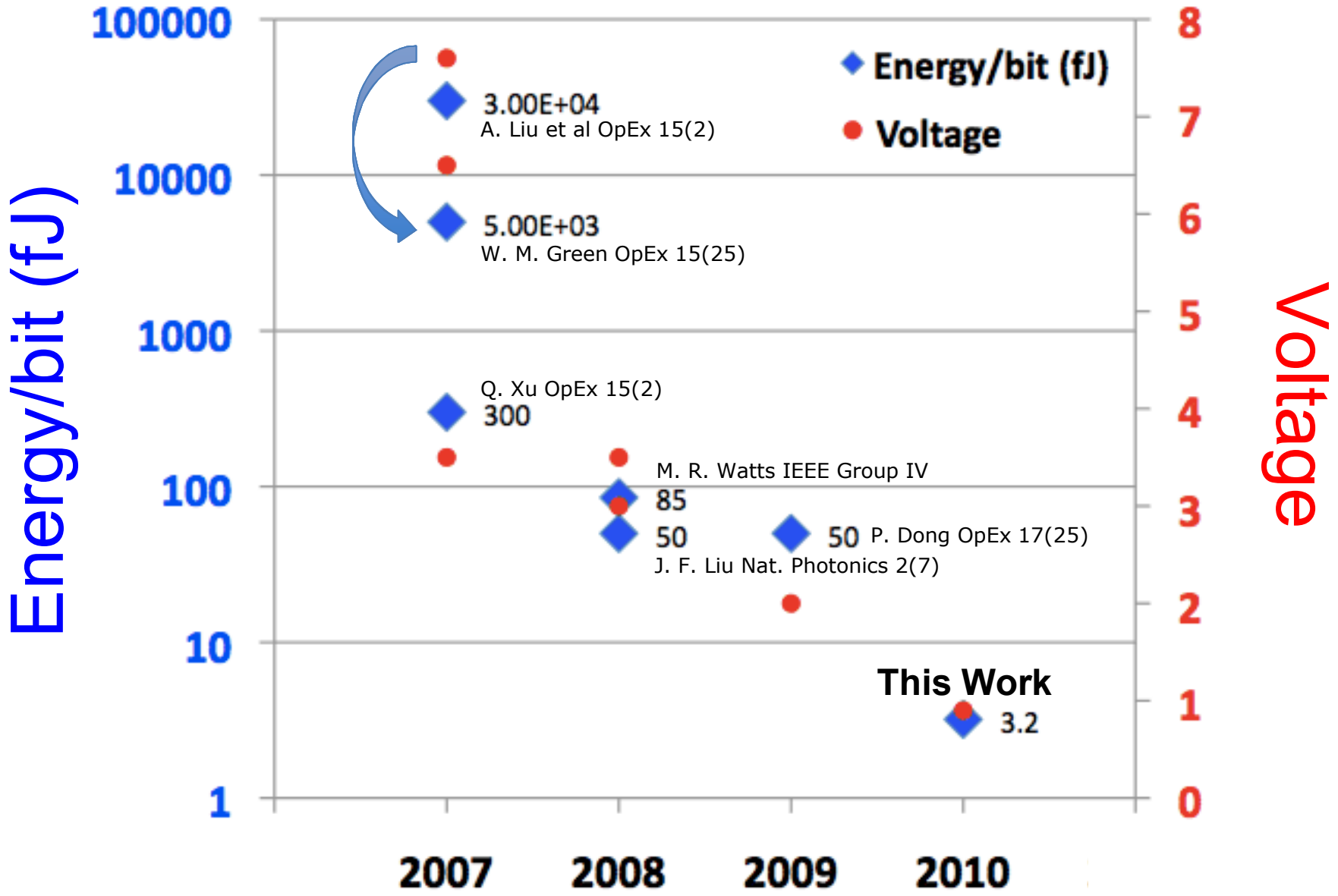




Energy/bit:	**0.9V**	**1.2V**	**1.4V**
Analysis:	**3.8fJ/bit**	**6.8fJ/bit**	**10.6fJ/bit**
Measured:	**3.2fJ/bit@1V**		**10.1fJ/bit@1.5V**

E_{bit}=3.2fJ @ 12.5Gb/s & 3.7dB Power Penalty

Silicon Photonics

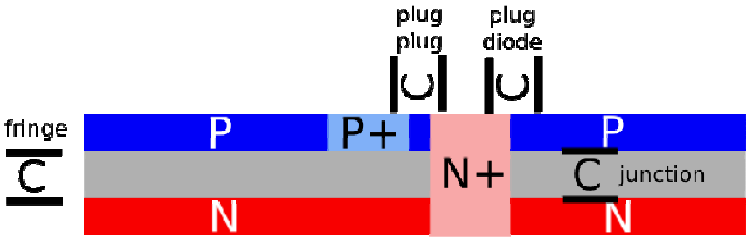


Energy Measurement and Theory

Analytical:

Using the depletion approximation

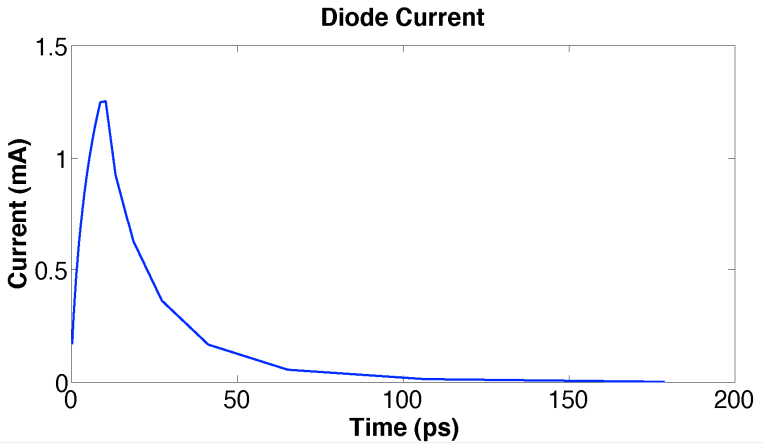
$$E_{bit} = \frac{V^2}{4}\sum C$$



Finite Element Model:

Tsupreme and Davinci TCAD from Synopsis

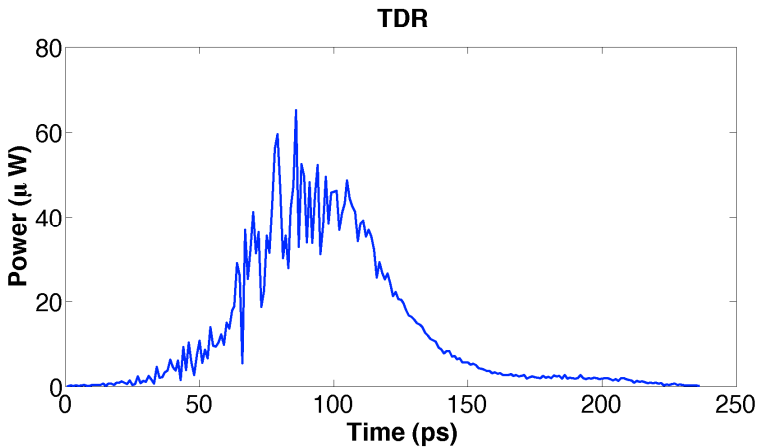
$$E_{bit} = \frac{V}{4}\int_0^t Idt$$

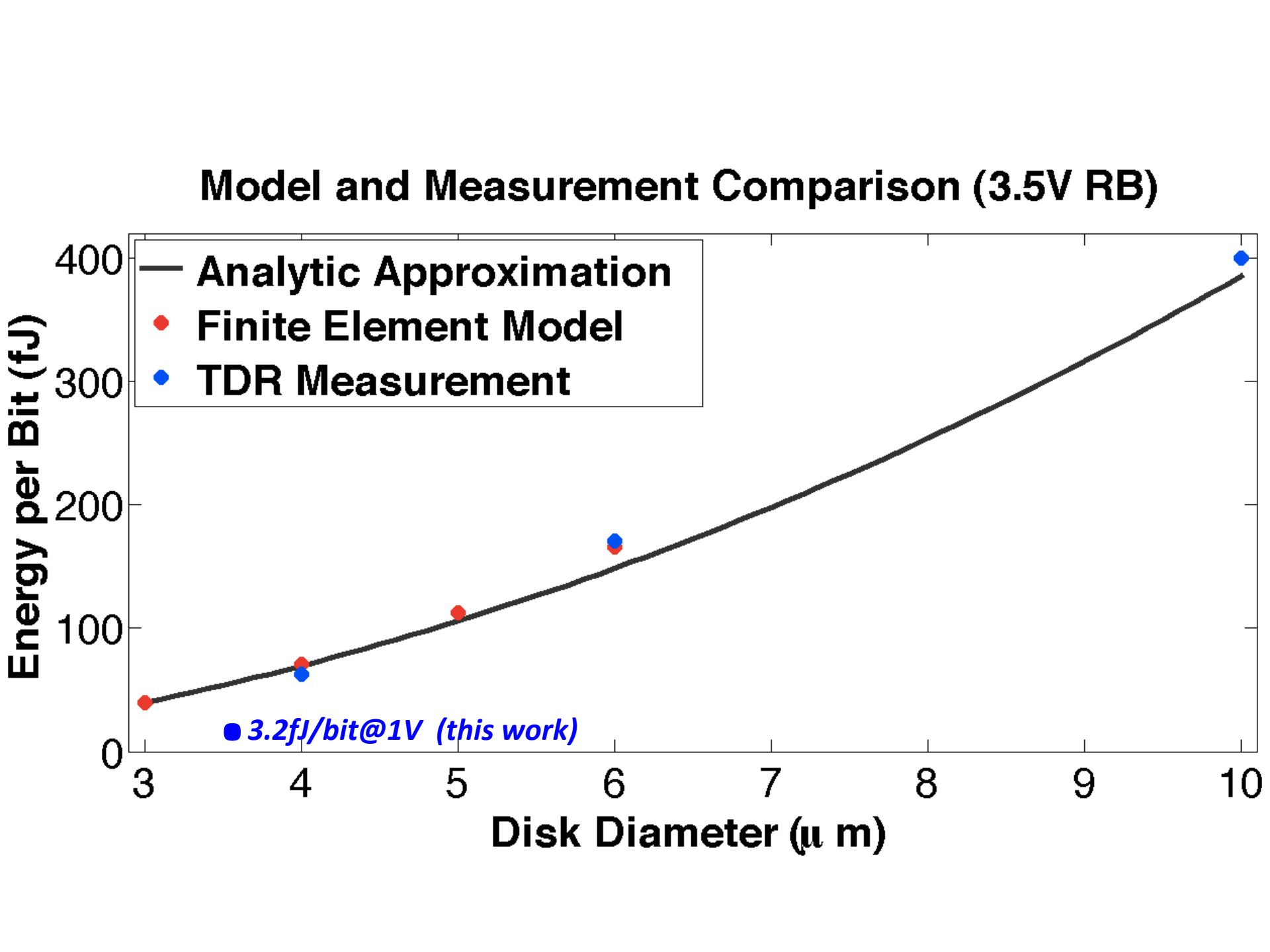


Measurement:

Time Domain Reflectometry

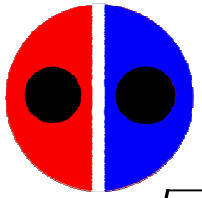
$$E_{bit} = \frac{\int_0^t \left(V_{input}^2 - V_{reflected}^2\right)dt}{4Z_0}$$



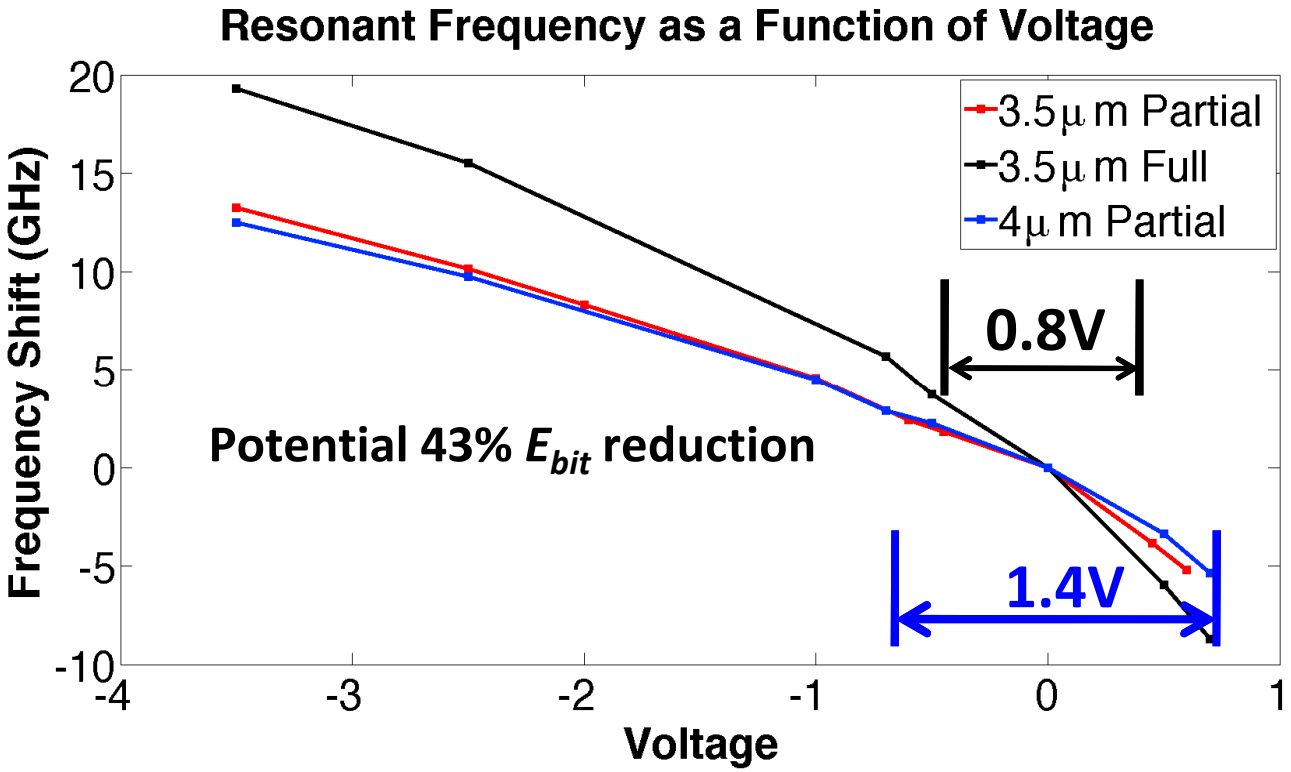

Model and Measurement Comparison (3.5V RB)
Analytic Approximation
Finite Element Model
TDR Measurement
3.2fJ/bit@1V (this work)
Energy per Bit (fJ)
Disk Diameter (μ m)
0
100
200
300
400
3
4
5
6
7
8
9
10

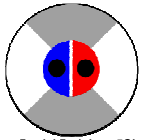
Another design approach for reducing voltage and Ebit

R=2X and C=2X



$$\Delta f \propto L\sqrt{\Delta V}$$

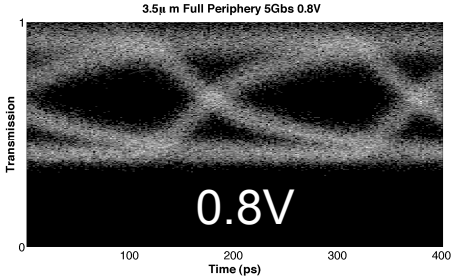


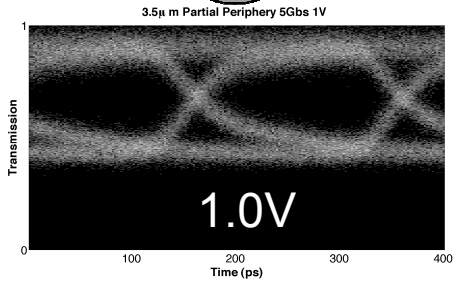


In practice, at 5Gb/s

20% E_{bit} reduction

~2.5fJ/bit 4dB extinction





Fully doped disks run at lower voltages in exchange for less bandwidth

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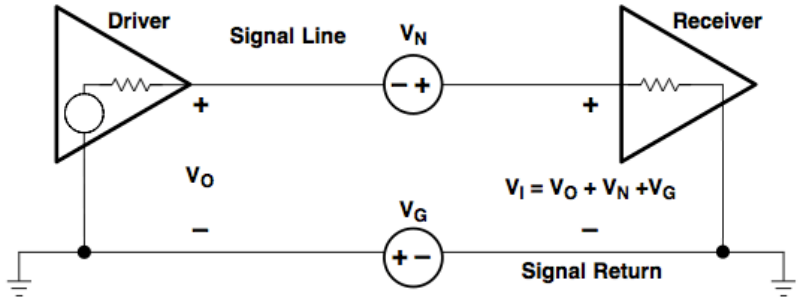
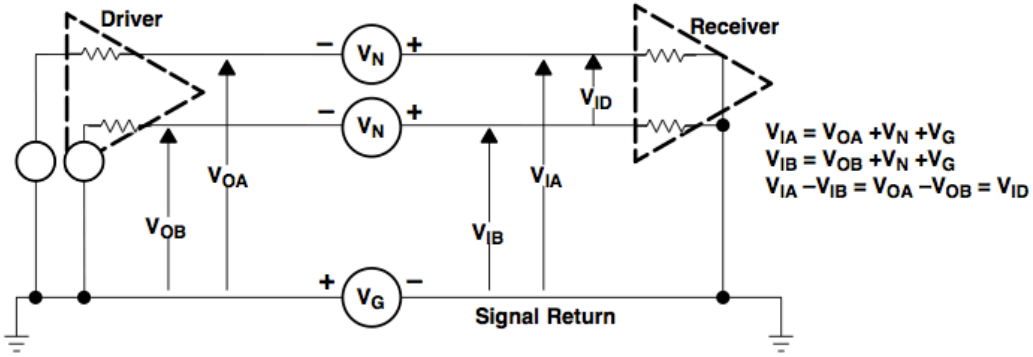
Fibers per exascale system	✔	**200 thous.**	**45.7 million**
Integration with TSV		✔	✔★
Monolithic with CMOS (electrical multiplexing)	✔	✔	**?**
Data center virtualization (long haul)	✔	✔	✔

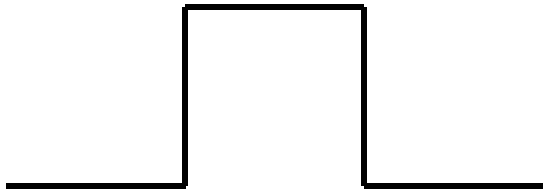
For even lower voltage drivers differential signaling is considered for driving the device

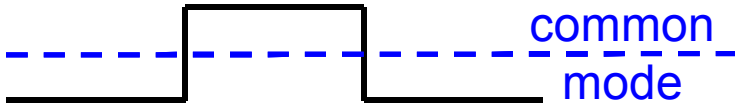
circuit

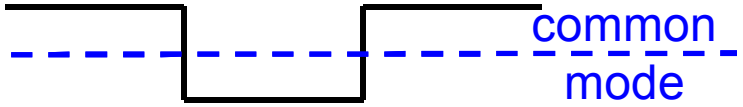


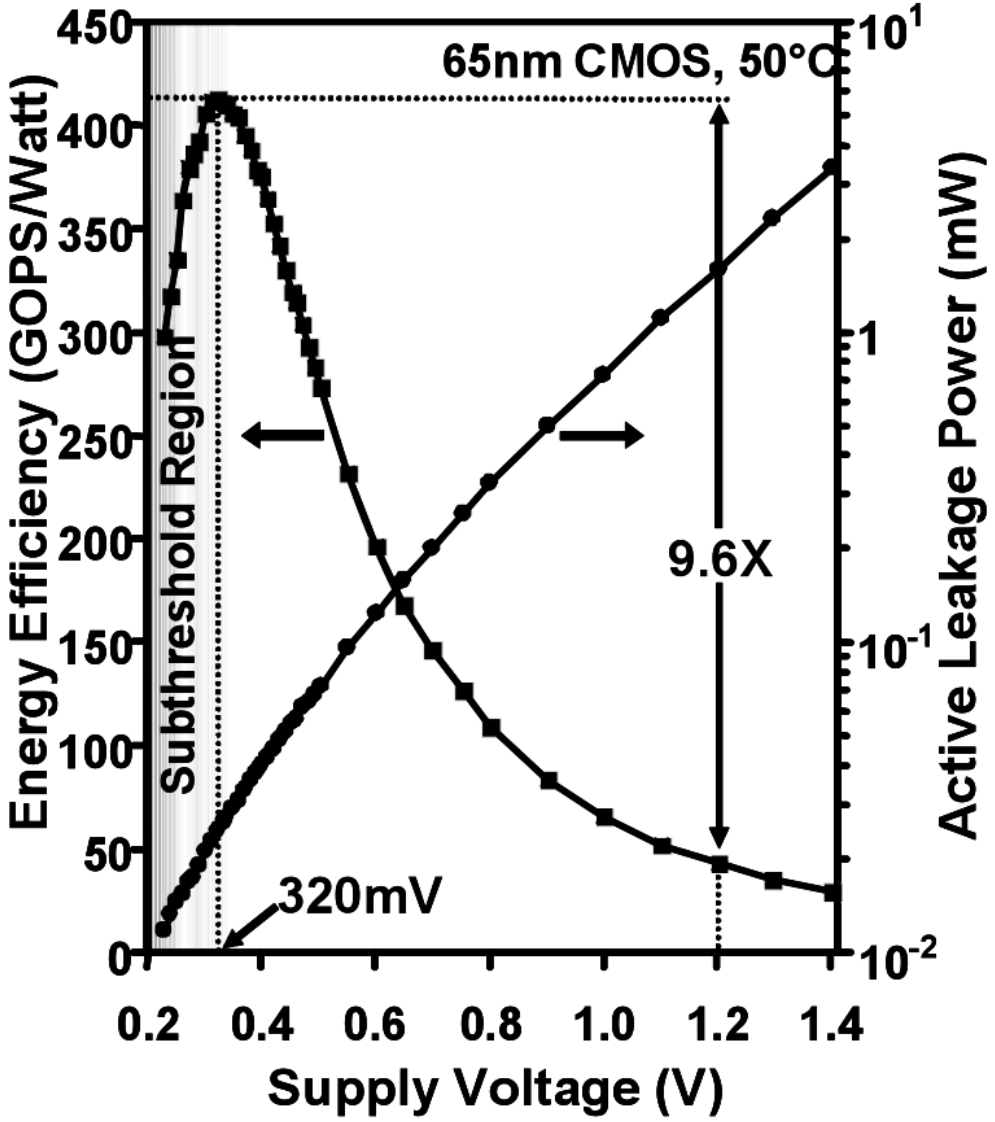


input waveform







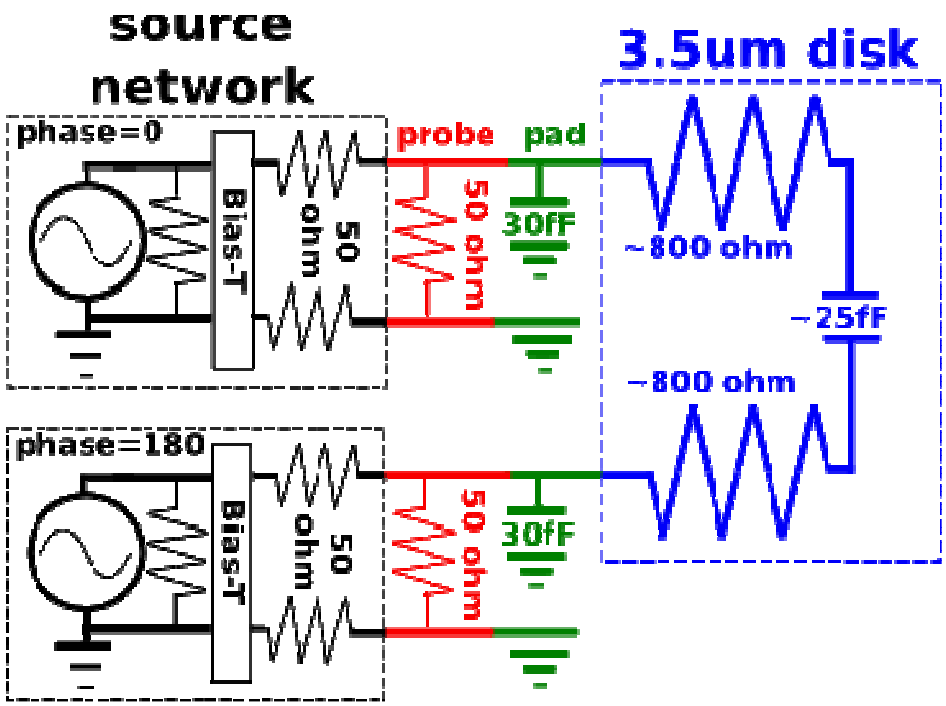


from Shekhar Borkhar, "The Exascale Challenge"

Differential signaling would ease integration with the potential for much lower V_{dd}

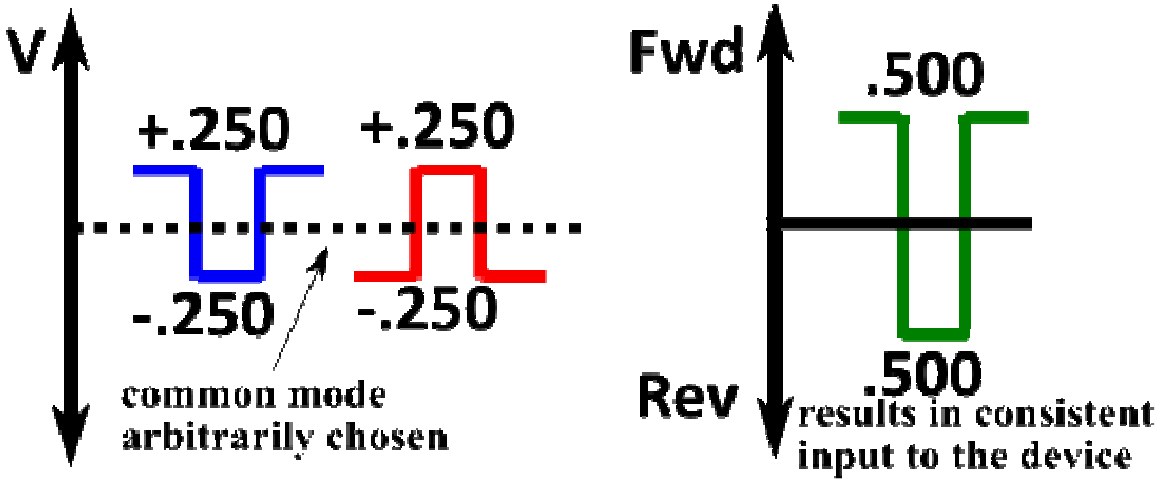
The experimental setup requires GSGSG 50Ω terminated probes.

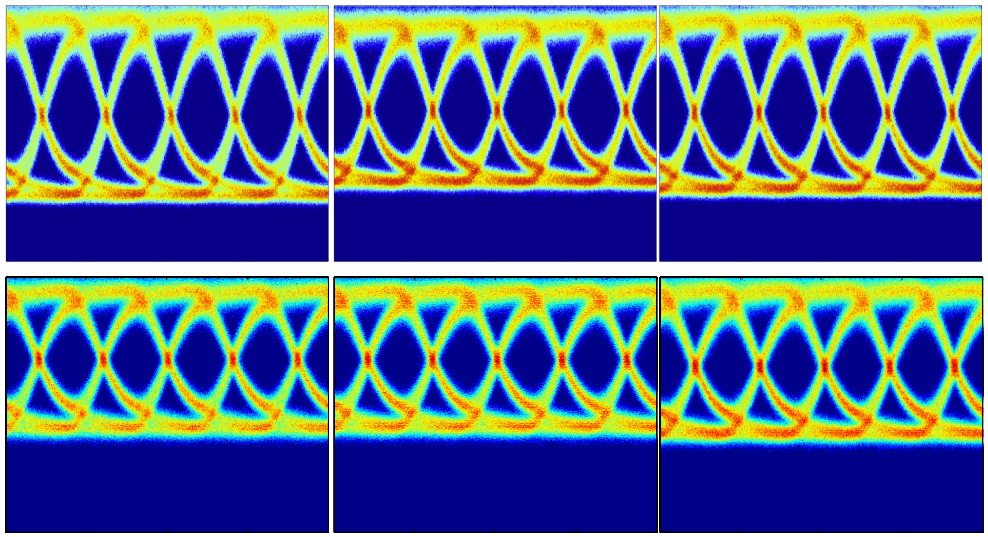
The S probe points are driven differentially into the N and P type silicon.



This demonstration uses one source networks and two outputs driven 180^{o} out of phase.

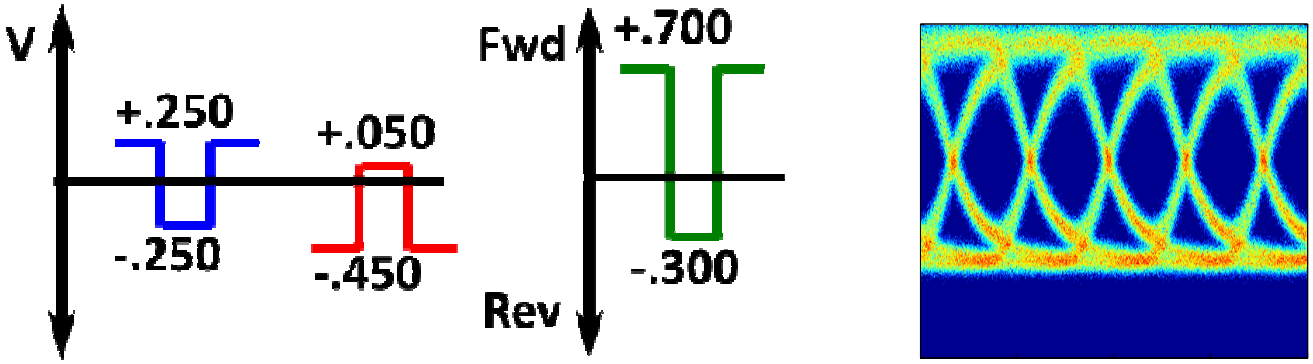
The easiest to implement is symmetric differential signaling … the common modes are the same

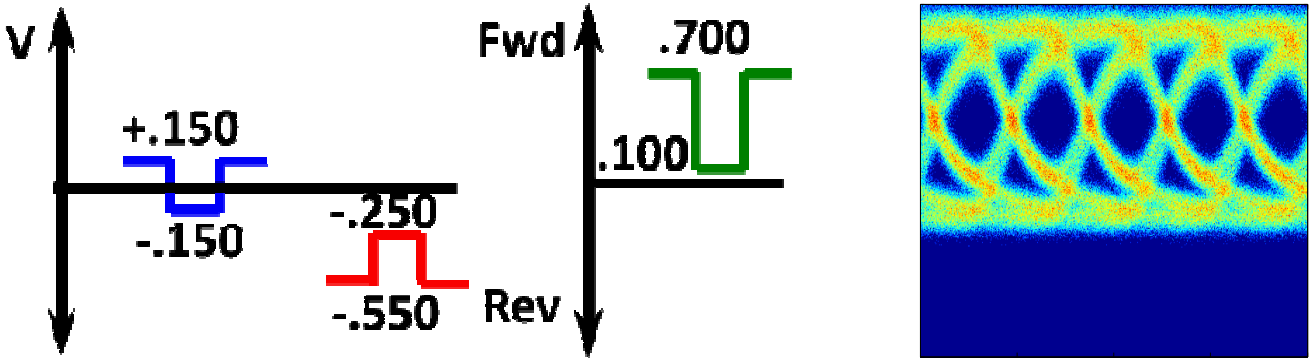


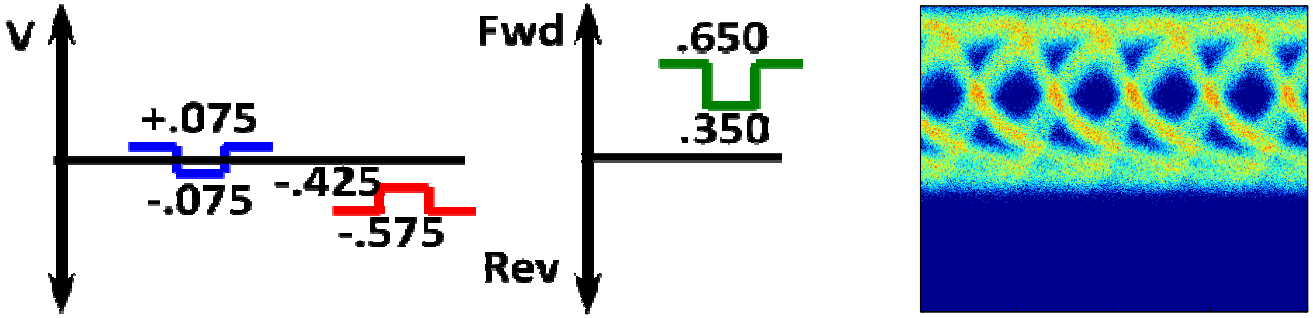


Assymetric signaling is a larger challenge

… the common modes are different and require negative voltages

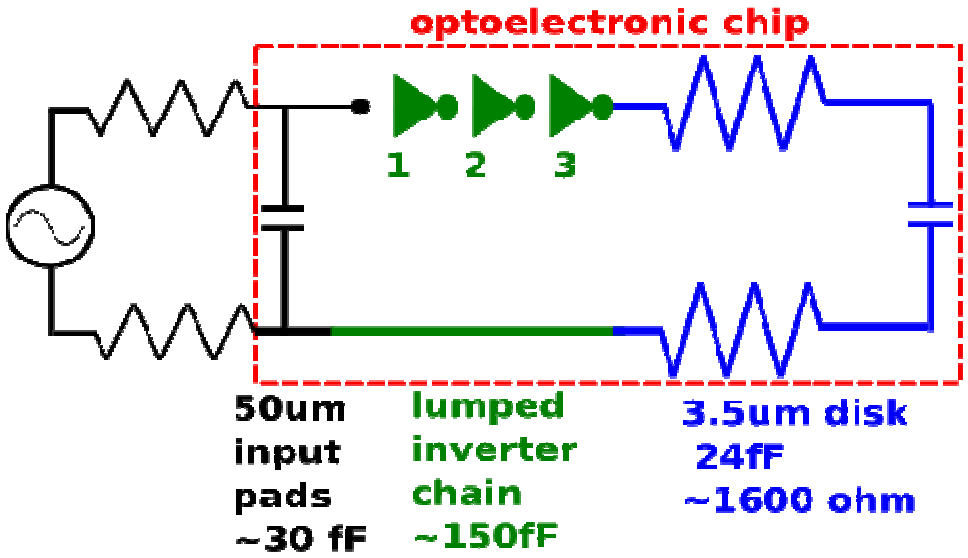


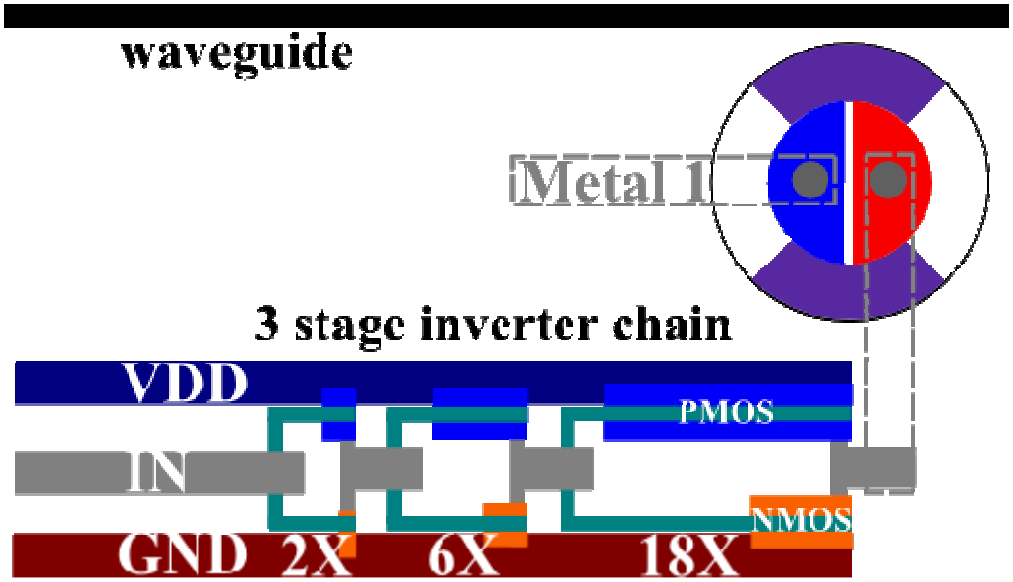




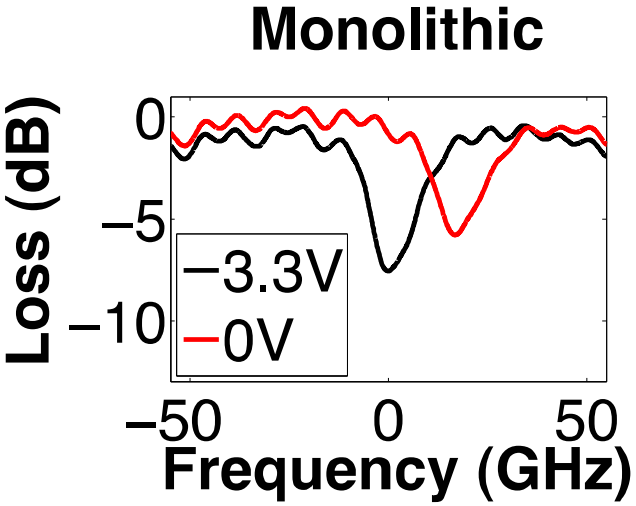
research device attributes for a 2018, 10 TFLOP chip	Dis	Si Photonics	VCSEL
Manufacturing volume to match server chips 1:1	✔	✔	✔
Energy/bit (on chip) (2018 ~100fJ/bit)	✔	**~100fJ/bit**	**~140fJ/bit**
Energy/bit (total)		~150fJ/bit	~140fJ/bit
Low Voltage Compatibility	✔	**(300mV) ✔**	?
Fibers per chip (assume 10Gbps SiP, 100 channels, 5THz)	✔	**2 (WDM)**	**457 (35Gbps)**
Fibers per exascale system	✔	**200 thous.**	**45.7 million**
Integration with TSV		✔	✔★
Monolithic with CMOS (electrical multiplexing)	✔	✔	**?**
Data center virtualization (long haul)	✔	✔	✔

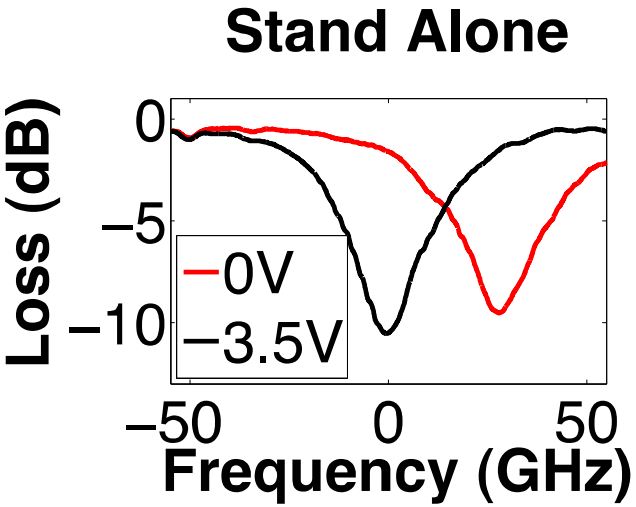
Monolithic Integration

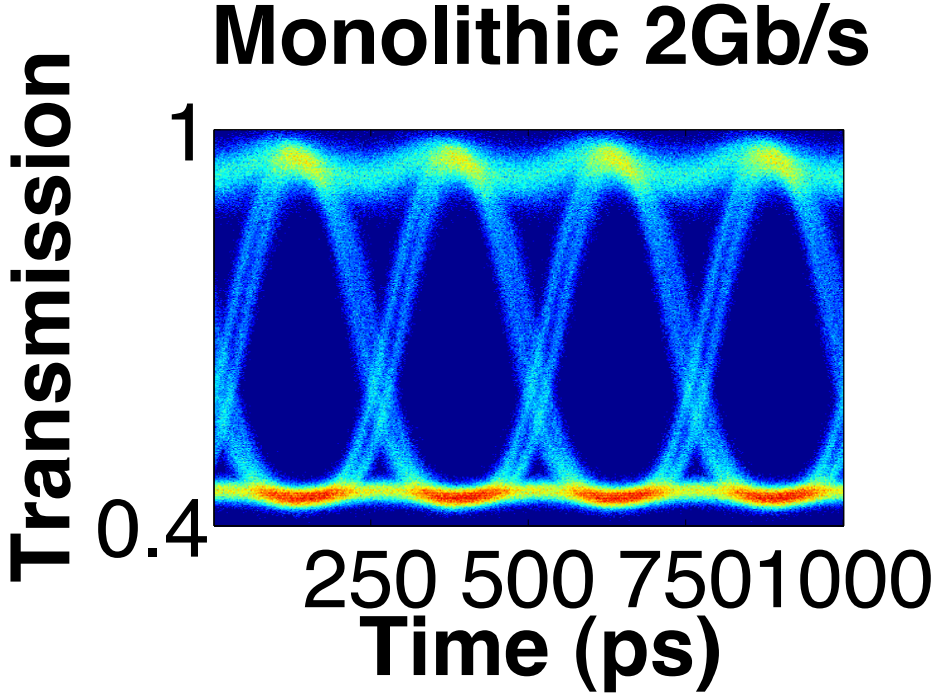




High Speed Modulation

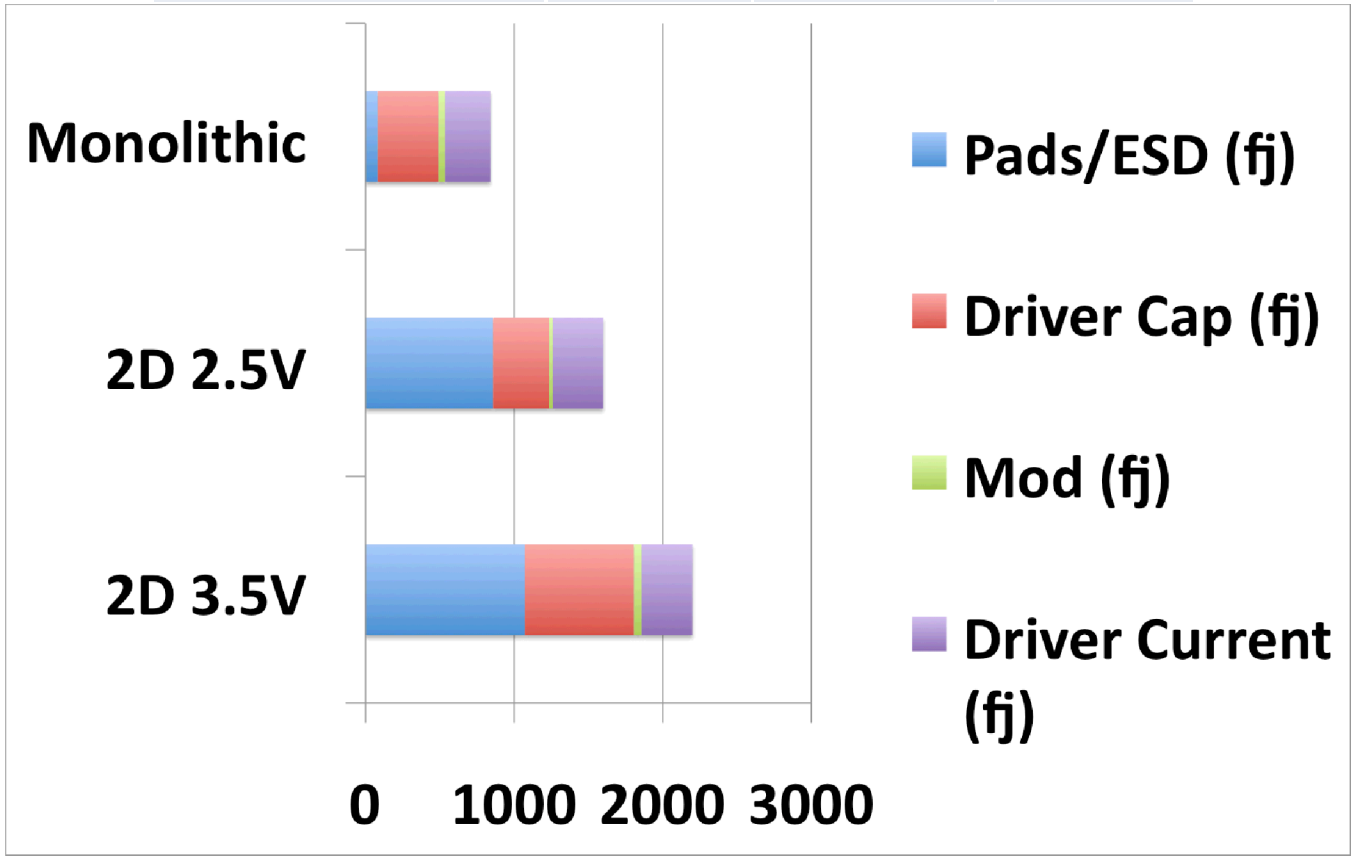






Power and Energy Consumption

Device	Power	Energy	BW
Discrete Disk 3.5V	200uW	~50fJ/bit	10Gbps
Monolithic 3.3V	1.68mW	840fJ/bit	2Gbps
2D 2.5V	8mW	1.6pJ/bit	5Gbps
2D 3.5V	11.2mW	2.2pJ/bit	5Gbps



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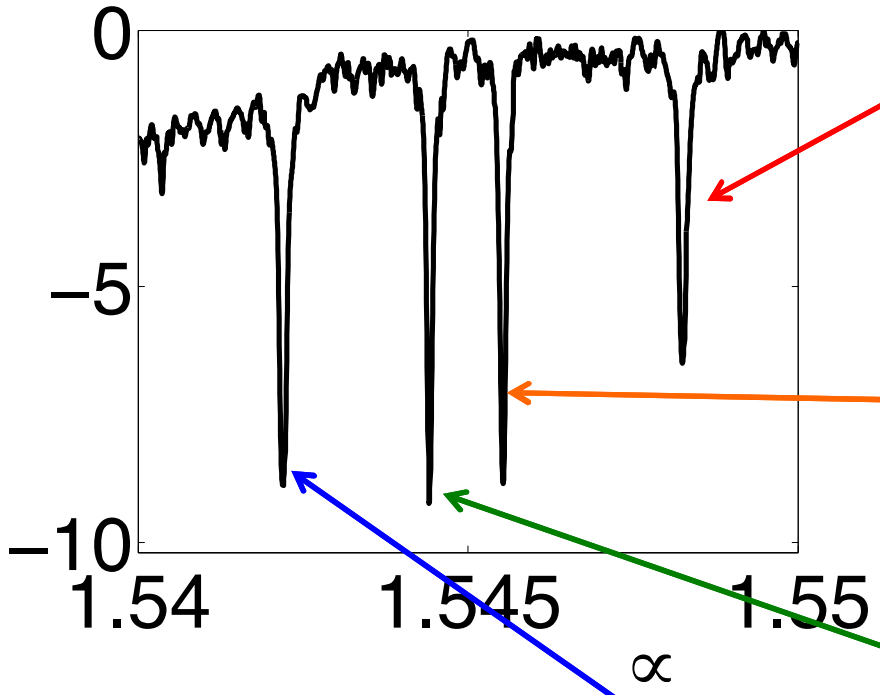
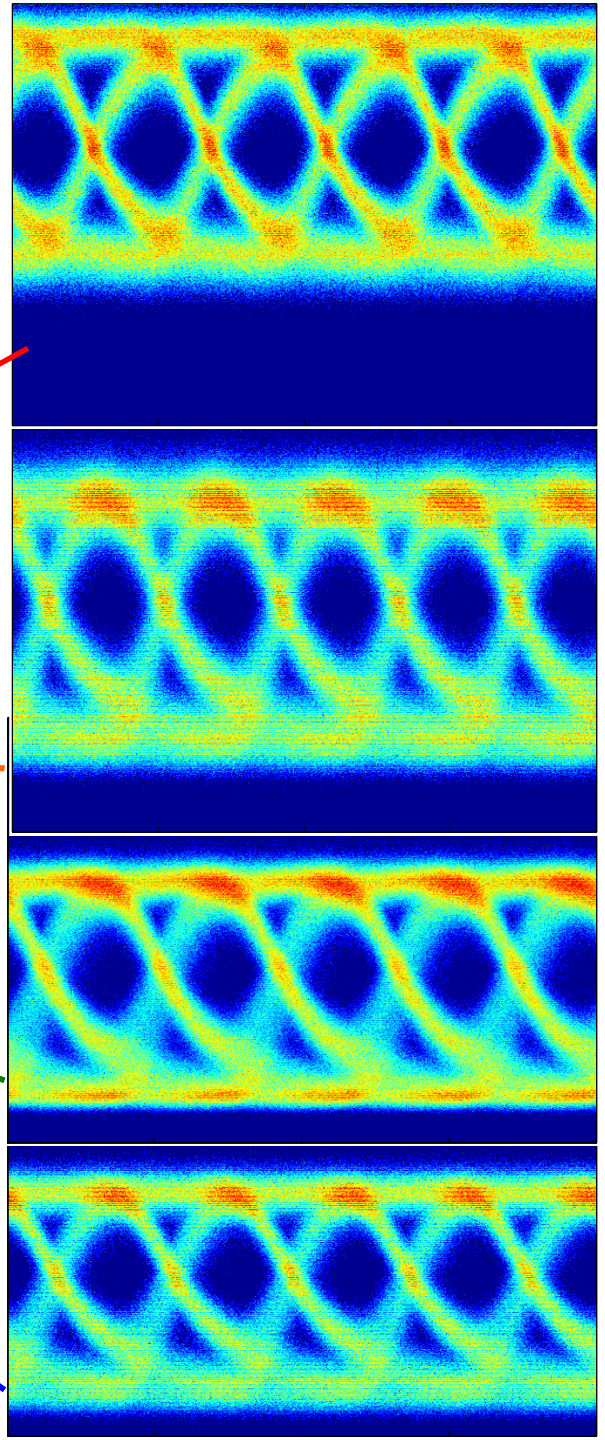
4 Channel Transmitter 40Gbps aggregate BW
@3fJ/bit, P~120μW





Channel spacing is 400GHz …

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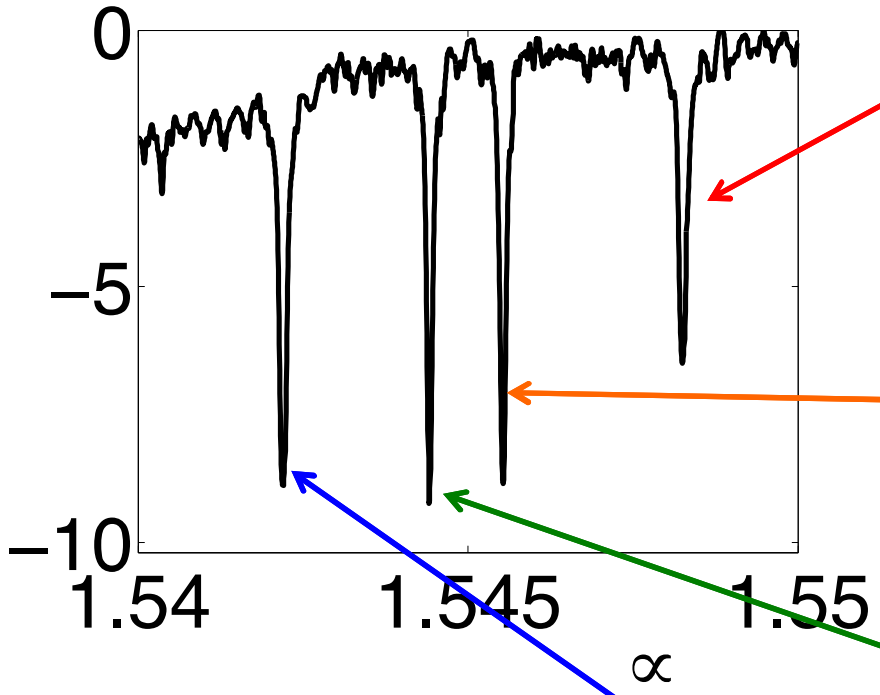
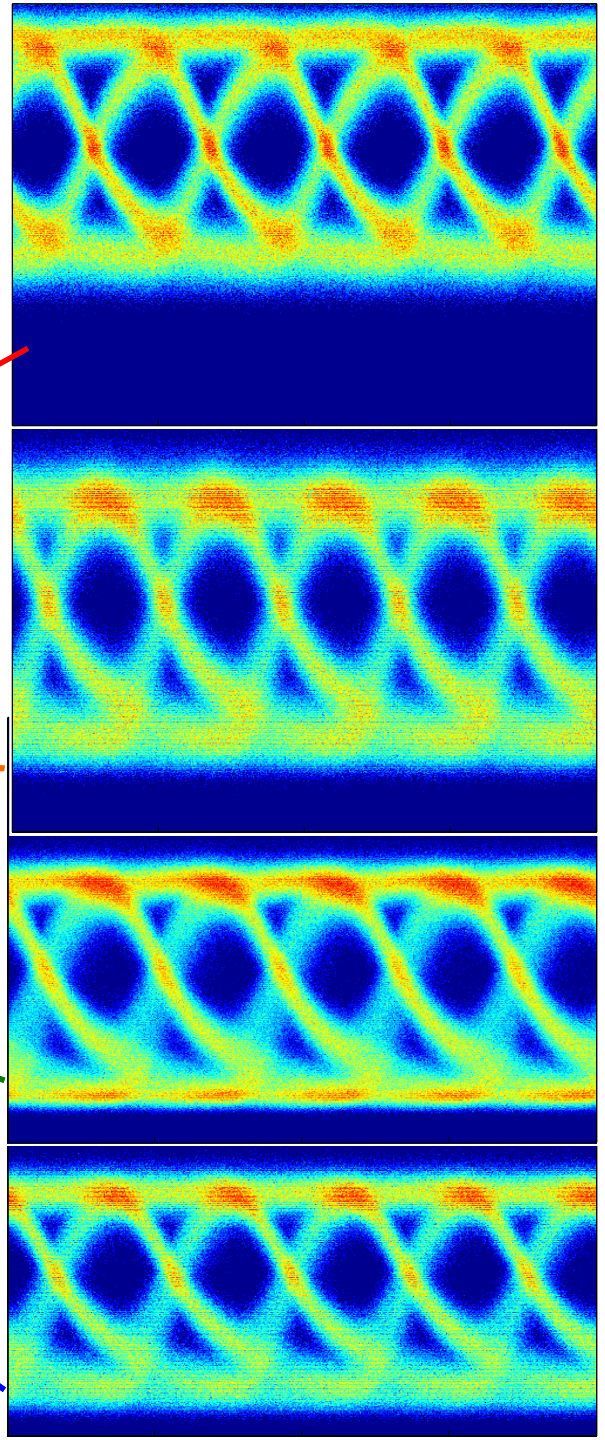
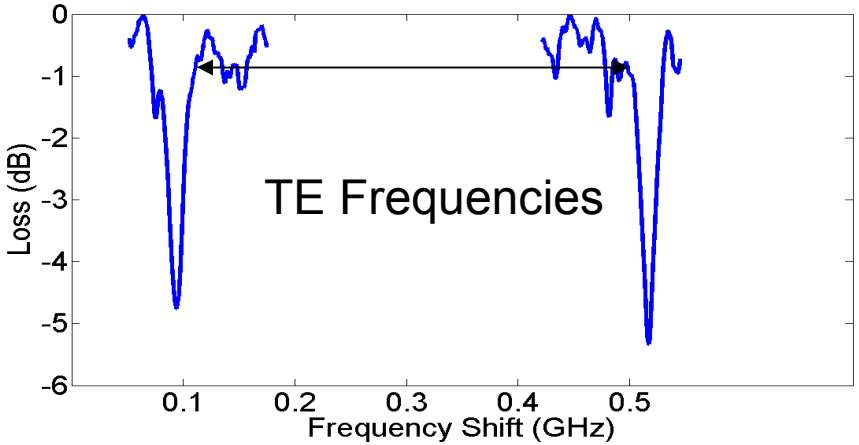
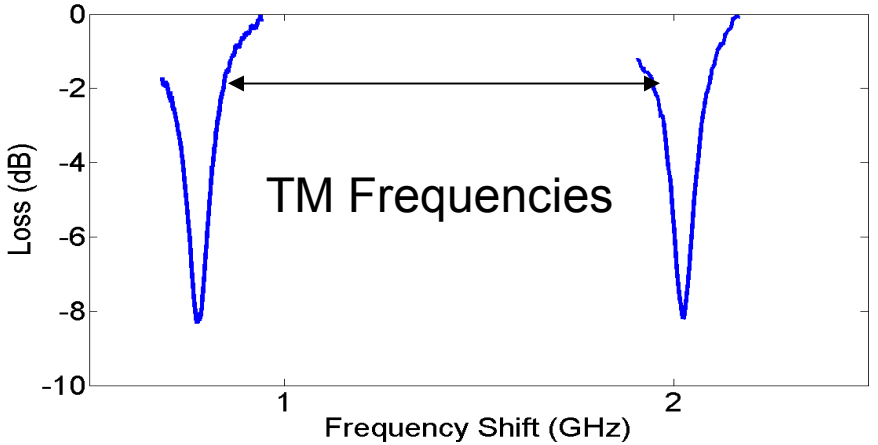




Channel spacing is 400GHz …
well it was designed that way anyhow!

If two identical resonators are fabricated using the same mask on a wafer in two different locations the frequencies usually will not match





This precludes the implementation of WDM signaling

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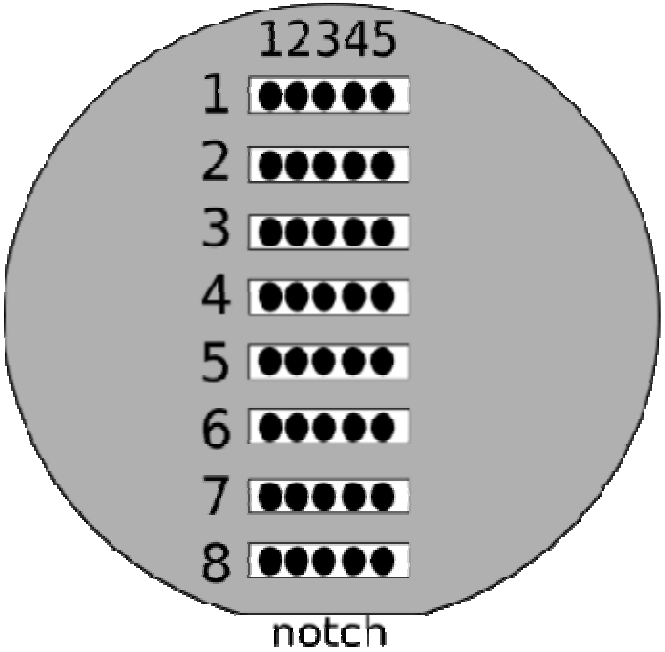
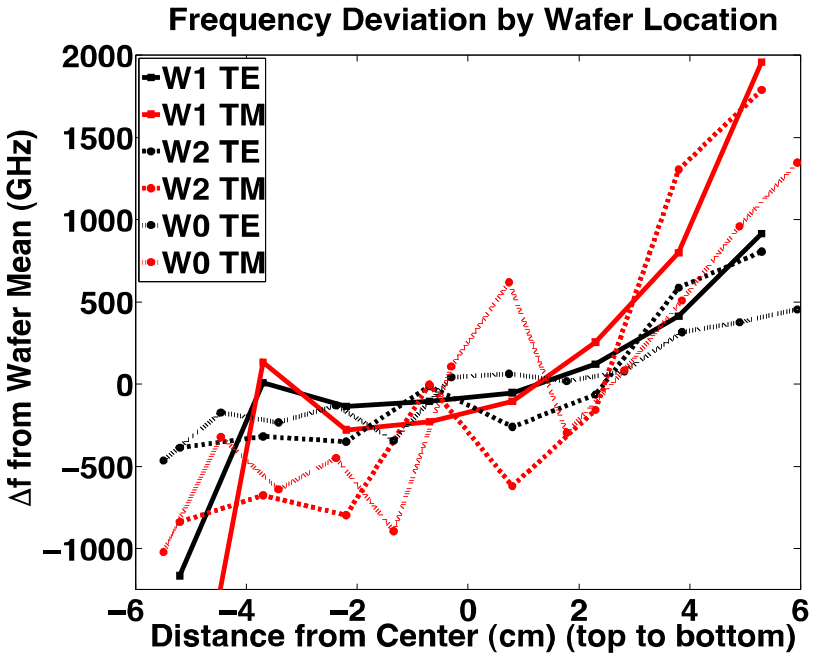
Monolithic with CMOS (electrical multiplexing)	✔	✔	**?**
Data center virtualization (long haul)	✔	✔	✔

To quantify this 5 identical disks per chip were fabricated on eight chips across a wafer





	W0 [metal] From [13]	W1 [metal] (filtered)	W2 [Si only]	|W1-W2|
TE Mean (THz)	192.0	191.0 (191.2)	192.2	1.117
TE Std Dev (GHz)	285	556 (357)	430	126
TE Median (THz)	192.0	191.0 (191.0)	192.0	0.966
TM Mean (THz)	195.8	194.1 (194.5)	194.8	0.666
TM Std Dev (GHz)	741	1,194 (749)	957	237
TM Median (THz)	195.7	194.2 (194.2)	194.4	0.215

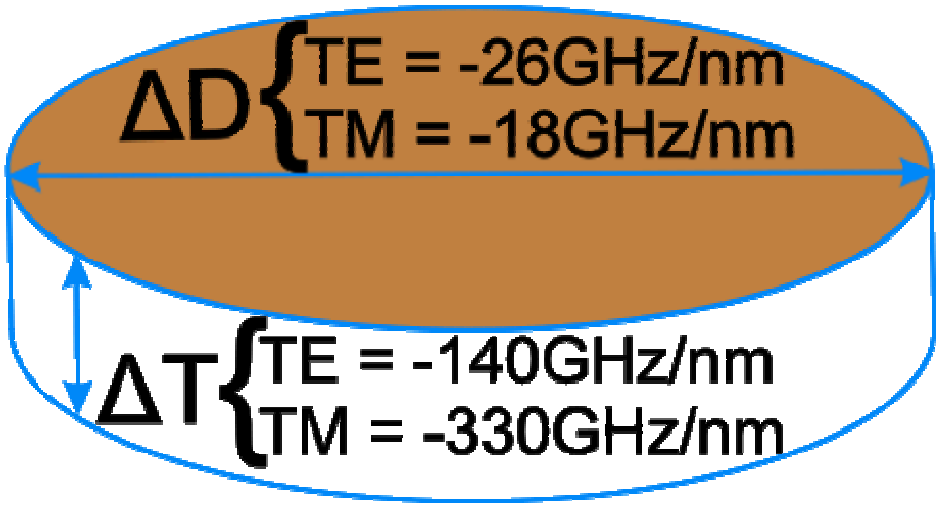
3 wafers were measured

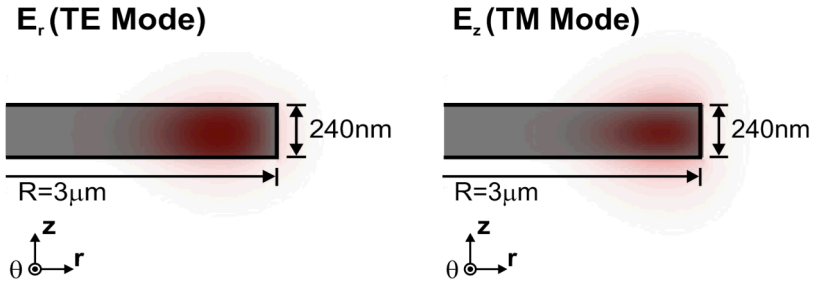
Focus from here is on W1 & W2

3σ=240MHz, with TEC @ 35°C

The cause of the frequency mismatch is segmented by measuring TE & TM frequencies

6μm disk is measured for the simplicity of its dimensions
It has a thickness and a width and the FSR is manageable





A 2D finite difference modesolver predicts the above dimension driven frequency shift

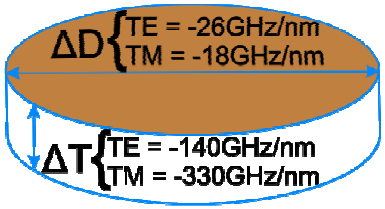
modesolver prediction

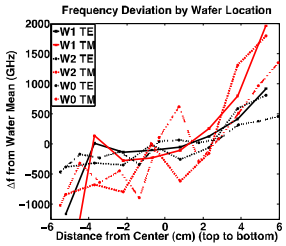
measured

$$\begin{bmatrix} \left.\frac{df}{dT}\right|_{TE} & \left.\frac{df}{dD}\right|_{TE} \\ \left.\frac{df}{dT}\right|_{TM} & \left.\frac{df}{dD}\right|_{TM} \end{bmatrix} \times \begin{bmatrix} \Delta T \\ \Delta D \end{bmatrix} = \begin{bmatrix} \Delta f_{TE} \\ \Delta f_{TM} \end{bmatrix}$$

Linear invertible matrix provides a unique solution

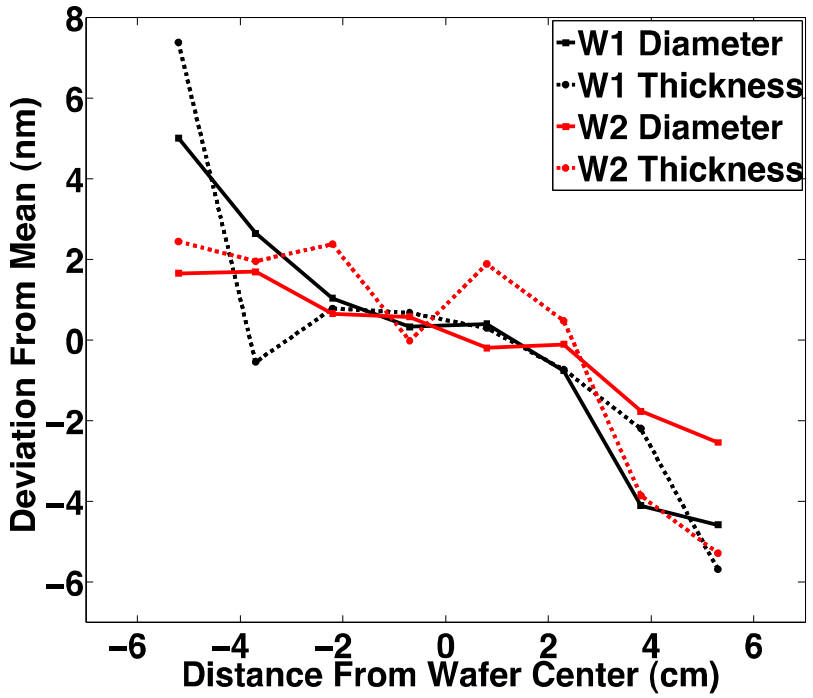
A finite element modesolver and linear system of equations are used to isolate the cause of non-uniformity in the resonator frequency

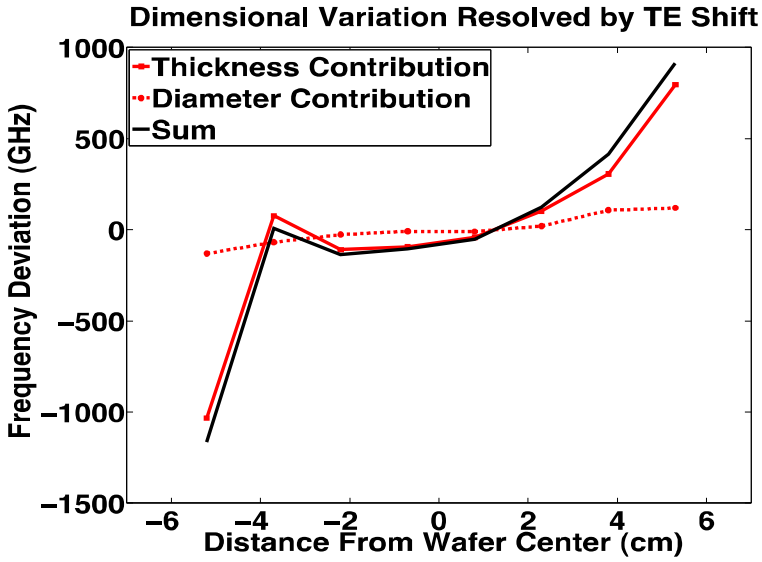




$$\begin{bmatrix} \left.\frac{df}{dT}\right|_{TE} & \left.\frac{df}{dD}\right|_{TE} \\ \left.\frac{df}{dT}\right|_{TM} & \left.\frac{df}{dD}\right|_{TM} \end{bmatrix} \times \begin{bmatrix} \Delta T \\ \Delta D \end{bmatrix} = \begin{bmatrix} \Delta f_{TE} \\ \Delta f_{TM} \end{bmatrix}$$

Dimension Deviation by Wafer Location

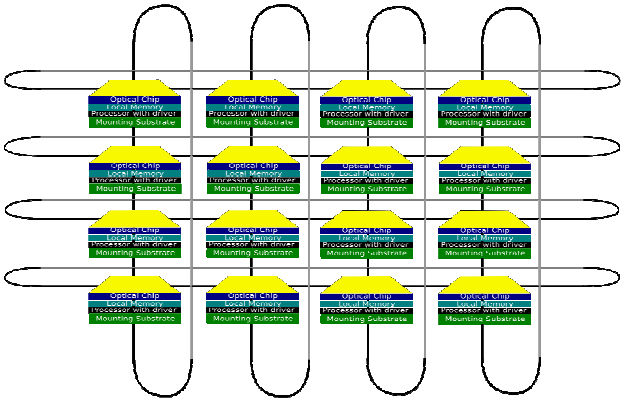




Thickness variation is the primary driver of frequency deviation

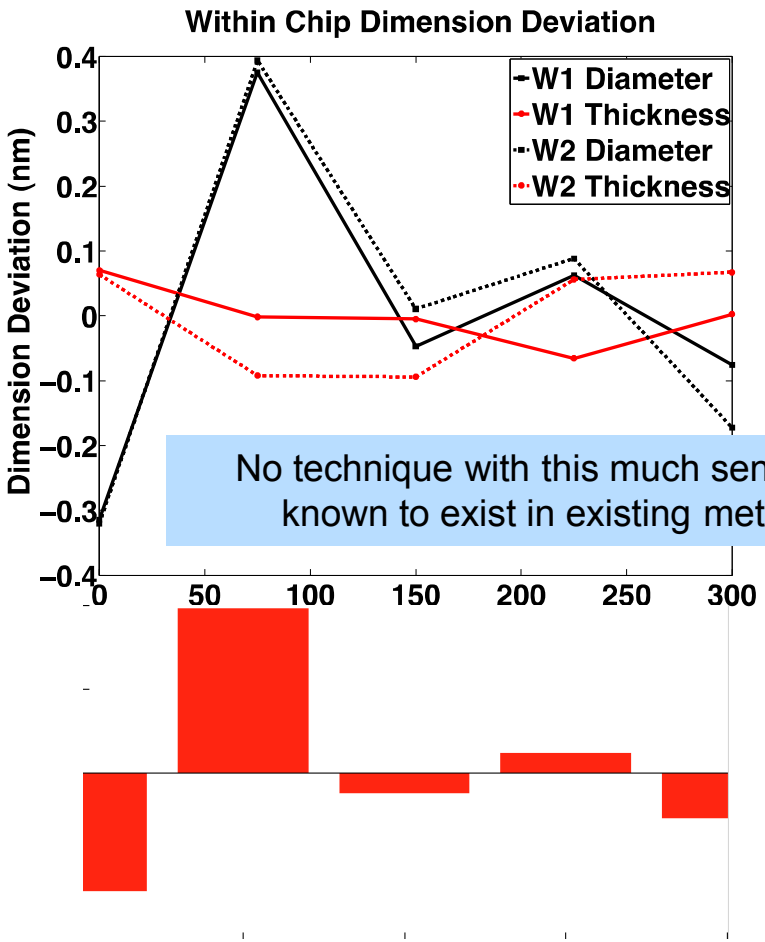
Remember that we don't need to connect wafers to each other, just chips

In the 2D torus it is 4 chips
in Blue Waters' 5D torus there are 10



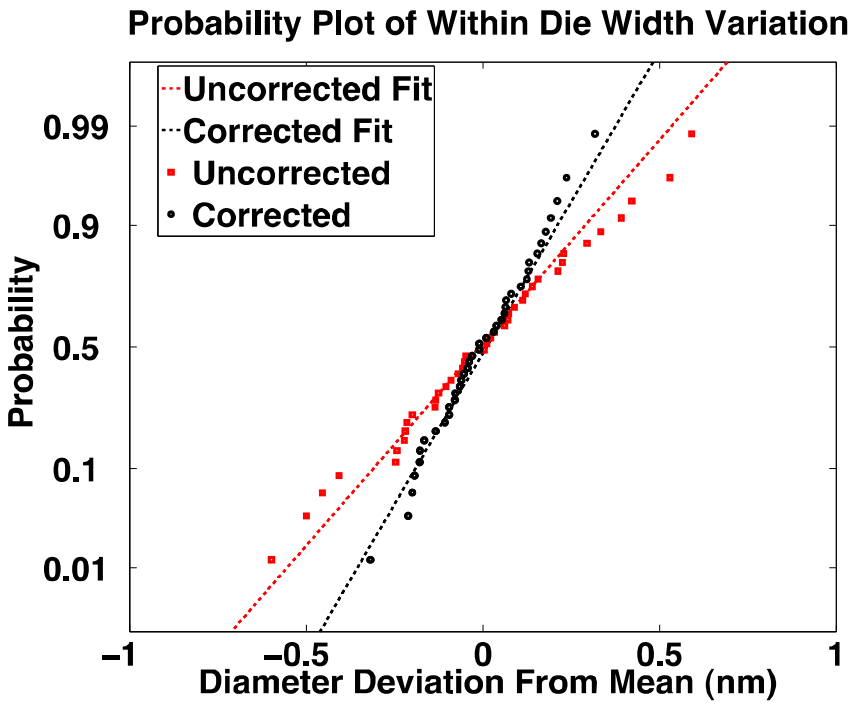
Silicon photonic chips manufactured on scale of server chips can be automatically sorted
250 die/wafer X 5000 wafers/fab = 1.25 million/fab/week

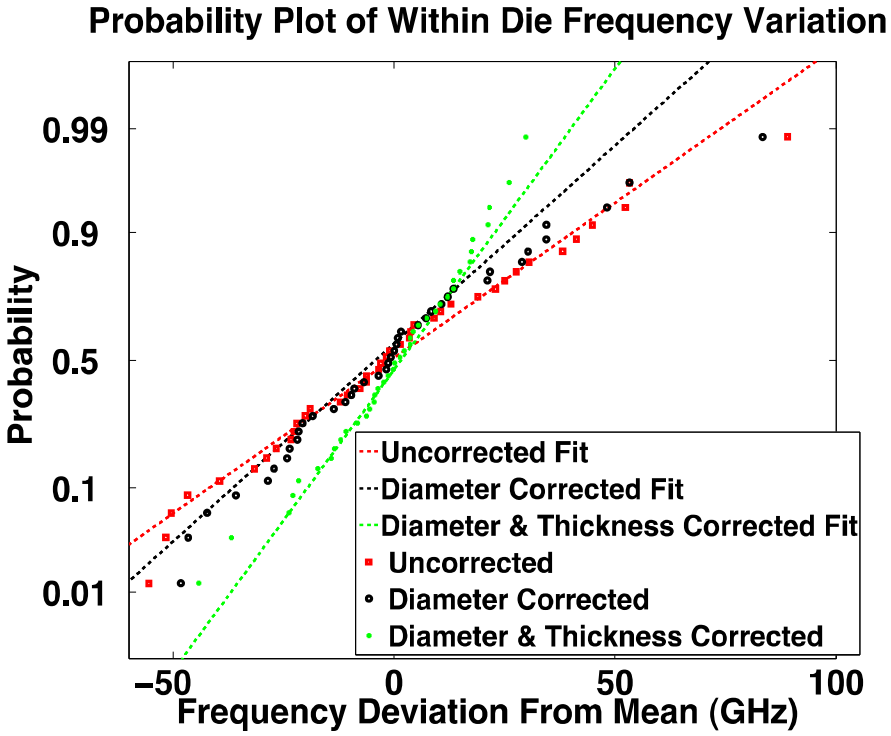
Using the 28 chips tested (3 wafers) it is possible to match micro-disk resonators of two chips to within 7GHz and 42% of the chips match within 25GHz



No technique with this much sensitivity is known to exist in existing metrology

Subtract the normalized mean of all points from the data on the left to get residual values

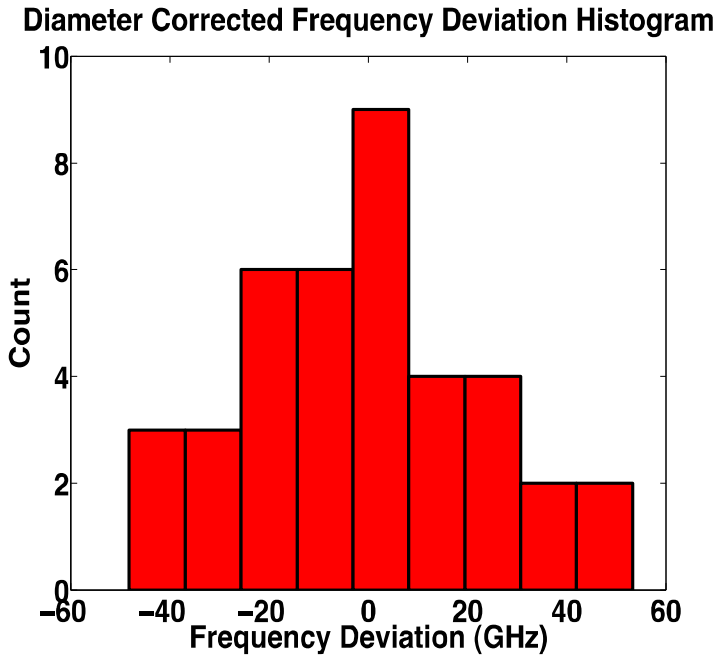




$$P_\delta = \frac{R}{2}\eta_H$$

η_H=7μW/GHz

Pδ=280μW



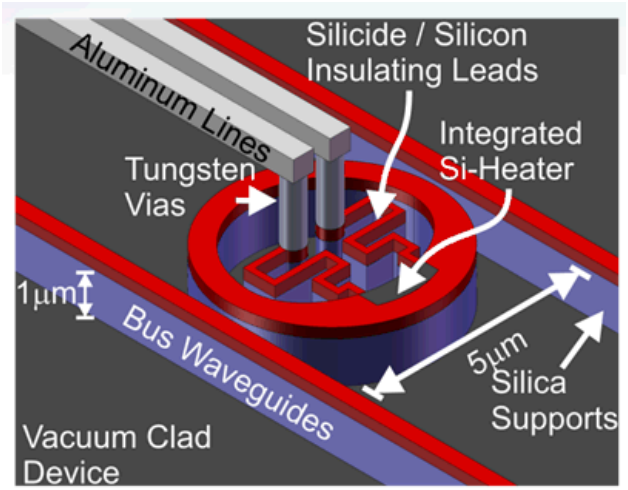
$$P_{\delta} = \frac{R}{2}\eta_{H}$$

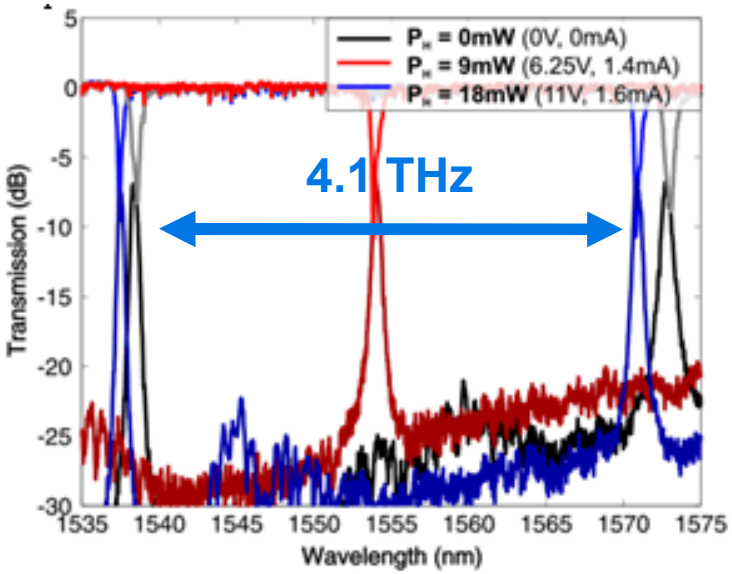
η_H=7μW/GHz

P_δ=280μW
@12.5Gbps=22.4fJ/bit

ΔT=25°C
1.14mW
91.2fJ/bit

Thermal Control - Partial Solution





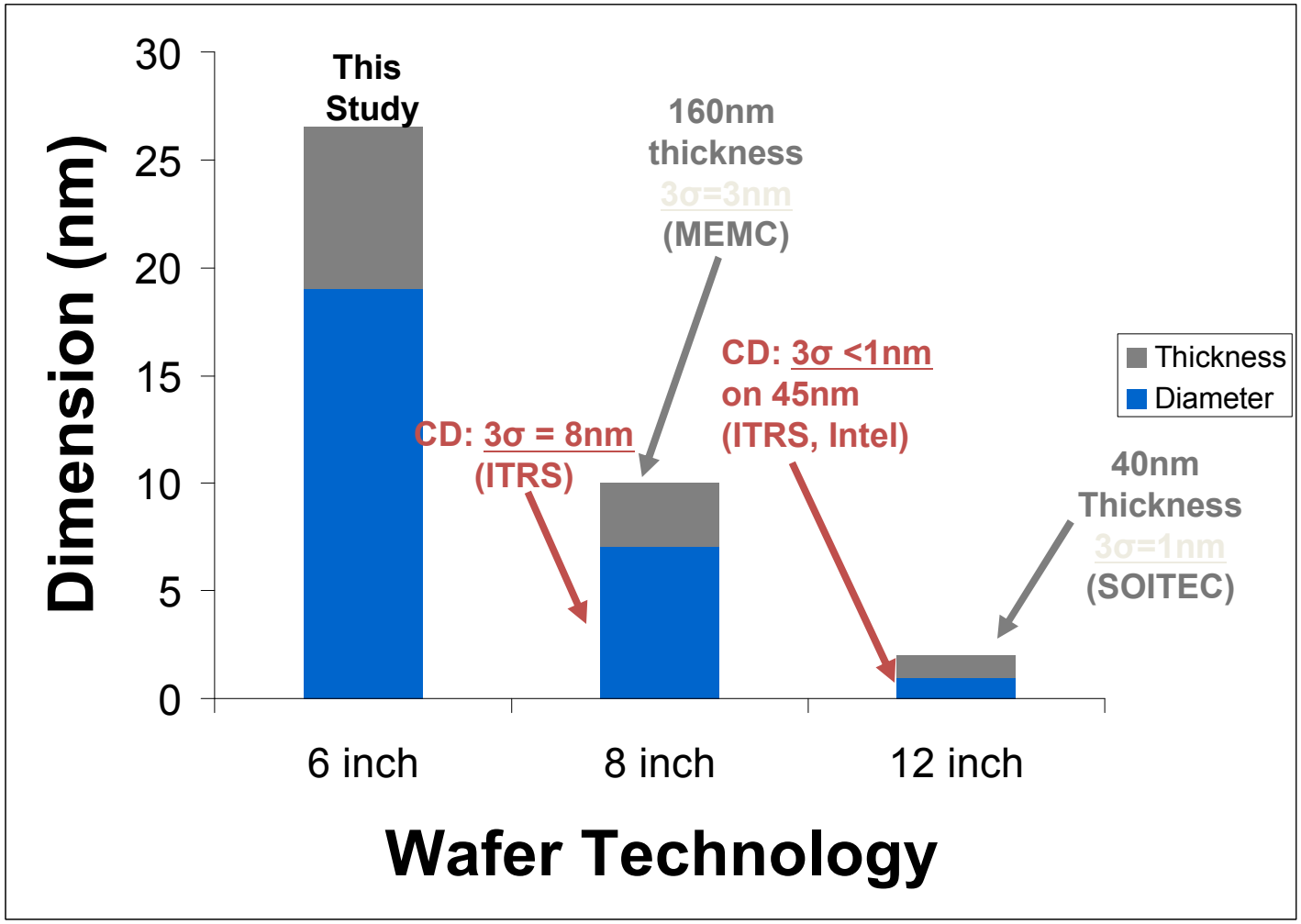
4.4uW/GHZ

At 10Gbs 1THz uses 1pJ/bit

Watts, Zortman et al, CLEO 2009

We prefer a system that is already close to the desired frequency so less tuning (energy) is required. This means limiting process induced variation

Industry Solutions and a Goal



Revisit your energy and bandwidth predictions

To match gate and processor core speeds the silicon industry has improved on the performance of six inch silicon which can be applied to silicon photonics

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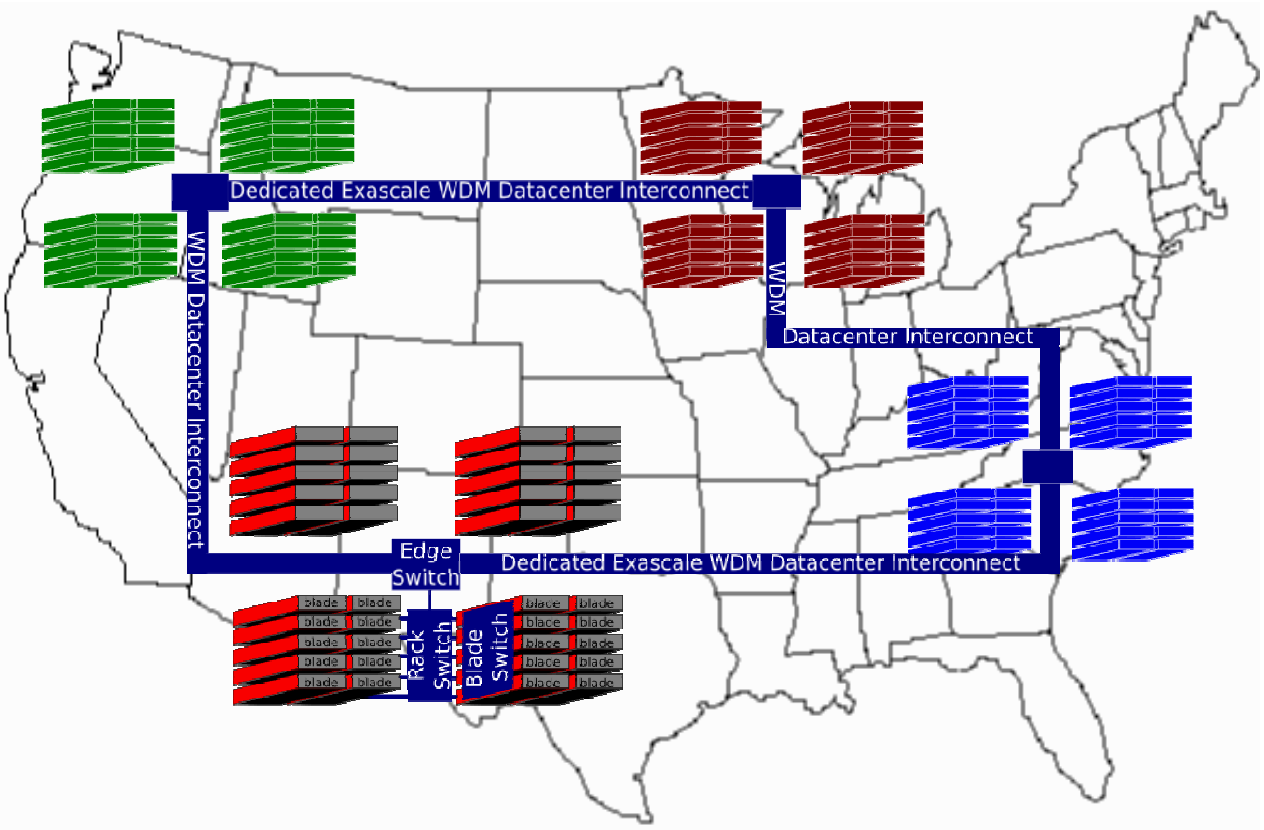
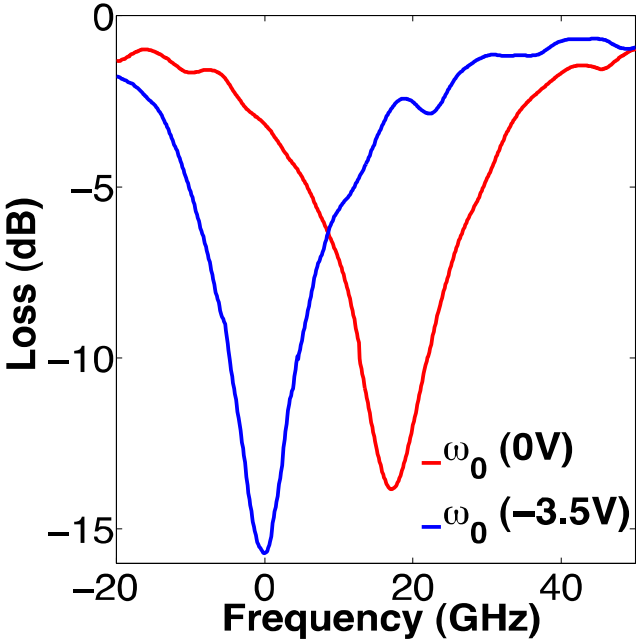
Data center virtualization (long haul)	✔	✔	✔

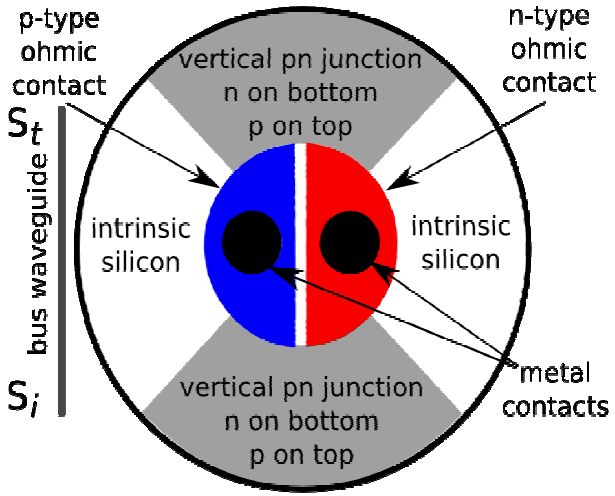
data centers are connected using existing long haul networks

virtualization is a routine server scaling procedure in a data center

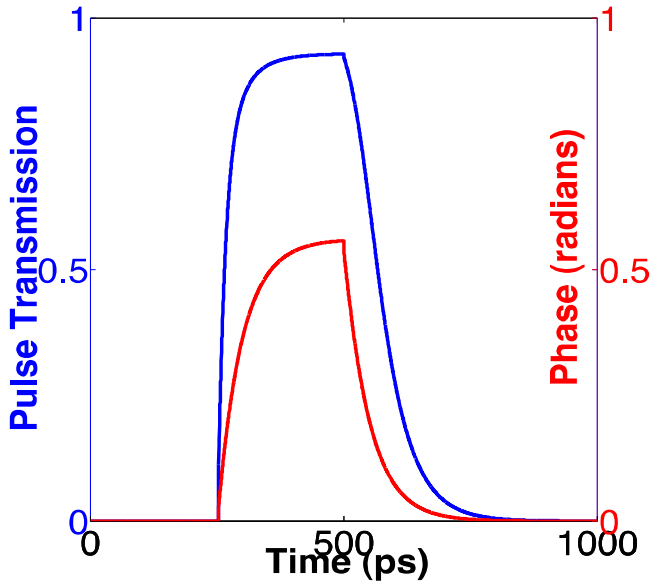


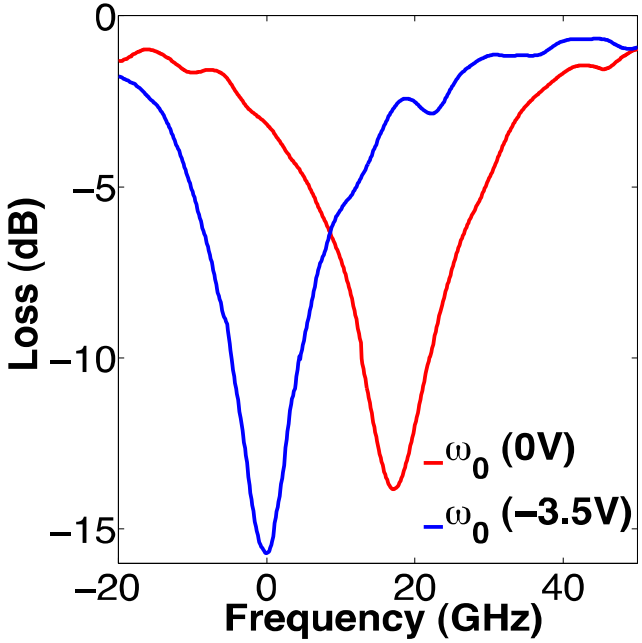
a photonic communication system that can provide low power short haul and long haul interconnect could allow true virtualization across geographies



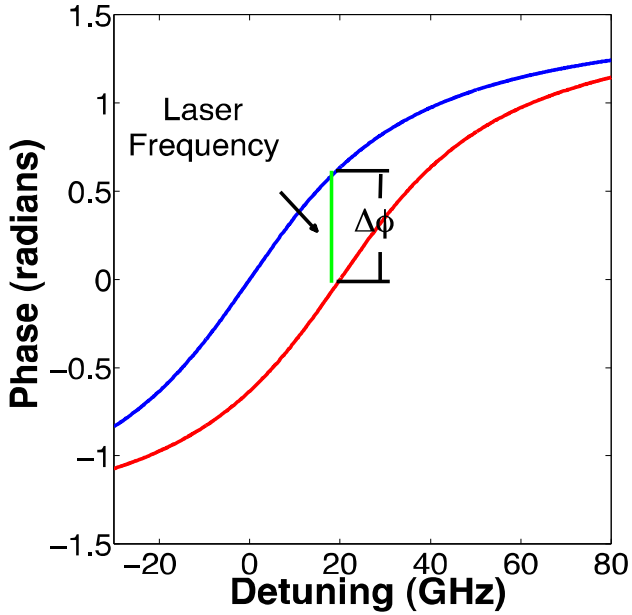


$$s_t = \frac{j(\omega - \omega_0(t))}{j((\omega - \omega_0(t)) + \frac{1}{\tau(t)}} s_i$$

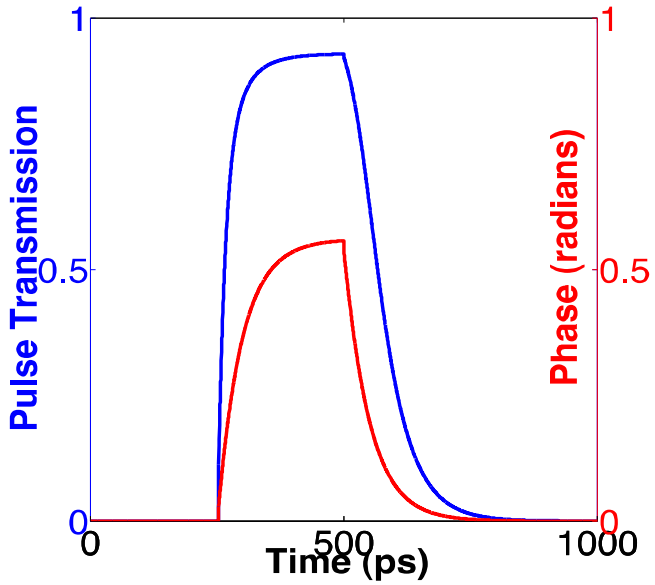




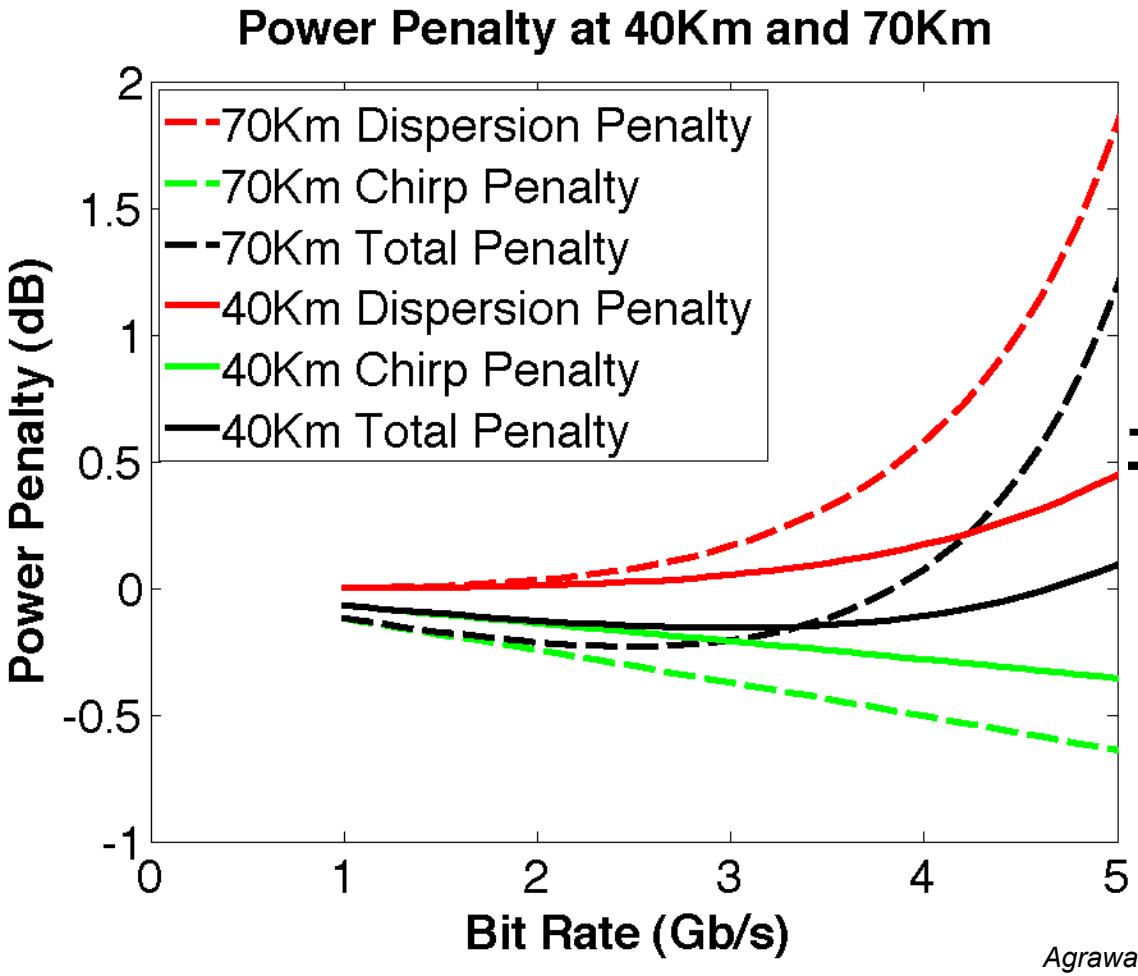
$$s_t = \frac{j(\omega - \omega_0(t))}{j((\omega - \omega_0(t)) + \frac{1}{\tau(t)}} s_i$$



$$\phi = \tan^{-1}\left\{\tau(V)\left[\omega - \omega_0(V)\right]\right\}$$



With normalization over the length of the pulse, the chirp is about 70MHz
Using a basic analysis, a power penalty estimate can be made



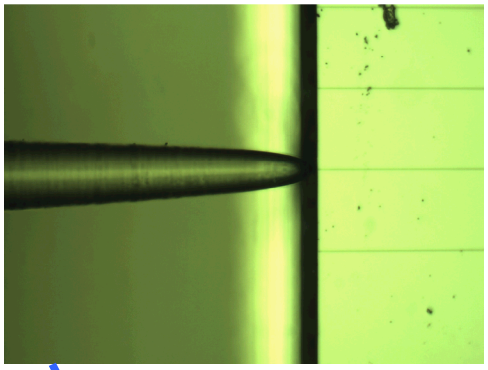
Dispersion $\delta_d = -5\log_{10}\left(1-\left(4BLD\sigma_\lambda\right)^2\right)$

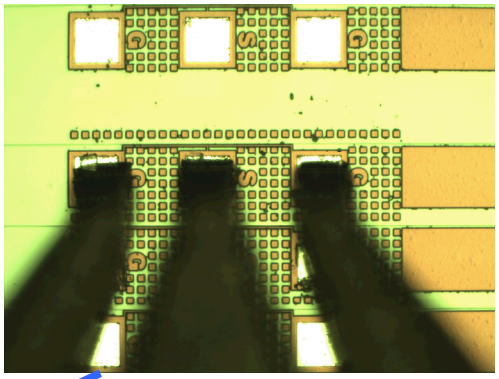
+Chirp $\delta_c = -10\log_{10}\left(1-4BLD\Delta\lambda_c\right)$

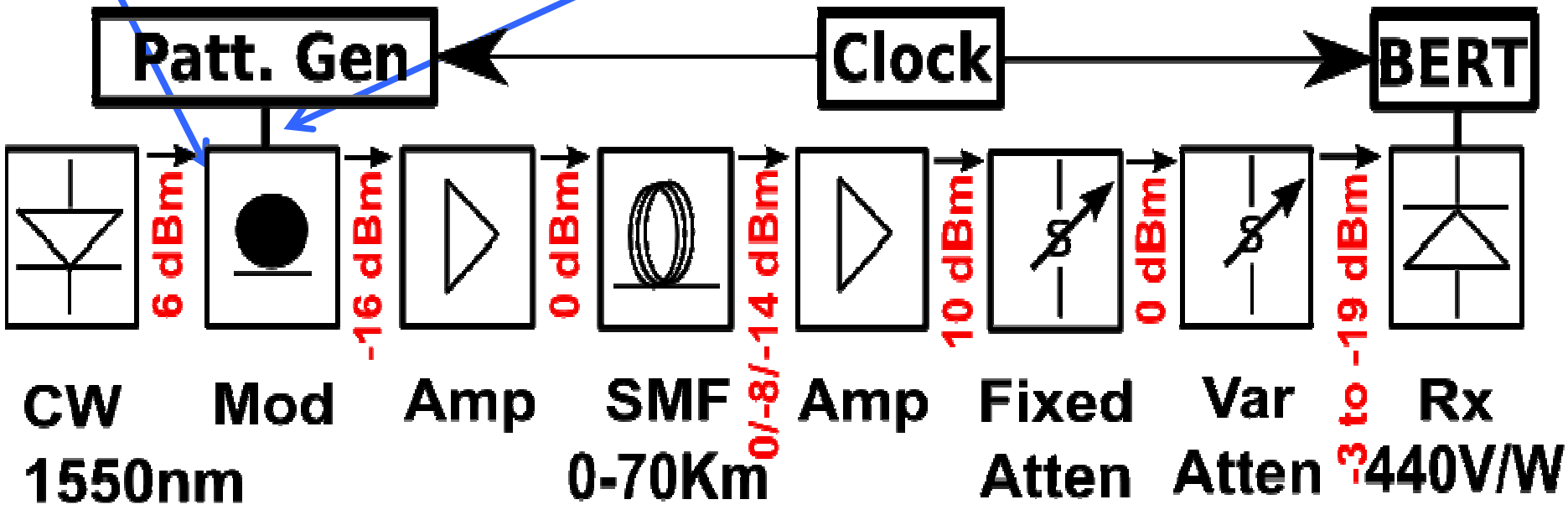
Total Penalty Penalty

Agrawal, G.P., "Fiber Optic Communication Systems" Wiley (2002)

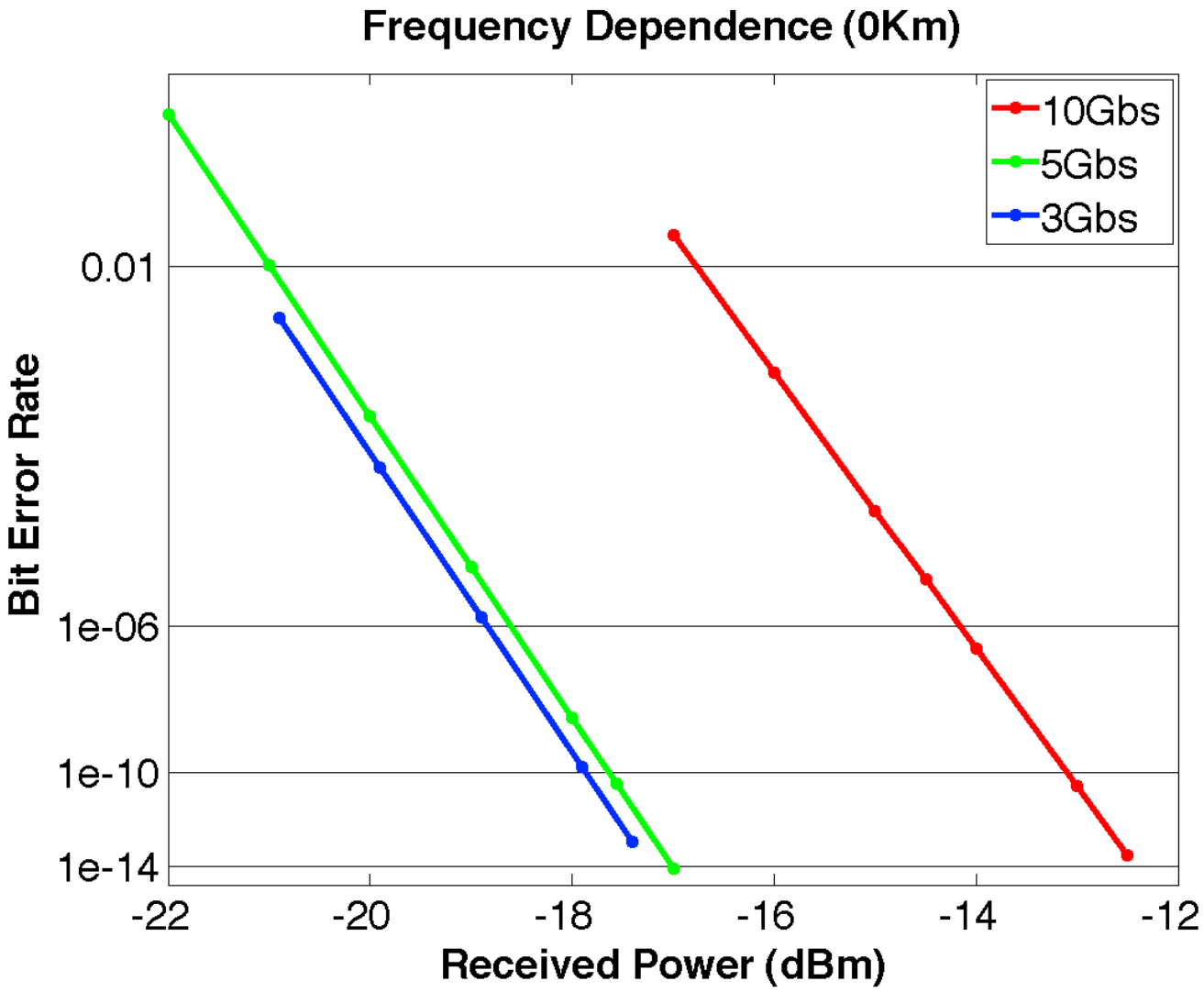
Measurement Setup





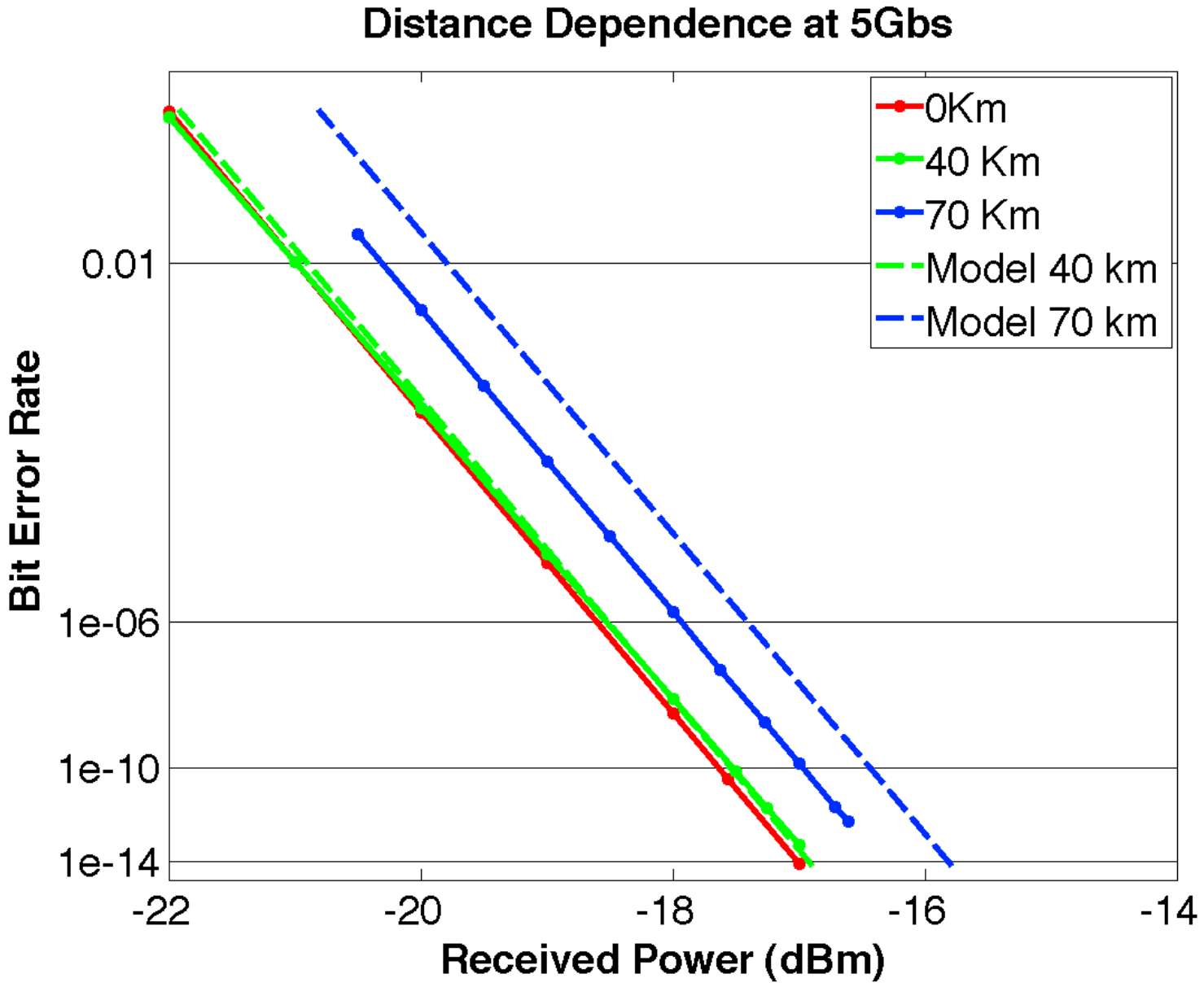


Bandwidth Limitation



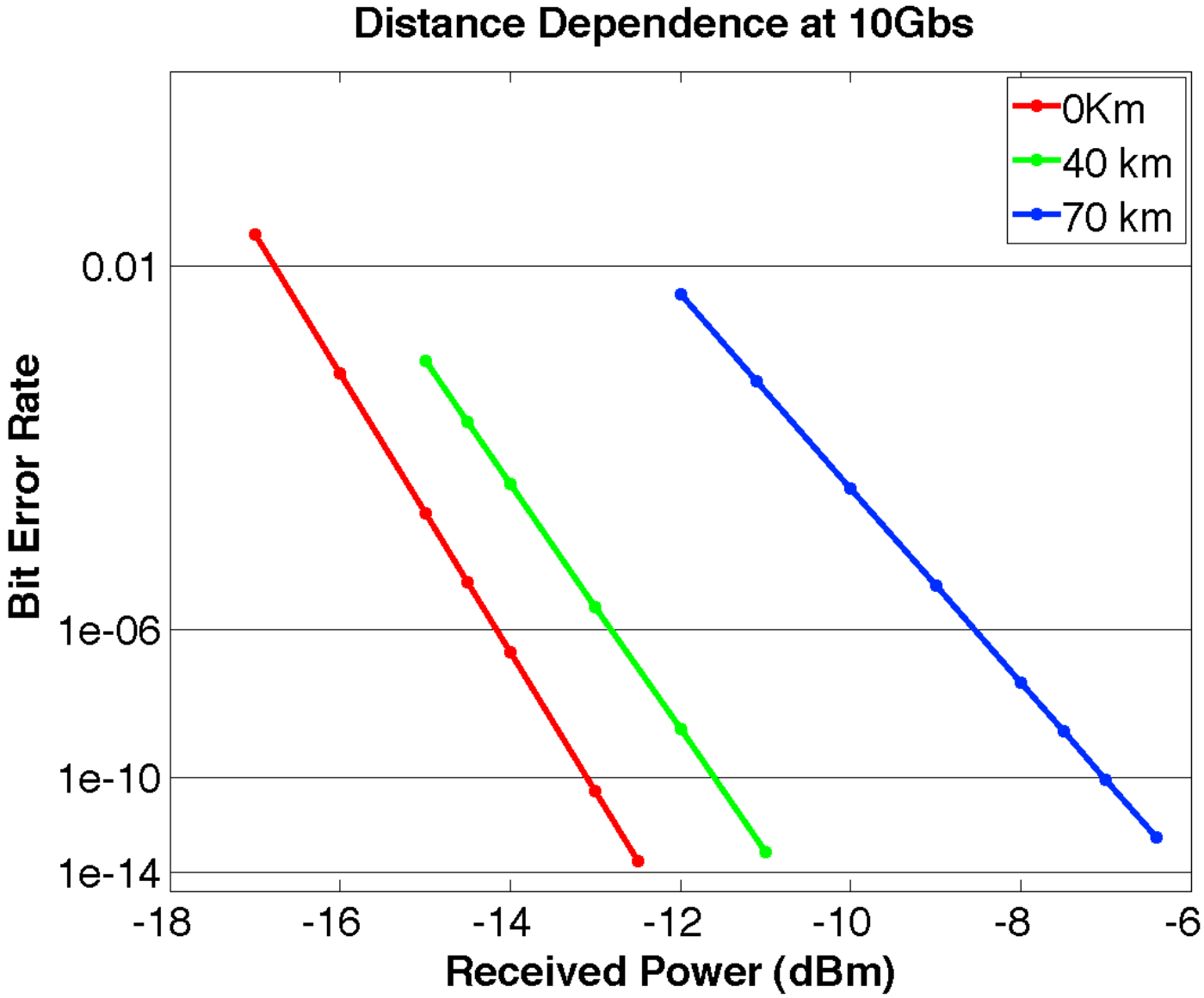
Resonator bandwidth is limited by the contact pad capacitance leading to a power penalty at 10Gb/s even in back to back measurements

Disk Resonator 5Gbs



Negative pulse chirp contributes to the minimal power penalty at 40km

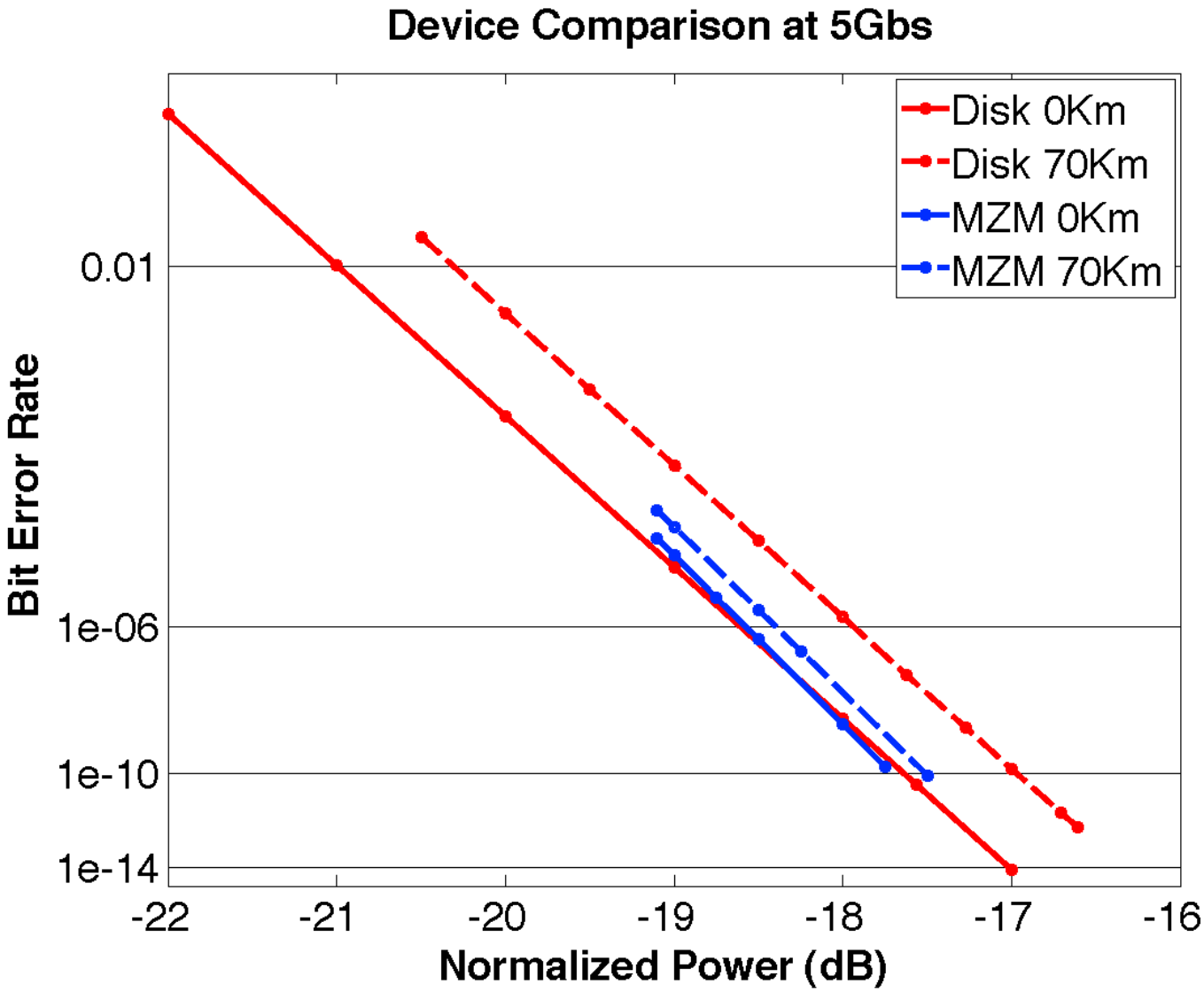
Disk Resonator 10Gbs



The bandwidth limitation exacerbates Inter-Symbol Interference at 10Gbs

Mach Zehnder Modulator Comparison

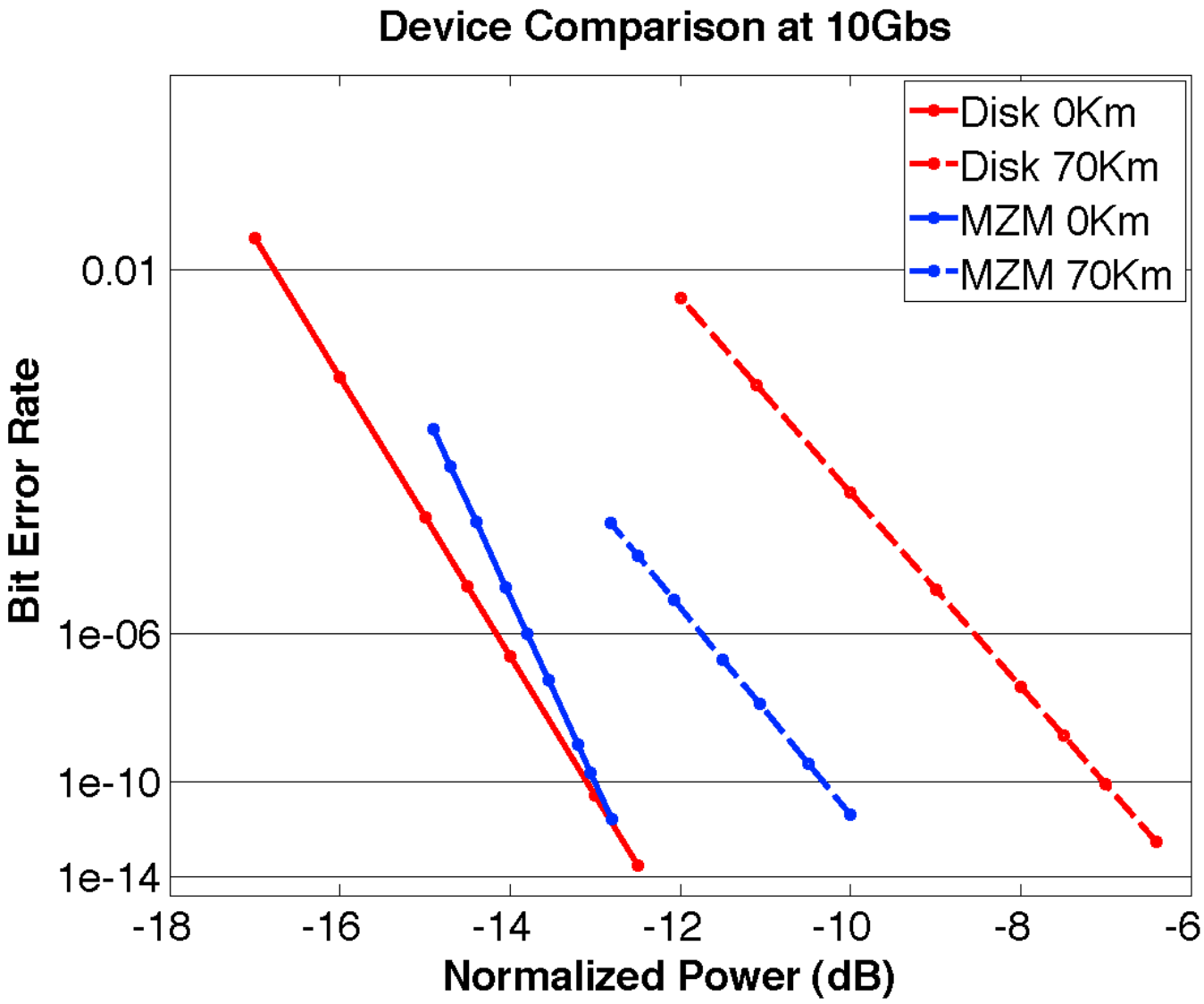
MZM is JDSU $LiNbO_3$ OC-192 $V\pi$=5.8V



The disk resonator is seen as a competitive technology out to 70km

Mach Zehnder Modulator Comparison

MZM is JDSU $LiNbO_3$ OC-192 $V\pi$=5.8V



With elimination of pad capacitance the 10Gbs should improve power penalty

research device attributes for a 2018, 10 TFLOP chip	Dis	Si Photonics	VCSEL
Manufacturing volume to match server chips 1:1	✔	✔	✔
Energy/bit (on chip) (2018 ~100fJ/bit)	✔	**~100fJ/bit**	**~140fJ/bit**
Energy/bit (total)		~150fJ/bit	~140fJ/bit
Low Voltage Compatibility	✔	**(300mV) ✔**	?
Fibers per chip (assume 10Gbps SiP, 100 channels, 5THz)	✔	**2 (WDM)**	**457 (35Gbps)**
Fibers per exascale system	✔	**200 thous.**	**45.7 million**
Integration with TSV		✔	✔★
Monolithic with CMOS (electrical multiplexing)	✔	✔	**?**
Data center virtualization (long haul)	✔	✔	✔

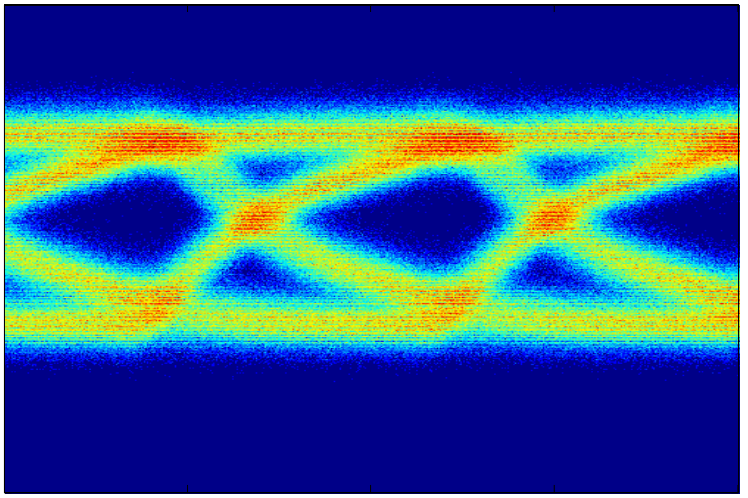
Transmitter to do list:

- method for locking the heater onto the resonance
- low loss fiber attachment

Receiver to do list:

- low capacitance high speed detector
- conversion of I_p to a voltage
- thermally controlled low loss filters

Link 2.5Gbps



Scientific Impact

- World record low energy modulator of any kind
- World record low voltage - same
- Two patent disclosures - vertical pn junction MZM, single mode disk resonator
- Only evaluation of high volume manufacturing in the field of silicon photonics
  Introduction of new high resolution metrology technique
- First demonstration of the long haul capabilities of silicon resonant technology, still the only one with a supporting theoretical model
- Only demonstration of LVS compatibility with silicon resonant technology
- Only 10Gbps modulator with integrated heater

4 Journal Articles, 17 Conference Publications
47 references as of May 2011

Journal Publications

1. **Zortman**, Trotter, Lentine, Robertson, Hsia, Watts, "Integration of Silicon Electronics and Photonics," IEEE Photonics Journal (2011) (in press)
2. **Zortman**, Lentine, Young, Trotter, Watts, "Long Haul Transmission Using Silicon Microdisk Modulators," Photonics Technology Letters (2011)
3. **Zortman**, Trotter, Watts, "Silicon Photonics Manufacturing," Opt. Express **18**, 23598-23607 (2010)
4. Watts, **Zortman**, Trotter, Young, and Lentine, "Low voltage, compact, depletion-mode, silicon Mach-Zehnder modulators" Journal of Selected Topics in Quantum Electronics (JSTQE), Vol. 16 pp 159-164(2010)

Conference Proceedings

1. A. Nejadmalayeri, H. Byun, J. Kim, D. C. Trotter, C. DeRose, A. L. Lentine, **W. A. Zortman**, M. R. Watts, and F. X. Kärtner, “Integrated optical phase-locked loop,” Conference on Lasers and Electro Optics (CLEO) 2011.
2. DeRose, Watts, Young, Trotter, Nielson, **Zortman**, Kekatpure, "Low Power and Broadband 2x2 Silicon Thermo-Optic Switch," IEEE Opitcal Fiber Conference (OFC) (2011)
3. **Zortman**, Lentine, Trotter, Robertson, Watts, "Monolithic Integration of CMOS with Silicon Photonics," SPIE Photonics West, San Francisco, Ca (2011)
4. **Zortman**, Trotter, Lentine, Robertson, Watts, "Integration of Silicon Electronics and Photonics," IEEE Photonics Society Winter Topicals, Keystone, Co January (2011)
5. Li, Breivik, Feng, Lin, Patel, **Zortman**, Crowley, Lester, A low repetition rate all-active monolithic passively mode-locked quantum dot laser, IEEE Photonics Annual Meeting, Denver, Co (2010)
6. Lentine, **Zortman**, Young, DeRose, Trotter, Watts "Silicon Microphotonic Backplane for Focal Plane Array Communications," Oak Ridge National Labs Sensors Workshop (*presenter*) (2010)
7. Shaner, Lentine, Young, Wright, Trotter, **Zortman**, Watts, "Thermal Microphotonic Focal Plane Array," Oak Ridge National Labs Sensors Workshop (*presenter*) (2010)
8. **Zortman**, Watts, Trotter, Young and Lentine, "Low-Power High-Speed Silicon Microdisk Modulators," OSA Conference on Lasers and Electro Optics (CLEO), San Jose, Ca. (2010)
9. **Zortman**, Lentine, Watts and Trotter, "Power Penalty Measurement and Frequency Chirp Extraction in Silicon Microdisk Resonator Modulators," (OFC), San Diego, Ca (2010)
10. **Zortman**, Watts and Trotter, "Determination of Wafer and Process Induced Resonant Frequency Variation in Silicon Microdisk-Resonators," OSA International Photononics and Nanophotonics Research and Applications, Honolulu, Hi(2009)
11. Watts, **Zortman**, Trotter, Young, and Lentine, "Low-Voltage, Vertical-Junction, Depletion-Mode, Silicon Mach-Zehnder Modulator with Complementary Outputs" IPNRA, Honolulu, Hi (2009) (PDPC) **(postdeadline)**
12. Watts, Lentine, Trotter, **Zortman**, Young, Campbell, and Shinde, "Low Power Silicon Microphotonics for Embedded Systems" Lexington, Ma (2009) **(invited)**
13. Watts, **Zortman**, Trotter, Nielson, Luck, Young, Adiabatic Resonant Microrings (ARMs) with Directly Integrated Thermal Microphotonics," OSA CLEO, San Jose, Ca (2009) **(postdeadline)**
14. **Zortman**, Trotter, Watts, "Analytical energy and bandwidth model for compact silicon photonic microdisk resonators," IEEE High Speed Interconnects Santa Fe, NM (2009)
15. Watts, Shaw, Rakich, Lentine, Nielson, Wright, **Zortman**, and McCormick, "Microphotonic Thermal Detectors and Imagers" SPIE, San Jose (2009) **(invited)**
16. Watts, Trotter, Young, Lentine, and **Zortman**, "Limits to Silicon Modulator Bandwidth and Power Consumption" SPIE, San Jose (2009**) (invited)**
17. Watts, Kim, Kaertner, Lentine, and **Zortman**, "Towards an Integrated Optic Phase-Locked Oscillator" 40th Annual Precise Time and Time Interval (PTTI) Meeting, Reston, Va (2008) **(invited)**

Doctoral Committee

Professor Luke F. Lester

CHTM | Center for High Technology Materials

Professor Michael R. Watts

rle AT MIT RESEARCH LABORATORY OF ELECTRONICS AT MIT

Professor (A) Anthony L. Lentine

Sandia National Laboratories

Professor Mani Hossein-Zadeh

CHTM | Center for High Technology Materials

Professor Nasir Ghani

UNM | Electrical & Computer Engineering

UNM | Electrical & Computer Engineering

CHTM | Center for High Technology Materials

Design and Integration of Discrete Components for Low Energy WDM Silicon Photonics on CMOS Systems

rle AT MIT RESEARCH LABORATORY OF ELECTRONICS AT MIT

MIT

Sandia National Laboratories

DARPA

NNSA National Nuclear Security Administration

LORD

QUESTIONS

BACKUP

Conclusions

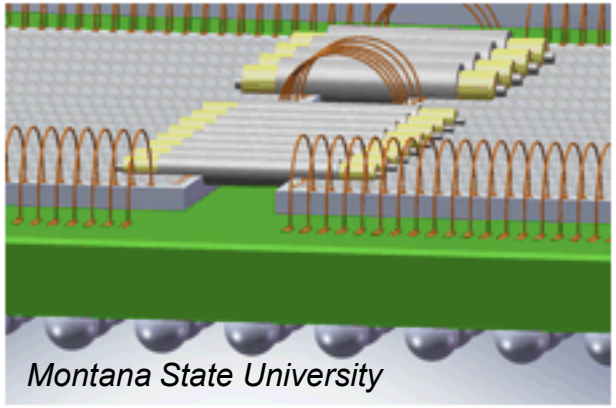
We modeled and measured the dispersion penalty of a Si Photonic Disk resonator

The negative chirp of the output pulse allows for zero power penalty at 40 km

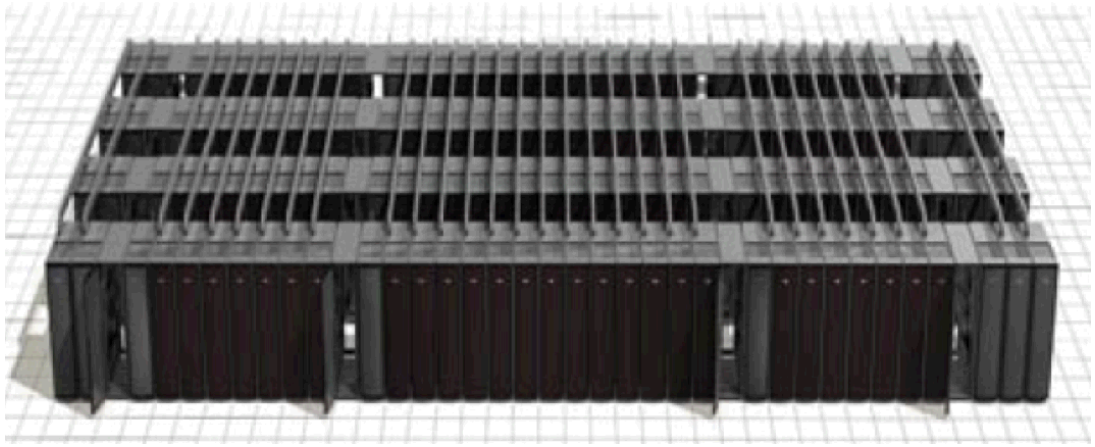
The performance is competitive for long distance at 5Gb/s indicating that if the pad capacitance is reduced or eliminated 10Gb/s should be competitive as well

Motivation and Requirements

Chip to Chip/Board to Board



Supercomputing

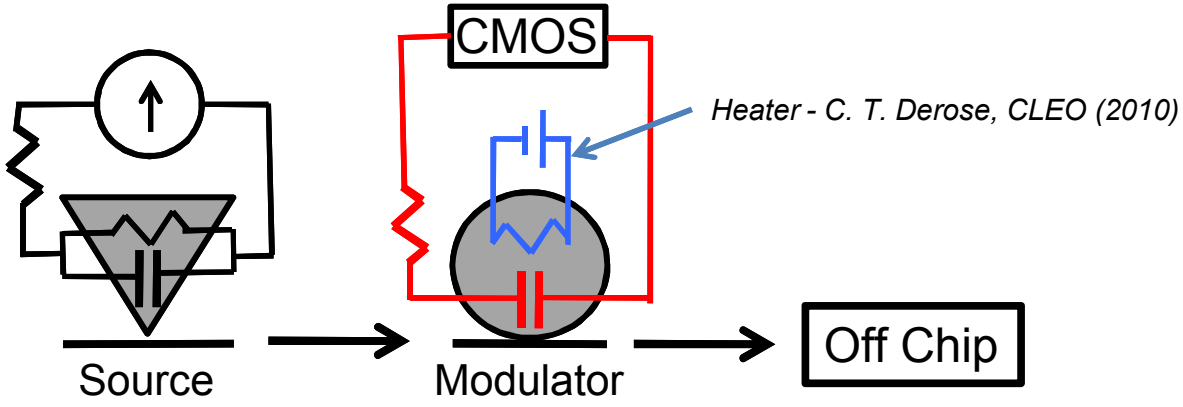


2015 off chip bandwidth forecast

D.A.B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips" Proceedings of the IEEE Vol 97 No 7 (2009)

Maintaining 1byte/flop on a 200W chip leaves only 97fJ/bit for the transmitter

→10fJ/bit in 2022

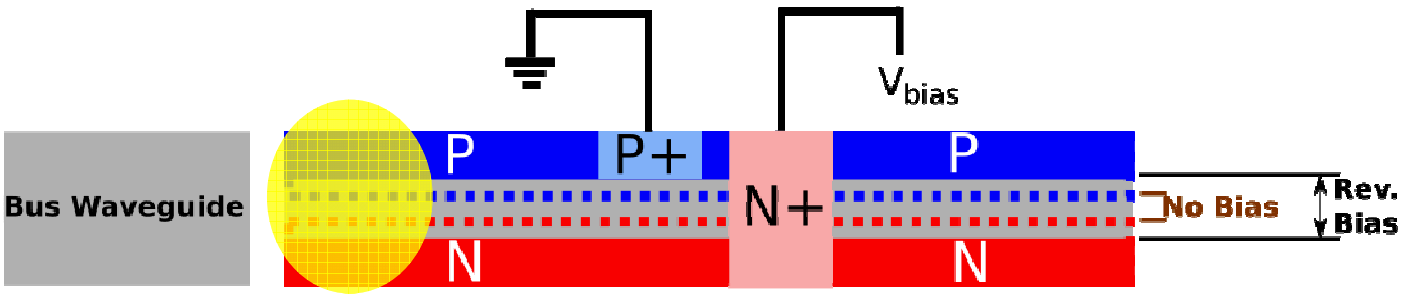


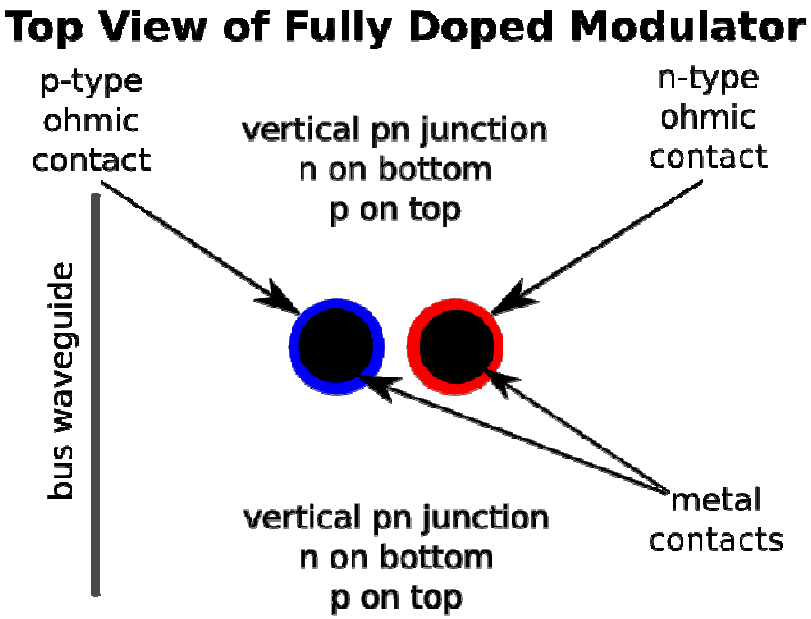
Zortman cleo 2010

Our focus here is the electrical energy/bit (E_{bit}) consumed driving the modulator

Disk Resonator Design

Depletion Mode Vertical PN Junction

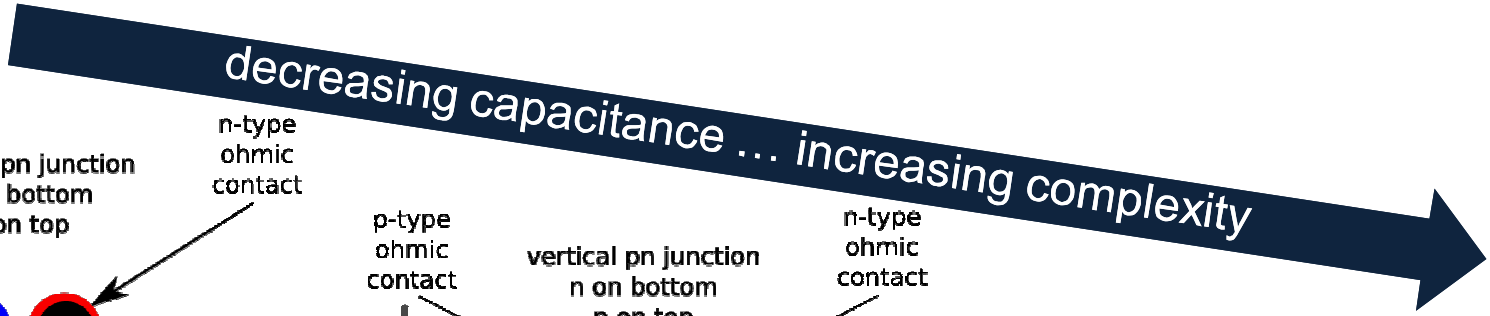


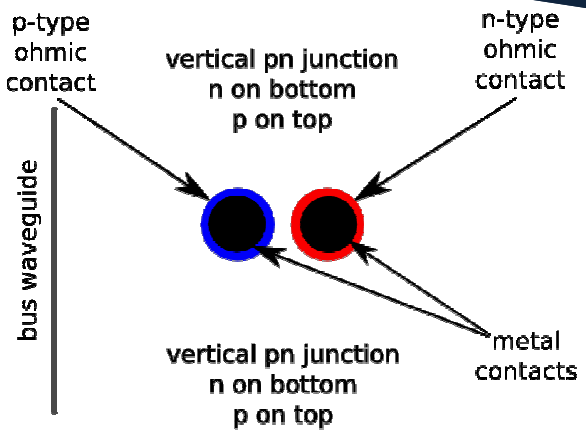


Zortman cleo 2010

Reverse bias enabled expansion of the depletion region sweeps out carriers and changes the refractive index via the plasma carrier dispersion effect

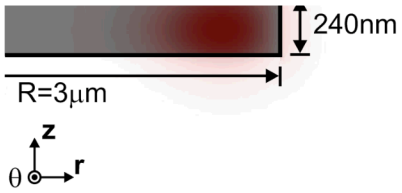
Disk Resonator Design Progression

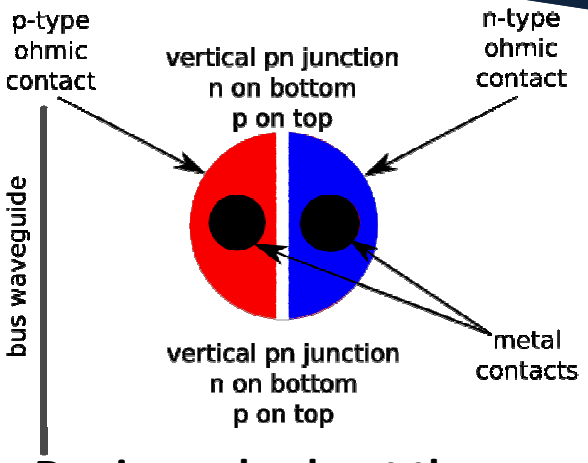




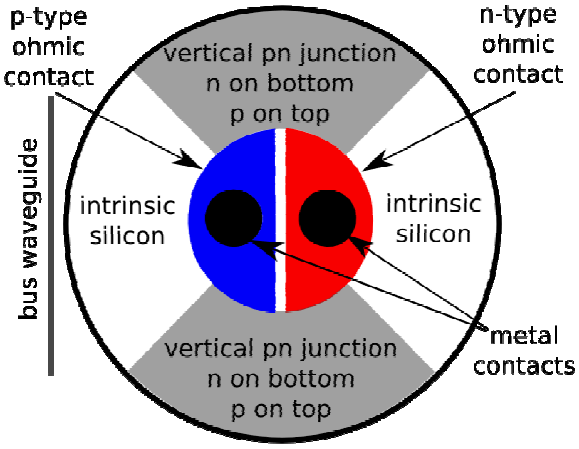
Blanket doping is inefficient considering a whispering gallery mode.

Watts et al, Group IV (2008)





Doping only about the periphery where the mode lives results in
Lower capacitance
Lower energy… Lower BW
Electrically – A ring
Optically – A disk
*See **Watts et al, CLEO 2009***
*and **Derose et al, CLEO 2010***

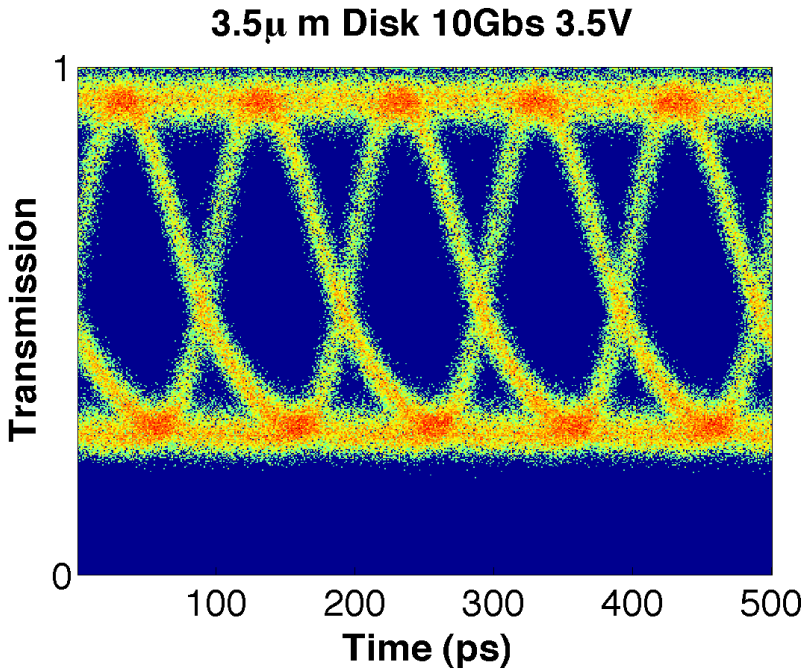


… to limiting **doping at π radians** resulting in even **lower** ***R* and *C* and a 12Gb/s disk**
This also results in a decrease in the mode-depletion interaction length, L, (higher E_{bit})

Zortman cleo 2010

The result of design iteration has been to reduce the energy and increase BW

Silicon Photonics



Disk Resonator

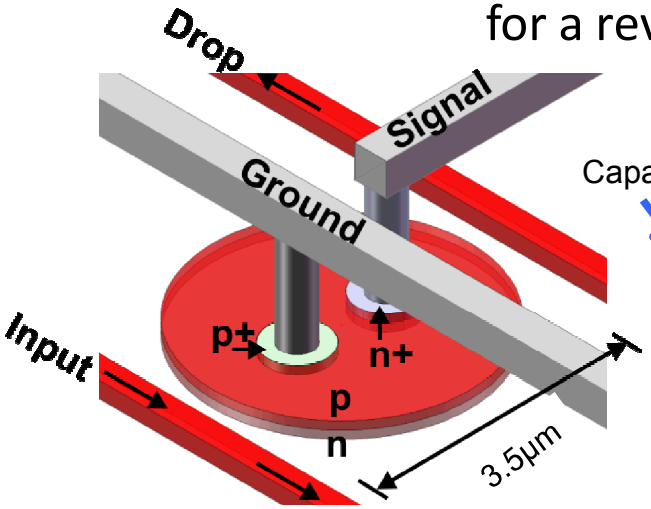
Dense Integration of filters, modulators and detectors on CMOS

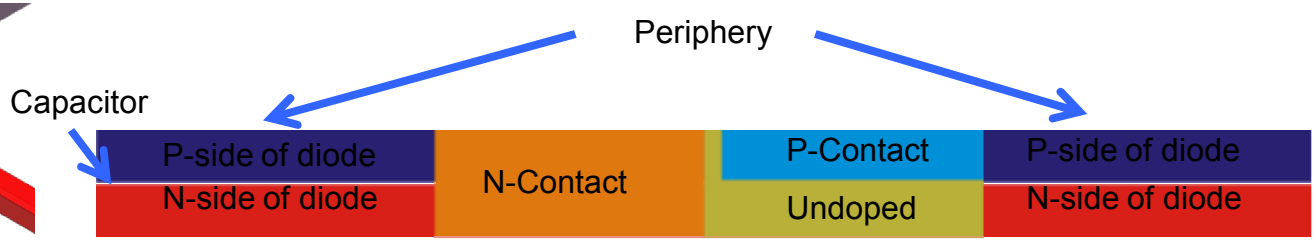
The potential to integrate complex functions consisting of many devices

Waveguide coupled resonators in silicon offer the potential to create low energy/bit scalable arrays of interconnects on a silicon platform

Resonance Sweep

for a reverse biased pn junction modulator





When viewed from the side, the disk is a capacitor

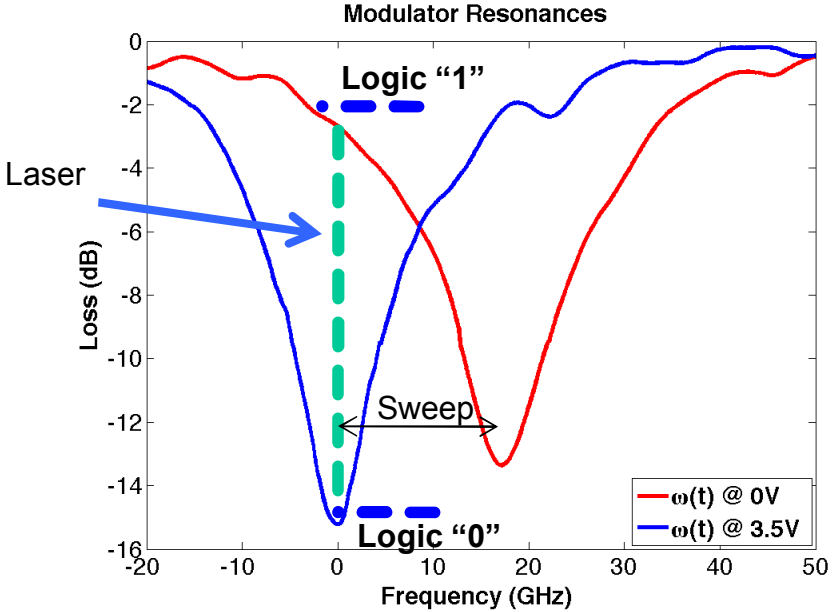
The amplitude of the wave in the disk:

$$\frac{da}{dt} = a_0\left(j\omega_0(t) - \frac{1}{\tau(t)}\right)$$

where τ and ω_0 are functions of time

$$\omega_0(t) = f\left(\exp\left(-\frac{t}{\tau_e}\right)\right) \quad \tau(t) = f\left(\exp\left(-\frac{t}{\tau_e}\right)\right)$$

Amplitude Modulation



Little, et al, Microring Resonator Channel Dropping Filters, JLT, Vol. 15 No. 6 (1997)

Overview

Motivation

Low power designs for off chip links

Disk Design

Optimization of mode interaction with PN junction

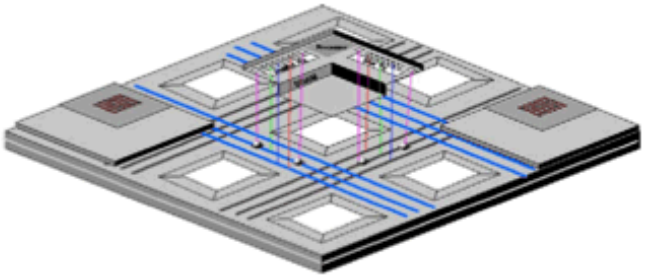
Performance

We demonstrate 3.2fJ/bit at 12.5Gb/s

Ideas for reducing E_{bit} further

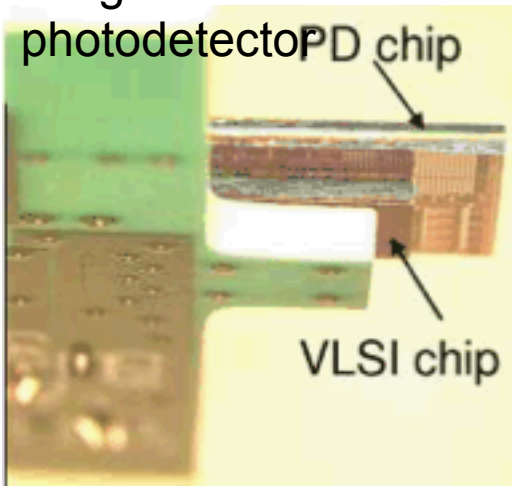
Photonic Integration – Very Active Area

Oracle/Luxtera/Kotura
Macrochip



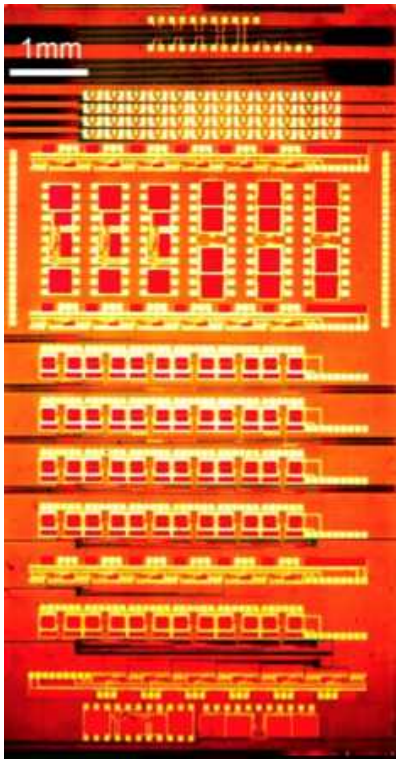
Krishnamoorthy et al Proc IEEE July 2009

CMOS integrated photodetector



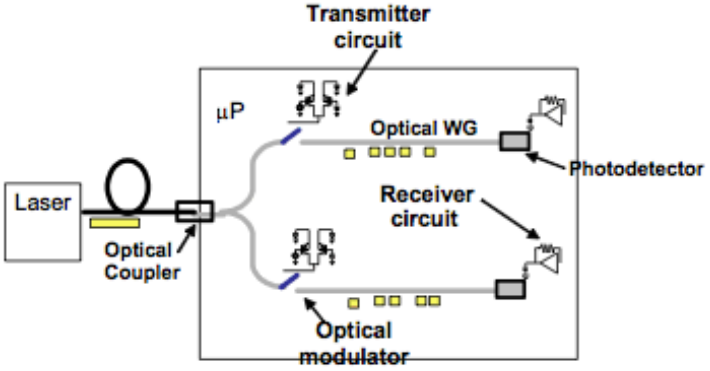
Zhen et al OPEX Dec 2009

IBM
Multichannel CMOS integrated modulators and detector



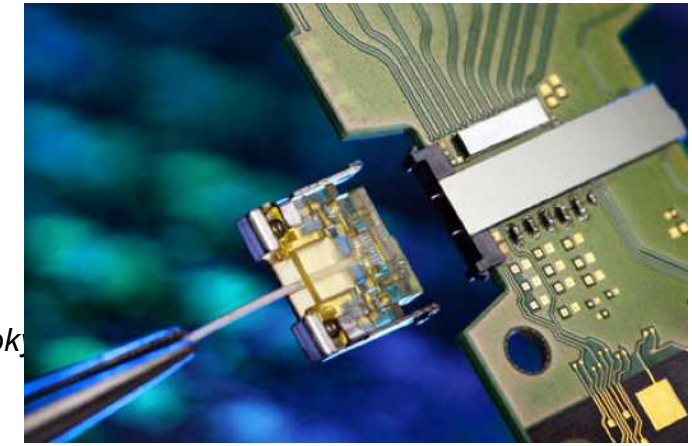
Green et al SEMICON 2010 Tok

Intel
On chip interconnect



Kobrinsky et al Intel Technology Journal 2004

Integrated transceivers



IPR Intel Press Release July 2010 Monterrey

Power Penalty Measurement and Frequency Chirp Extraction in Silicon Microdisk Resonator Modulators

•William A. Zortman, Anthony L. Lentine, Michael R. Watts
•and Douglas C. Trotter
•(UNM Advisor: Luke F. Lester)

•Sandia National Labs Albuquerque, NM
•Applied Photonic Microsystems

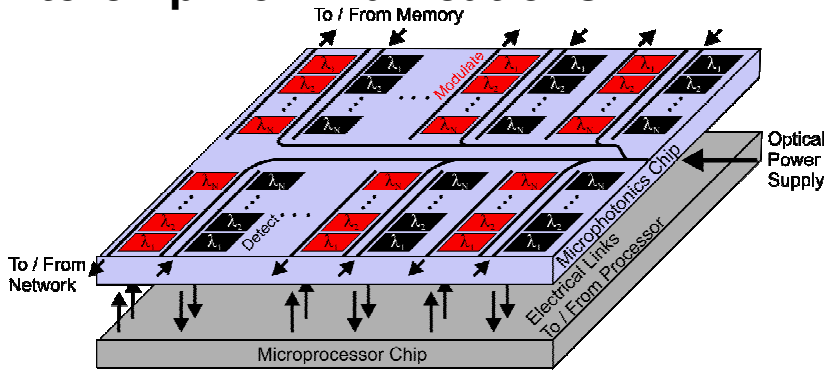
Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company,
for the United States Department of Energy's National Nuclear Security Administration
under contract DE-AC04-94AL85000

NNSA National Nuclear Security Administration
LORD
THE UNIVERSITY of NEW MEXICO
CHTM
Sandia National Laboratories

Motivation: Large Arrays of Resonators

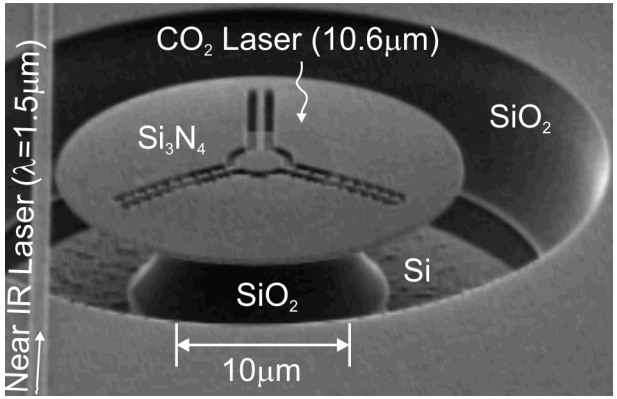
Filters, Modulators, Sensors

Interchip Communications

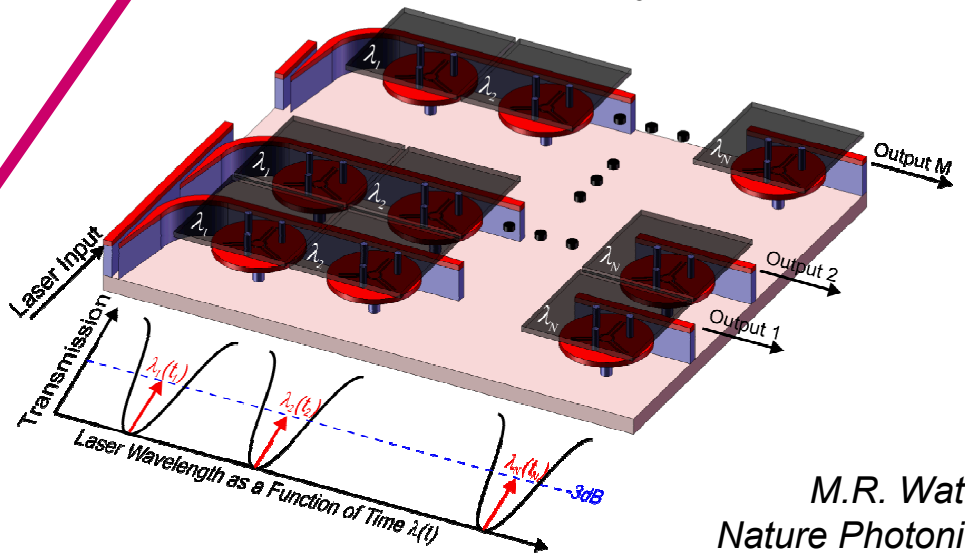


… for servers/datacenters

IR Sensitive Disks



… for focal plane arrays

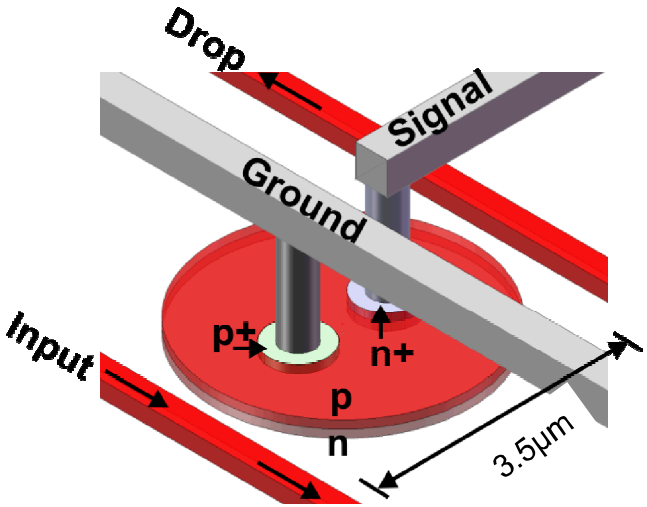


M.R. Watts et al, Nature Photonics 2007

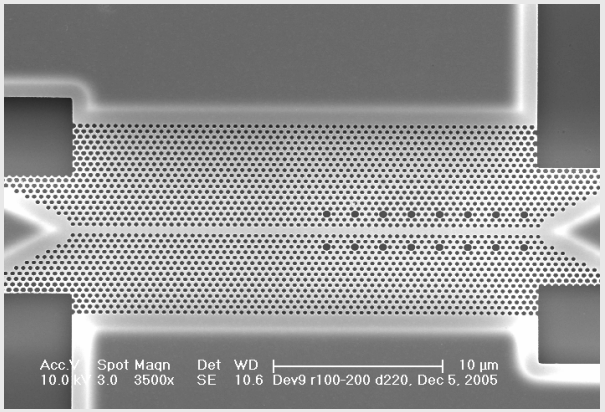
Process non-uniformity leads to frequency variation across wafers inhibiting applications requiring large arrays of resonators

Silicon Photonics

Disk Resonator

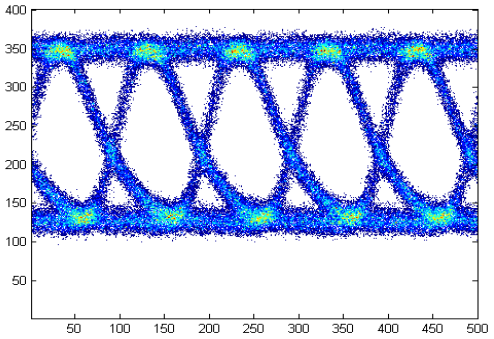


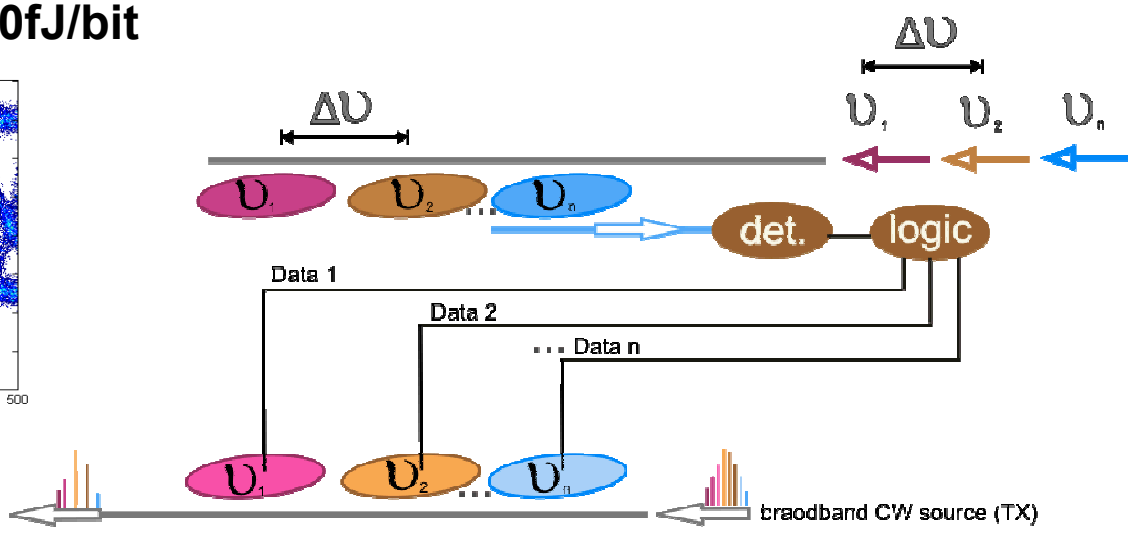
Photonic Crystal



Ndi et al, Optics Express 2006

10Gbs, 10^{-13}BER, E<100fJ/bit





Waveguide coupled resonators in silicon offer the potential to create low energy/bit scalable arrays of CMOS interconnects

Summary

Modulation optimization and efficient junction design

3.2fJ/bit

12.5Gb/s (limited by pads and test equipment)

3.7dB Power Penalty

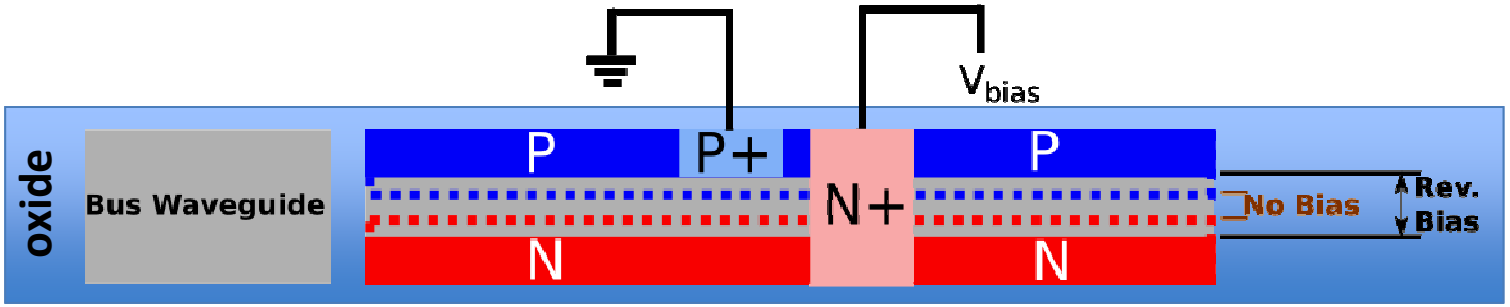
Questions?

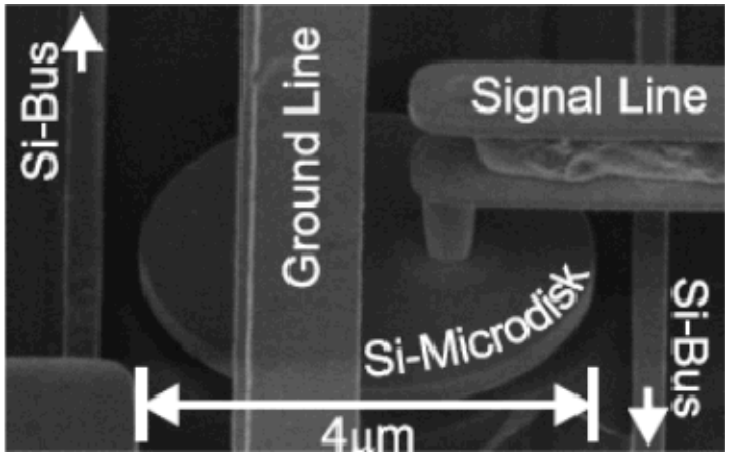
Sandia National Labs Albuquerque, NM
Applied Photonic Microsystems

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company,
for the United States Department of Energy's National Nuclear Security Administration
under contract DE-AC04-94AL85000

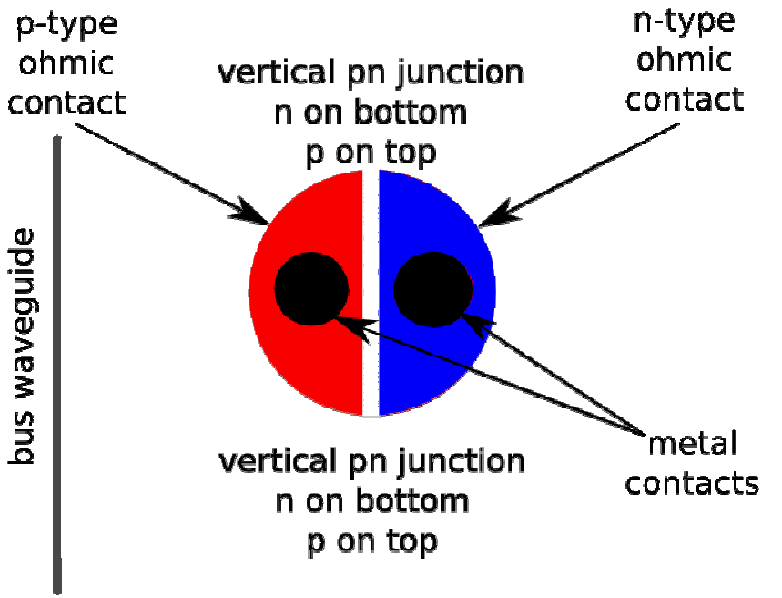
The Integrated Device

Depletion Mode Vertical PN Junction built on Silicon on Insulator



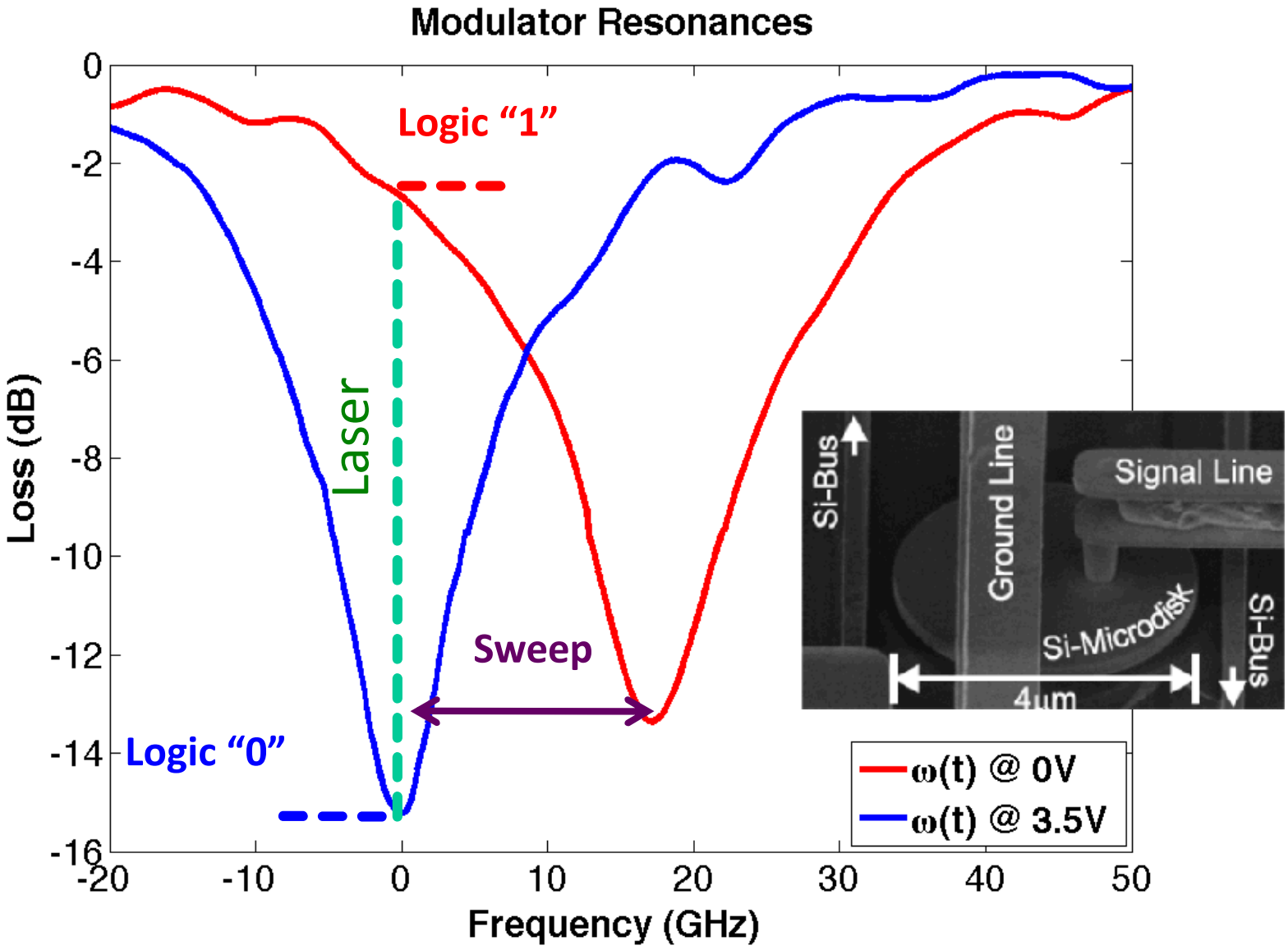


Top View of Fully Doped Modulator



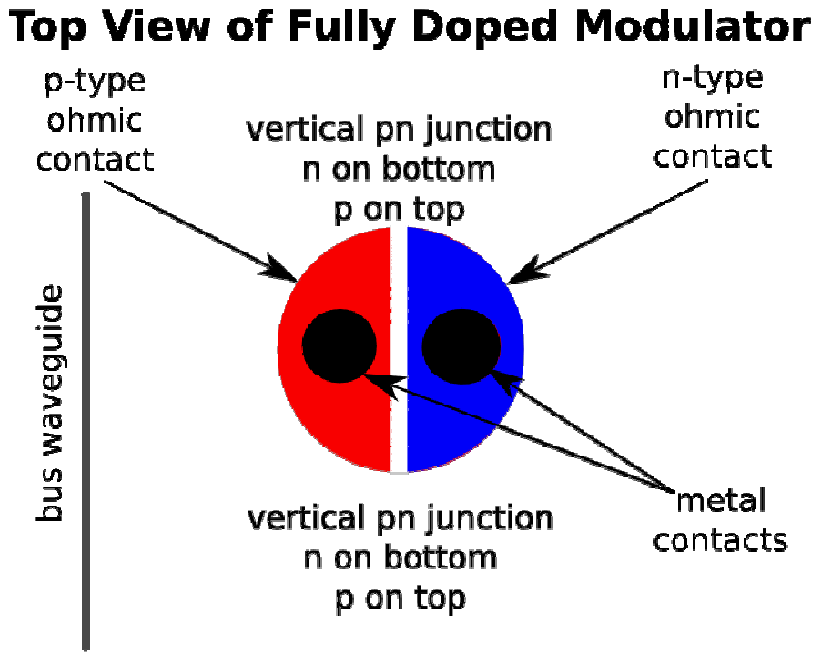
Reverse bias enabled expansion of the depletion region sweeps out carriers and changes the refractive index via the plasma carrier dispersion effect

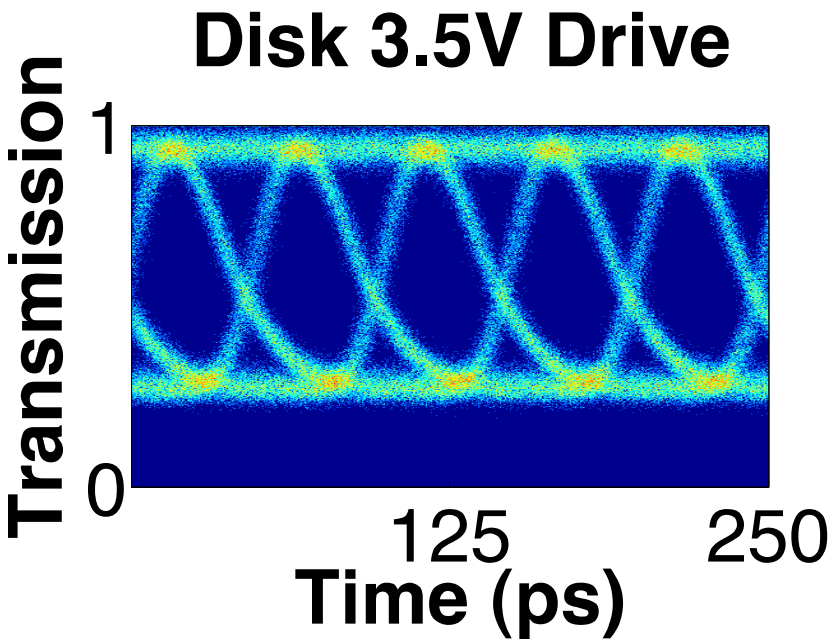
Reverse Bias Modulation Action



Resonator Integrated with CMOS

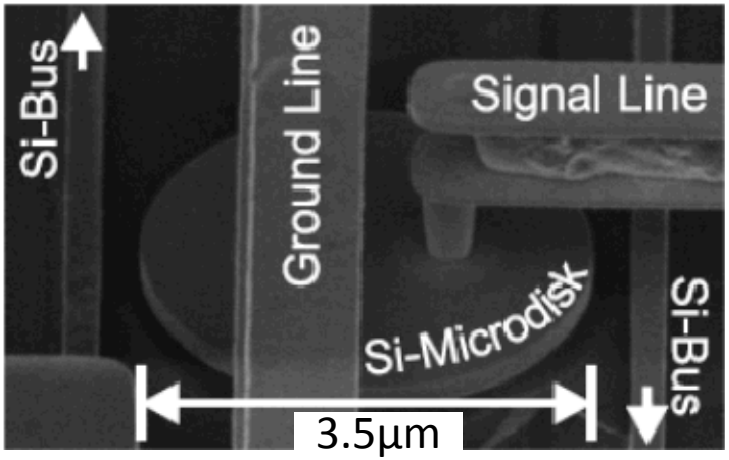
10Gbps

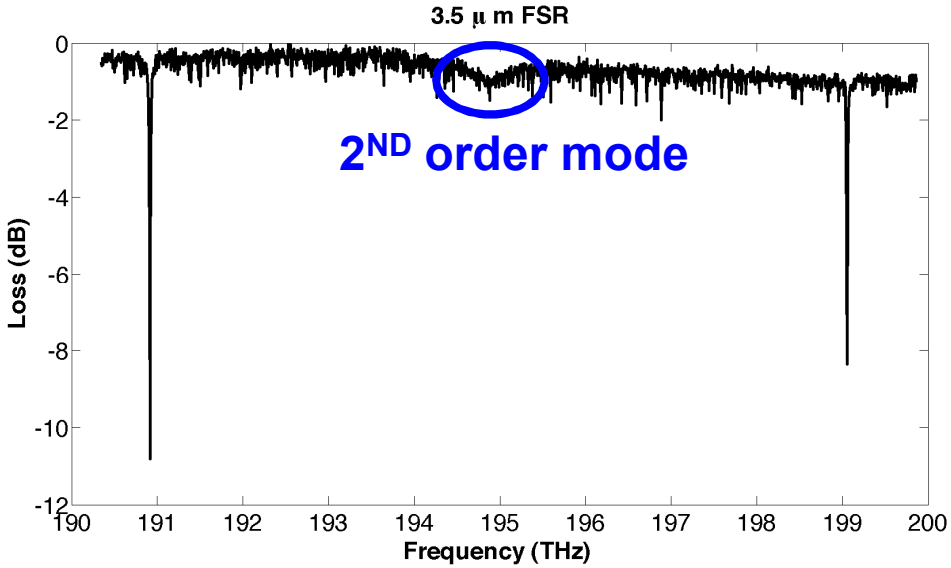




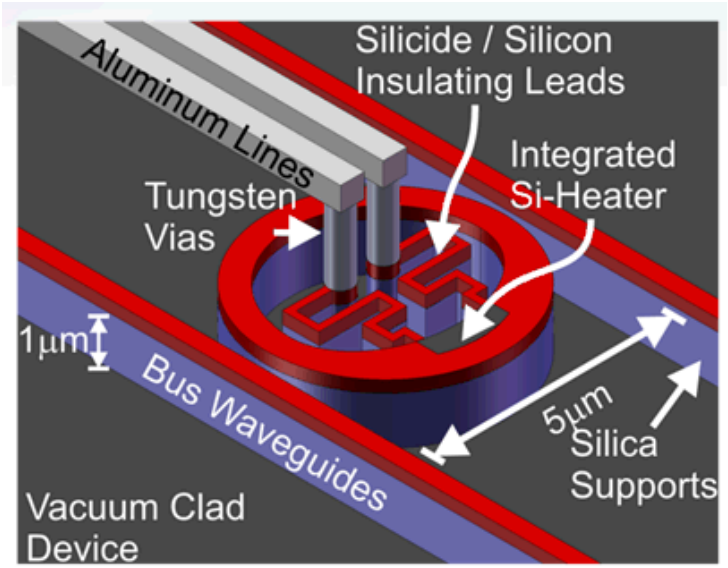
Disks and Rings

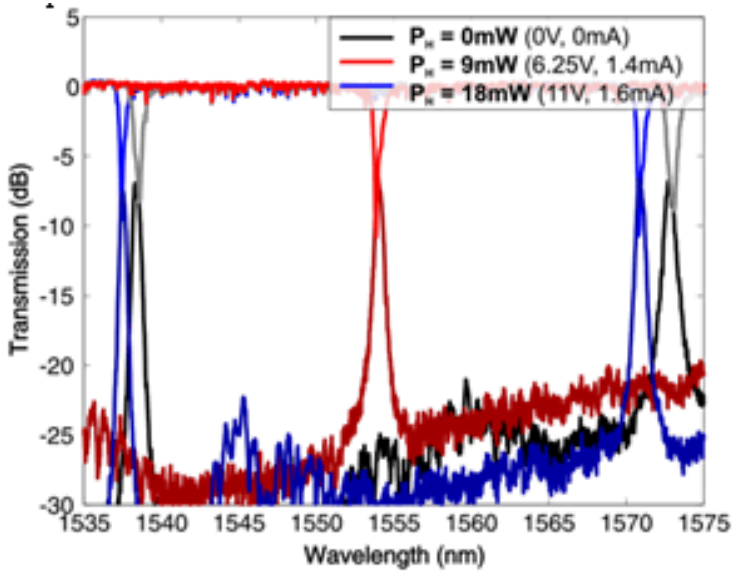
DISK





ARM



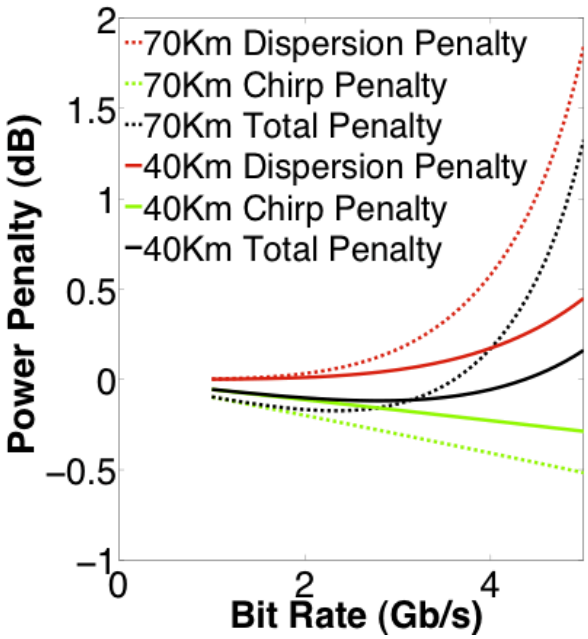


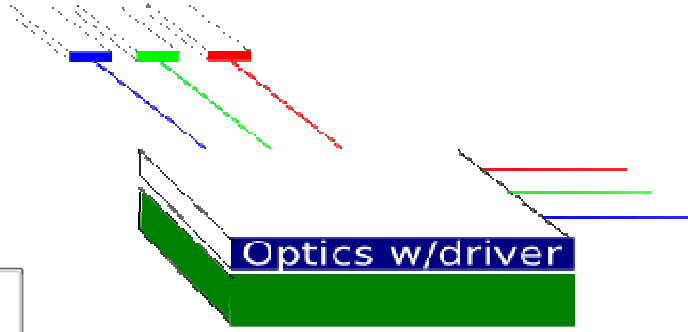
Watts et al, "Adiabatic Resonant Microrings" CLEO 2009

Zortman cleo 2010

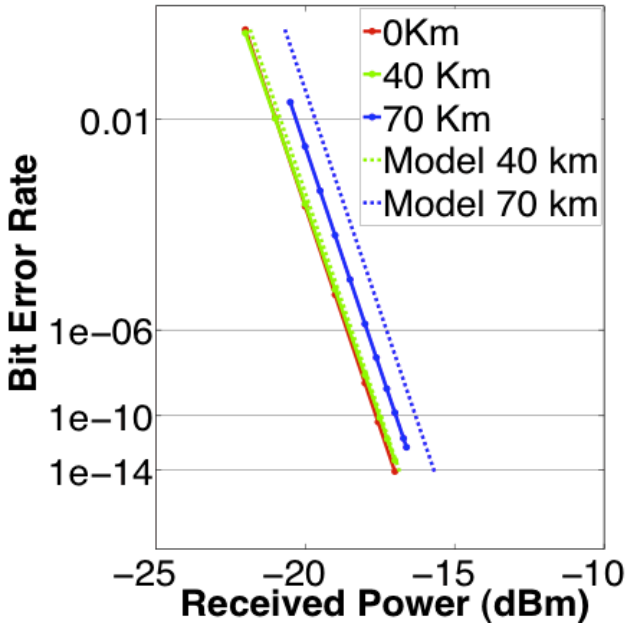
Long Haul Performance

Modeling

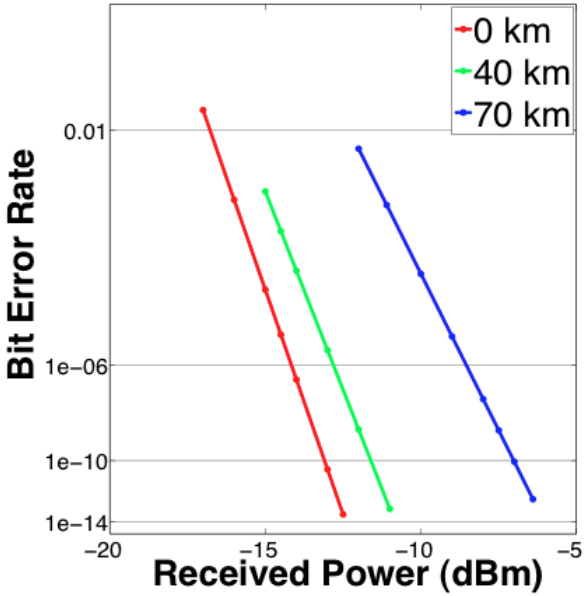




5 Gbps



10 Gbps



WA Zortman, AL Lentine et al OFC San Diego (2010)

Silicon Photonic Resonator Integration with CMOS Electronics

platform for manufacturing of integrated parts

William A. Zortman, Douglas C. Trotter, Anthony L. Lentine, Gideon Robertson, Alex Hsia, Michael R. Watts*
wzortm@sandia.gov

Sandia National Labs Albuquerque, NM
Applied Photonic Microsystems
*Massachusetts Institute of Technology
Research Laboratory of Electronics

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000

Determination Of Wafer And Process Induced Resonant Frequency Variation In Silicon Microdisk-Resonators

•William A. Zortman, Michael R. Watts and Douglas C. Trotter
•(UNM Advisor: Luke F. Lester)

•Sandia National Labs Albuquerque, NM
•Applied Photonic Microsystems

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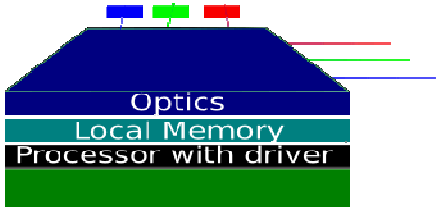
NNSA National Nuclear Security Administration | LDRD | THE UNIVERSITY of NEW MEXICO | CHTM | Sandia National Laboratories

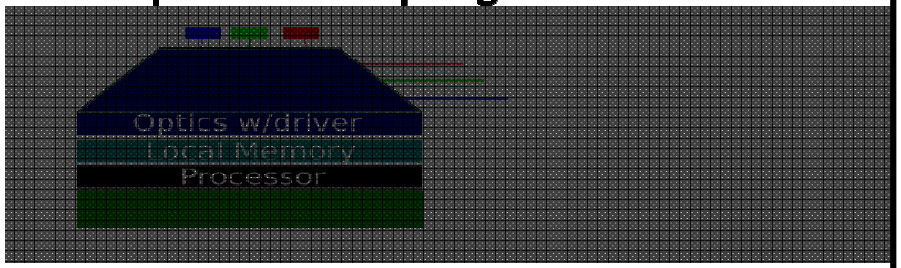
Two Demonstrations

Wire Bonded

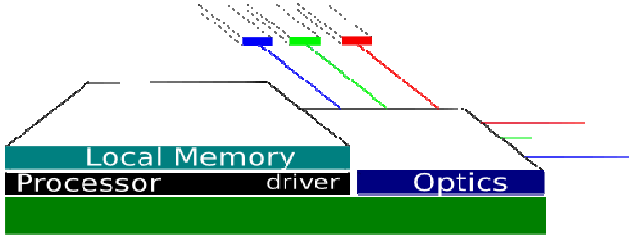
Monolithic

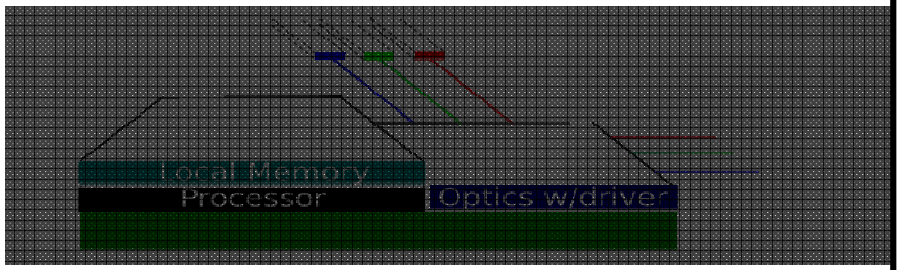
Potential 3D Integration Utilizing TSV or Capacitive Coupling



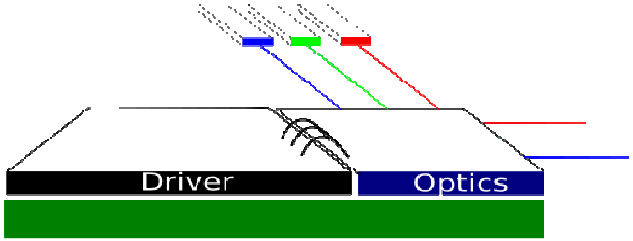


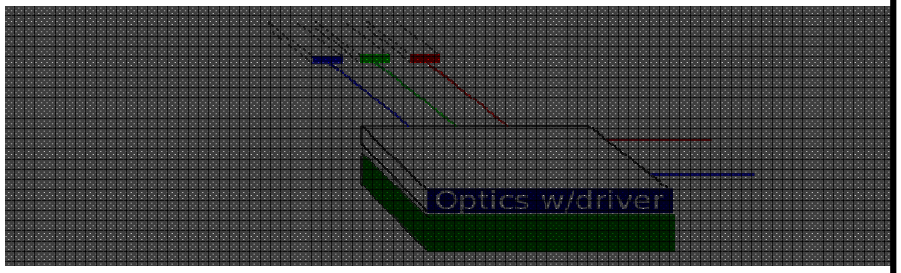
2D Integration for Large Machine Interconnect



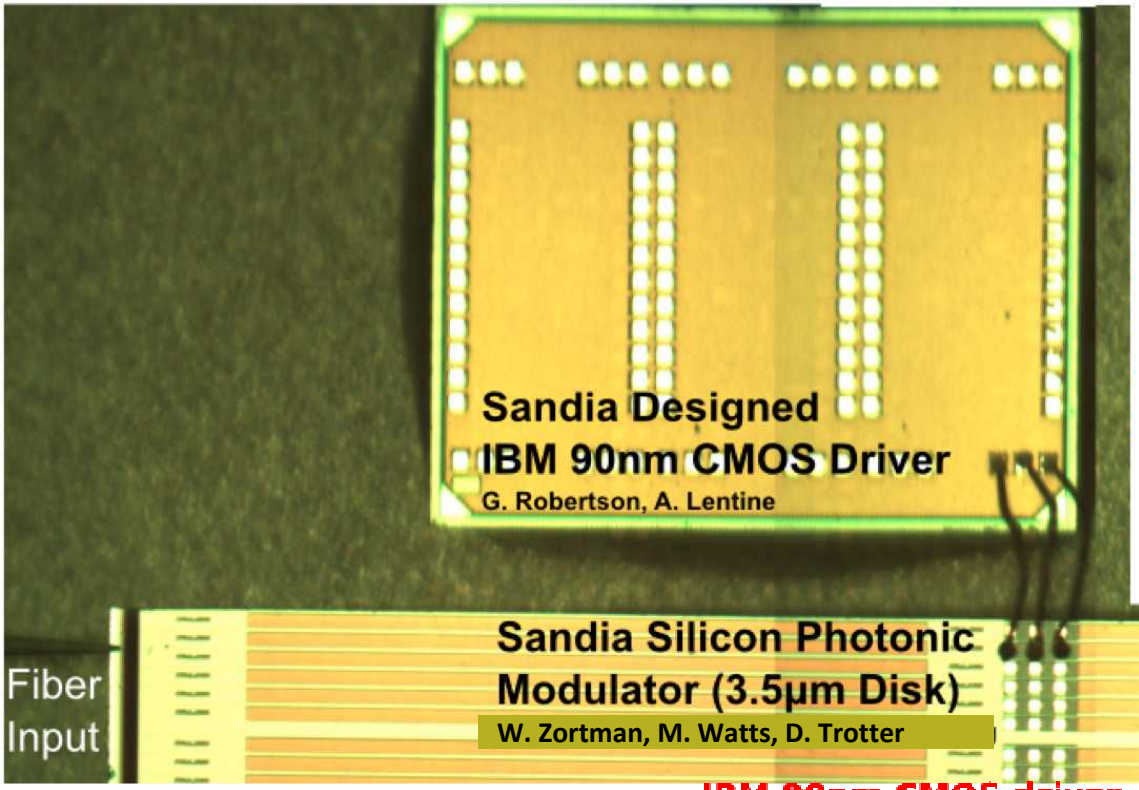


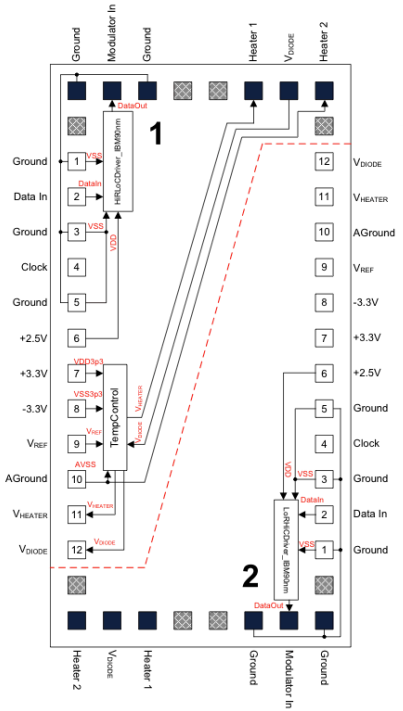
2D Integration for Long Distance Communcations/Data Center Virtualization

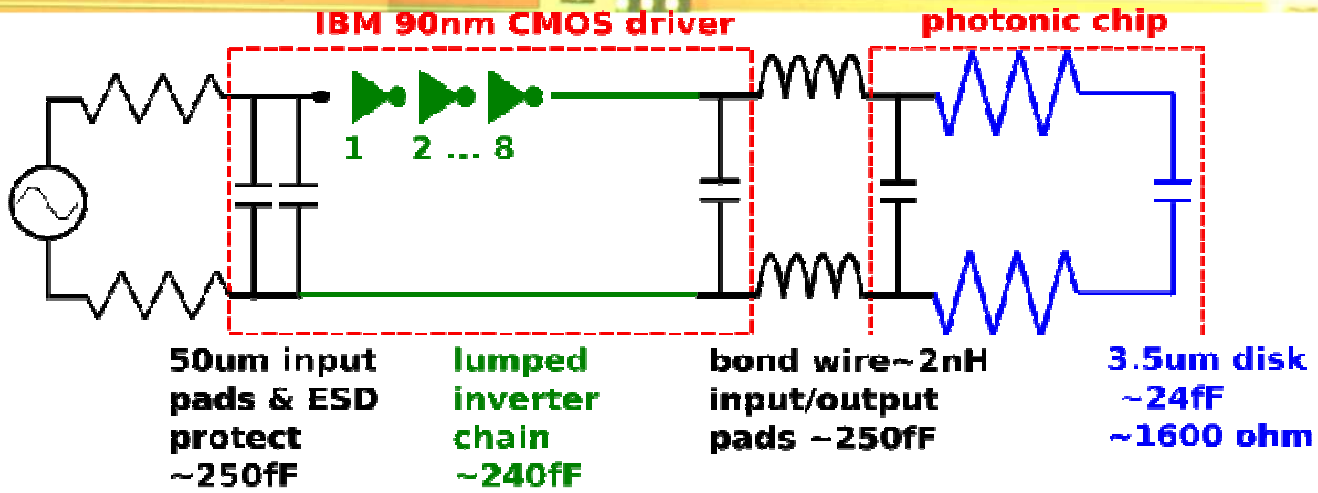




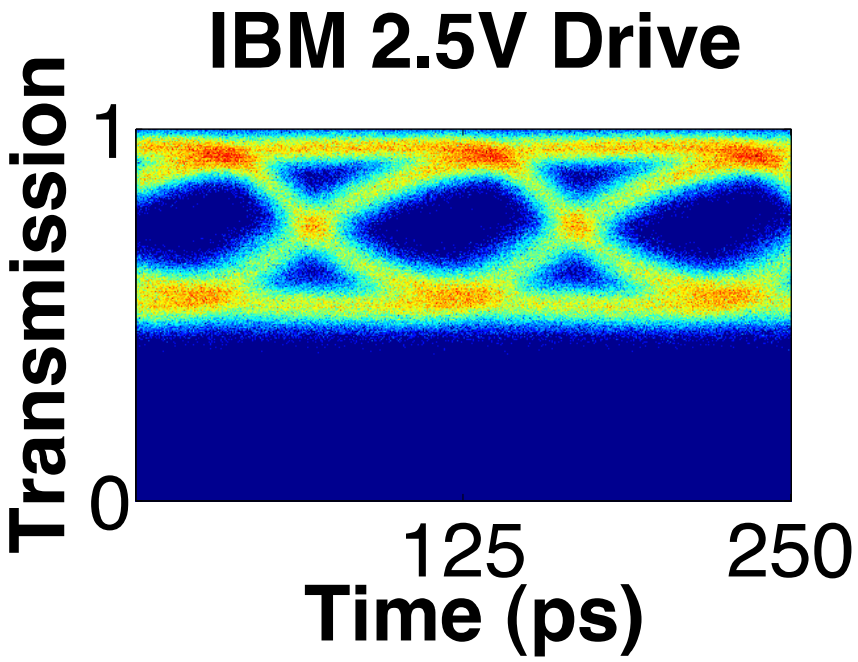
Wire Bonded

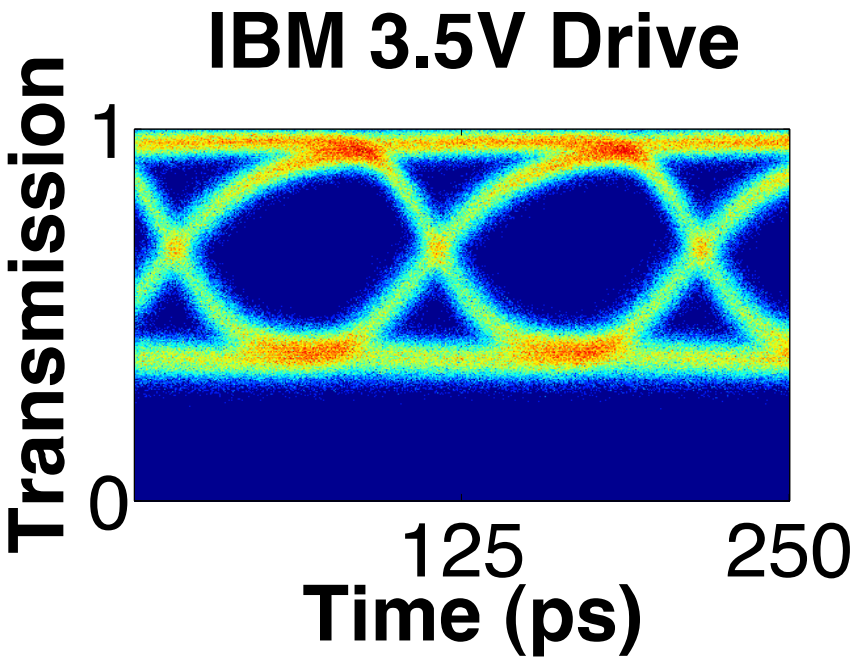

Sandia Designed
IBM 90nm CMOS Driver
G. Robertson, A. Lentine
Sandia Silicon Photonic
Modulator (3.5μm Disk)
W. Zortman, M. Watts, D. Trotter
Fiber
Input
Fiber
Output


Ground
Modulator In
Ground
Heater 1
Heater 2
1
2
Ground
Data In
Clock
+2.5V
+3.3V
-3.3V
AGround
TempControl
Data In
Clock
-3.3V
+3.3V
+2.5V


IBM 90nm CMOS driver
photonic chip
1 2 ... 8
50um input pads & ESD protect ~250fF
lumped inverter chain ~240fF
bond wire~2nH input/output pads ~250fF
3.5um disk ~24fF ~1600 ohm

Two Dimensional Integration at 5Gbps





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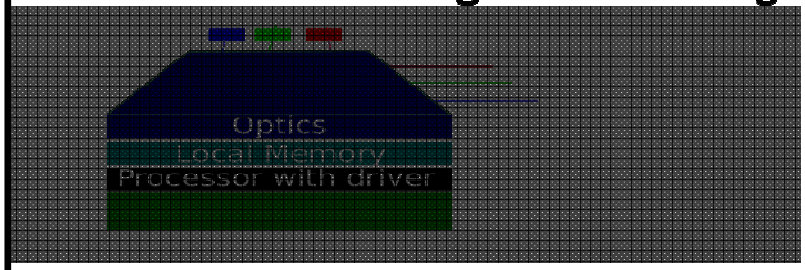
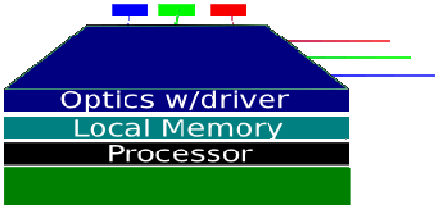
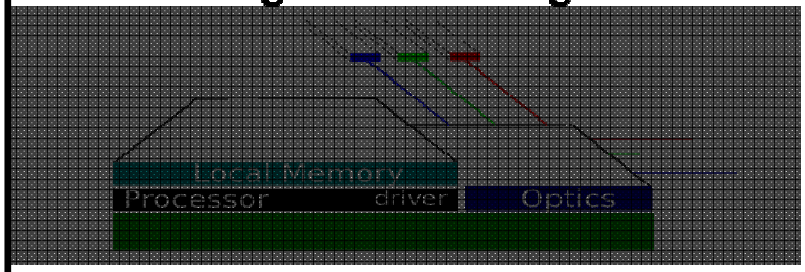
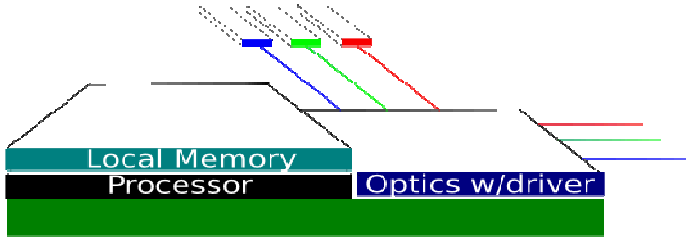


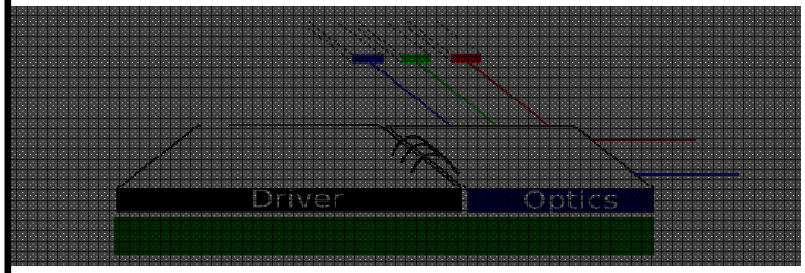


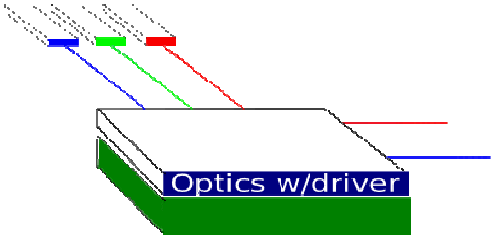
2D Integration for Large Machine Interconnect





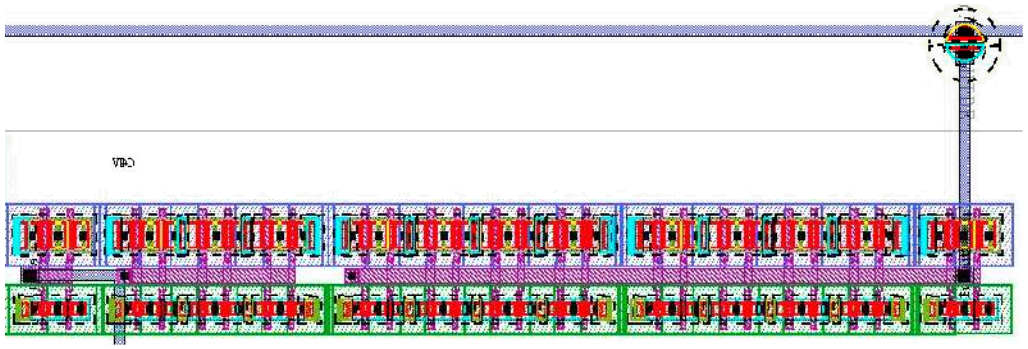
2D Integration for Long Distance Communcations/Data Center Virtualization



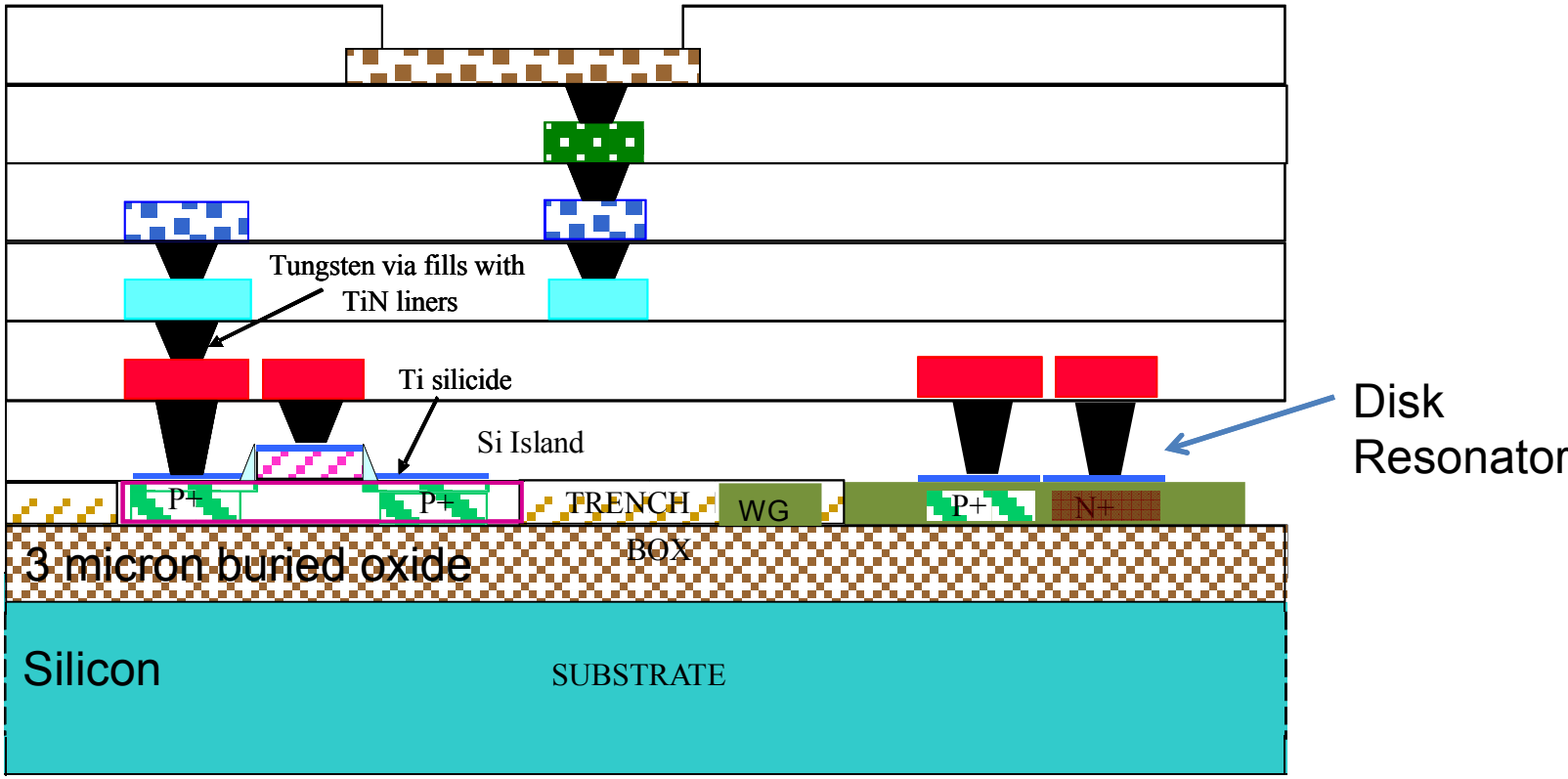


Layout of the Monolithic Chip

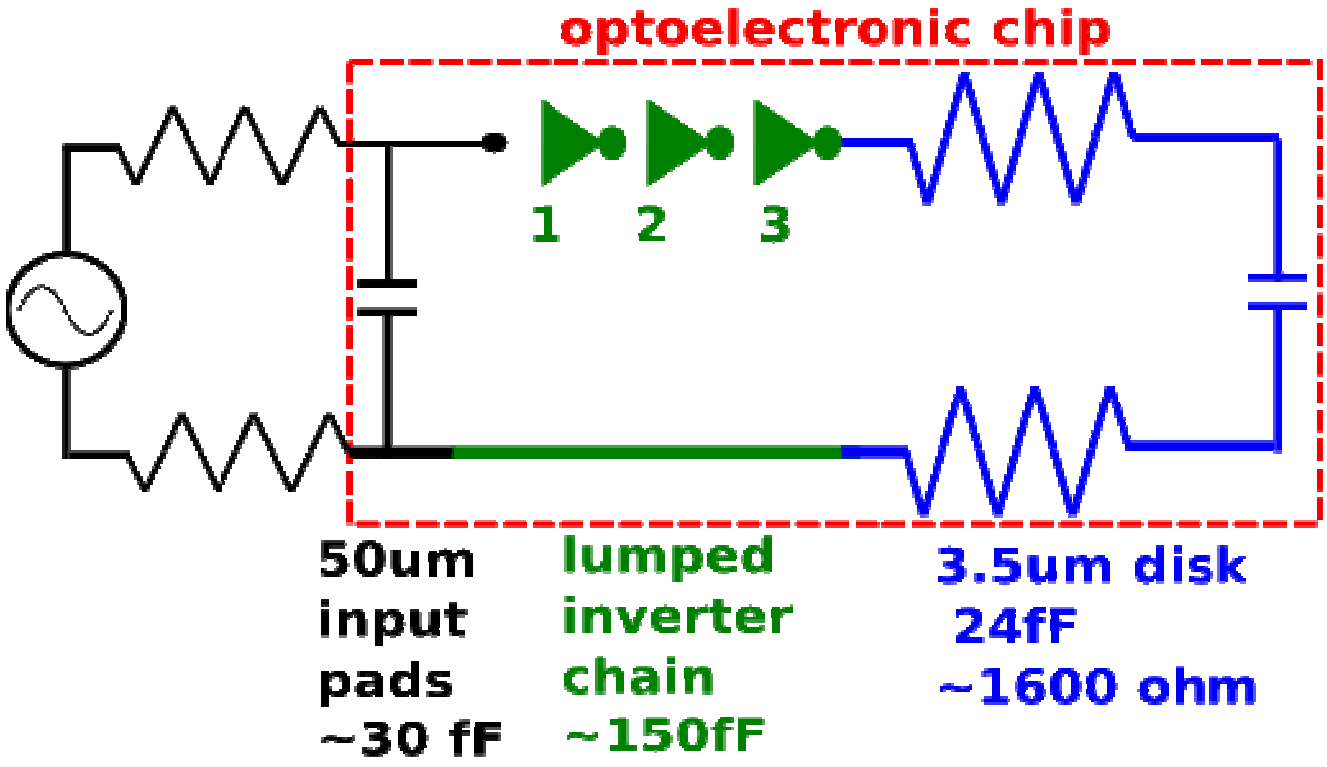
Top view from L-edit shows the driver and optics



Standard CMOS stack



Equivalent Circuit



Multiprocessor chip and large machine performance is increasing the need for high bandwidth off chip solutions

Integration of low power modulators in monolithic and 2D regimes has been demonstrated

The potential exists for using a 1V low current (3mW) driver in monolithic integration.

A special thanks for support from my advisors:

Luke F. Lester

CHTM

THE UNIVERSITY of NEW MEXICO

Michael R. Watts

rle AT MIT RESEARCH LABORATORY OF ELECTRONICS AT MIT

MIT

NNSA National Nuclear Security Administration

LDRD

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000

Back Up

Requirements:

☐ *Small footprint*

☐ *Gate level switching*

Temperature Stability

<10fJ/bit modulation

Low power source

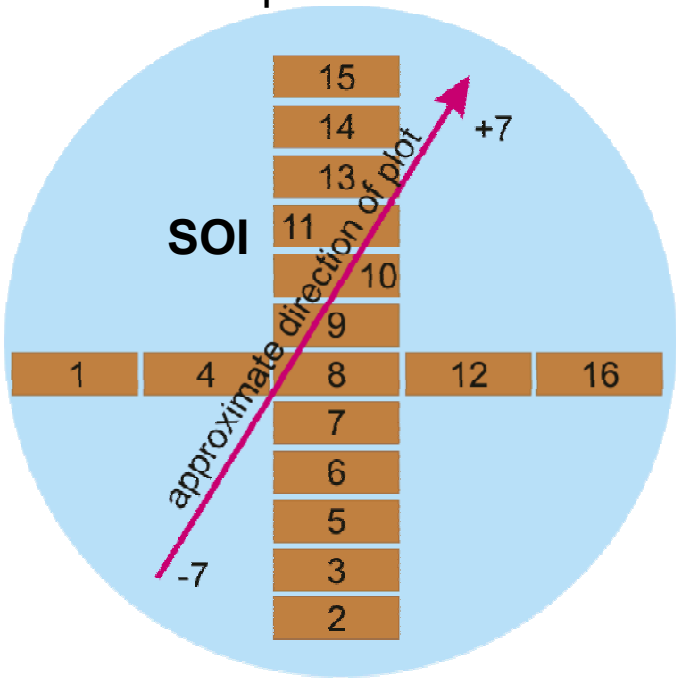
Integration

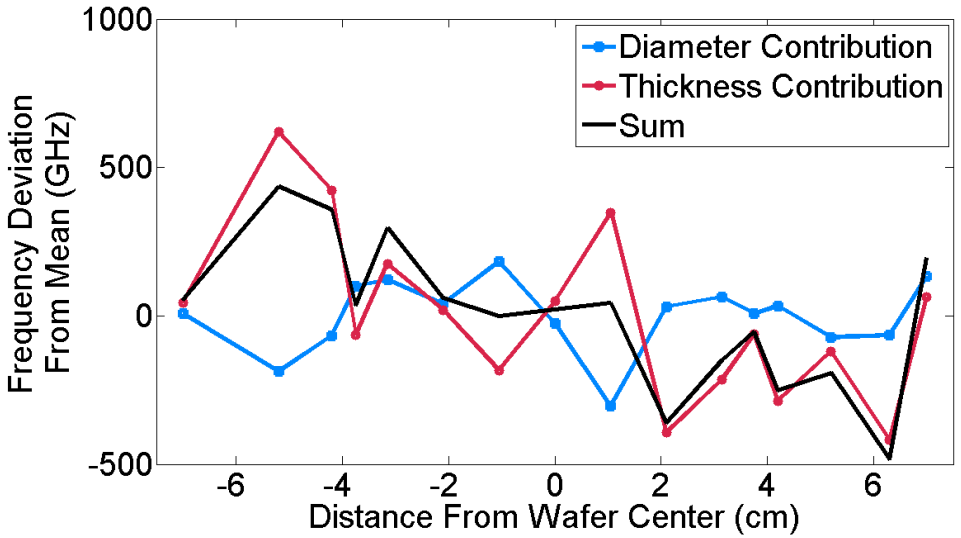
Overview

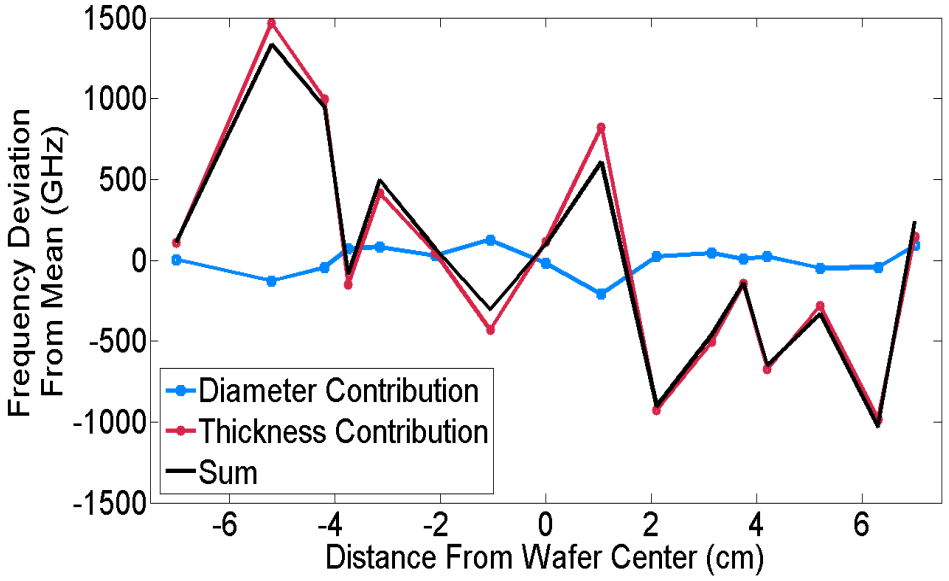
- Motivation
- Theory
- Measurement

Within Wafer Frequency Variation

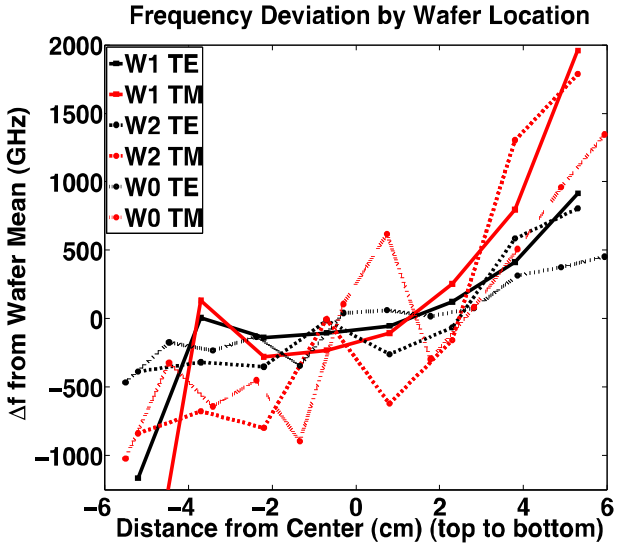
Wafer Map of Measured Devices



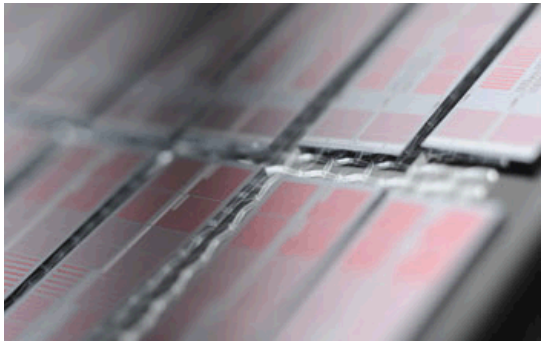


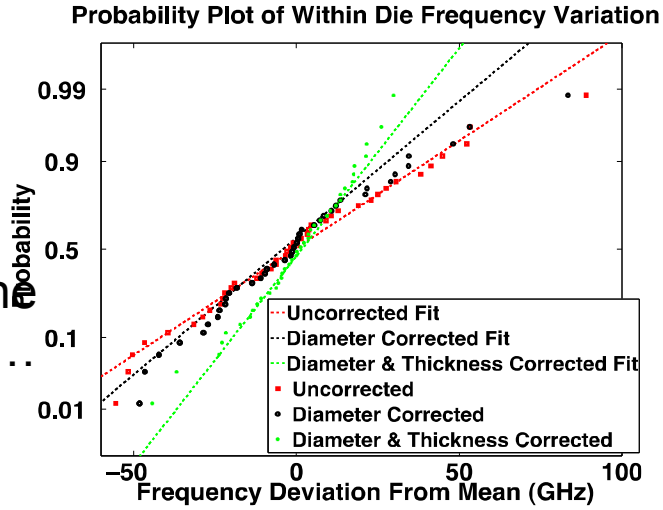


Manufacturability

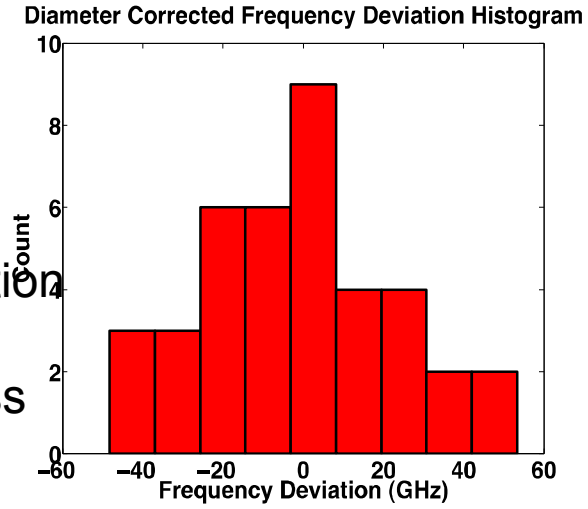


Wafer level there is 1THz variation!





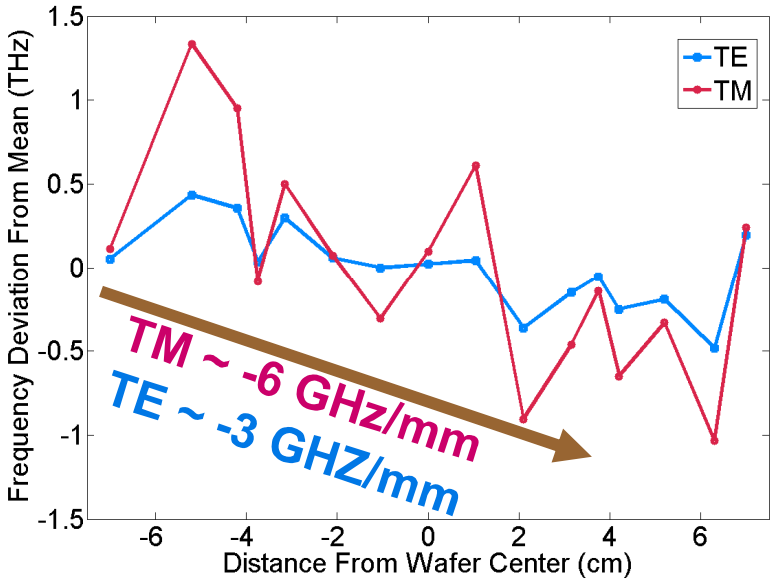
Through residual analysis of the special causes in our process…



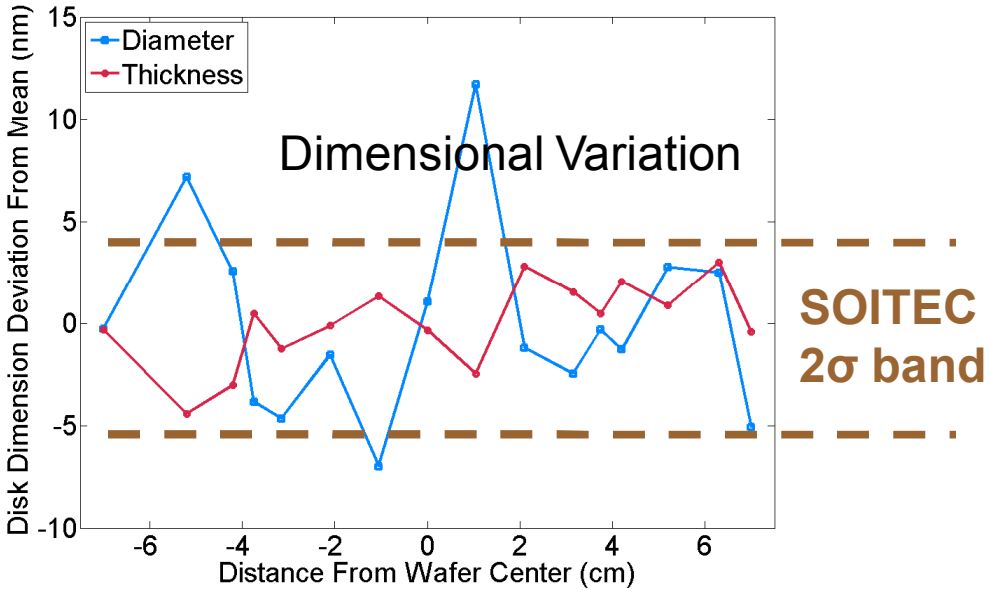
We can achieve 80Ghz variation on chip across 5 waveguides
- on a six inch, .35um process

WA Zortman, DC Trotter et al OPEX (2010)
WA Zortman, MR Watts et al IPNRA Honolulu (2009)

Dimension Contribution to Variation

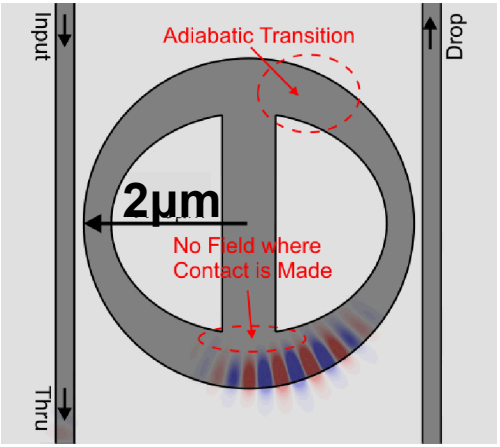


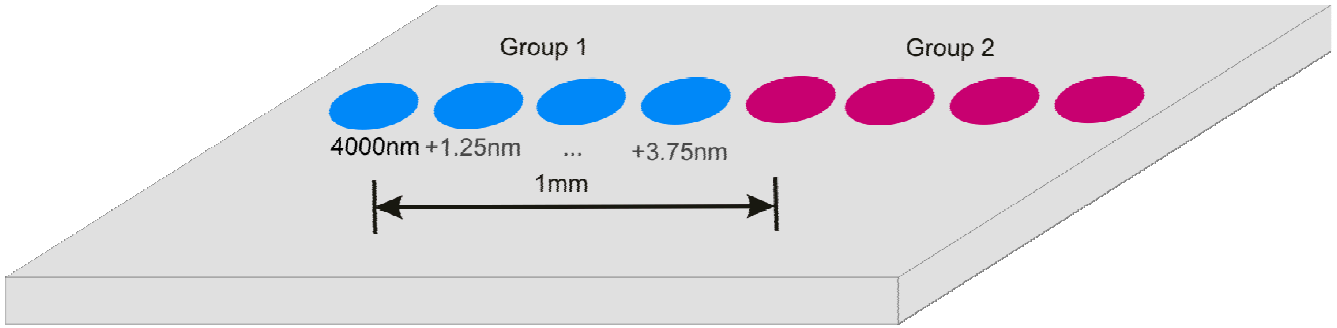
TM Modes

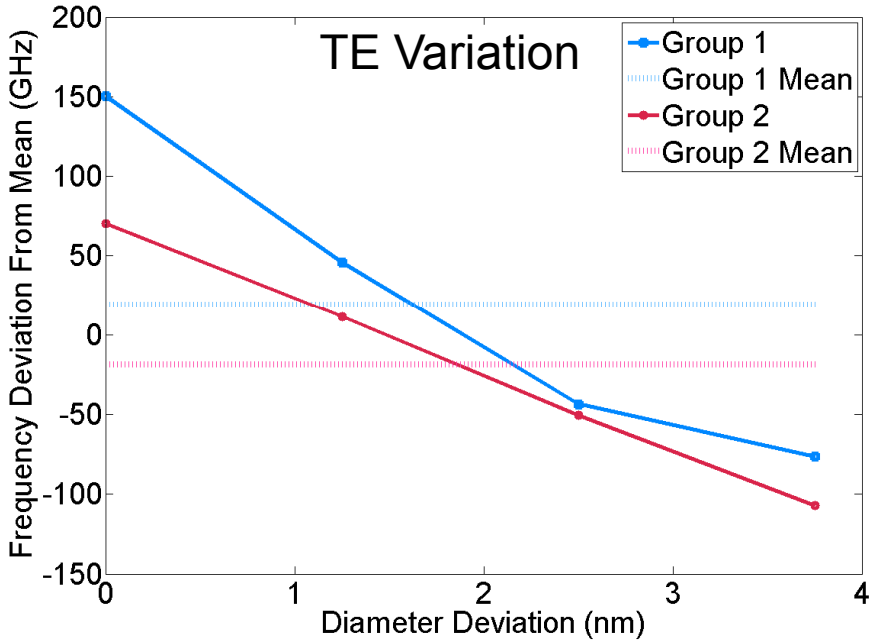


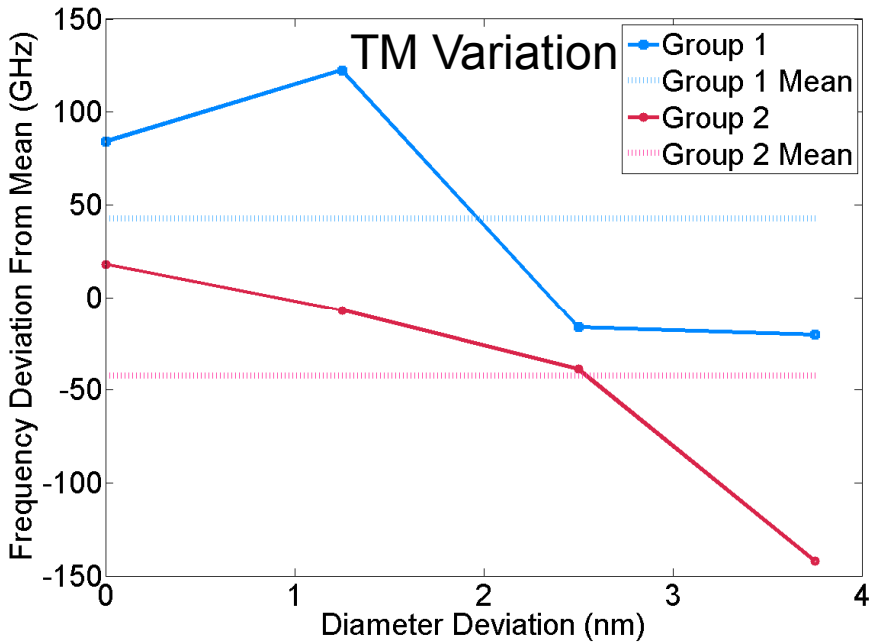
Thickness variation is the major source of frequency shift for TE and TM

Local Relative Frequency Control





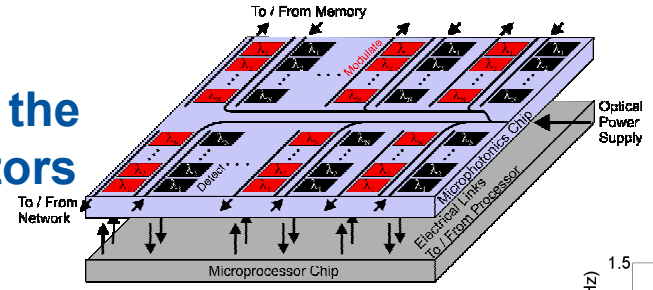




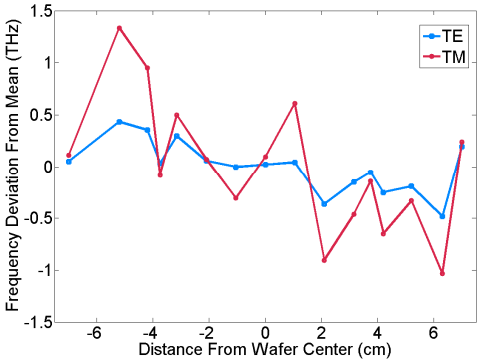
Within 1mm chip variations in TE modes < 50GHz, TM modes ~ 100GHz

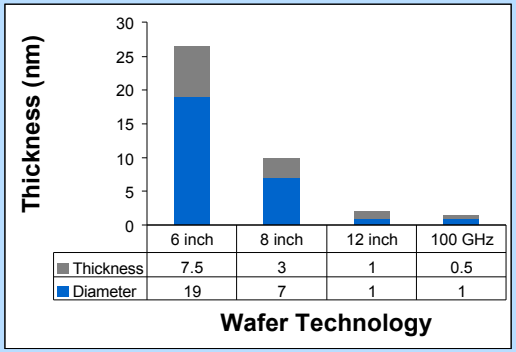
Summary

Wafer uniformity is motivated by the desire for large arrays of resonators

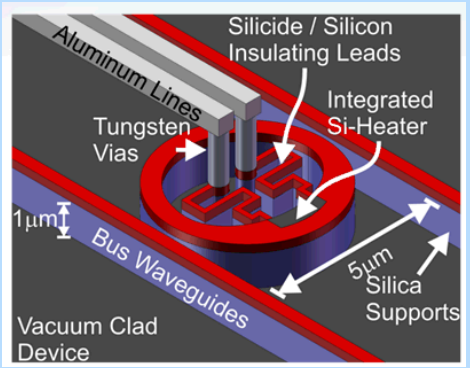


Frequency deviation and the underlying cause can be understood through measurement and simulation





Industry progress and thermal control show that a path to large arrays of low energy resonators exists



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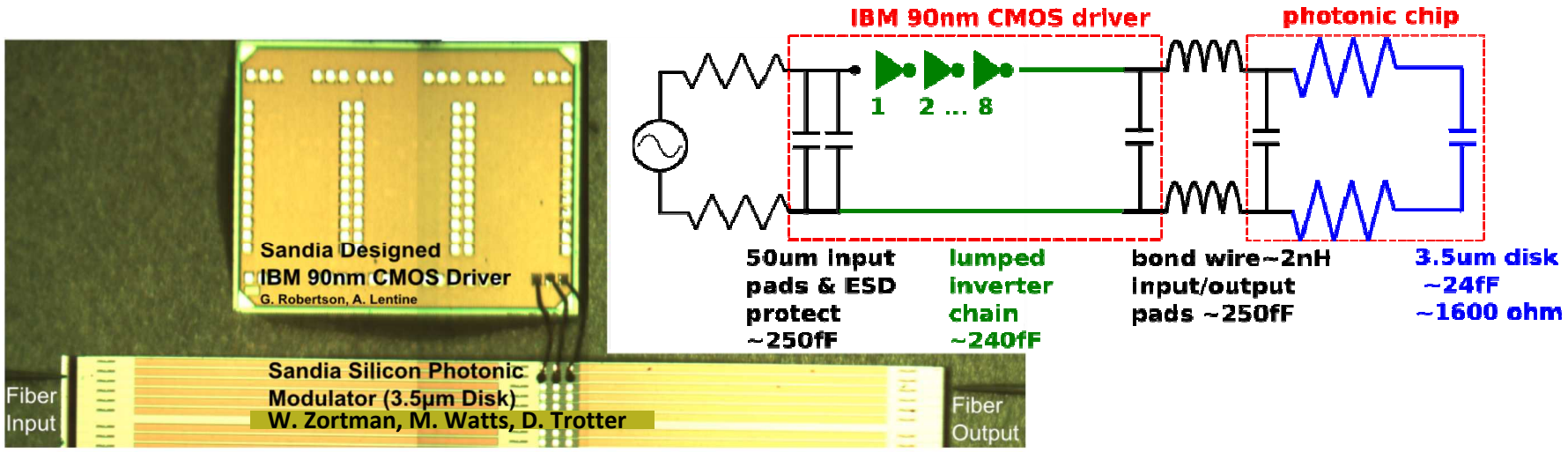
Shadi Naderi - matrix solutions

SOITEC – uniformity statistics

2D or Hybrid Integration



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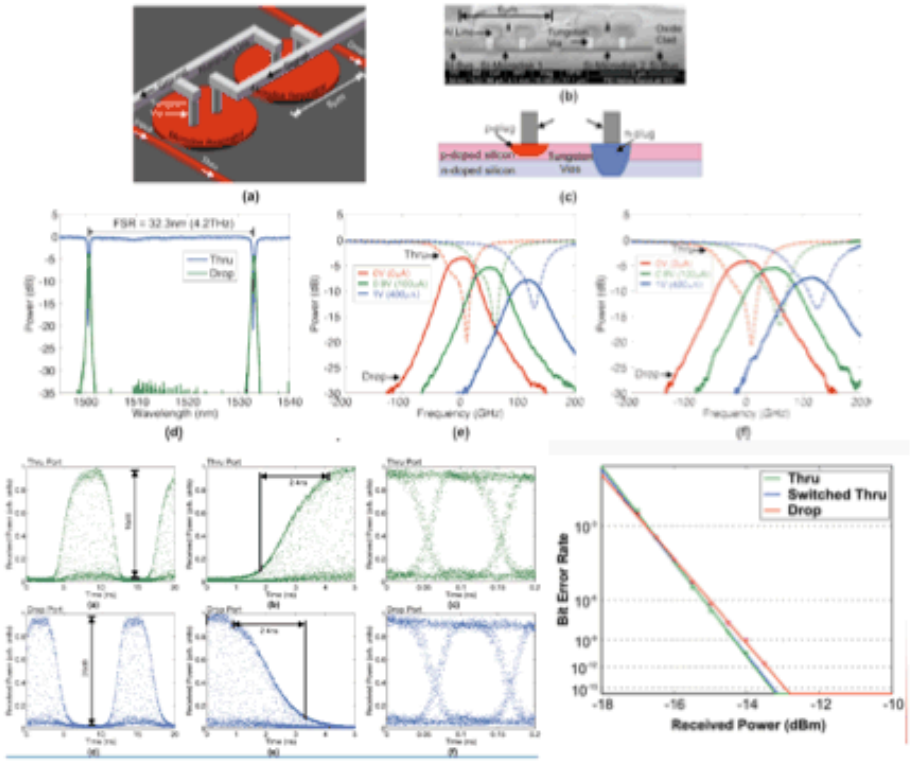
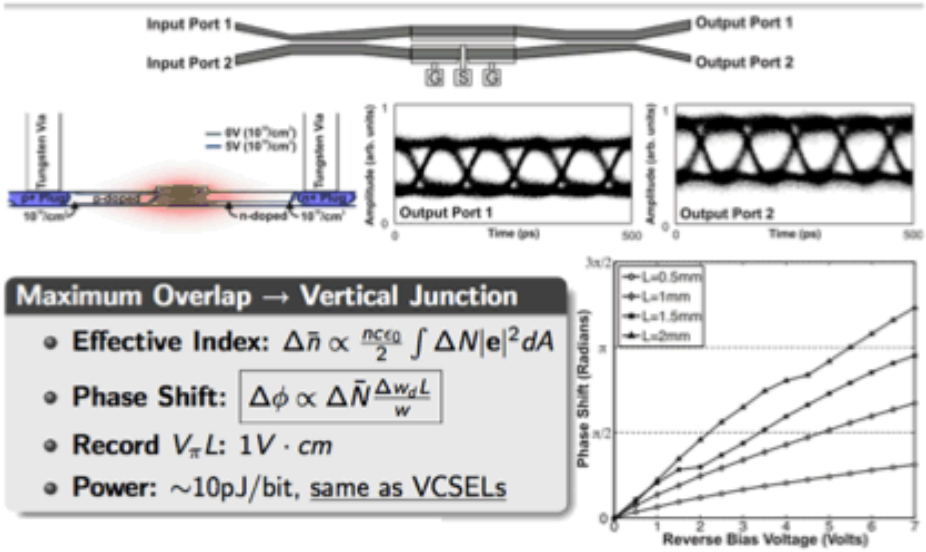
Filter



MR Watts, AL Lentine, et al OFC (2008) (postdeadline)

Mach-Zehnder Modulator



MR Watts, WA Zortman, et al JSTQE Vol 16 2010
MR Watts, WA Zortman, et IPNRA Honolulu, Hi, 2009

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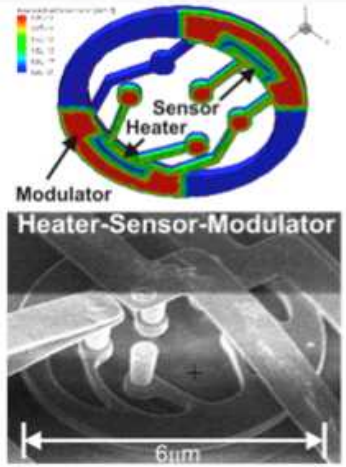
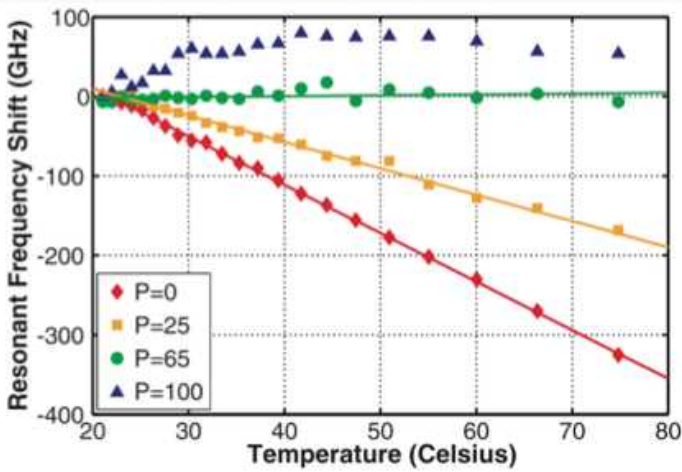
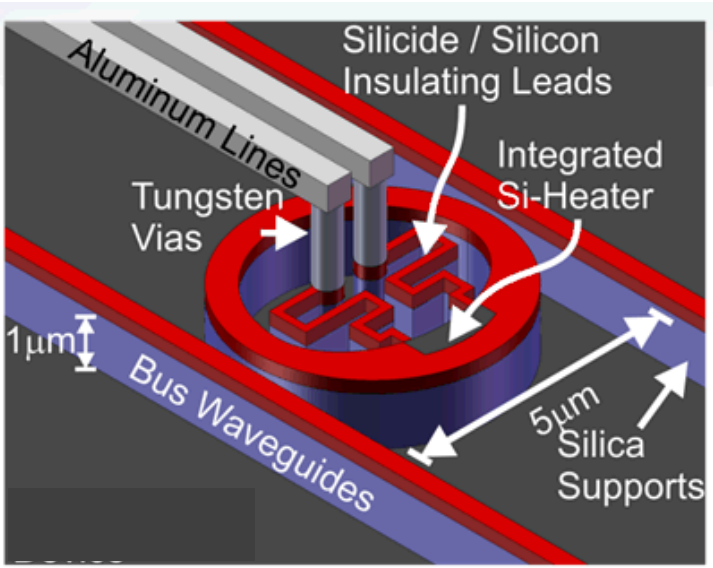
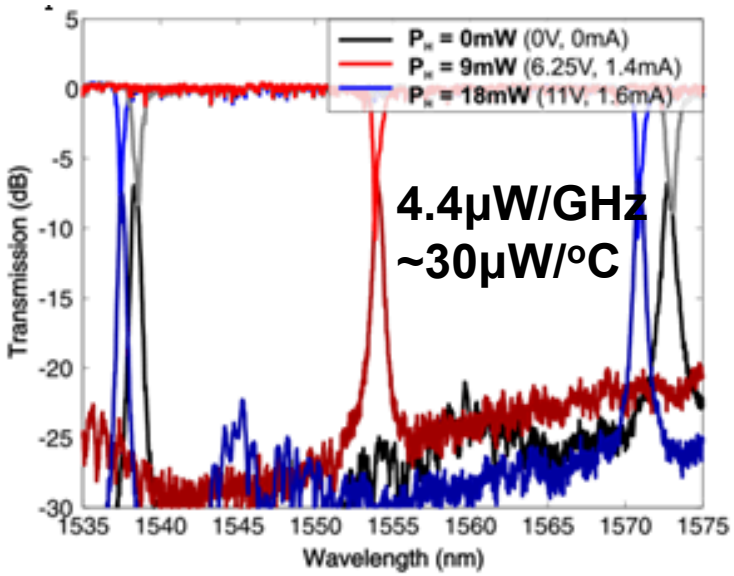
Single Mode Compact Tunable Resonators

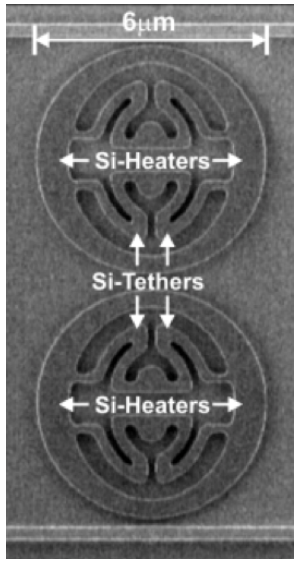




CT DeRose, MR Watts et al CLEO San Jose (2010) (post deadline)







MR Watts, WA Zortman et al CLEO San Jose (2009) (post deadline)