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Asynchronous Ballistic Reversible Computing using Superconducting elements

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ABSTRACT

Computing uses energy. At the bare minimum, erasing information in a computer increases the entropy. Landauer [1] has calculated ~ $k_B T \log(2)$ Joules is dissipated per bit of energy erased. While the success of Moore's law has allowed increasing computing power and efficiency for many years, these improvements are coming to an end. This project asks if there is a way to continue those gains by circumventing Landauer through reversible computing.

We explore a new reversible computing paradigm, asynchronous ballistic reversible computing or ABRC. The ballistic nature of data in ABRC matches well with superconductivity which provides a low-loss environment and a quantized bit encoding—the fluxon. We discuss both these and our development of a superconducting fabrication process at Sandia. We describe a fully reversible 1-bit memory cell based on fluxon dynamics. Building on this model, we propose several other gates which may also offer reversible operation.

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ACRONYMS AND DEFINITIONS

Abbreviation	Definition
CMOS	complementary metal oxide semiconductor
SFQ	single flux quantum
ABRC	asynchronous ballistic reversible computing
RM-cell	reversible memory cell
LJJ	long Josephson junction
JJ	Josephson junction
J_c	Josephson junction critical current density
β_c	Stewart-McCumber damping parameter
SiO_2	silicon dioxide
Ic	critical current
Nb	niobium
TaN	tantalum nitride
Al	aluminum
NbAl/AlOxNb	niobium/aluminum/aluminum-oxide/niobium
SNS	superconductor-normal metal-superconductor
k_B	Boltzmann constant
Δ	superconducting gap
AlOx	aluminum oxide
DOE	Department of Energy

1. INTRODUCTION

This project focuses on creating reversable logic using superconducting elements. In this section we will give a brief overview of the project. We will introduce the concept of reversible logic operations. Then we will discuss why superconducting elements provide an interesting set of elements from which to build up reversible logic.

1.1. A case for approaching computing from a different angle

Computers drive every aspect of our society, from entertainment such as Facebook and Netflix, to information storage and search exemplified by Google, to the national security tasks that Sandia undertakes for its customers. Until recently, the computational power, complexity, and energy efficiency of computers has steadily improved, a phenomenon known as Moore's Law, but now that progress is stalling. With the end of Moore's law in sight, where can we look for new breakthroughs in computing performance?

Energy usage poses a technological barrier that is most easily seen by examining high performance computing. Until recently, the most powerful supercomputer in the United States was DOE's Titan [2], is capable of about 16 petaflops/sec—a petaflop is 10^{15} floating point operations—while consuming approximately 8 MW of power. This is about 2 petaflops/MW of power. A Titan like machine scaled to exaflop/sec size would consume 500 MW—about one quarter of the total electrical output of the Hoover Dam.

In recent years DOE's Summit, the replacement for Titan, improves on both performance and energy usage. It uses about 10 MW of power to perform about 149 petaflops/sec, about 15 petaflops/MW. Japan's Supercomputer Fugaku currently holds bragging rights for the most powerful computer in the world and uses 28 MW of power to perform about 416 petaflops, about 20 petaflops/MW. While these gains in efficiency are laudable, the underlaying technology is not getting more efficient. At 15-20 petaflops/MW, an exascale supercomputer's is ~ 50 MW which is still technologically and economically problematic. There is simply not enough energy available to power for all the data centers and supercomputers that humanity will eventually want. One possible answer is implementing reversible computing.

1.2. Reversible Computing

Gates in conventional (irreversible) computation discard information each time they operate, increasing entropy and hence dissipating energy as heat. The fundamental energy dissipation required per logical bit operation in conventional (irreversible) logic—independent of the technology used—is $k_B T \log 2$ or about 3×10^{-21} Joules at room temperature, as calculated by Landauer [1, 3]. If instead, a gate locally transforms states one-to-one so that no information is destroyed then, energy need not be dissipated, entropy need not be generated, and the computer could theoretically operate with gates that dissipate less than the $k_B T \log 2$ limit—Landauer's limit. This computational paradigm is called reversible computing [4].

The challenge we took up in this project was how to implement physically reversible logic circuits that consume on the order of $k_B T \log 2$ of energy per bit operation or less. Even measuring such tiny power consumption is challenging! A successful demonstration of reversible logic in this regime would enable computers that dissipate 10^5 times less energy per fundamental

bit operation than current computers, revolutionizing high performance computing. A myriad of national security tasks from weapon yield, to plasma confinement, to weather prediction depend on such high-performance computing.

This project attempted to implement reversible computing using the lowest energy logic elements currently known—Josephson junctions with superconducting interconnects. Logic in superconducting circuits is based on the presence or absence or polarity of a flux quantum (a fluxon) trapped in a superconducting wire loop [5]. In a superconductor, fluxons behave like particles and can be shuttled around analogous to charge in conventional electronics. The ballistic nature of the fluxon makes superconducting logic well matched to ballistic approaches to reversible computing.

As an aside, conventional superconducting logic has recently been the focus of much research, such as the IARPA C3 and SuperTools programs, and in its conventional irreversible form has demonstrated at clock speeds above 700 GHz [6]. A Josephson junction dissipates about $\sim 10^{-19}$ J per switching event [5]. Complex integrated circuitry has been demonstrated [7] indicating a high level of maturity. This is fertile ground for approaching reversible computing which would allow the energy per switch (per bit operation) to be reduced by an estimated additional 3 orders of magnitude.

2. ELEMENTS OF SUPERCONDUCTIVITY FOR COMPUTATION

In superconducting circuits, many of the principles of operation are different from those used in semiconductor-based circuits. For example, with transistors, one applies voltages to gates, sources, drains etc. and then current flows as those voltages dictate. With superconductors, voltages are mostly zero except for transients and so one applies currents as biases.

Since superconductors quantize magnetic flux [8], they provide an attractive quantized unit, for use in computation. The circuits discussed here use single magnetic flux quanta, SFQ, to encode data [5]. As we will discuss below, inductances in the form of superconducting wires and Josephson tunnel junctions form the basis of SFQ.

2.1. Josephson junctions

Figure 1. (a) Josephson junctions are formed by a weak link between two superconducting leads. The weak link can be a narrow bridge of superconducting material, a tunnel barrier, or a normal metal. (b) The "IV" characteristic for a damped Josephson junction. (c) Electrical symbol for the JJ.

The Josephson Junction or JJ is to superconducting circuits what transistors are to semiconductor circuits. It provides a switchable element that can be current biased and allows magnetic flux quanta to be moved between superconducting loops.

The JJ is formed by a weak link between two superconducting leads. The weak link can be a narrow bridge of superconducting material, by a thin normal (non-superconducting) metal, or by a tunnel barrier [8]. It is characterized by a critical current, I_c, which is the maximum supercurrent the device will carry without developing a voltage across it and by its damping parameter β_c also known as the Stewart-McCumbre parameter. Above I_c, the JJ asymptotically approaches the behavior of a resistor. Critically damped JJs have $\beta_c = 1$, underdamped have $\beta_c > 1$ and overdamped have $\beta_c < 1$. Damping comes from a sub-gap resistance and in SFQ circuits designed for conventional logic, from an explicit shunt resistor. However, in reversible circuits, such shunt resistors would cause excess dissipation and so are largely removed. This lack of shunting resistors is one of the key differences between conventional SFQ and reversible SFQ circuits. The choice of materials also affects the JJ properties. For this project, as for most SFQ projects, we used Nb based JJs and wiring. The superconducting gap of Nb, $\Delta = 1.4$ mV. The transition temperature of pure Nb is about 9.2 K, permitting easy operation and testing at 4.2 K in liquid helium. However, Al could equally well be used if operation at temperatures below 1 K were needed.

2.2. Inductors.

The second key ingredient in SFQ circuits after JJs are inductors. All wiring inherently has inductance. Inductance is a result of magnetic fields spreading through space and depends on the geometry as well as the kind of superconductors used. Since low value magnetic fields do not penetrate into superconductors beyond the London penetration length, superconducting circuits constrain magnetic fields substantially differently from circuits involving only normal. In general, determining inductances accurately requires a finite element calculation of the fields around a wire and includes all neighboring pieces of metal that constrain those fields.

Since magnetic fields cannot cross superconductors of width greater than the London length, they can be contained within loops of superconducting wire. Adding a JJ to a loop of wire provides an element that allows flux to enter or leave such a loop whenever the JJ's critical current is exceeded.

In the case of SFQ and multi-fluxon circuits, the product of loop inductance, L, and I_c determines how much flux can be stored inside a loop. Consider that a screening current flows around the loop to cancel the field contained within or outside that loop. When this screening current exceeds the I_c of the JJ, flux enters or leaves the loop until the required screening current is less than I_c. Thus, accurately knowing the value of inductances is important to SFQ circuit design.

On method of determining inductances is to build resonant circuits out of them. We chose to make transmission line resonators with resonant frequencies in the range 3-4 GHz range. We fabricated these resonators in the Sandia process (described below). They took the form of $\lambda/2$ micro-strip transmission line resonators coupled into a 50 Ω feedline at each end [9]. These measurements conducted at temperatures between 1.4 and 8.4 K informed us about microwave losses in superconducting transmission lines and in the SiO_2 wiring insulator used. We also extracted the London penetration depth of the Nb metal and the inductance per unit length versus temperature. On a practical level, it was gratifying to know 2 um wide lines of greater than 15 mm in length could have high yield in our process.

2.3. Sandia's superconducting circuit fabrication process

Sandia's superconducting circuit fabrication process leverages the Mesa Micro-Fabrication facility and multiple years of development of Nb films [10,11]. The process builds on oxidized six-inch silicon wafers and includes up to 3 superconducting metal layers of Nb separated by planarized SiO2 dielectric layers. It is built around a superconductor-normal metal-superconductor (SNS) Josephson junction. Tantulum-nitride (TaN) is used for the normal metal weak link and is tuned to have a resistivity just below the metal-insulator transition to avoid significant temperature dependence. Work on the TaN JJs started during an earlier LDRD [12]. When nitrided, the Nb deposition has also been used as a base for ferro-electric deposition [13].

The strength of this process is that the Nb/TaN/Nb JJ barrier is between 10 and 20 nm thick instead of the ~ 1 nm thick oxide barrier typical of Nb/AlOx/Nb JJs. Thicker barriers allow much more process space for fine tuning critical current density. The composition of the barrier can also be tuned, e.g. to increase the resistance and hence the I_cR_n product. In addition, the SNS JJ is self-shunted eliminating the need for external shunt resistors that eat up space. TaN is also more tolerant of temperature excursions during processing—for example during deposition of SiO_2, than AlOx. Thus, JJs with TaN barriers potentially offers many advantages. Wolak et al. [14] presented results on JJs made in this process. Several talks and posters have also been given discussing TaN JJs made at Sandia, for example [15,16].

We have worked on extensions to this process such as having multiple layers of JJs. And mixing different JJ technologies in different layers. Since the process is planarized, Josephson junctions can be grown on any layer and J_c of individual layers can be tuned for different functionality. A poster presented at the JJWorkshop in Santa Cruz, 2017 discussed JJs on multiple layers [17].

Ultimately, we decided to move away from our internal "Sandia" process for several reasons. First, TaN SNS junctions are not ideal for reversible circuits. SNS junctions are self-shunted and hence dissipate a portion of the SFQ fluxon energy. Tunnel barriers formed from AlOx have much lower loss and shunt resistors are usually added externally meaning that they can be omitted from layouts. Second, the level of complexity required for our reversible test circuits requires a mature process capable of high yields. At this time, the resources and personnel to advance the Sandia process to sufficient maturity are not available.

2.4. The SeeQC process

After realizing that Josephson junctions fabricated in Sandia's Nb/TaN/Nb process would be too lossy for reversible circuits, we explored other fabrication processes. SeeQC is a technology company based in Albany, NY which recently split from Hypres Inc. SeeQC has retained the fabrication facility that was formerly part of Hypres. Their superconducting fabrication is a mature multi-layer process [18,19] featuring Nb/AlAlOx/Nb Josephson junctions, ideal for reversible circuits. They are also willing to adjust the critical current density (Jc) of their junctions based on customer needs over the range from about 30 A/cm^2 up to about 10 kA/cm^2.

The SeeQC process we used is an unplanarized 4 layer + a resistor process. Metal layers are Nb with a T_c of approximately 9 K and interlayer dielectrics are SiO_2. In addition to ours, several demonstration SFQ circuits have been fabricated in this process [7, 20].

2.5. Other superconducting fabrication processes

For completeness, we list other superconducting processes of which we are aware.

Star Cryoelectronics, located in Santa Fe, NM [21] can fabricate simple superconducting circuits. Other programs have used their services to fabricate single layer analogue circuits. StarCryo will also fabricate SQUIDs and multi-layer superconducting ciruits, but they don't have a set multi-layer process.

MIT-Lincoln Laboratory has an 8-layer Nb superconducting process that is fully planarized. The standard process goes by SFQ5ee [22] and features 10 kA/cm^2 critical current density. The high critical current density makes adapting our circuit designs complicated. Also, this multilayer process has a slow fabrication turn and so was not ideal for our needs.

SkyWater [23] has a superconducting process available to users and fabricates circuits for D-Wave and for Northrop Grumman Corp.

Well developed processes also exist in Japan and Europe.

2.6. Design tools

Several specialized design tools are available for SFQ circuits. Perhaps the most useful of these tools is WRspice which is available as shareware from Whitely Research [24]. WRspice has implementations of JJs that allow one to define all relevant parameters including Ic, capacitance, superconducting gap energy, sub-gap resistance, and more. One can also parametrize a shunt resistor if one chooses.

As discussed, accurate inductances are also important to designing and laying out working circuits. Since the inductance of a planar wire is affected by all the other pieces of superconducting metal nearby, software is also available for estimating these values. We used Inductex which is supplied by Sun-Magnetics.com [25], a small company located in South Africa. Inductex permits the extraction of both self-inductances and mutual inductance for multilayer stacks.

We used DW2000 for mask layout. This choice was purely by convenience because we have experience with this layout tool.

2.7. Testing tunnel barriers

During this project, we became aware of defects within aluminum-oxide tunnel barriers. These defects cause the critical current of a JJ to vary in time and in worst case can short the junction rendering it inoperable. The AlOx tunnel barrier is ~ 1 nm thick, barely 10 atoms, so a single atom out of place can cause a conduction hot-spot or cold spot. Other defects caused by hydrogen, or other atoms attached to the oxygen can occur. Grain boundries oxidize more readily by admitting more oxygen. However, all these defects are hard to analyze because the tunnel barrier is a partial oxidation of the aluminum surface—terminal oxidation is slightly thicker at about 3 nm—and on removing an oxidized aluminum surface from the growth chamber additional oxide forms.

Studying defects within the oxide is complicated by the fact the oxide changes the moment it is taken out of the growth chamber due to ambient oxygen in the air. Nancy Missert came up with an elegant solution to this problem. She realized that capping the oxide with a few nanometer

deposition layer of gold (Au) would create a discontinuous Au film. This film would have a distribution of Au islands approximately 10 nm across. Under the Au, protect the oxide is protected from further oxidation and is stable. The few nano-meter thick discontinuous Au layer permits local study of the oxide through transport measurements, for example with contact atomic force microscopy technique. Portions of this work have been presented at ISEC2019 in Riverside, CA [26] and more work will be presented at the applied superconductivity conference 2020 to be held virtually [27].

3. A REVERSIBLE 1-BIT MEMORY GATE

Current computing applications using complementary metal oxide semiconductor transistors (CMOS) have switching energies equal to the bit energies of ~10^5 k_BT. If the ITRS semiconductor roadmap [28] is followed to its end, bit energies cannot physically be reduced below about ~100 k_BT or thermal noise creates too many bit errors, and in practice, bit energies in end-of-roadmap CMOS stop decreasing at a much higher level of approximately 10,000 k_BT. The ability of Moore's law to further reduce energy consumption in CMOS based computers has mostly passed.

Instead of consuming the energy of input bits, gates can be configured to redirect inputs conditionally towards outputs. In this case, the ~100 k_BT (or more) energy needed to represent a bit is recycled and reappears at the output. This mode of operation is called reversible computing because gates that approach zero energy dissipation can be run in reverse. The price of reversible computing is temporarily maintaining outputs that are no longer necessary for the computation at hand because allowing them to be erased would dissipate the bit energy.

3.1. Developing the ABRC concept

Most existing concepts for implementation of reversible computing hardware use an adiabatic computing paradigm. This requires that individual degrees of freedom (e.g., node voltages) are synchronously transformed under the influence of externally supplied driving signals (e.g. clocks). But, distributing these "power/clock" signals to all gates and efficiently recovering the energy in these signals is non-trivial. Hence, we identify clocking as a necessary evil. Can clocking overhead be reduced by using a ballistic approach, wherein data signals self-propagate between devices driving most state transitions?

Many traditional concepts of ballistic computing, such as the classic Billiard-Ball Model [4], rely on a precise synchronization of interacting signals. These can fail due to amplification of timing differences when signals interact. Hence, we would like to relax timing requirements as much as possible and instead assume that gates operate on input when it arrives to the maximum extent reasonable.

We develop a general model of asynchronous ballistic reversible computing (ABRC) which aims to address these problems. We eliminate the requirement for precise synchronization between signals—removing timing differences as a source of error. In this model, asynchronous reversible devices are isomorphic to a restricted set of Mealy finite-state machines. We explore devices having up to 3 bidirectional I/O terminals and up to 2 internal states. We identify a simple pair of such devices that comprise a computationally universal set of primitives [29].

To restate the principles of ABRC used in this LDRD;

- Asynchronous operation which doesn't require local clocking of gates.
- Ballistic propagation of data through a network of gates.
- Reversible operation of those gates.

Two prototype ABRC "primitives" were chosen as a starting point. Combined together these primitives allow universal computing operations to be accomplished [29]. These two primitive operations are shown in figure 2. They are the "Rotary" and the "Toggle barrier". Trying to implement these primitives was a major objective of this project.

The other starting point of this LDRD was to assume data would be encoded using SFQ pulses. Gates would take the form of networks of superconducting elements, JJs, inductors, and possibly capacitors, but no dissipative elements would be included.

Figure 2. Asynchronous ballistic revers-ible primitives. (a) The rotary element. (b) the toggle barrier. (c) combining the elements to implement

conductors, we explored how the ABRC model might be realized in practice using single flux quantum solitons (fluxons) in superconducting Josephson junction (JJ) circuits [30]. One natural realization could use fluxon polarity to represent binary data in individual pulses propagating near-ballistically, along either discrete or continuous long Josephson junctions. The flux charge (−1, 0, +1) of a JJ-containing superconducting loop with $\Phi_0 < I_c L < 2\Phi_0$, or equivalently the polarity, could encode a ternary state variable internal to a device.

A natural question then arises as to which of the definable abstract ABRC device functionalities using this data representation might be implementable using a JJ circuit that dissipates only a small fraction of the input fluxon energy. To help sort through the myriad possibilities, we investigated the conservation rules and symmetries considered as constraints to be obeyed in these circuits. We also began the process of classifying the possible ABRC devices in this family having up to three bidirectional I/O terminals, and up to three internal states [30].

This work [30] also taught us how SFQ pulses propagate along long-Josephson junctions (LJJs). In particular, a pulse continues to propagate if it sees a regular impedance. The impedance of the LJJ can be stated as the a combination of the series inductances and the shunt inductance and capacitance of the JJs and reduces to $Z_{LJJ} = \sqrt{Z_L(Z_L + Z_{jj})}$. If a large impedance mismatch is encountered, the pulse will reflect. This simple realization implies several possible gates based on fluxons propagating along LJJs.

Table 1. Truth table for the RM-cell

Input Syndrome	Input Syndrome	Output Syndrome	Output Syndrome
Incoming Fluxon polarity	Initial state stored in RM cell	Final state stored in RM cell	Outgoing fluxon polarity
+1	+1	+1	+1
+1	-1	+1	-1
-1	+1	-1	+1
-1	-1	-1	-1

One realization we had was that an LJJ terminated by a large junction and an inductance could serve as a reversible 1-bit memory [31]. We called this device the "reversible memory cell" or just RM-cell. It is a 1-port device which mates to the end of an LJJ transmission line and has the logic table shown below.

The operation of the RM-cell is to swap the stored state with the incoming state. If the incoming state has the same polarity as the stored state, it reflects—the stored state effectively increases the impedance seen by like polarity pulses at the input port. On the other hand, if the input state and the stored state differ, then the RM-cell matches impedances and the two states exchange. Here, we define the polarity of the stored state the incoming state by the direction of current flow associated with each. Clockwise circulating currents correspond to positive pulses and counterclockwise to negative pulses. The RM-cell is fully described in [31]. An important design consideration is that the I_c of the JJ terminating the LJJ must be large enough to carry most of the current pulse of an

incoming SFQ and must be matched carefully with the inductance used such that $I_cL \sim \Phi_0$. If the RM-cell is viewed as a single junction SQUID—superconducting quantum interference device—the potential that is plotted has 3 stable minima. The outer two at +/- Φ_0 are the two working states of the RM-cell. The RM-cell is fully reversible in concept. Future work plans to measure the energy dissipated during operation.

3.2. Application to quantum computing

Superconducting qubits are tuned with small currents that bias the qubit with a weak magnetic field. Such tuning changes the operational frequency of the qubit and can be used to bring it into resonance with another circuit element for two-qubit gate operations, to transfer the state, or to cause a rotation of the qubit state about the Z axis of the Bloch sphere—a phase gate. Currently, such signals are applied by room temperature electronics. However, one would expect that in the future, control much closer to the qubits will be required.

Superconducting qubits operate at low temperatures of approximately 10 mK in dilution refrigerators. In such equipment, heat lift is limited and is measured in μWatts. In this environment, transistorized circuitry produces far too much heat. It actually requires purposeful design to ensure semiconductor devices even operate at such low temperatures.

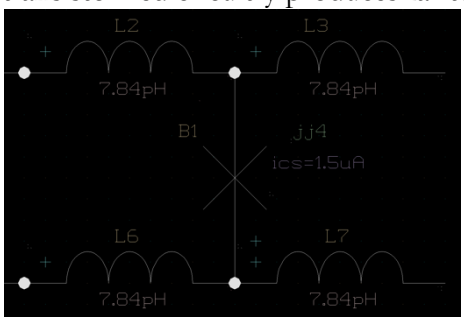

Figure 3. Figure 3. Schematic diagram of the unit cell of an LJJ.

The RM-cell provides a small bias current of the correct size for biasing qubits. Because we expect the RM-cell to use very little energy, it is ideal for an application such as biasing a qubit. Also, because it is a superconducting device, it could be fabricated alongside the qubits, or in a similar fabrication process. In short it should be compatible with qubit fabrication.

Finally, in ideal operation the RM-cell flips from +1 to -1 fluxon stored, providing a 1-bit change in bias. However, pairs of RM-cells can provide cancelling or summing biases. A multi-bit bias circuit could be built by combining several RM-cells pairs with different couplings to the qubit.

3.3. Polarity filter

The RM-cell provides the insight that a terminating an LJJ transmission line with a different impedance can be used to manipulate fluxons. An example unit cell of a discrete LJJ is shown in Figure 3. If a much larger JJ than that in the unit cell is substituted instead, the fluxon sees a superconducting wire instead of a JJ and it can't pass through. Instead the fluxon reflects. From the unit cell shown in Figure 3, it is clear that such an arrangement is symmetric from left and right. Inputs can come from either side, left or right and outputs can leave from either left or right. The exact size of the JJ required to realize this effect is a function of the elements in the LJJ, however, increasing the JJ to 4-5 times that in the unit cell is a good rule of them.

A defect that reflects all pulses looks like a superconducting short in the line. However, the JJ can be influenced by a bias current, and so biasing the "defect" JJ with either a dc current or an inductively supplied current provides a way to break symmetry. In this case, a bias current allows one polarity of the fluxon pulse to pass—because the circulating current associated with that polarity is parallel to the bias current and sums with it. The other polarity—with a circulating current anti-parallel with the bias—reflects.

At the time of this report, we have shown that the polarity gate functions in simulations when the bias is supplied directly through by a current source or when the bias is supplied inductively with a current source. These results were obtained through simulation with WRspice. Unfortunately, a current source can act as a damping element, so we cannot say this gate is reversible at this point. If a persistent current in a current loop were inductively coupled to bias this gate, that would provide a dissipationless gate. However, we have not yet been able to simulate the circuit with such biasing.

4. CONCLUSIONS

This LDRD has discovered that reversible gates are possible using ballistic fluxons (SFQs) on LJJ elements. The RM-cell is definitive proof that at least one reversible operation is possible. Follow on work will quantify how much energy the RM-cell uses in operation. Following the principles embodied in the RM-cell, we have discovered several other functions that can be implemented by putting a controllable impedance at the end of an LJJ. Since a major goal of this LDRD was to demonstrate at least one reversible function, this LDRD has been a success. We are sure that as the rules governing fluxons propagating on LJJs are fully understood, more functions for manipulating ballistic fluxons will be discovered enabling reversible logic circuits.

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