Doping $CdSe_xTe_{1-x}$/CdTe Graded Absorber Films with Arsenic for Thin-Film Photovoltaics

Amit H. Munshi[1*], Adam H. Danielson[1], Santosh Swain[2], Carey L. Reich[1], Tushar M. Shimpi[1], Seth W. McPherson[2], Kelvin G. Lynn[2], Darius Kuciauskas[3], Andrew Ferguson[3], Jinglong Guo[4], Robert Klie[4] and Walajabad S. Sampath[1]

[1]Colorado State University, Department of Mechanical Engineering, Fort Collins CO 80523, United States
[2]Center for Materials Research, Washington State University, Pullman, WA 99164, United States
[3]National Renewable Energy Laboratory, Golden, CO 80401, United States
[4]University of Illinois at Chicago, Chicago, IL 60607, United States

***Abstract* — CdTe thin-film photovoltaics have demonstrated some of the lowest costs of electricity generation owing to its low material cost and ease of manufacturing. However, the full potential of polycrystalline CdTe photovoltaics can only be realized if the open-circuit voltage can be increased beyond 1 V. Open-circuit voltage ~850-900 mV has been consistently observed for state-of-the-art polycrystalline CdTe solar cells. Open-circuit voltage of over 1V has been demonstrated for single crystal CdTe devices by doping with Group V elements. Therefore, this study is aimed at understanding behavior of polycrystalline CdTe devices with arsenic doping, its activation and process and performance optimization in order to overcome current voltage limitations in CdTe solar cells.**

I. Introduction

Thin-film CdTe photovoltaics is an important technology for large scale electricity production and is recognized as a prominent technology for utility scale energy generation [1]. Owing to its low material cost and ease of manufacturing, CdTe photovoltaics have demonstrated some of the lowest cost of electricity generation, such as the power purchase agreement by First Solar Inc. of ¢3.8/kWh for a 100 MW solar field [2]. With improvements in fabrication methods and understanding of CdTe material properties, research scale small area devices with efficiency of 22.1% [3] and production module of efficiency as high as 18.6% [4] have been fabricated. Academic researchers have fabricated devices with efficiency of 18.7% [5] using CdTe absorber and up to 19.2% using $CdSe_xTe_{1-x}$ (CST)/CdTe graded absorber [6]. All of these high efficiency solar cells have shown improvements in short-circuit current (J_{SC}) and fill-factor, however the open-circuit voltage (V_{OC}) in all of these devices is under 900 mV.

Achieving higher device efficiency in CdTe based technology is primarily limited by V_{OC} remaining well below what is possible for a material with the bandgap of 1.4-1.5 eV. This is demonstrated by the higher V_{OC}s which have been measured for GaAs solar cells, even though GaAs has a comparable or lower band-gap [3][7]. Shockley-Queisser calculations for the thermodynamic efficiency limit predicts that V_{OC} of ~1.2V can be ideally achieved with CdTe (band-gap of ~1.45 eV) [8]. Modeling simulations by Kanevce *et al* suggest that devices with V_{OC} of over 1 V and efficiency over 24% can be fabricated if surface recombination velocity $S \leq 100$ cm/s, bulk recombination lifetime $\tau \geq 10$ ns and doping density $\rho \geq 10^{16}$ cm^{-3} can be achieved [9]. For polycrystalline CdTe-based devices, recombination lifetime $\tau > 400$ ns [10] and surface recombination velocity $S < 100$ cm/s have been demonstrated [11]. Copper is mostly used dopant for CdTe-based devices. However, in addition Cu_{Cd} substitutional acceptor Cu can also exist in interstitial sites as a donor which, being a trap, is not desirable [12][13]. The study by Perrenoud *et al* also shows that doping CdTe devices with Cu may have a fundamental limitation [12]. Group V doping for CdTe and achieving over 1 V V_{OC} and hole density greater than 10^{16} cm^{-3} has been demonstrated for single-crystals [14]. Here arsenic doping is investigated to achieve high p-type doping density while maintaining other desirable properties, which should allow fabrication of polycrystalline CdTe devices with $V_{OC} >$ 1V and efficiency over 22%.

In a past study, $CdSe_xTe_{1-x}$/CdTe:As graded absorber films were fabricated by sublimation and devices with efficiency up to 16.8% were demonstrated [15]. Secondary Ion Mass Spectroscopy (SIMS) depth profile showed arsenic from CdTe:As layer diffusing into the CST layer suggesting doping CST with As may be more favorable. In contrast, in comparison to CdTe, it is more difficult to dope CST with Cu (Sankin and Krasikov, 2019). In this study, bilayer absorber consisting of $CdSe_xTe_{1-x}$ (x=40%) doped with arsenic followed by undoped (?) CdTe is used for fabricating devices and device as well as materials characterization is presented.

II. Experimental

Devices in this study were fabricated on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). A 100 nm $Mg_xZn_{1-x}O$ (x=23%) (MZO) buffer layer was deposited on the TCO using RF sputter deposition. CST:As film was deposited using a co-sublimation hardware designed and fabricated at Colorado State University; a computer aided model of which is shown in figure 1. The fabrication was performed in a two station

sublimation chamber which had one preheating station and one CST:As co-sublimation station containing $CdSe_{0.4}Te_{0.6}$ in the upper source and Cd in the lower source. The substrate was transferred from one station to another without breaking vacuum using a magnetic transfer arm. The co-sublimation hardware's lower source had Cd pellets and was heated to

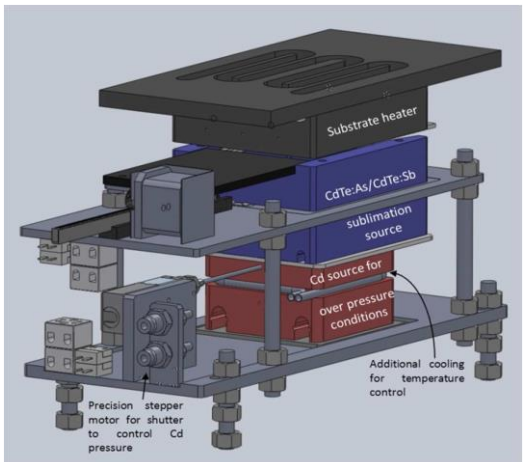

Fig 1. CAD model of the hardware used for this study

~260ºC to provide a Cd-rich environment during $CdSe_xTe_{1-x}$:As deposition [16]. This was done to endure a Cd-rich deposition to avoid formation of As clusters and other defects allowing As to situate itself in Te sites.

Following the deposition of $CdSe_xTe_{1-x}$:As, the films were removed from the sublimation source and stored in vacuum. Thereafter, the substrate was moved into the primary sublimation system with multiple sublimation sources where ~3.5 µm thick CdTe film was deposited and the film stack was passivated using a $CdCl_2$ treatment [17].

To enable studies of As-doped CST absorbers, the $CdSe_xTe_{1-x}$ crystals were grown by high pressure Bridgman technique at Washington State University. For crystal growth, CdTe and CdSe of 6N or higher purity were used as raw material. Arsenic $>10^{20}$ cm^{-3} was added to the raw materials before growth. The mixture was enclosed in a fitting graphite crucible. The CdTe and CdSe were mixed in melt kept at 1160ºC. An inert gas pressure of ~80 atm was maintained in the chamber. The crystal was grown by an imposed growth rate of ~4mm/hr.

A similar device was fabricated using $CdSe_xTe_{1-x}$ (x=20%) (CST20) and CdTe bilayer absorber was used as a reference [18]. This CST20 material had no Group V doping in the source charge. TEC 10 glass substrate was used and 100 nm MZO was deposited identical to the other substrate. 1 µm CST20 was deposited followed by CdTe deposition and $CdCl_2$ passivation treatment. Deposition of CST20 and CdTe were performed in single vacuum chamber with multiple sublimation sources without breaking vacuum [17]. The reference device was treated with CuCl for bulk doping with Cu as well as forming an ohmic back-contact [19].

Following the above process, a 30 nm Te layer was deposited using vacuum evaporation on both the substrates. This Te layer is known to improve from a pure C/Ni paint back-contact leading to higher device performance. These films were then painted with graphite and nickel paint to form the back electrode. 25 devices were delineated on the substrate using a mask and removing the excess material by use of a plastic medium in a masked blasting process. Indium was soldered on the TCO between the delineated cells to form the front contact. The device performance was measured using a Model 10600 solar simulator from ABET Technologies that uses a high-pressure xenon arc lamp with an AM1.5 filter. The current-density vs voltage data was generated based on electrical measurements preformed using the Keithley 2420 SourceMeter controlled by a LabView program. The J_{SC} was calibrated to a CdTe cell measured by National Renewable Energy Laboratory, Golden, Colorado, U.S.A.

III. Discussion

Extensive characterization was performed on the two device structures described in the experimental section. In the J-V measurements of the devices (figure 2A), the device with arsenic doped $CdSe_xTe_{1-x}$ shows higher J_{SC} and lower $V_{OC.}$This is attributed to higher Se content, and thus lower bandgap, in the 1µm at the front of the device. Overall device efficiency and fill-factors were comparable. Both devices had a similar PL intensity (Figure 2B). Slight shift in the band-gap of the $CdSe_xTe_{1-x}$ layers can be clearly seen for x=0.40 (arsenic doped) and x=0.20 absorbers.

To further understand the behavior of the arsenic doped films Time Resolved Photoluminescence (TRPL) measurements were performed at the National Renewable Energy Laboratory. The decays were measured at 819 nm and 870 nm are shown in figure 3. The decay curves were analyzed using a triple exponential function. The highest recombination lifetime was about 7 ns. A typical $CdSe_xTe_{1-x}$ film without arsenic doping in the past has shown TRPL lifetime of about 30 ns [5]. The lower lifetime with arsenic doped material can be attributed to undesirable defects in the film such as arsenic clusters, dimers, tetramers and AX centers [20]. All of these can act as recombination centers in the film leading to low recombination lifetime, high recombination velocity and thus low open-circuit voltage. Low-temperature PL measurements are being performed to identify the defect types and understanding the form of arsenic in the devices.

EQE shows greater carrier collection from blue photons and photons with a wavelength greater than ~850 nm in the film with arsenic doping, which can also be attributed to lower band-gap CST material (figure 2C). Capacitance vs voltage plot suggests greater carrier concentration with arsenic doped material (figure 2D and 2E).

Further characterization using methods such as time-resolved photoluminescence (TRPL), low-temperature PL, DLTS and SIMS is in progress to achieve a better

understanding of behavior, concentration and activation of arsenic in the fabricated devices. Arsenic activation experiments are also under progress as have been described in literature. Furthermore, fabrication of devices with different device structures such as using arsenic doped CdTe source charge and undoped $CdSe_xTe_{1-x}$ are being planned.

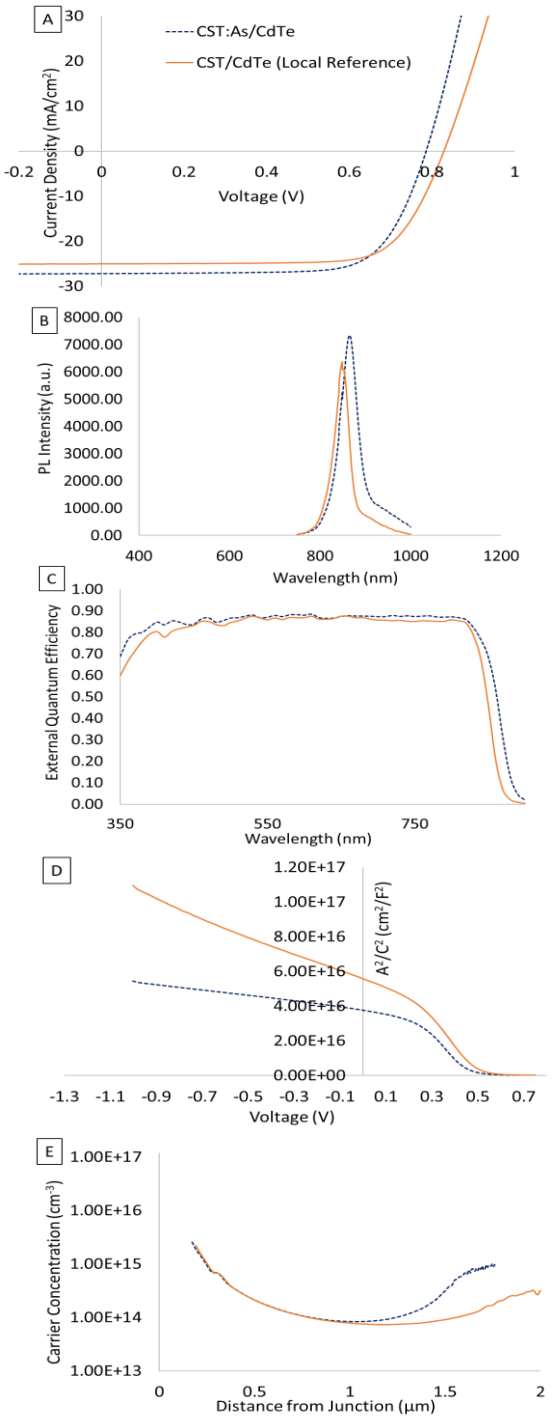

Fig 2. (A) Current density vs voltage, (B) Photoluminescence emission spectra, (C) External quantum efficiency (D) capacitance vs voltage, (E) carrier concentration vs distance for devices under study.

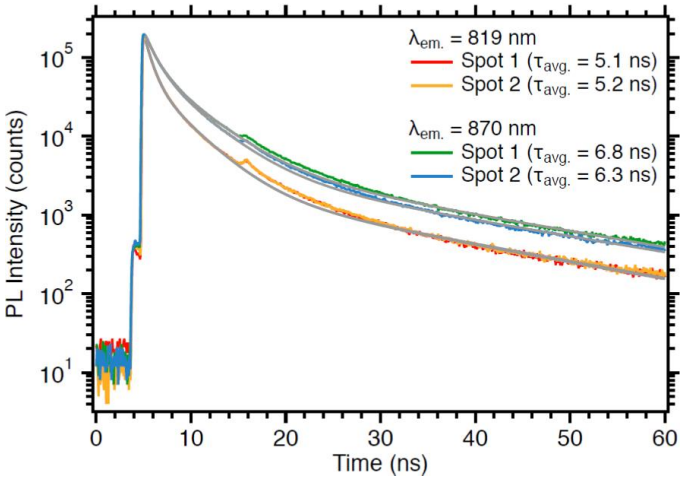

Fig 3. Time Resolved Photoluminescence measurement performed on arsenic doped device with two difference emission band-pass filters.

IV. Conclusions

Based on current characterization it can be deduced that arsenic doping is effective in the deposited films. Activation of arsenic as a dopant may lead to better device efficiencies and higher open-circuit voltage. Currently the activation of arsenic is a fundamental challenge. Further investigation of various post deposition annealing and post deposition annealing under cadmium vapor is planned. Such treatments have shown promise in studies by other research groups and their impact on current device structures will be critical to our device performance.

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