

Analysis of Defect Clustering in Semiconductors using Kinetic Monte Carlo Methods

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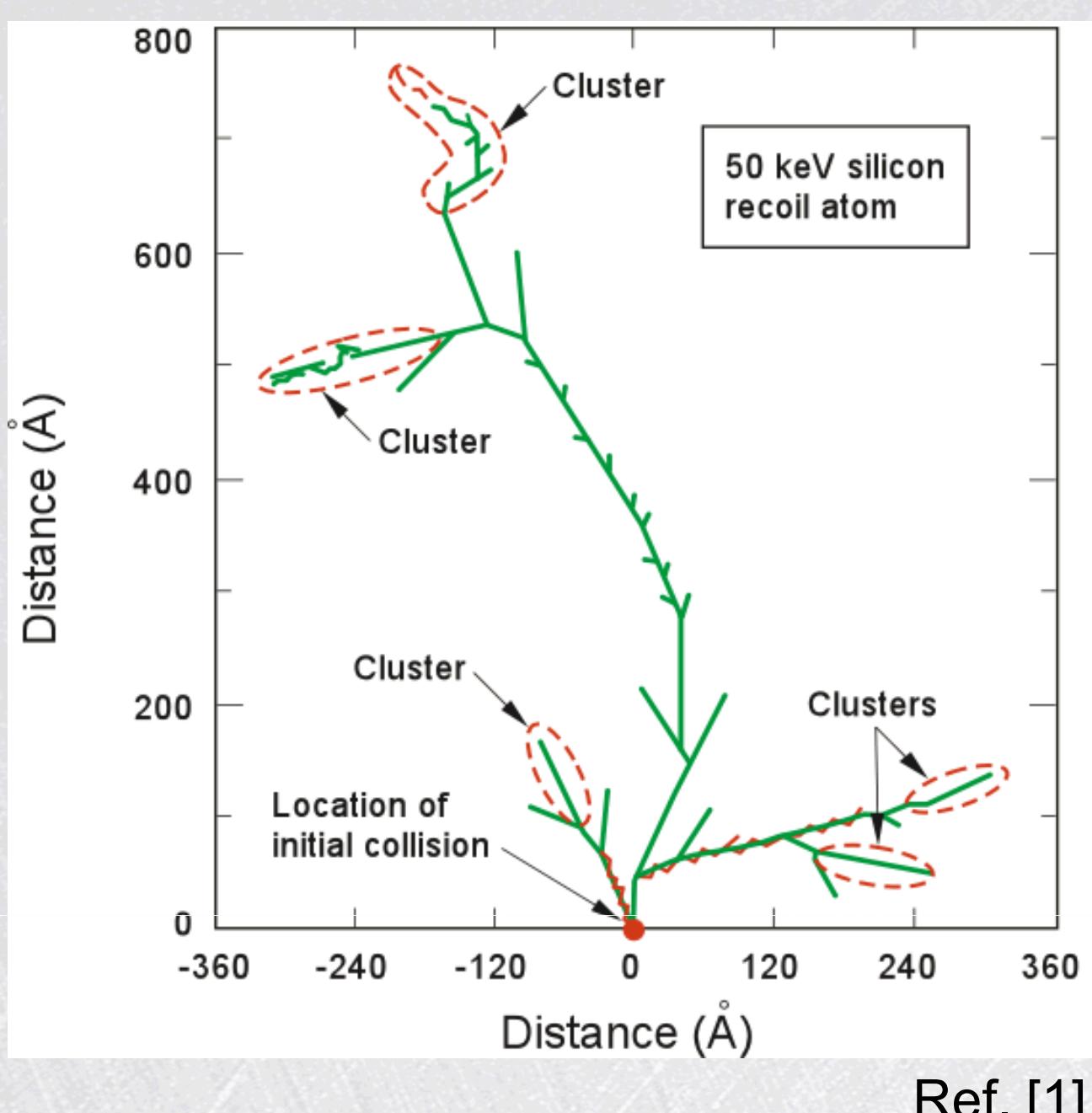


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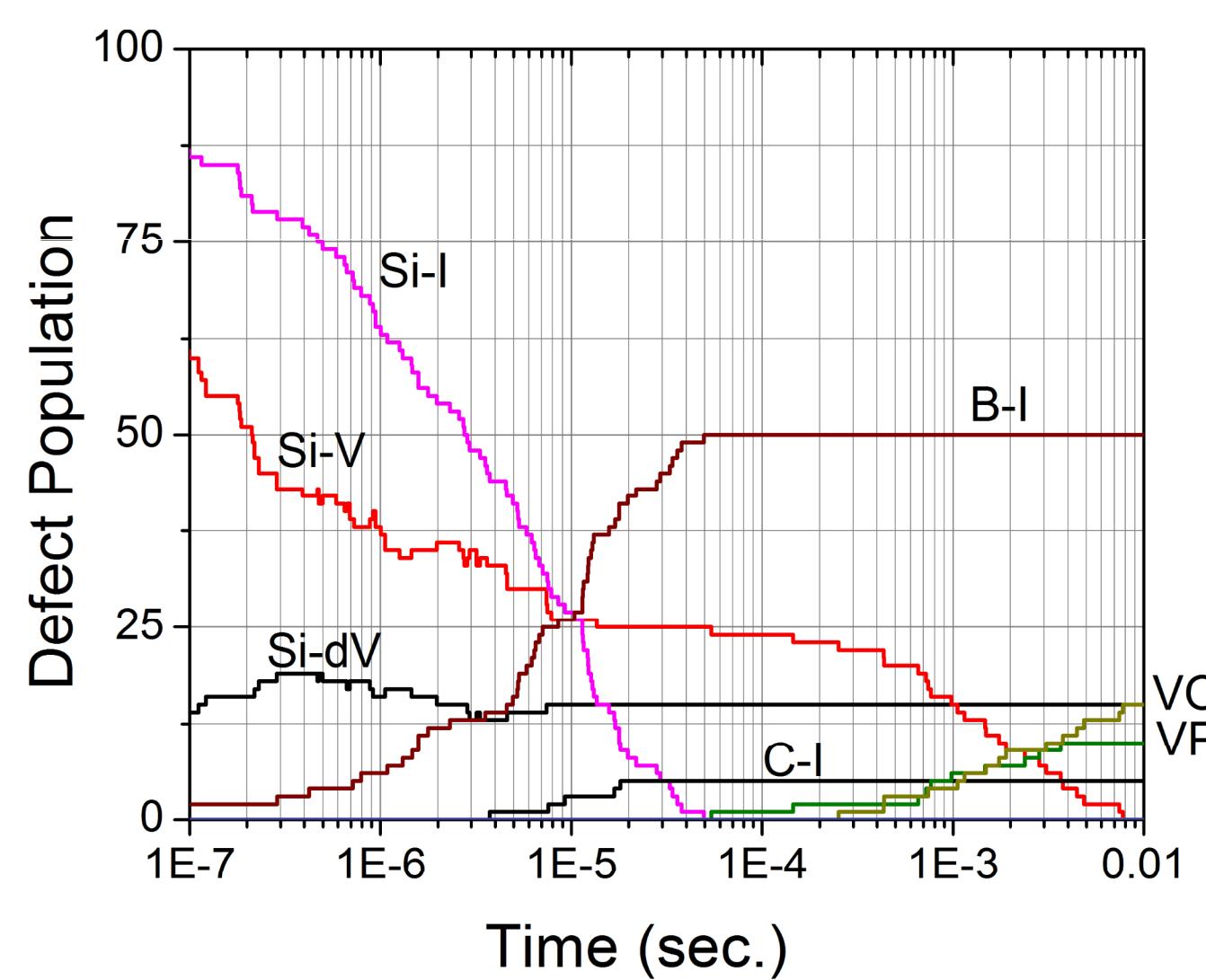
Problem

- The transient degradation of semiconductor device performance under irradiation has long been an issue of concern.
- Typically, the initial defect formation phase is followed by a recovery phase. Clustering of defects, in particular, can have a significant impact on the annealing process.
- The purpose of this project is to develop a kinetic Monte Carlo (KMC) code capable of modeling both thermal and carrier injection annealing



Ref. [1]

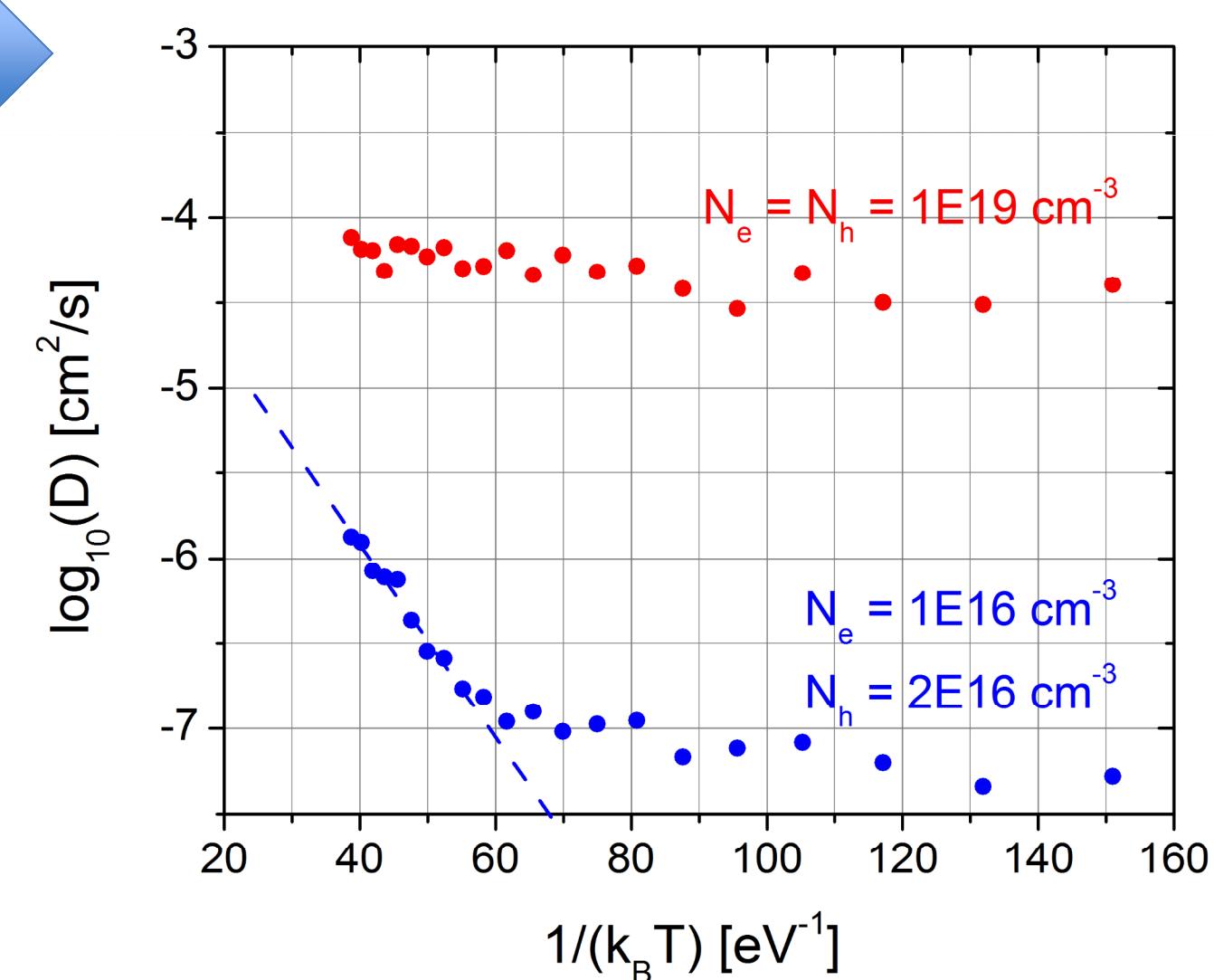
Results



Defect population vs. time within a single cluster at the depletion region midpoint

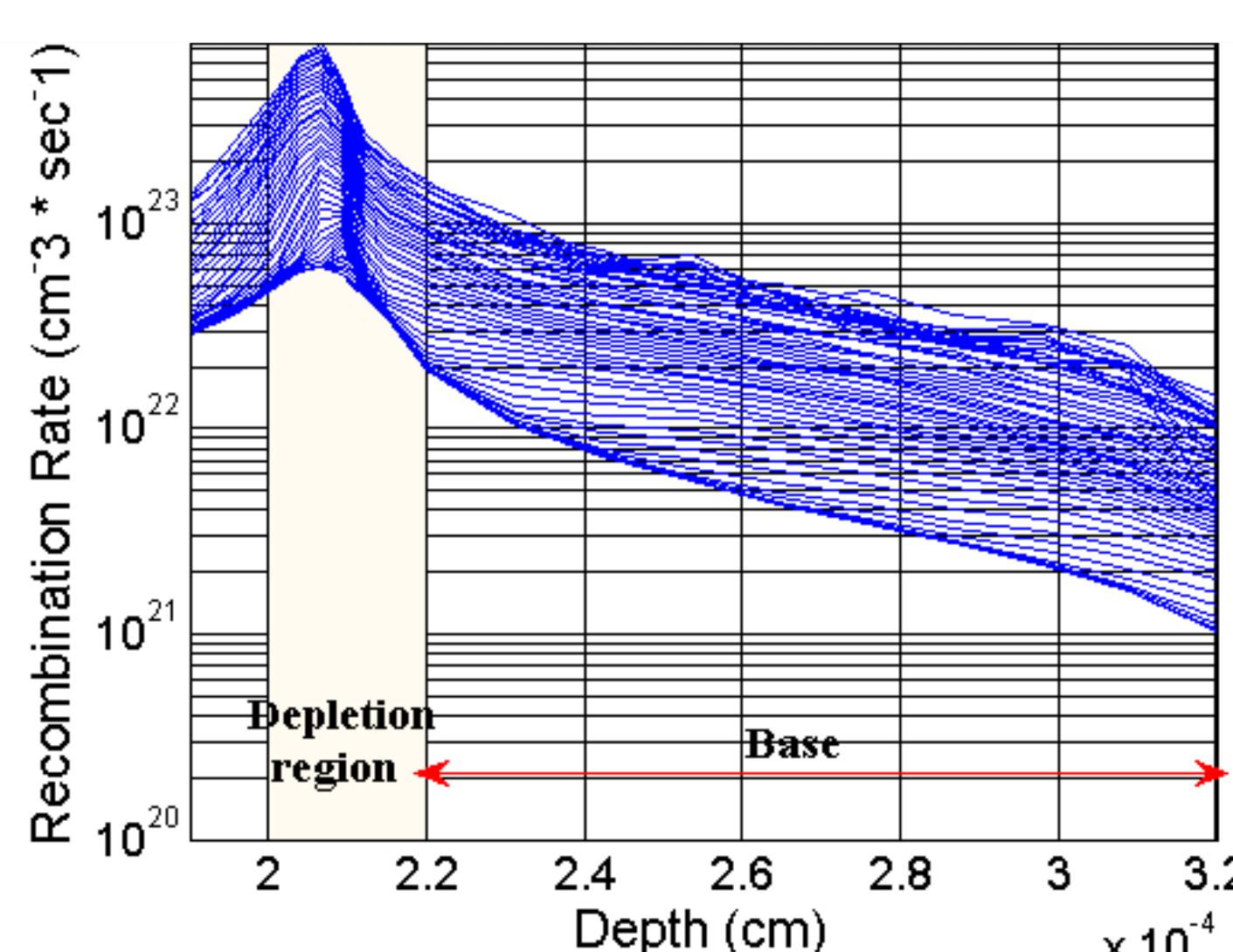
Defect-impurity complexes become important at late times

Calculated diffusion coefficient of Si-I vs. temperature and carrier concentration



Athermal migration dominates at low temperatures

Thermal migration dominates at higher temperatures (see dashed line)



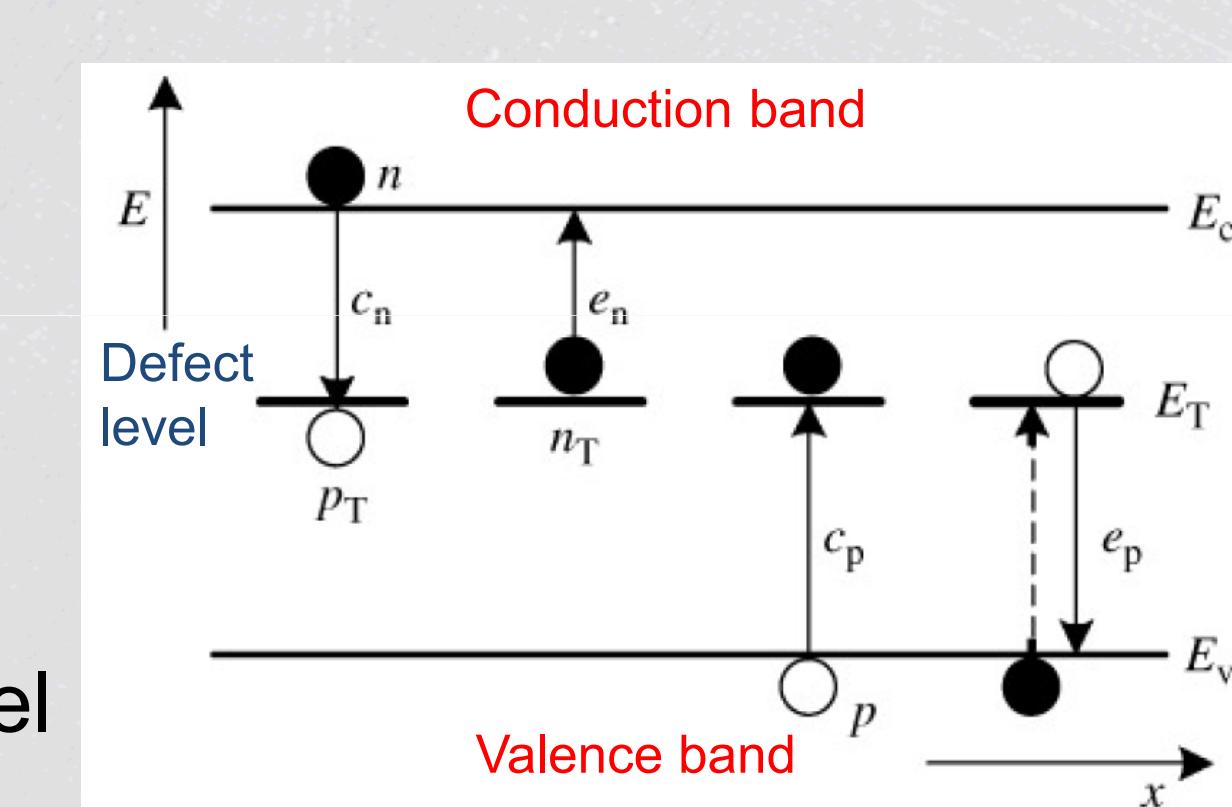
Time-lapse plot of carrier recombination rate vs. time and depth in a 2N2222 npn transistor driven at 9 mA.

Interval (log spaced): 0 – 1 ms

Comparisons ongoing against data from:
• LANSCE neutron irradi.
• Electron irradi. of bulk p-type silicon

Problem definition:

- Initial defect arrays obtained from MARLOWE code
- Defect cluster surrounded by array of discrete impurity atoms
- Boundary conditions can be cubic or ellipsoidal



Can determine, as a function of time:

- Defect populations and positions
- Carrier recombination rate
- Carrier concentrations, consistent with periodic boundaries (no device model coupling yet)

Significance

The transient annealing of semiconductor devices is a critical factor in assessing their performance during and after irradiation. Operational parameters such as transistor gain vary based on the microscopic details of defect motion and interaction within the device. This project provides the capability to evaluate defect evolution and its effects using a fundamental, physics-based approach which will enable greater accuracy in device- and circuit-level performance assessments.

[1] S. Kayali, "Space Radiation Effects on Microelectronics." JPL, Section 514.
[2] P. A. Schultz. Phys. Rev. Lett., **96**, 246401 (2006).