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Reliability Evaluation and Prediction of Commercial 4H-SiC Power MOSFETs

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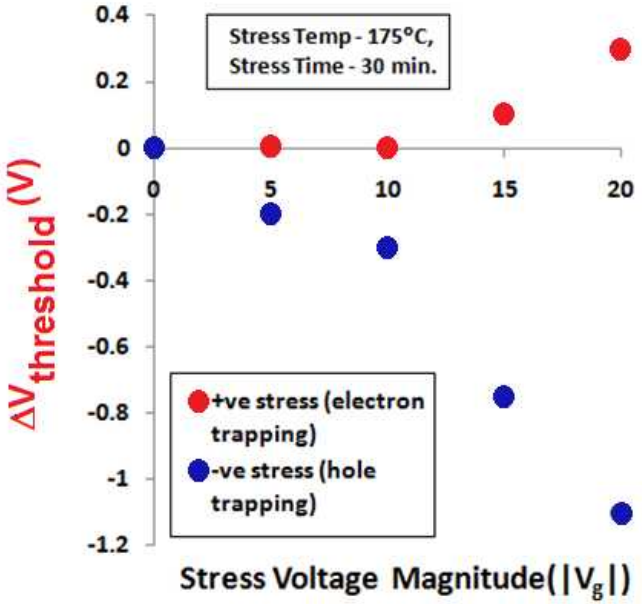
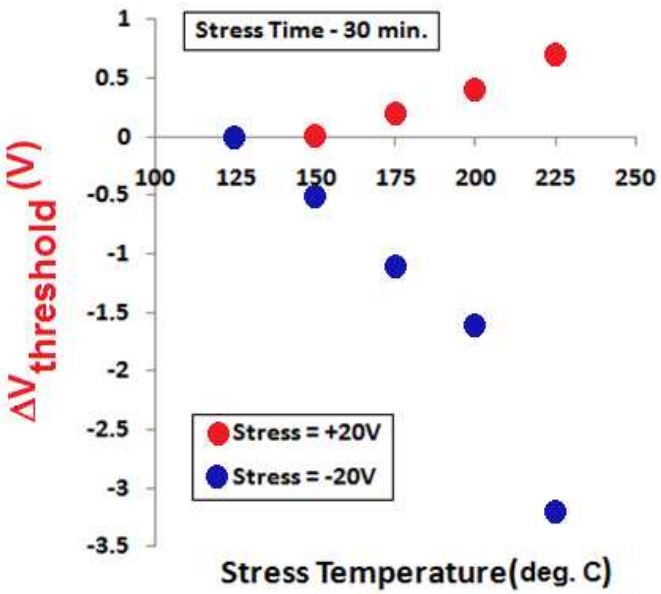
Overview

- **Reliability Evaluation of Commercial (1200 V, 33 A, $T_{j,max}$ = 125°C) 4H-SiC MOSFETs :**
  - **DC stress, electron vs hole trapping**
  - **Can degradation be predicted from starting device characteristics ?**
    - **Freewheeling diode ideality factor and hole trapping.**
  - **Pulsed Overcurrent Operation**
- **Separation of D_{IT} and near interface trapped charge and N_{OT} from subthreshold *I-V***

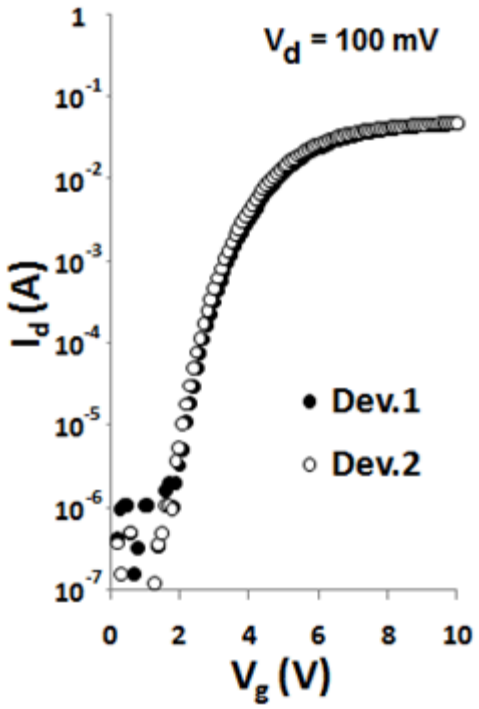
Trapping at High Temp & Bias



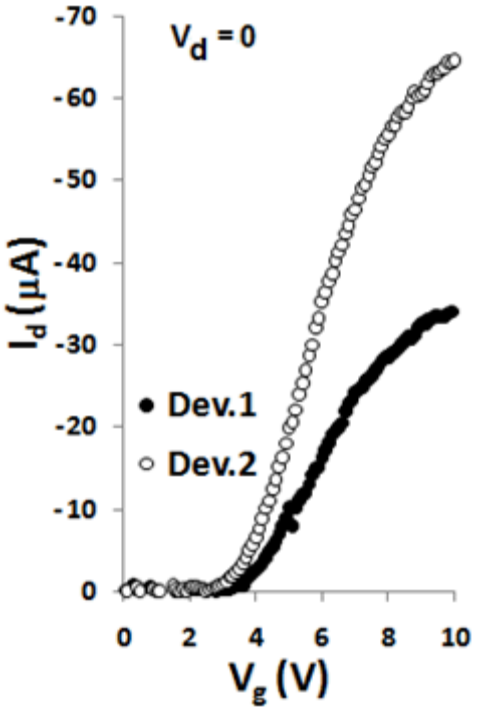


- **No V_{th} instability up to 125°C over Vg = ±20 V**
- **Hole trapping more efficient then electron trapping for a given bias and temperature**
- **Both kinds of trapping completely recoverable under opposite bias and same temperature.**

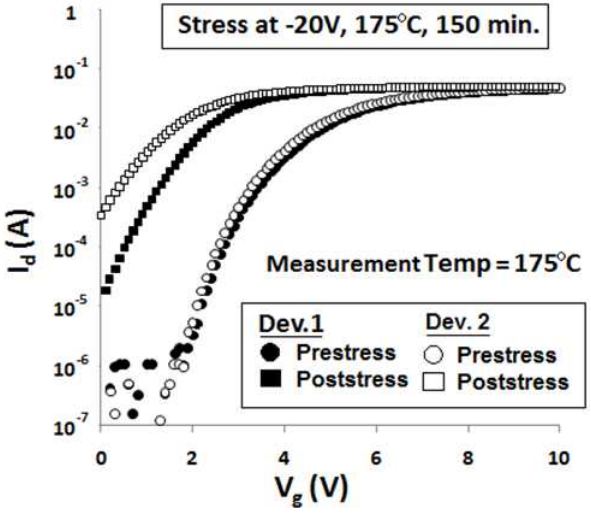
Initial Device Uniformity and Hole Trapping Characterization

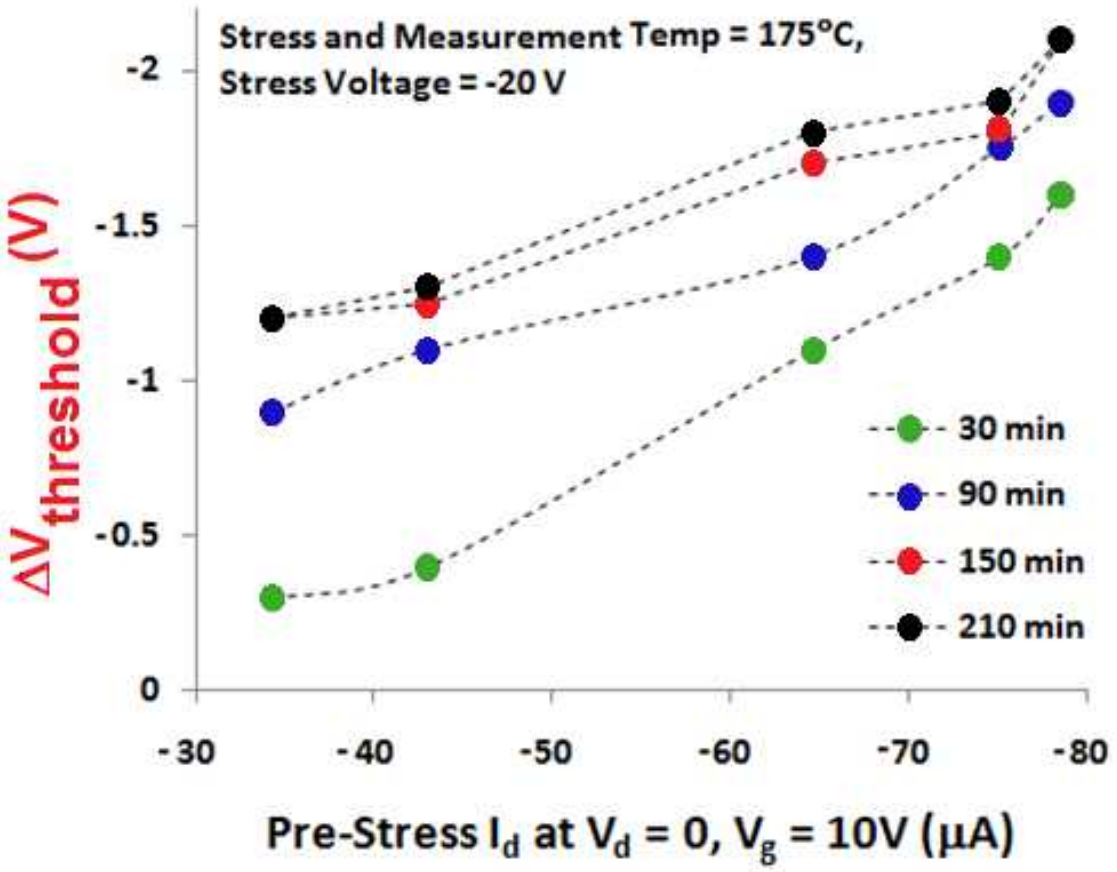


- **Excellent uniformity in all devices, even for the subthreshold V_{th} for nonzero drain bias**
- **Significant drain current at zero drain bias with positive V_g**
- **Zero bias drain current correlates well to hole trapping efficiency**



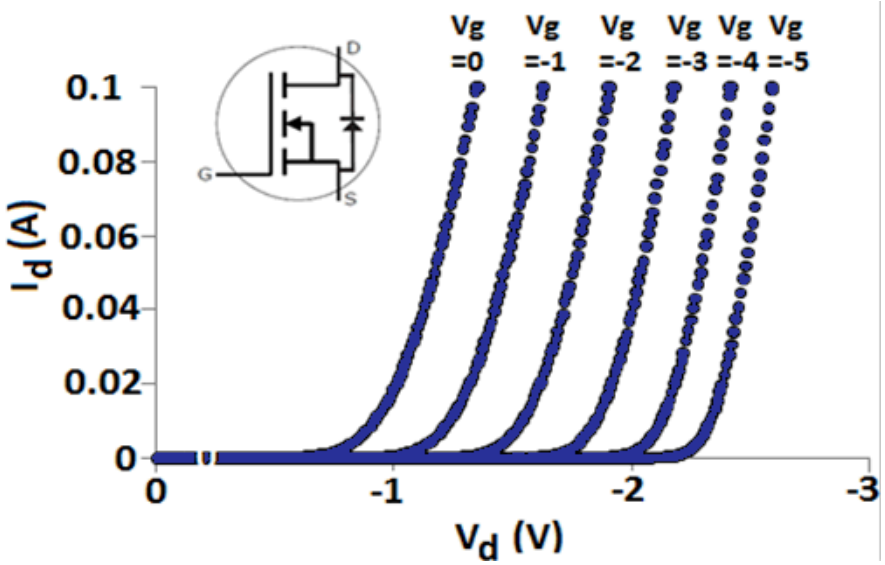
Zero Bias I_d and Hole Trapping

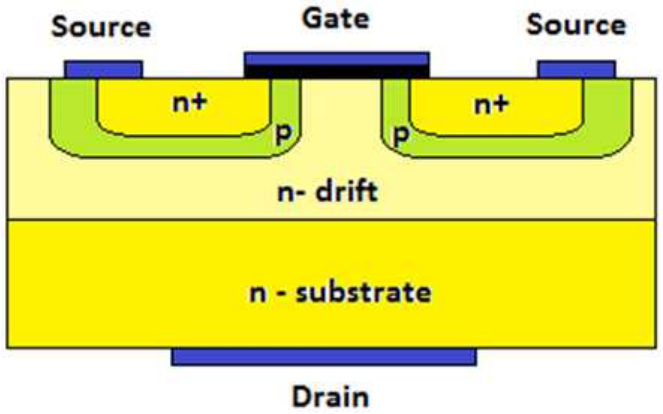




Both hole trapping rate and saturation values of V_{th} shift show strong correlation to pre-stress zero-bias I_d

Cause of Nonzero I_d at Zero V_d – The Freewheeling Diode

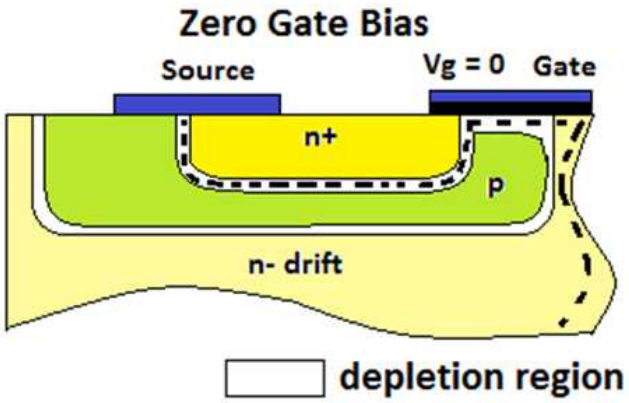


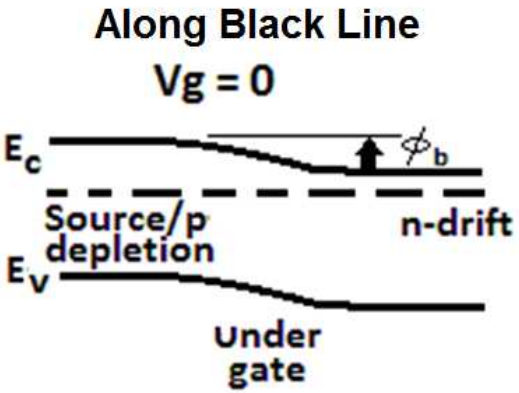


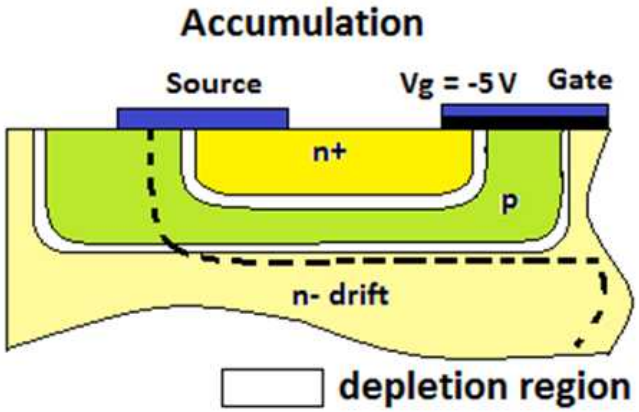
- **Freewheeling diode – for protection against discharging inductive loads in off-state**
- **Strong dependence on V_g**

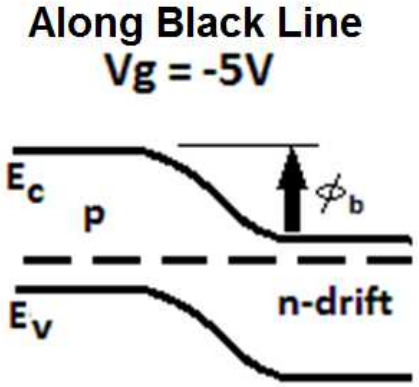
At V_G=0, diode turn-on voltage of ~0.8 V is too low to be the built-in potential between bulk p & bulk n-type in 4H-SiC

Diode Turn-on Paths







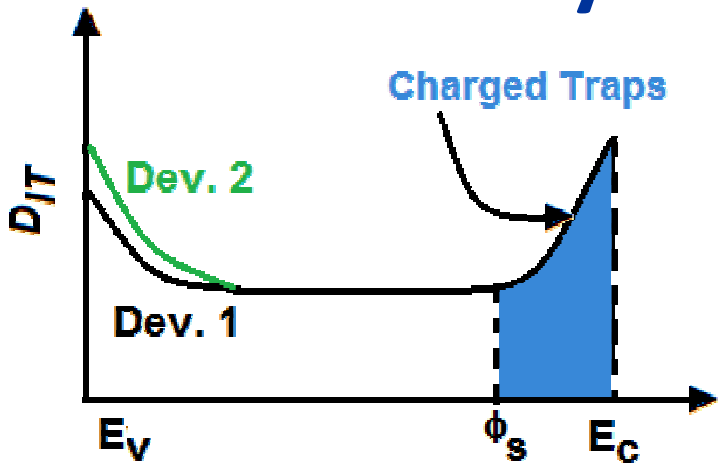


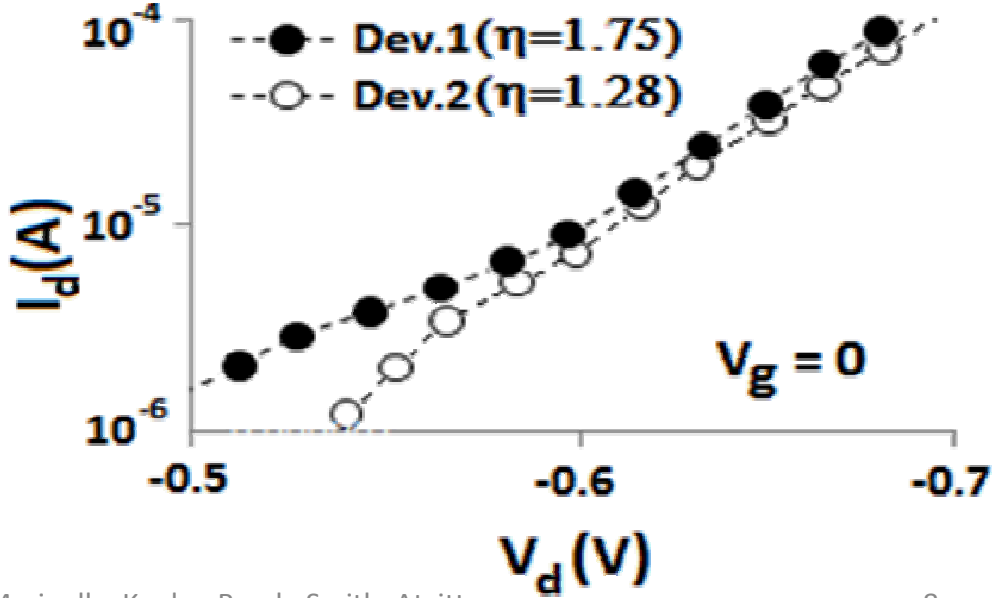
- Zero gate bias – turn-on path at surface.
- High negative gate voltage – turn on path goes to p/n boundary

Reducing diode potential barrier by applying gate bias causes zero bias I_d – consistent with direction of current (source to drain – diode fwd. current)

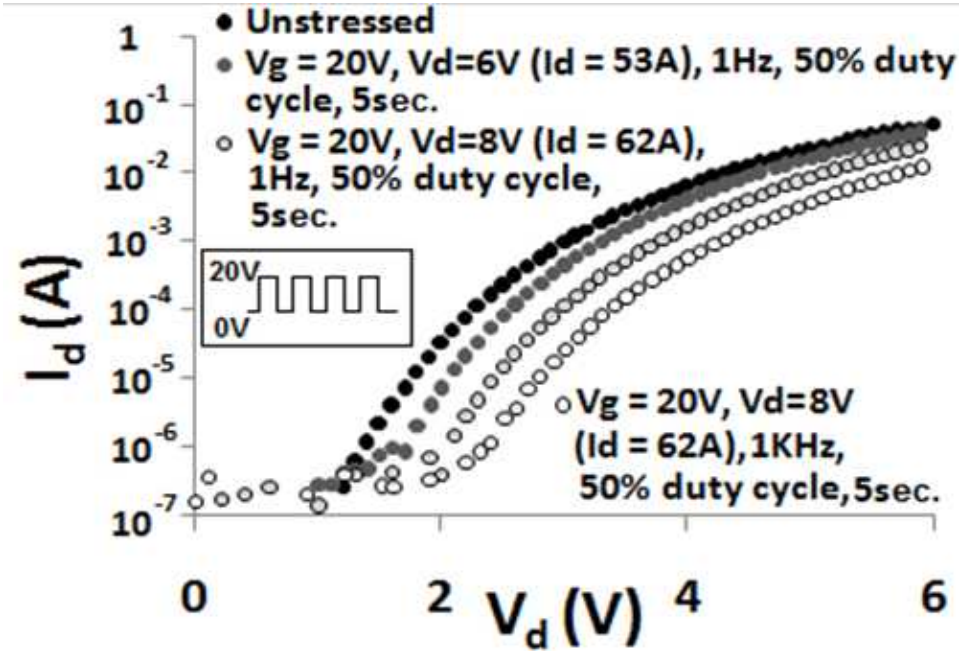
Correlation Between Hole Trapping VB edge D_{IT}, and Diode Ideality

- Higher VB edge D_{IT} lowers the surface fields at high positive gate bias → this decreases hole trapping
- This is consistent with higher FW diode η due to greater recombination current in devices less prone to hole trapping
- If interface traps are neutral when filled, subV_T I-V not affected by difference in VB edge D_{IT}



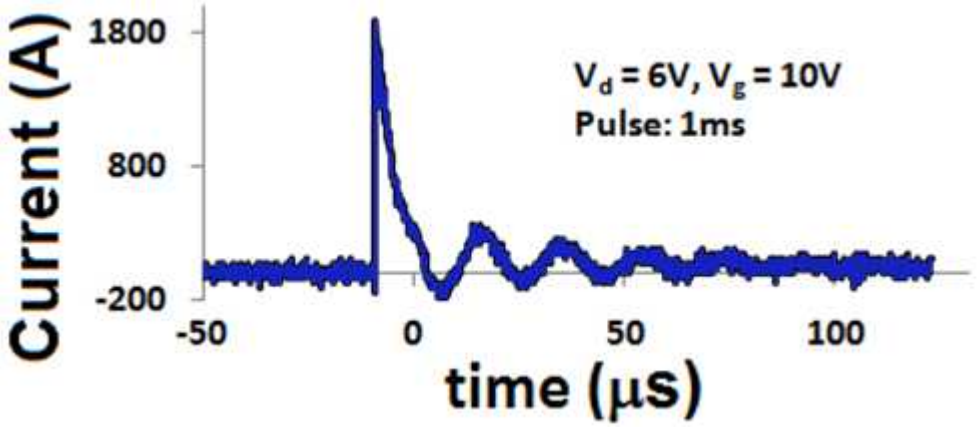


Pulsed Overcurrent

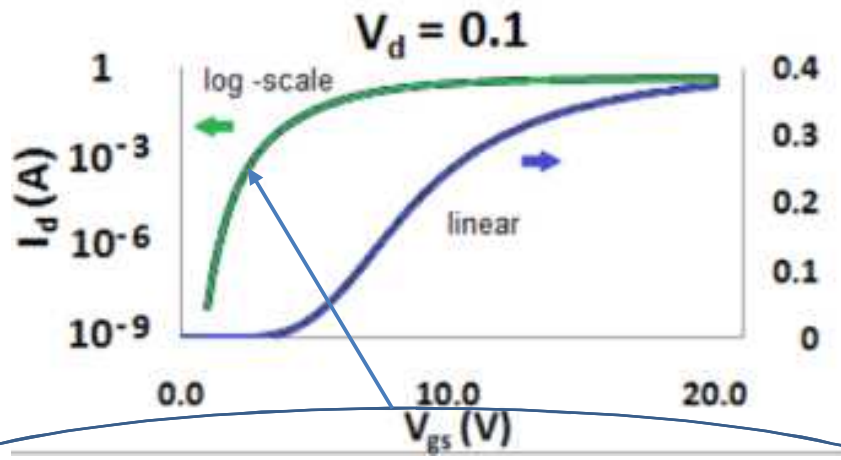


Rise in junction temperature above spec at positive V_G increases electron trapping

High frequency switching – high transient current pulse introduces more trapping



Near CB Edge D_{IT} and subV_T Slope



Non-constant subthreshold slope, high D_{IT} gradient

In FET subthreshold region,

$I_d = Ke^{qVa/KT}$,
or $d\ln I_d = q dV_a/KT$.

For significant N_{IT}, $I_d = Ke^{q(Va - VIT)/KT}$,
For significantly large V_{IT} not proportional to V_a, subthreshold slope is non-constant.

D_{IT} Extraction From subV_T Slope

In subthreshold operation, surface potential controls current,

$$I_D = \mu_n (Z/L)(aC_i/2\beta^2)(n_i/N_A)^2(1-e^{-\beta V_D})e^{\beta\varphi_s}(\beta\varphi_s)^{-1/2}$$

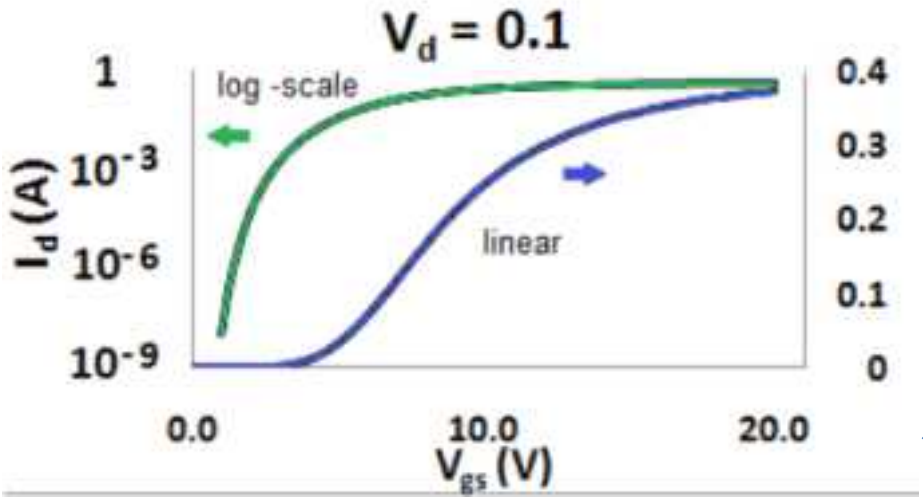
Surface potential $\rightarrow$ Gate Voltage

$$\varphi_s = (V_G - V_{FB}) - a^2/2\beta\{[1+4/a^2(\beta V_G - \beta V_{FB} - 1)]^{1/2} - 1\}$$

In presence of D_{IT},

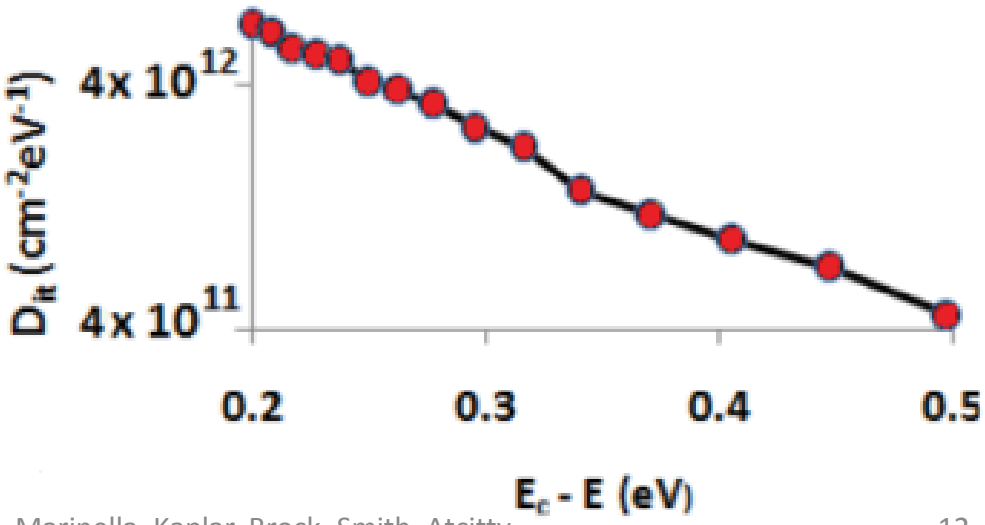
$$\varphi_s = (V_G - V_{FB} - V_{IT}) - a^2/2\beta\{[1+4/a^2(\beta V_G - \beta V_{FB} - \beta V_{IT} - 1)]^{1/2} - 1\}$$

D_{IT} Extraction From subV_T Slope

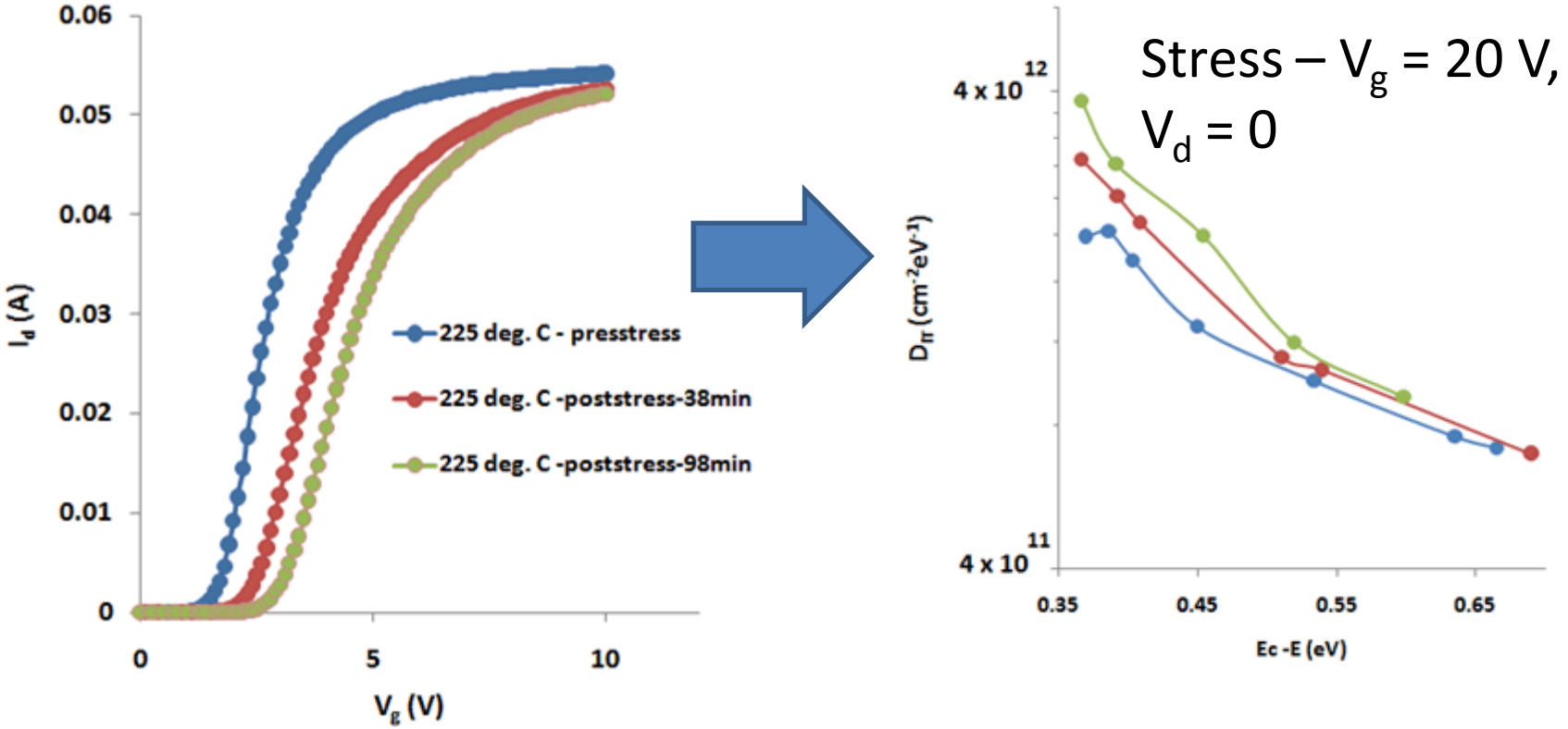


Low noise measurement systems → accumulation voltages → larger fraction of bandgap

D_{it} values similar to reported SiC MOS D_{it} extracted through C-V techniques

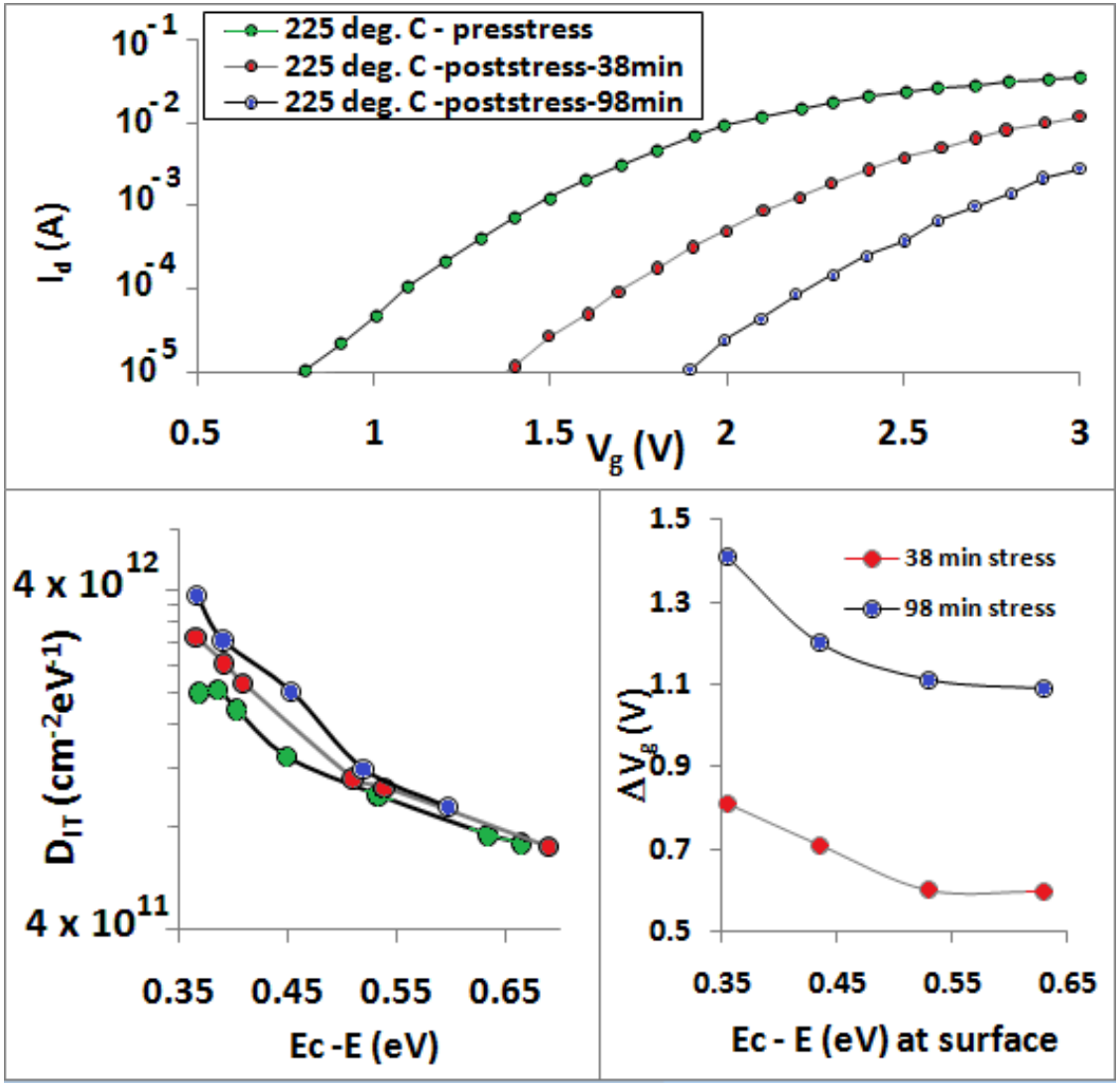


Devices Fabricated with Older Process



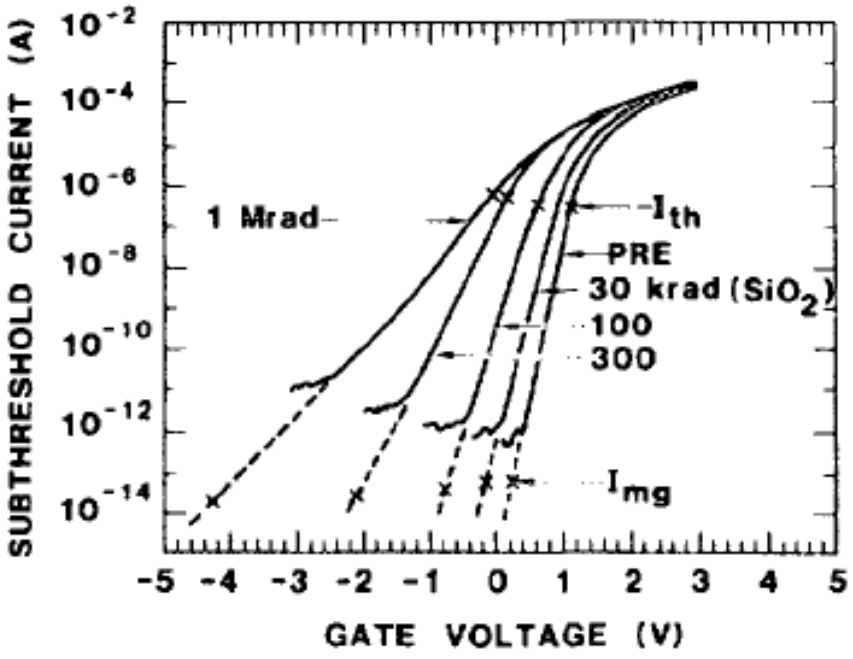
- D_{IT} increases under high-temperature high-field stress
- No negative bias, so measurement not likely to be contaminated by slower (ms range) emission of trapped carriers

Contribution of D_{IT} to V_{th} Shift



- ~ 0.5 eV from CB, ΔD_{IT}, and Δ subV_T slope are almost zero
- Incremental V_G to maintain same I_G flattens out

Separation of D_{IT} from Slow Traps: Winokur – McWhorter Model



$$\Delta V_{ot} = \Delta V_{mg}$$
$$\Delta V_{it} = \Delta V_{th} - \Delta V_{mg}$$

- **Negligible contribution of interface traps towards midgap to net voltage shift in SiC.**
- **ΔV_{mg} can be extrapolated with better accuracy.**

Extracted ΔN_{ot} - 4.4×10^{11} cm^{-2} and 2.46×10^{11} cm^{-2} at 98 and 38 min (reasonable)

Summary

- **Detailed reliability characterization of commercial (1200 V, 33 A) 4H-SiC MOSFETs :**
  - **Hole trapping heavier than electron trapping**
  - **I_d at zero V_d and freewheeling diode ideality factor in unstressed device good indicators of vulnerability to hole trapping**
  - **Degradation under pulsed overcurrent operation similar to electron trapping at high temperatures**

- **Simple technique to derive D_{IT} and N_{OT} from subV_T *I-V* discussed**

Questions & Discussion