SAND2011-8563P

Enhanced High Temperature Power Controller

Frank Maldonado, Sandia National Laboratories
PO Box 5800
Albuquerque, New Mexico 87185
Ph: (505)284-3533, Fax: (505)844-3952, email: fjmaldo@sandia.gov

Abstract

This paper describes an implementation strategy used to develop a high temperature power controller. The system is based on using high-temperature (HT) silicon-on-insulator (SOI) technology with silicon carbide (SiC) based integrated circuits (ICs) to create an efficient, high-temperature power controller. The development of the controller implements a pulse-width modulation (pwm) scheme in a minimal design space. Such circuit designs will improve the efficiency of future smart grid power controllers.

Keywords: SOI, SiC, Power Controller, High Temperature, H-bridge, JFET, Smart Grid, Pulse width modulation (PWM)

Background

In the coming years, modernization of the U.S. power grid will necessitate finding solutions to improve the distribution networks and decrease the size of the system components. At the heart of this modernization is the need to reduce energy loss throughout the grid and reduce peak power load at the power plant. Concepts such as 'microgrids' or 'smart grids' are emerging and will depend on exercising a high level of control over the electric utility delivery system to increase the system's efficiency, reliability, robustness, and flexibility. Such systems will use intelligent controls based on digital communication and sensors to maximize benefits of various local alternative energy sources by controlling system loads or power flow.

These new types of system controls must operate efficiently and be non-intrusive. That is, they must operate in the background with high levels of reliability over their design life. Many of these new power conversion systems could be utilized between the power plant and consumer. The applications for these controls include transportable energy storage systems (Figure 1) that can be quickly and easily added to the grid for peak shaving, grid stabilization, or VAR compensation, to name a few.

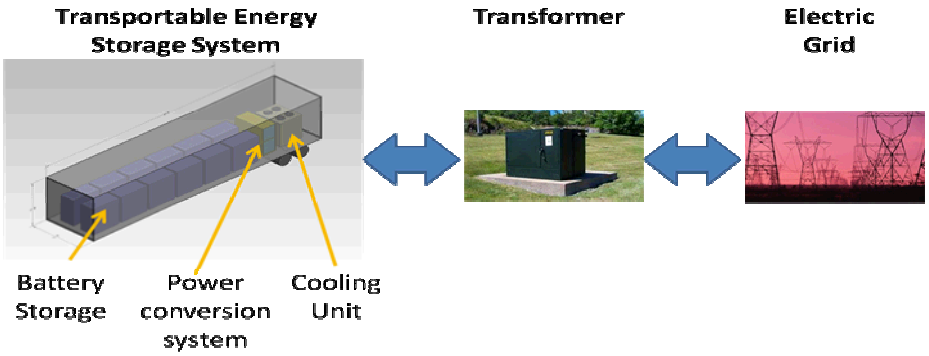


Figure 1. Transportable energy system with grid interface

A transportable energy storage system includes battery storage, a power conversion unit, and a large cooling unit. The power conversion unit is an inverter with many subcomponents, including a power controller, gate drive, power stage, AC disconnects, DC disconnects, communications, and filtering.

The current method of deployment of these systems involves using standard electronic components that are dependent on large cooling units to keep the temperatures of the electronics within their operating range. The cooling units typically control the environment to 75°F (24°C). This need requires the cooling units to be scaled adequately for operation in harsh environments where the transportable energy systems are deployed. Internal temperatures due to the external environment and heat generated from the power switching can easily exceed 150°F (65°C). The cooling unit limits the power density of the transportable system in two ways: 1) The space needed by the cooling unit could be used for additional battery storage and power conversion components, and 2) the energy required to operate the cooling unit reduces the overall power contribution of this system to the grid.

Sandia National Laboratories is working to design a portion of the power conversion unit based on high temperature electronics with the target of reducing the size of the individual power controllers up to 30% and increasing the power density by a factor of 2.

Project Description

The focus of Sandia's program is the design and development of an integrated power controller, gate drive, and power stage into a single, minimal space design that requires no active cooling. The high temperature electronics for the power controller utilize SOI components and are being integrated with a gate drive and power stage that make use of SiC power devices. The system creates the basic building block for power converters and is applicable to other applications beyond the focus of this project. The target operating temperature for the system is 240°C. This temperature was selected based on the temperature limits of the electronic components available.

This project is a collaborative effort of a small team at Sandia National Laboratories. There are two major areas of focus for the team: the gate drive/power stage and the power controller. The gate drive/power stage and board layout were performed by other members of the team. My focus is on the development of the power controller, particularly the field programmable gate array (FPGA) used to perform the control logic. The following discussion will focus on the development of the controller, in particular the first stage of its design which is focused on building a pulse-width modulation controller that utilizes minimal space within the FPGA. Later stages, such as smart grid interface communications, will need to make use of the remaining space.

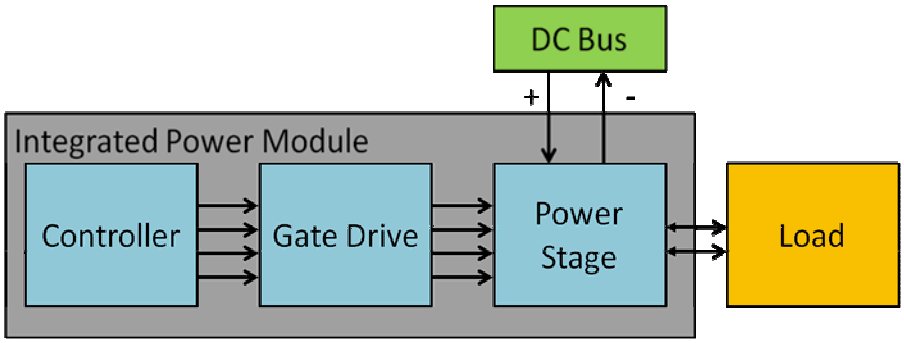


Figure 2. High Level System Description

Specifications

The desired system operating temperature is 240°C. At this temperature, few electronics exist. The high temperature electronics that do exist, as mentioned above, employ either SOI or SiC technology. The available device options are severely limited in comparison to today's standard device options. For this design, the key components are a field programmable gate array (FPGA) and an analog-to-digital converter (ADC).

An FPGA is a configurable logic device that allows the user to design logic to perform desired functions. Unlike a microcontroller, it has the ability to perform multiple tasks in parallel, making it substantially faster. A high temperature FPGA is currently still in development, but is very small in comparison to a modern day design. The architecture is based on an obsolete chip design from approximately 20 years ago. For development, we are using a low temperature FPGA similar in size to the HT FPGA being developed. For relative comparison, a modern day FPGA will have up to 2 million logic cells while the FPGA we will be using has 1,232 logic cells. This requires the design to be very efficient to achieve the desired functionality. A common design technique for modern FPGA development is to use IP cores. These cores are commonly used component that are optimized for each device. This allows the user to quickly build designs by using previously developed components. Due to the age of the architecture we must use, there are no IP cores available for these FPGAs to drop into the design, so the code will need to be developed. The low temperature FPGA being used is an Actel A42MX16 84-pin device. It is built using anti-fuse technology, which is a single-burn device that cannot be reprogrammed.

The ADC being used has 10-bit resolution (1024 quantization levels) and a maximum sampling speed of 25kS/s. It accepts a 0-10V input, creating 102.4 levels/V. It was determined to use a 20kHz sampling frequency instead of the maximum sampling speed to allow for derating of the ADC due to temperature. The ADC is a Cissoid CHT-1074 (it has since been renamed CHT-ADC10) and is rated to 225°C, although it has been successfully tested to 240°C.

Theory of Inverter Operation

The power system being implemented is a single-phase voltage source inverter using an H-bridge configuration to drive a load. For our demonstration the load will be a motor.

The topology of the inverter consists of four switching devices (SiC JFET devices) connected in the form of a bridge with two legs and a load connected between. Each leg has a high side switch connected to the upper DC rail and a low side switch connected to the lower DC rail.

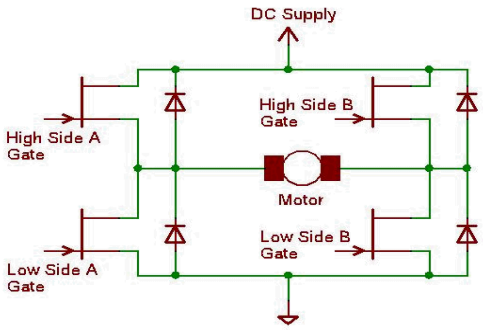


Figure 3. Single-phase H-bridge voltage source inverter

In order to drive the H-bridge switching mechanism, a pulse-width modulation (pwm) scheme is used. The system uses a unipolar three-level naturally sampled sine-triangle pwm process to drive the gates of the bridge. Using this method will decrease the amplitude of the voltage harmonics and, coupled with using a 20kHz sampling frequency (which effectively maximizes the use of the ADC) decrease the size of the filter components required to achieve a low total harmonic distortion (THD).

The unipolar three-level modulation method uses a triangular carrier waveform (V_{tri}) and two sinusoidal fundamental waveforms 180° opposed for each leg ($V_{ref,}$ - V_{ref}). The fundamental phase legs may be defined by

$$v_{az}^* = V_{dc}M\cos(w_0 t)$$

$$v_{bz}^* = V_{dc}M\cos(w_0 t - \pi)$$

where

V_{dc} = DC bus voltage

M = modulation index, the normalized output voltage magnitude ($0 < M < 1$)

w_0 = target output angular frequency

v_{az}^*, v_{bz}^* = Fundamental phase leg voltages referenced to the DC bus voltage zero midpoint

The line-to-line output voltage across the two legs is given by

$$v_{ab} = v_{az}^* - v_{bz}^* = 2V_{dc}M\cos(w_0 t)$$

The output from this system is a three-level naturally sampled sine-triangle pwm with the three levels being $+2V_{dc}$, $-2V_{dc}$, and the zero midpoint (Figure 4).

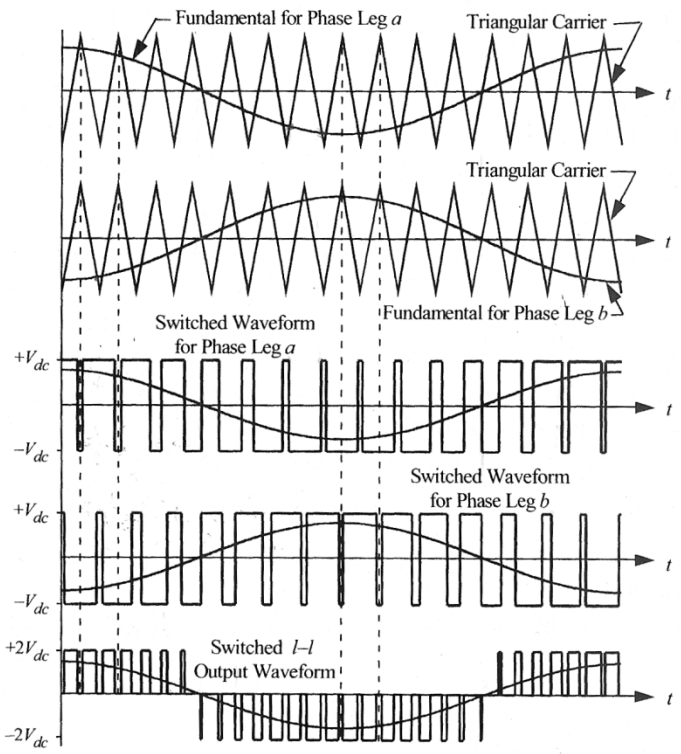


Figure 4. Three-level modulation method

The modulation of a phase leg must have the high side and low side switch operate complementary to one another. If this does not take place a condition referred to as "shoot through" may occur, in which both switches enter an "on" state at the same time, creating a short across the voltage bus through the phase leg. This is a very dangerous state that will damage the system.

Referring to Figure 4, Leg A and Leg B are controlled separately. Leg A is controlled by comparing the carrier waveform (V_{tri}) to V_{ref}; Leg B uses the comparison between V_{tri} and $-V_{ref}$. The switches states operate as follows:

$V_{ref} > V_{tri}$: High side gate A ON

$V_{ref} < V_{tri}$: Low side gate A ON

$-V_{ref} > V_{tri}$: High side gate B ON

$-V_{ref} < V_{tri}$: Low side gate B ON

Controller Design

The input to the system is a 60Hz sine wave (6Vpp, 5Vdc offset) that is wired into the ADC. This input in reality would be the line voltage from the utility which our system would need to synchronize. For the demonstration it is fed into the circuit from a signal generator.

Another consideration for the H-bridge is the timing of the switching sequences. If both legs switch simultaneously, an unknown state can occur, resulting in possible damage to the devices or the motor, or causing undesirable transients through the system. To mitigate this effect, a 1.4us delay between any phase leg switching is implemented.

Startup of this circuit could put the outputs in an undesirable state. When the circuit is initially powered, the FPGA will hold the gate controls in an off state to allow the ADC and other functions to settle to steady state.

The ADC samples the fundamental waveform every 20kHz. The controller uses zero-order hold to obtain the ADC value for the sampling interval during which time each phase leg will modulate when a crossing between the carrier and each respective fundamental occurs.

Timing of the system will help determine what resolution is expected from the system. The input sine wave is known to range from 2V to 8V. Applying the transfer function of the CHT-ADC10,

$$D = Offset+(A-A_{min})*(1024/(A_{max}-A_{min}))*(1-GE/100)$$

where

D=Digital value (dv)

A = Analog input value

A_{min} = lowest value of selected analog input range

A_{max} = highest value of selected analog input range

Offset = value of D when $A=A_{min}$. Temperature dependent, ideal case = 0

GE = Gain Error (in %). Temperature dependent, ideal case = 0

The expected range is determined,

$$ADC_{min} = 0+(2V-0V)*(1024/(10-0))*(1-0) = 204.8 \approx 205$$

$$ADC_{max} = 0+(8V-0V)*(1024/(10-0))*(1-0) = 819.2 \approx 819$$

$ADC_{range} = ADC_{max} - ADC_{min} = 819 – 205 = 614$

The gate controls need to have a duty cycle greater than zero, so the carrier must have a range greater than 614 dv. Using a 16.384MHz clock to control the system means that for a 20kHz sampling rate, there are a maximum of 819 dv that the carrier may span.

$Carrier_{dv} = 16.384MHz/20kHz = 819$

Since the ADC should have a range of 614 dv (this number may vary due to noise in the system), there are approximately 205 clock periods (819 – 614) to collect new samples and condition appropriately prior to the next modulation cycle of the carrier signal. Using the 20kHz sampling rate will create 333 phase modulations per leg per 60Hz period.

Leg Modulations/60Hz period = 20kHz/60Hz = 333

The pulse width (PW) ranges from 12.4% to 87.5%.

$PW_{min} = Trans/Period = 205/1650 = 12.4\%$

$PW_{max} = (2*CarrierRange + Trans)/Period = 1455/1650 = 87.5\%$

where

Trans = transition period, 205 dv

CarrierRange = range of the carrier, 620 dv

Period = complete carrier period; (2**CarrierRange* + 2* *Trans*), 1650 dv

Figure 5 shows a representation of the actual system. The carrier waveform has flat transitional areas at its boundaries. During these periods is where the new signals are prepared for the next modulation cycle.

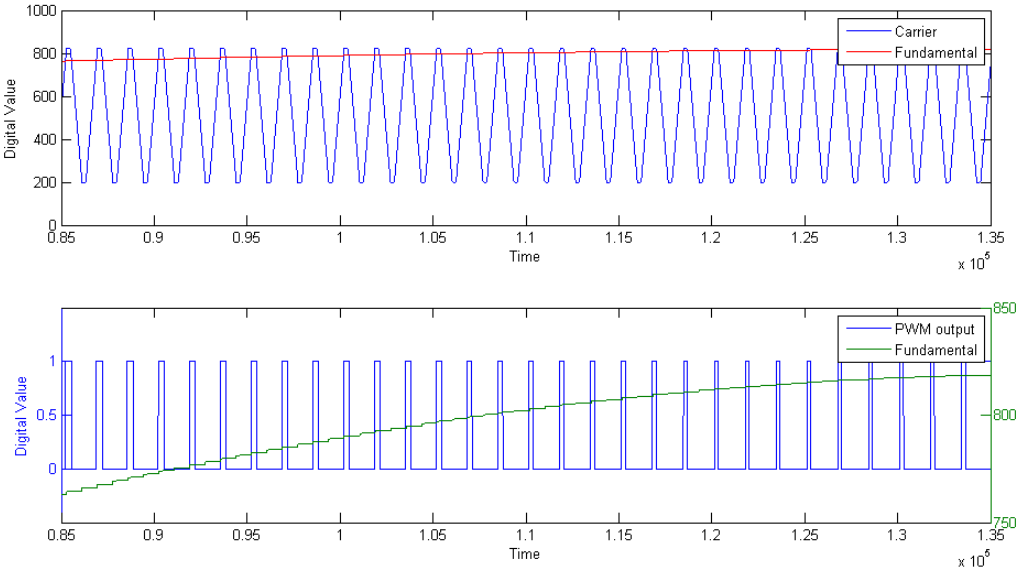


Figure 5. Representation of designed system

Digital Design

In order to layout the FPGA in an effective manner, the primary signals are identified and calculations are made. The primary signals include,

Carrier = the triangular carrier waveform, represented as a counter ranging over the interval 200 to 825, as determined above

Leg_A = fundamental waveform for phase leg A

Leg_B = fundamental waveform for phase leg B, 180° out of phase to *Leg_A*

HSA,LSA = high side and low side gate controls for phase leg A

HSB,LSB = high side and low side gate controls for phase leg B

The controller will make use of a state machine to control function activity along with other signals to protect the system from sending incorrect values to the gate controls. Figure 6 illustrates the high level functions in the FPGA architecture.

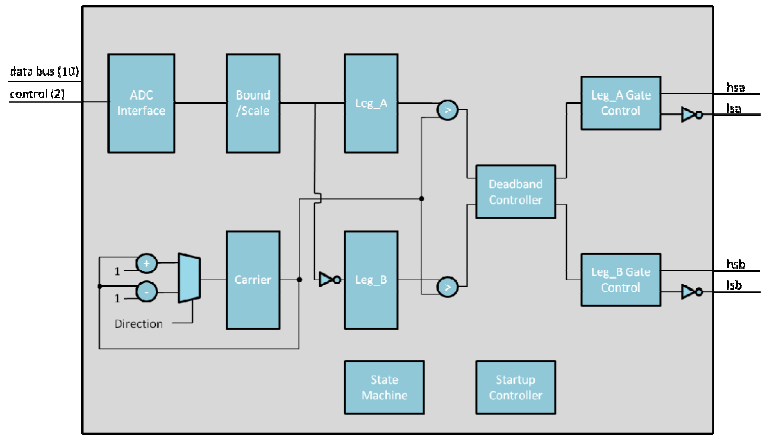


Figure 6. FPGA Architecture

The states of the state machine and their functions are:

Init = initialize system to know state

Startup = allows time for glitches to settle and conditioning circuit to reach steady state

Hold = wait for ADC control to signal that a sample is available

Read = read sample from the ADC, this sample is the fundamental waveform

Convert = scale the signal and make sure it is within the carrier boundaries

Update = load Leg_A with the fundamental and Leg_B with an inverted copy of the fundamental; this state waits until control signals indicate the deadband controller is not operating to ensure no lost modulation from the previous pwm period

Align = sets several control signals that operate the gate control signals.

PWM= modulates the carrier depending on a directional signal; every cycle the legs are compared to the carrier and, if a modulation of either leg is triggered, the deadband controller will become active and manage the switching of the gate controls; when the carrier reaches a boundary, the state will switch to *Hold*

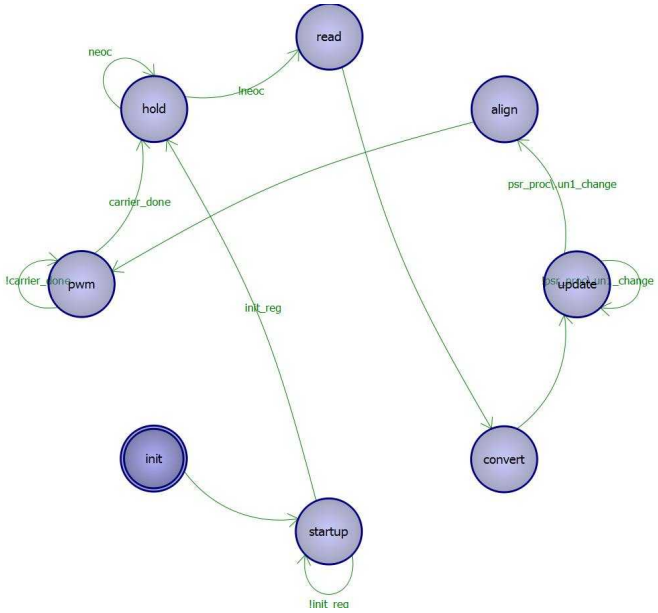


Figure 7. State machine for the controller

To implement the carrier, a counter was created ranging from 200 to 825 with a directional signal that changes state once either limit was reached to signal the direction, increment or decrement, the carrier should move in the next cycle.

On each count, each fundamental waveform dv is compared to the carrier. If one is equal to the carrier, a flag is sent to the deadband controller that monitors the switching between the two phase legs. The deadband controller ensures a minimum 1.4us deadband between opposing leg switching. The deadband is a very important safety feature needed to keep the switches in a proper configuration. Once the signal clears the deadband control, the respective phase leg is modulated.

During preliminary testing the system was found to have glitches when the circuit was initially powered due to metastable states inside the FPGA, the ADC, and the conditioning circuit providing the fundamental waveform to the ADC. To eliminate this, an initialization timer was added to allow the system time to settle to a steady, stable state. This procedure also initializes all of the internal signals of the FPGA to a known state.

Simulations

Simulations were used to verify the correct operation of the controller prior to the design being programmed onto a chip. Using the background information from Holmes & Lipo (see Figure 4), the design was verified using ModelSim. Figure 8 is a simulation of the expected output. Comparing the switch outputs (hsa, lsa, hsb, lsb) to Figure 4, it can be verified that the device switching pattern is correct.

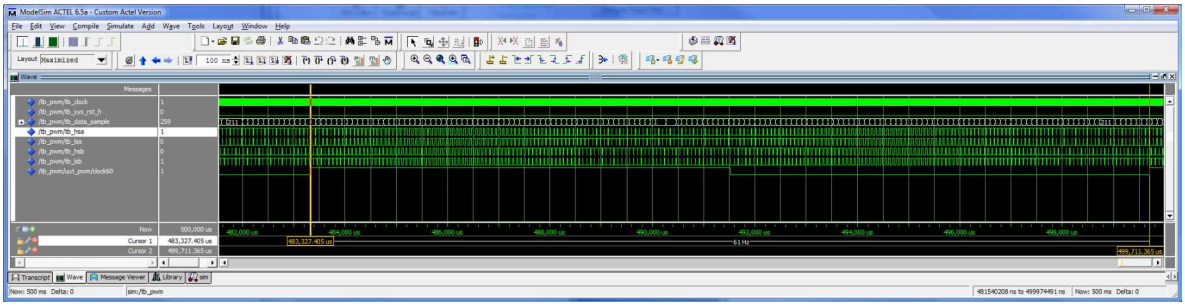


Figure 8. ModelSim simulation showing gate controls

The simulations also verified the deadband control is working properly and that the minimum switching deadband is 1.4us (Figure 9).

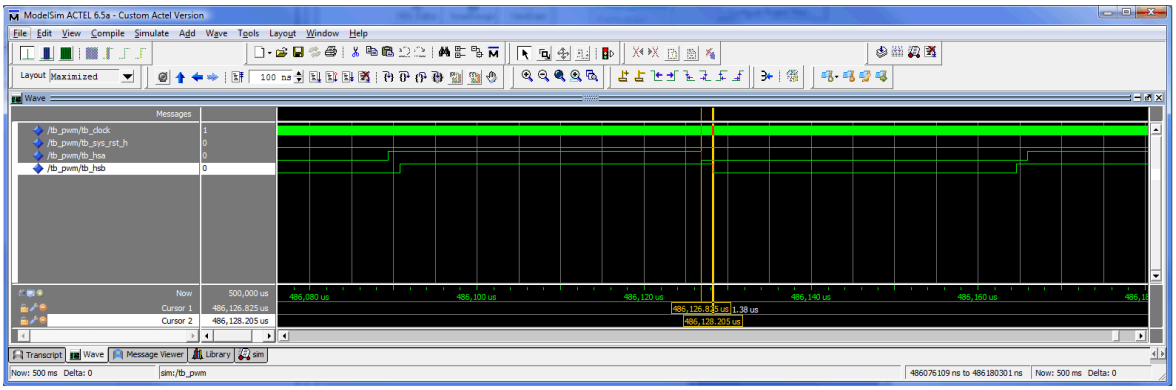


Figure 9. ModelSim simulation showing minimum deadtime of 1.38us

After functionality was verified in simulation, the completion steps were taken to program the FPGA. Place-and-route procedures were performed and the FPGA design was verified to ensure it met all timing requirements. Once this was complete the design was programmed onto the target FPGA and testing proceeded.

Testing

Testing was performed using two different gate drive/power stages to ensure the controller was robust and the performance was acceptable for use on multiple output devices.

Initial system verification was performed using an oscilloscope with no load connected. The gate control signals were analyzed at the output of the FPGA and across the terminals where the load would be located. Comparing the open load signals to both the theoretical and simulated models validate the sequencing and system timing requirements are met. Figure 10 shows the 3-level waveform measured across the load terminals, the fundamental waveform (shown in red) is used for comparison.

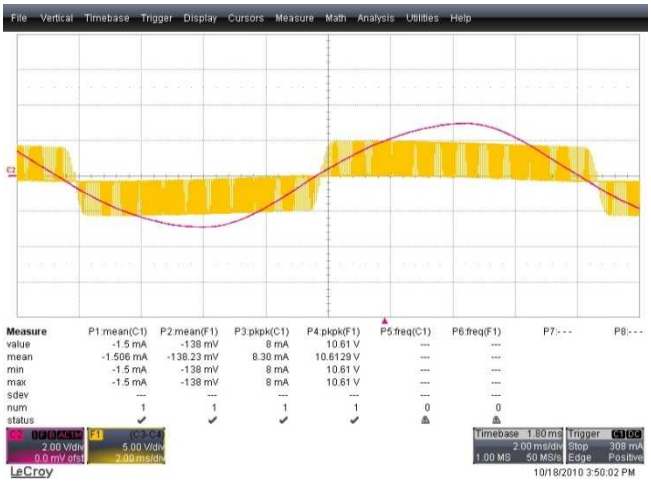


Figure 10. Three-level PWM waveform

Verification of the deadband controller, illustrated in Figure 11, shows the minimal timing delay between opposing phase legs to be 1.4us.

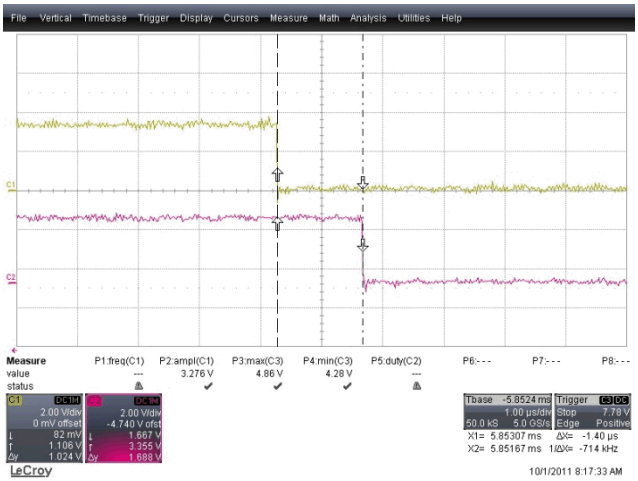
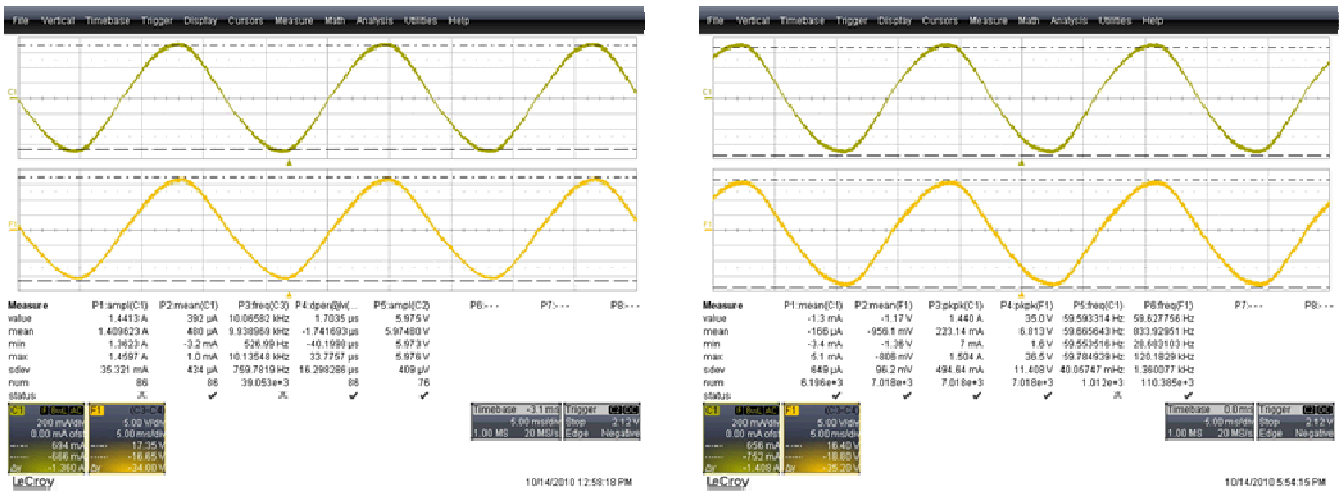


Figure 11. Minimum deadband switching between high side switches

Once confirmation of the controller was complete, a filter and load were added to the system and tested at room temperature. The system was validated using a low voltage DC bus at room temperature (25°C). After room temperature tests verified the design, several other temperatures were tested up to 225°C to verify that enough margin, particularly in the deadband controller timing, was given to allow for derating of the parts. Figure 12 illustrates safe and correct operation to elevated temperatures.



(a) (b)

Figure 12. Output across load at (a) room temperature (25°C) , and (b) 200°C

FPGA Utilization

One of the goals for this phase of the project was to minimize the usage of the FPGA due to its limited space and the desire to add more functionality in future work. Initial designs utilized significant space (Figure 13) which would not allow much design space for further functions. The high use of combinational cells (74%) is problematic and would severely limit further design.

```
Target Part: 42mx16-s
Combinational Cells:    450 of 608 (74%)
Sequential Cells:     223 of 624 (36%)
Total Cells:          673 of 1232 (55%)
DSP Blocks:           0
Clock Buffers:        2
IO Cells:             23
```

Figure 13. Initial FPGA Utilization

Optimizing the design involved several steps, including minimizing register usage and streamlining timing, the total space utilization was reduced from 50% to 36% of the total cells in the device (Figure 14) and a 29% reduction in the use of the combinational cells. Performing these optimizations opens up significant design space sufficient to implement additional functionality.

```
Target Part: 42mx16-s
Combinational Cells:    271 of 608 (45%)
Sequential Cells:    169 of 624 (27%)
Total Cells:         440 of 1232 (36%)
DSP Blocks:          0
Clock Buffers:       2
IO Cells:            23
```

Figure 14. FPGA Utilization after optimization

Conclusion

The digital design successfully implemented the unipolar three-level naturally sampled sine-triangle pwm process utilizing minimal space within the FPGA. Using this design will allow additional phases of the project to proceed with the ability to add more functionality to the overall system while adhering to the overall project goals of producing an integrated power controller, gate drive, and power stage in a minimal design space.

References

1. J.A. Henfling, S. Atcitty, F. Maldonado. “Development of an Integrated Power Controller Based on SOI and SiC”. Sandia National Laboratories. 2010.
2. A. Barnes. “Best Practices for High-Temperature SiC JFET Inverter”. 2010.
3. Holmes, D. Grahame, and Lipo, Thomas A. Pulse Width Modulation for Power Converters. Piscataway: IEEE Press, 2003.
4. N. Aphiratsakun, S. Bhaganagarapu, K. Techakittiroj. “Implementation of a Single-phase Unipolar Inverter Using DSP TMS320F241”. 2005.

Acknowledgements

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy’s National Nuclear Security Administration under contract DE-AC04-94AL85000.

The author would also like to thank the Department of Energy Office of Electricity and Dr. Imre Gyuk for financial support of this research.