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Practical RF Design Considerations

Or, *RF Design in the "Real World"*

Presented to ECE663, "RF Electronics Design"
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Discussion Topics

- Background
- Introduction to RF Engineering
- Substrates
- Microwave Printed (Distributed) Circuits
- Lumped-Element Passive Components
- System Concepts
- Test Equipment
- Summary
- Open Discussion, Q&A

Background

- This presentation is intended to highlight some practical design considerations typically learned “on the job”
  - The idea came while discussing implementation details w/ Anthony Ernest at work one day
    - Full disclosure: Anthony is an intern in my department
  - Feel free to contact me anytime

- Who am I?
  - BSEE UNM 1992, MSEE U. Arizona 1994
  - Jobs
    - PNM (intern): Power transmission planning
    - Motorola, now General Dynamics: High-speed packaging (EM), RFIC
    - Amtech, now TransCore: RF modules
    - Sandia National Laboratories: Everything RF thru 17 GHz, now a technical manager within the Advanced RF group

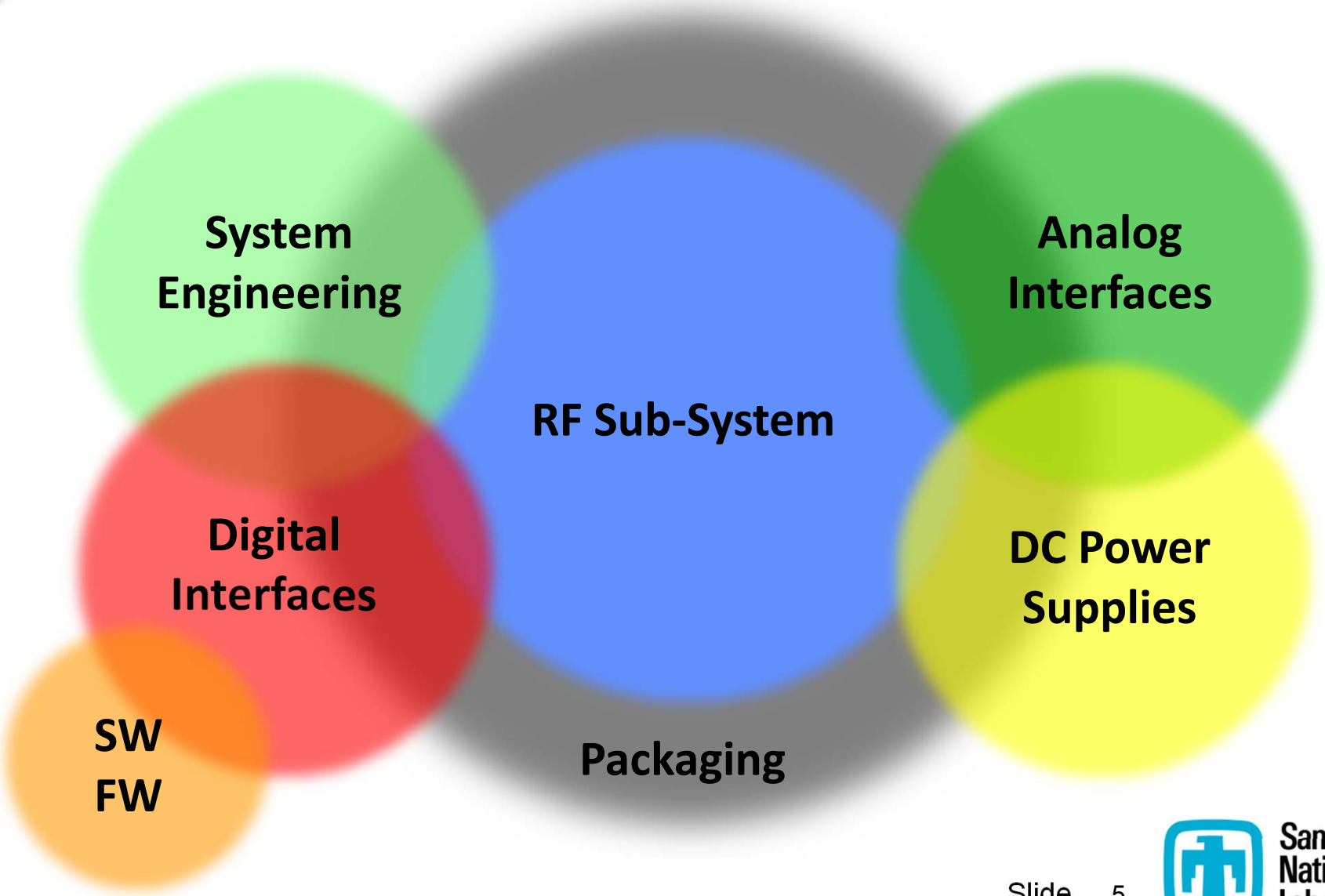
- **Rules of Thumb (ROT)** and **Important Practical Knowledge (IPK)** are highlighted → remember these!

Introduction to RF Engineering

- What does an RF/microwave engineer do?
  - Circuit design
    - Active and passive, antennas, substrates, launches, simulations
  - Sub-system planning
    - RF chain analysis, frequency generation & conversion schemes, RF/EMI shielding, interfaces (analog, digital, and DC power)
  - System engineering
    - Requirements, link analysis, trade studies, architecture studies, device/system packaging, documentation
  - Testing
    - Laboratory, field, compliance, test plans/reports
  - Production support
  - Customer interface and CONOPS development

- What's old is more important than what's new!
  - Solid foundation in theory balanced with implementation details learned by experience
  - Technology has made design and simulation easier but has also opened the door for oversights in practical details and the knowledge of "why"
    - **IPK: "Garbage in → garbage out"**

Influences Around the RF System ("Concurrent Engineering")



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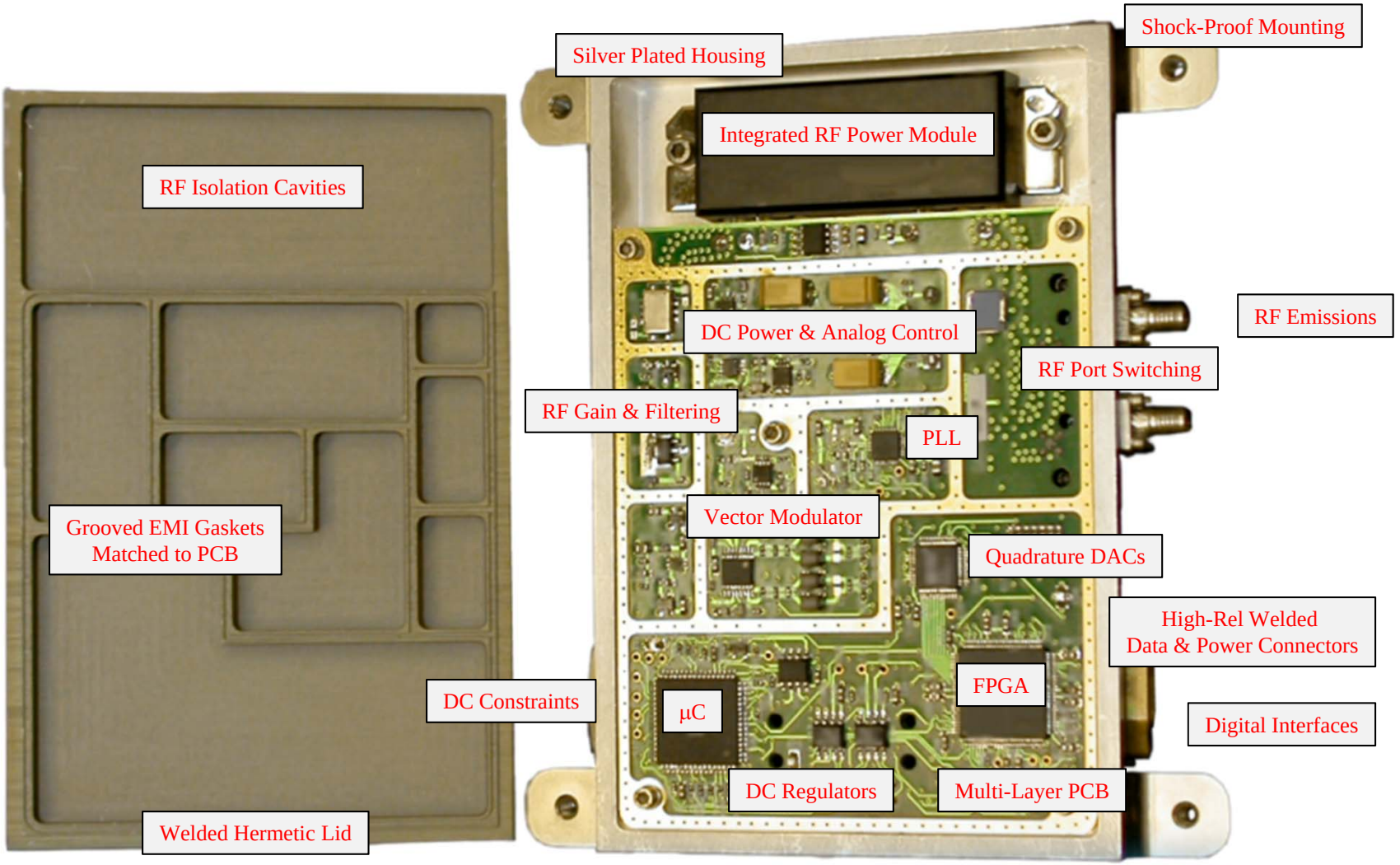
Designs like this require Concurrent Engineering



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IDEAL Career Development for RF Engineers

- Interns, 0-2 years: Component design, lab testing
  - Coupler, filter, linear amplifier, detector, mixer
- 2-5 years: Sub-circuit design, system testing
  - RF strip: high-freq amps, attenuators, filters, biasing
  - IF chain: low-freq amps, attenuators, filters, biasing
  - STALO (stable local oscillator): tuning speed, phase noise, PLL
  - Power amplifiers (with extreme requirements): wideband/high-efficiency
  - Advanced modulation schemes including digital interface
- 5-10 years: Small/sub-systems, complex circuits, testing oversight
  - Receiver with low noise figure and high linearity (IIP3)
  - Frequency-hopping transmitter mated to digital controller
  - RF planning and or analysis
- 10+ years: RF system design
  - System planning and analysis
  - System requirements development or interpretation
  - System concept derived from customer CONOPS

Components

Systems

- Example: Chief RF system engineer for GPS satellite
  - ~ 8 transmitters and 4 receivers
  - Thousands of requirements including EMI/EMC compliance, reliability, radiation…
  - System cannot be touched after launch!

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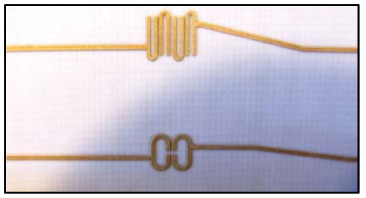
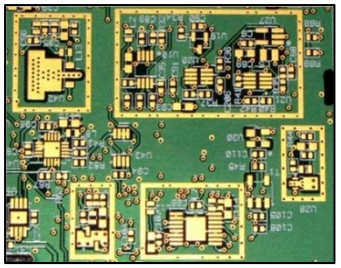
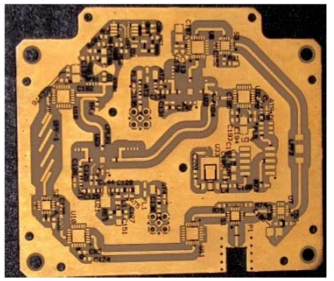
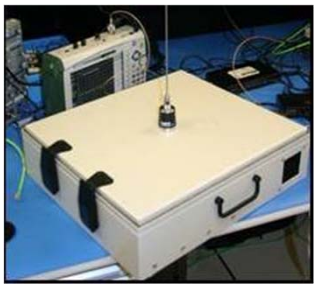
Career Development for RF Engineers
The Real Story

- Interns, 0-2 years
  - Your senior engineer: "Make me a band-pass filter at 10.25 GHz with about 500 MHz of bandwidth, low loss, decent harmonic rejection. We may have some 4003 laying around somewhere, just cut it out with scissors."
- 2-3 years
  - Your lead project engineer: "We need -10 dBm at the RF down-mixer for the 350 MHz IF and a LO for our 9.545 GHz input. I'm thinking high-side mix, what do you think?"
- 3-5 years
  - You, the lead engineer: "I recommend we use a vector modulator and I/Q DACs to generate the baseband waveform and direct-drive the LO via PLL locked to the GPS reference output, gain it up and filter to meet MIL-461. I'm concerned about phase noise in the PLL, however."
- 5+ years
  - You, the project lead: "The customer wants to locate their people from at least 10 km stand-off using their existing sensor and a deck-of-cards sized device. I propose we use about 40 dB net gain and multi-tone vector modulation, but we'll need Jimmy Bob to figure out how to skirt their clutter rejection algorithms. I think we can meet their field lifetime goals with 2 AA batteries. Let's sketch out the hardware architecture."









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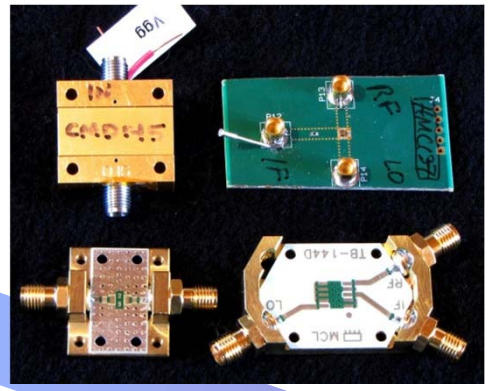
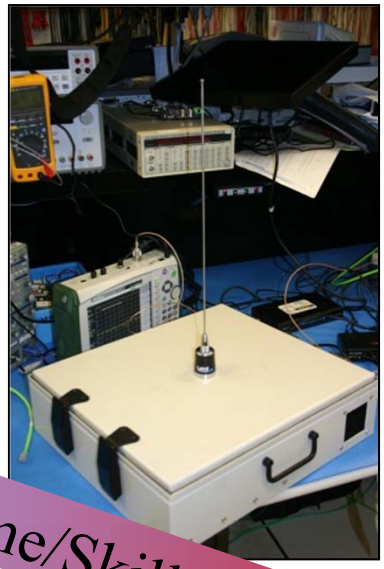
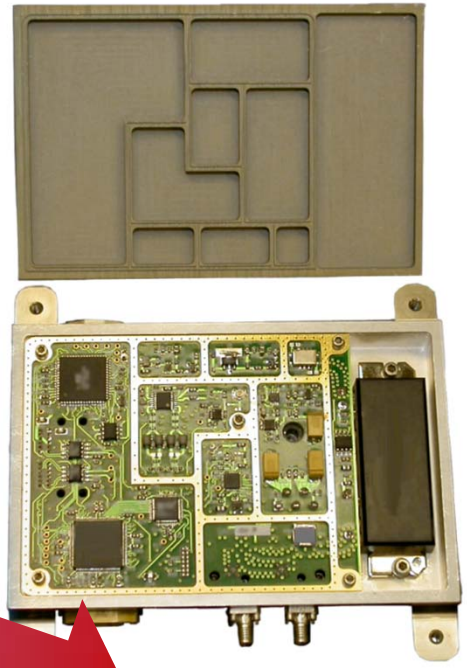
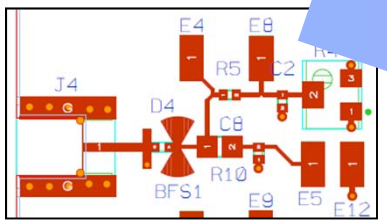
Things you will be asked to do…

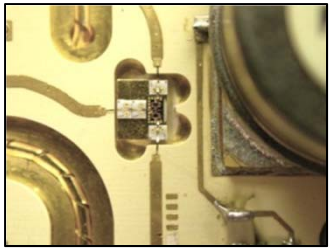


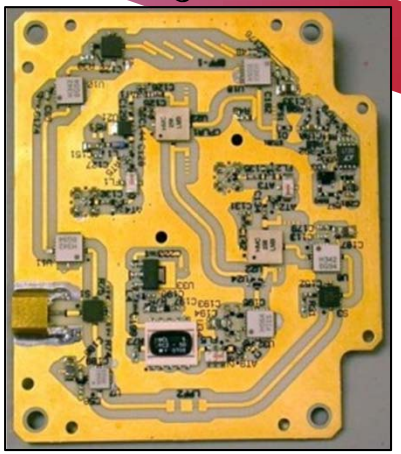


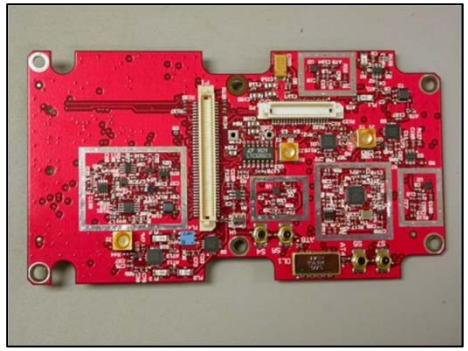




Increasing Time/Skills







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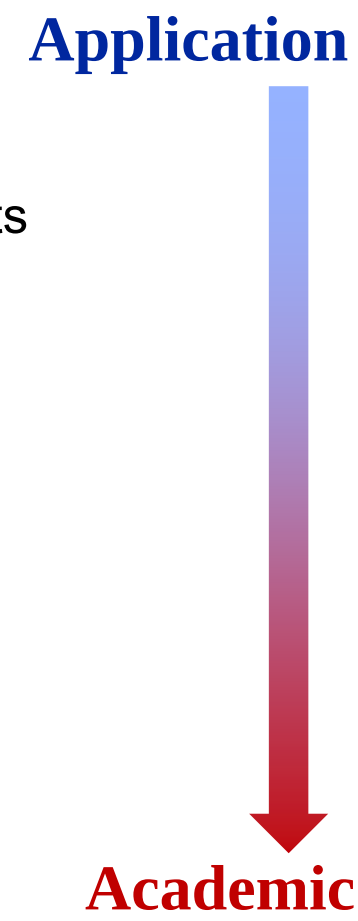
Educational Tools, in Order of Utility (to me)

- **Other engineers in your company and in your network**
  - RF/microwave/antenna, analog, digital/DSP
- **IPK: Vendor datasheets and application notes**
  - Agilent/HP, Analog Devices, Mini-Circuits, W-J (obsolete)
- Industry journals (print and on-line), communities, web events
  - RF Globalnet, Microwave Journal, RF Design, EDN
  - NASA Tech Briefs, Defense Tech Briefs
  - Microwave Journal “Besser Webinar Series”
  - Agilent Webcast Series
- Simulator example files and canned routines
  - ADS/Genesys, Microwave Office
  - CST, HFSS
- Continuing education
  - Georgia Tech, UCLA, Besser
- Professional societies and conferences
  - IEEE MTT/IMS (combined, spring each year)



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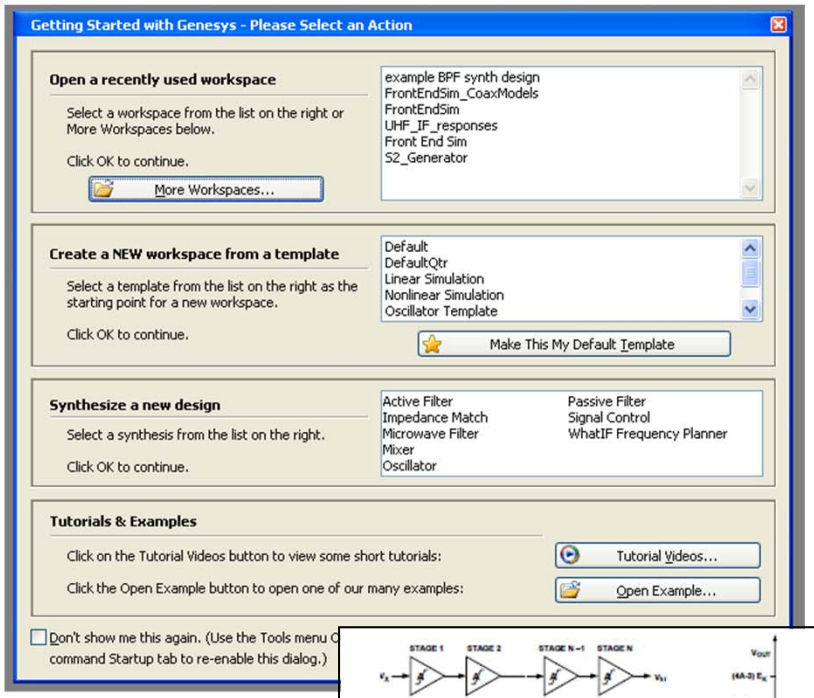
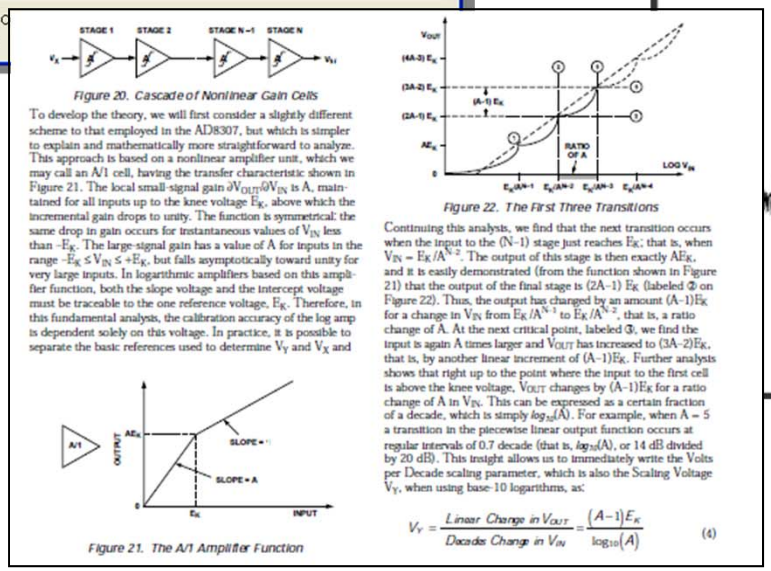
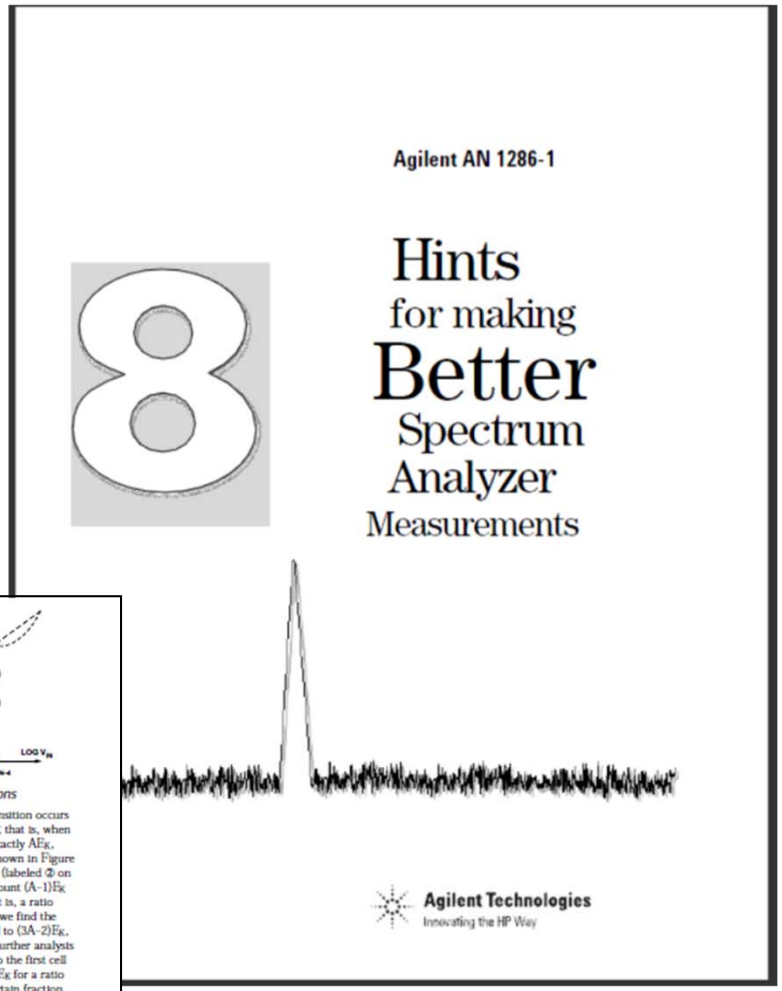
Examples







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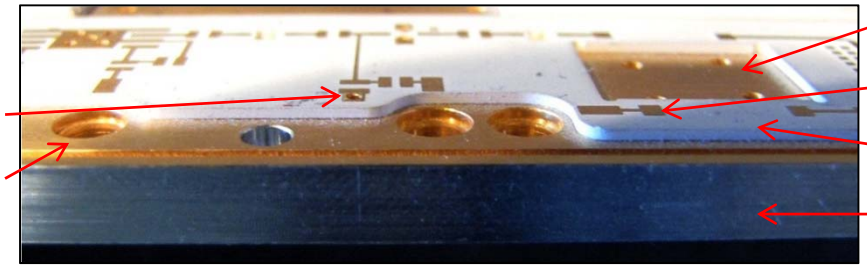
RF and Microwave Substrates

- Early microwave designs and today's "point designs" use single-layer substrates (one dielectric core with copper cladding on both sides)
  - Top metal is for circuits (active and passive) plus extra ground
  - Bottom metal is ground and is shared with the chassis, connected by vias
- Microwave substrates are manufactured under strict controls and offer stable performance from lot-to-lot (e.g., over time) and over temperature



- Rogers RT/duroid is a PTFE (Teflon)-based "soft substrate"
  - Extremely low loss (tan δ) is excellent for large, distributed structures
  - Very low ε_r which means electrical size is larger than other dielectrics
  - PTFE requires special chemical processing; no wirebonding
- Rogers TMM is a ceramic-loaded plastic "hard substrate"
  - Very low loss but with ε_r up to 9.9 (smaller structures)
  - Good for MMIC die and wire bonds, but needs thick metal backing (cracks)

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Multi-Layer Substrates

- Digital and other folks use generic dielectrics such as FR-4 (fire retardant #4) which is manufactured by many vendors but will vary in all performance aspects
  - Ideal for low-cost, multi-layer designs such as low-speed digital, power supplies, analog electronics, etc.
  - **IPK: DO NOT use FR-4 as your substrate for microwave circuits!**
    - OK for low-frequency designs based on RFICs and passives with short interconnects, i.e., very short transmission line between “matched” interfaces
- Modern designs require analog/digital/power/RF on one board
- “Multi-layer” PTFE-based substrates are available (e.g., Rogers RO3000-series)
- However, newer types of microwave substrates for multi-layer apps are available from reputable vendors (e.g. Rogers RO4000-series)
  - These substrates are essentially epoxy resins loaded with ceramic dust to create a low loss dielectric that has stable performance
  - Cost is low enough to integrate all circuits on one “RF” board
  - Or, can use hybrid approach and fuse “RF layers” and FR-4 layers

The PCB Stack-Up: Cores, Pre-Pregs, …

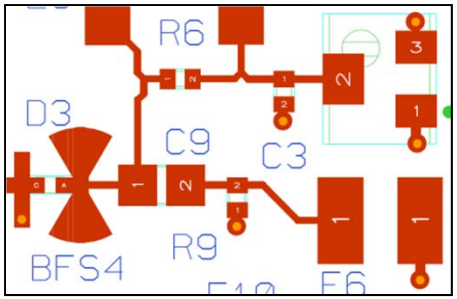
- A substrate core is a stable dielectric sheet clad in copper foil
  - Thickness of core is measured in mils (1 mil = 0.001”)
  - Copper cladding has thickness and surface roughness
    - Thickness is a result of the amount of copper rolled into 1 square foot
    - **ROT: 1 oz. Cu → 1.4 mils thick** (remember, this is before plating)

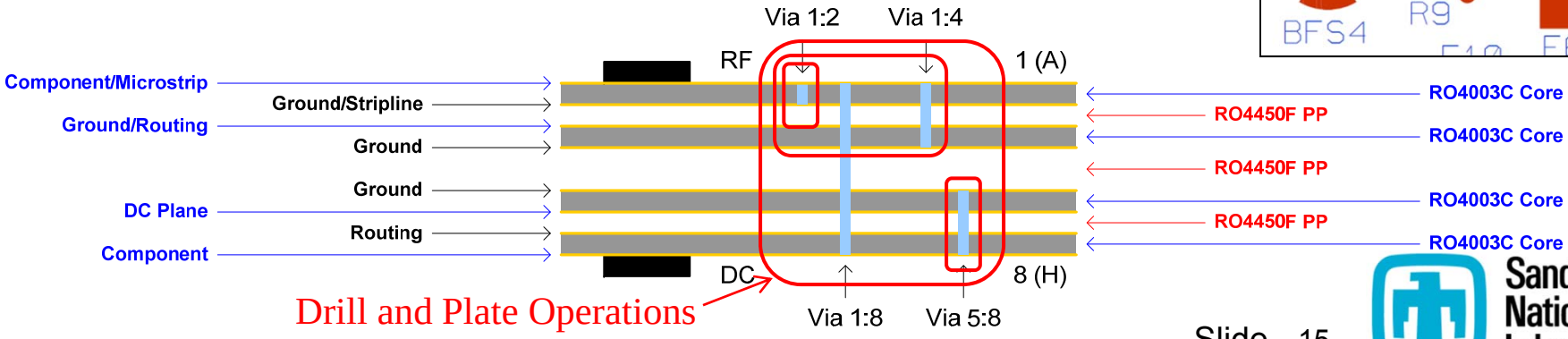
- Multiple cores can be bonded together to form a multi-layer stack-up
- The dielectric “bonding layer” is called a pre-preg
  - **IPK: Pre-preg is dielectrically SIMILAR, but not exactly equivalent, to a core in its dielectric properties**
- Normally, microstrip is etched out of one side of a core
- Stripline has a core on one side and pre-preg on the other

- **IPK: Often, the final metal is plated in gold (over nickel) to prevent oxidation, corrosion, etc., and will increase the thickness and conductivity**

The PCB Stack-Up: …and Vias

- Vias are holes that are drilled thru the substrate (mechanically or by laser) that interconnect metal layers by a copper plating process
- A PCB "stack" can have one or more via interconnect layers which affects the ultimate metal plating thickness on the top and bottom
  - **IPK: For every "drill and plate" via operation, the plating thickness on the exposed surfaces get thicker**
- Vias are notoriously difficult to model in terms of parasitic L&C
  - **ROT: Thinner substrate → lower parasitic L&C**
  - **ROT: Every ground location gets (at least) one via**
    - Place your via IMMEDIATELY near your element/pad
    - Eliminates T-line length (phase shift)





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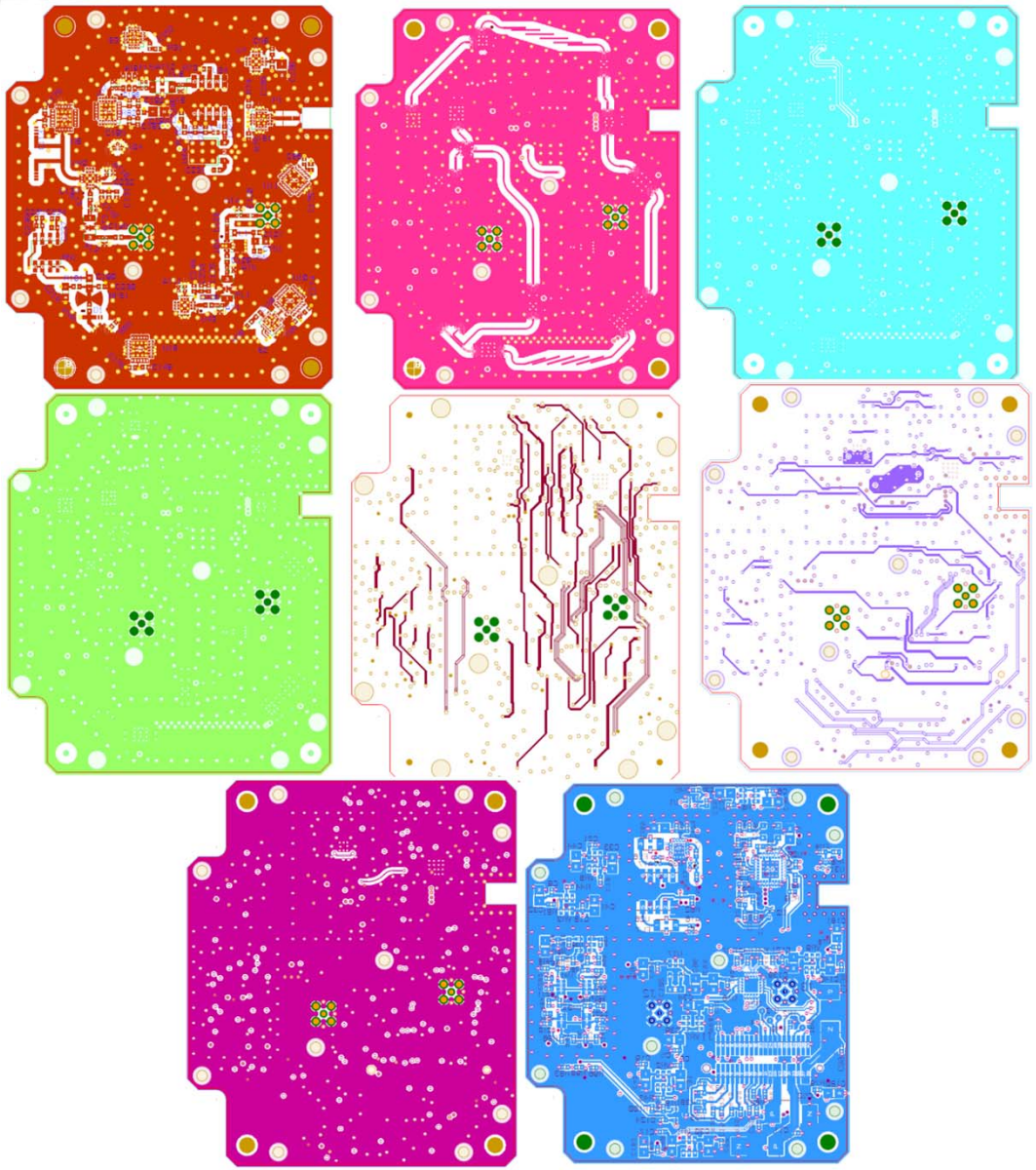
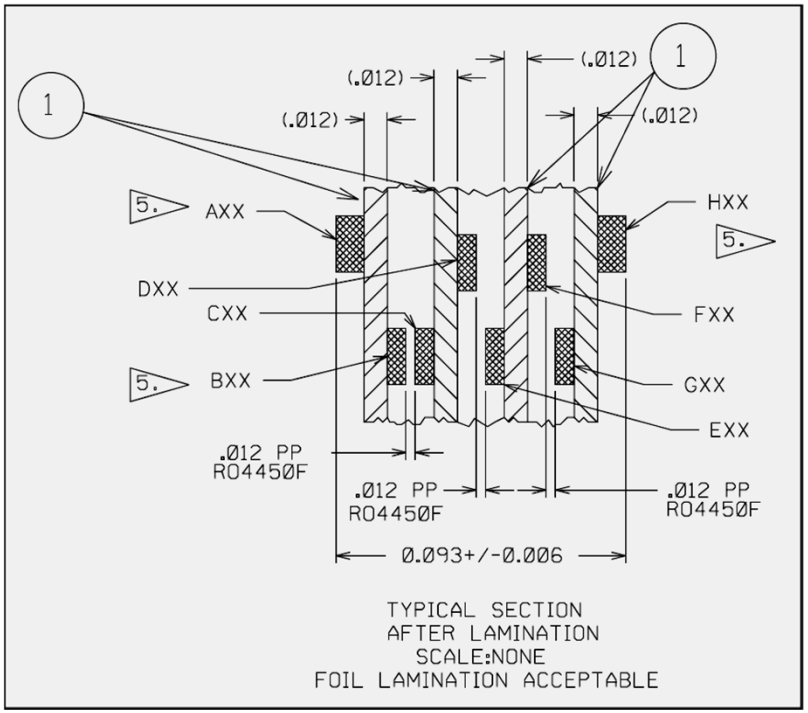
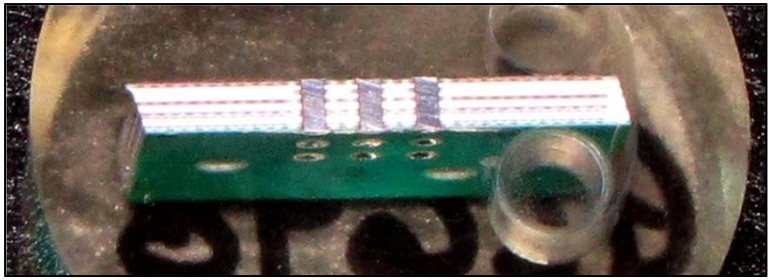
Microwave Substrate Examples







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Microwave Printed Circuits

- Choose the substrate according to the impedance characteristics you require (and the required circuits, packaging, cost, etc.)

Microstrip Substrate	ε_r	Width for 50Ω, 8 mil thickness	Width for 50Ω, 12 mil thickness	Width for 50Ω, 20 mil thickness
RT/Duroid 5880	2.20	23.8 mils	36.1 mils	60.6 mils
RO4003C	3.55	17.2 mils	26.0 mils	43.9 mils
TMM-10i	9.9	7.1 mils	10.9 mils	18.5 mils

Summary of LineCalc results at 1 GHz

→ Varies ~ thickness

- Choose to use printed (distributed) circuits vs. lumped elements based on frequency (electrical → physical length)

Microstrip Substrate	ε_r	λ/4 @ 430 MHz	λ/4 @ 5.8 GHz	λ/4 @ 16.7 GHz
RT/Duroid 5880	2.20	5023 mils	372 mils	36 mils
RO4003C	3.55	4142 mils	307 mils	105 mils
TMM-10i	9.9	2720 mils	201 mils	68 mils

Varies ~ sqrt(ε_r) ↓

Summary of LineCalc results for 20 mil thick

ROT: The frequency break point for printed vs. lumped is 2-3 GHz. (this is also due to parasitics in passives, which we'll get to…)

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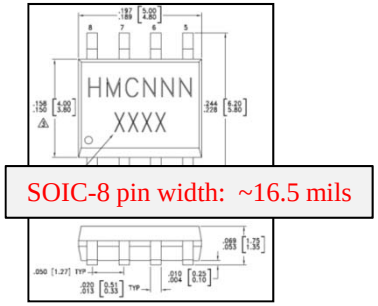
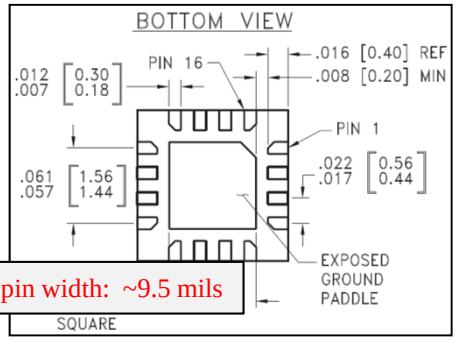
Printed Circuit Interfaces

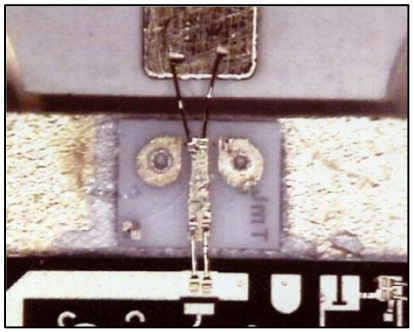
- ALL microwave structures (which includes transmission lines) will connect other semiconductor or passive devices
  - Q: What is the optimum width for a 50Ω transmission line?
  - A: Balance between requirements for printed circuits, fabrication tolerances, and launches into/out of other devices
    - **IPK: IC package pin widths + extra width for PCB solder pads**
      - Pad sizes vary but can be 5-10 mils all around
    - **IPK: Width of in-series passives + PCB pads**

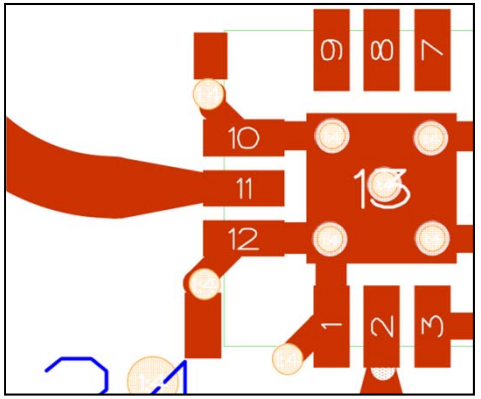


SOIC-8 pin width: ~16.5 mils

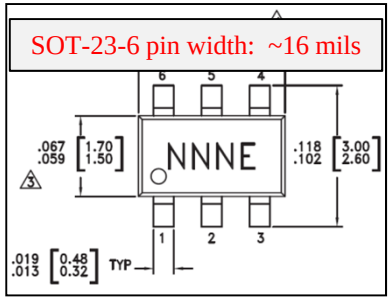


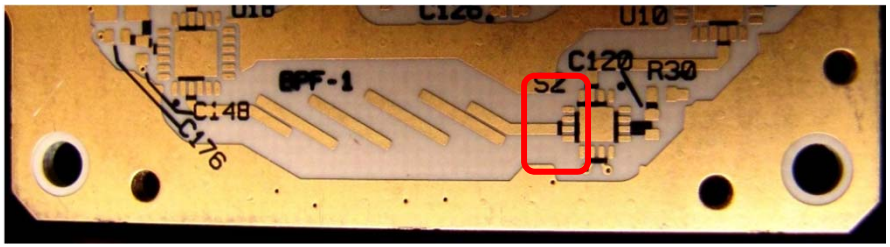
QFN pin width: ~9.5 mils





SOT-23-6 pin width: ~16 mils





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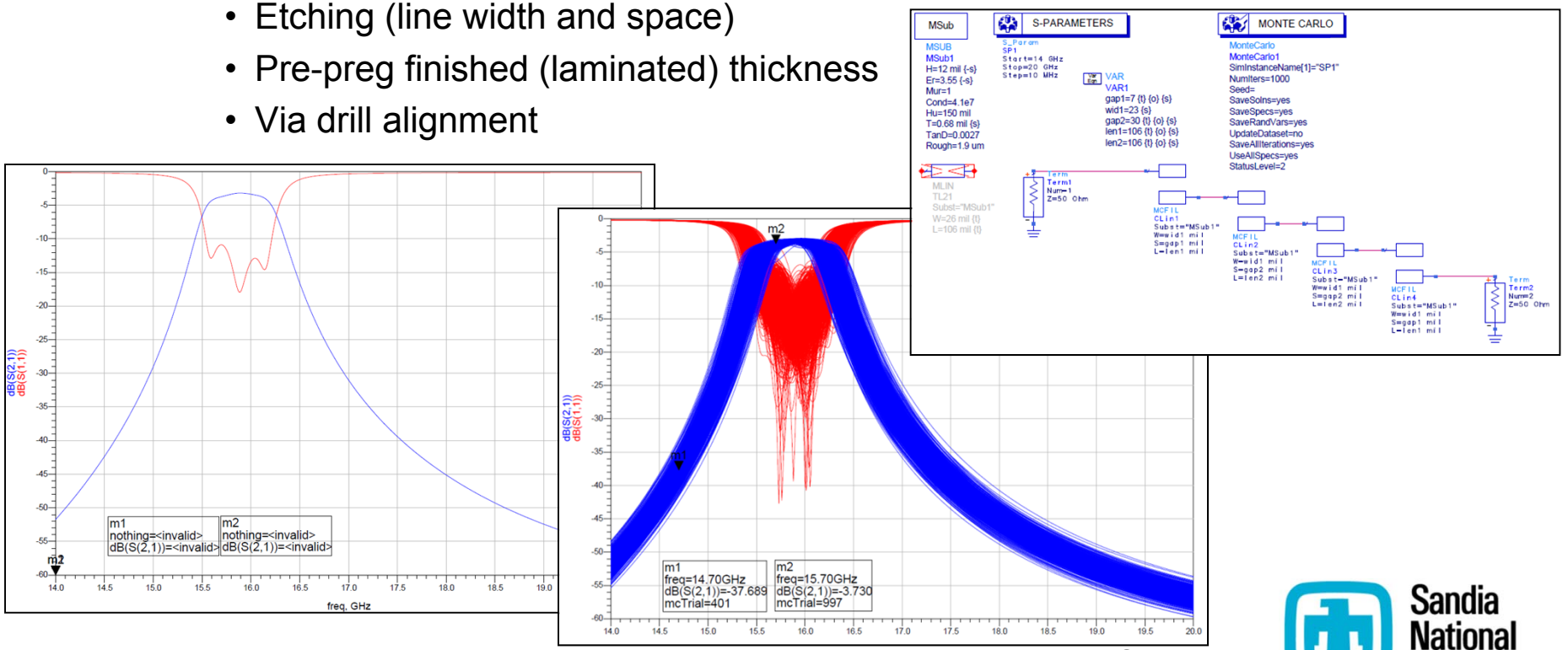
Implementation Issues for Printed Circuits

- **IPK: Every parameter has a tolerance**
  - The tighter you specify these tolerances, the more costly your board (or, machine limits will be reached)
  - You need to find out what these are and model or design for them
    - Dielectric constant
    - Etching (line width and space)
    - Pre-preg finished (laminated) thickness
    - Via drill alignment



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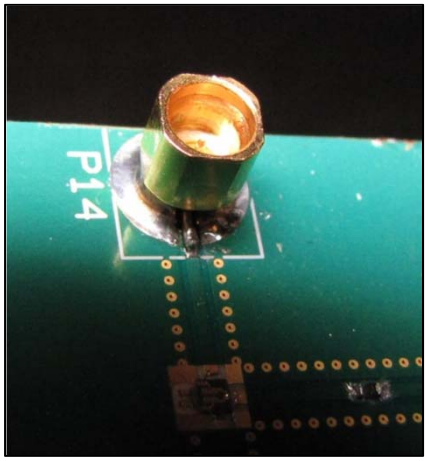
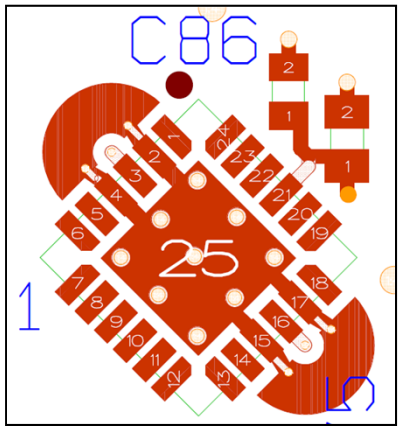
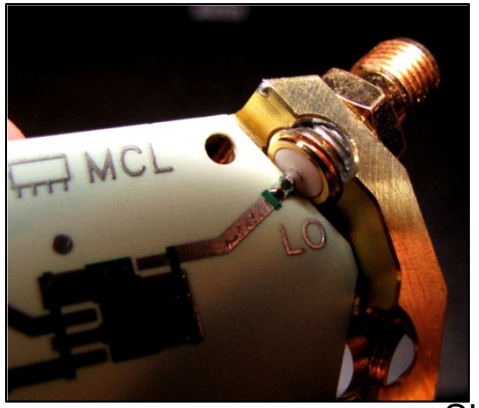
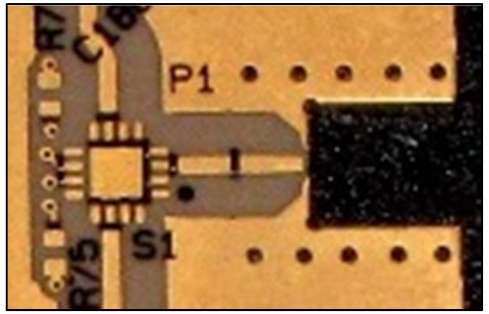
RF/Microwave Launch

- A launch is a controlled-impedance interface, usually into or out of a defined structure or sub-system
- The “interior” circuits can be world-class, but the launch may ruin system performance (EMC, RX NF, PA reflected power, etc.)
- **IPK: Connector interfaces to RF boards are usually the worst RL in the chain and must be modeled/designed appropriately**
- Q: How good should the RF launch be?
- A: As good as possible! RL = 10 dB is not acceptable
  - SW Microwave “Super SMA”: RL < -29 dB to 27 GHz
  - **ROT: Do NOT use BNC connectors! Use TNC if necessary.**









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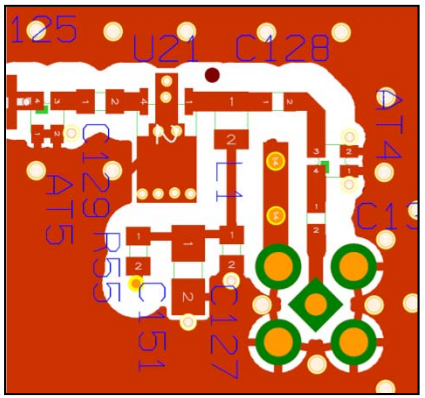
Lumped-Element (LE) Passives Components

- Include resistors, capacitors, and inductors
- Each of these can take >10 pages to describe their complexities
  - Excellent resources
    - ATC app notes, Capacitor Handbook, and S2P files
    - Coilcraft app notes, performance specs, and S2P files
    - muRata also provides S2P files for many passives, as do other vendors
    - Mini-Systems (MSI) has low-parasitic microwave resistors
- There are specific “RF” or “microwave” devices that are far superior to cheaper, general-grade passives
- **IPK: Physically smaller passives have lower parasitic L/C**

- Resistors are the least tricky
  - Parasitic capacitance
  - Pad width when used in series
  - Power rating
  - Must block w/ capacitor if there is DC on the node



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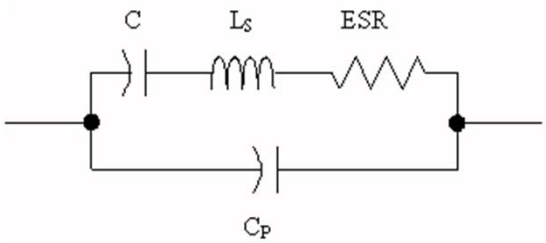
Capacitors



- Use
  - Series: Tuning, LE filters, DC block
  - Shunt: Tuning, LE filters, AC by-pass
  - Tuning and filtering: Must maintain $X_C = 1/(2\pi fC)$
  - Blocking and by-passing: Desire lowest RF impedance possible
  - Most caps are multi-layer caps; single-layer for extreme performance
- **IPK: A capacitor will enter series-resonance (min Ω) at a frequency determined by the parasitic inductance**
  - This is the "self-resonant frequency" (SRF), beyond which the capacitor will trend inductive!
  - Tuning and filtering: Must operate well below the SRF
  - Blocking and by-passing: Optimal near the SRF, but SRF can vary!
    - **ROT: $X_C < 1\ \Omega \rightarrow C > 1/(2\pi f)$ as long as f is not >> SRF**
- Temp coefficient of capacitance must be stable
  - **ROT: Choose NPO and C0G dielectrics over X7R, X5R, and Y5V**

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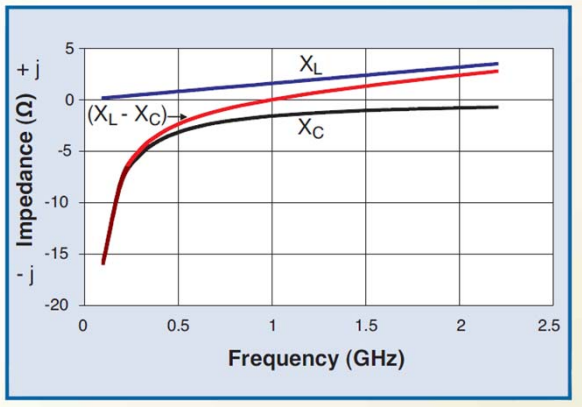
Example Capacitor Data



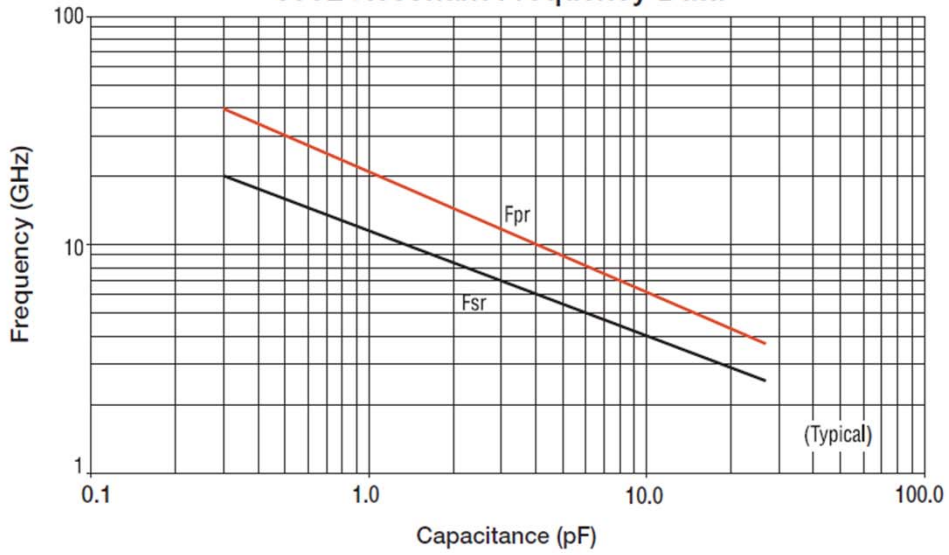
ATC 600L Series Ultra-Low ESR, High Q, NPO RF & Microwave Capacitors

Capacitance Values*

Value (pF)	Cap Code	Tolerances
0.1	0R1	A, B
0.2	0R2	A, B
0.3	0R3	A, B, C
0.4	0R4	A, B, C
0.5	0R5	A, B, C
0.6	0R6	A, B, C
0.7	0R7	A, B, C
0.8	0R8	A, B, C
0.9	0R9	A, B, C
1.0	1R0	A, B, C, D
1.1	1R1	A, B, C, D
1.2	1R2	A, B, C, D
1.3	1R3	A, B, C, D
1.5	1R5	A, B, C, D
1.6	1R6	A, B, C, D
1.8	1R8	A, B, C, D
2.0	2R0	A, B, C, D
2.2	2R2	A, B, C, D
2.4	2R4	A, B, C, D
2.7	2R7	A, B, C, D
3.0	3R0	A, B, C, D
3.3	3R3	A, B, C, D
3.6	3R6	A, B, C, D
3.9	3R9	A, B, C, D
4.3	4R3	A, B, C, D
4.7	4R7	A, B, C, D
5.1	5R1	A, B, C, D
5.6	5R6	A, B, C, D
6.2	6R2	A, B, C, D
6.8	6R8	B, C, J, K
7.5	7R5	B, C, J, K
8.2	8R2	B, C, J, K
9.1	9R1	B, C, J, K
10	100	F, G, J, K, M
11	110	F, G, J, K, M
12	120	F, G, J, K, M
15	150	F, G, J, K, M
18	180	F, G, J, K, M
20	200	F, G, J, K, M
22	220	F, G, J, K, M
24	240	F, G, J, K, M
27	270	F, G, J, K, M

*Non-standard values and custom tolerances are available upon request.

600L Resonant Frequency Data



TOLERANCE CODE TABLE

Code	A	B	C	D	F	G	J	K	M
Tol.	±0.05 pF	±0.1 pF	±0.25 pF	±0.5 pF	±1%	±2%	±5%	±10%	±20%

Operating Frequency (MHz)	Effective Capacitance (C_E), pF	Impedance, (Ω)
10	100.01	0.013 – j 159.13
100	101.01	0.023 – j 15.76
500	133.34	0.051 – j 2.38
900	526.29	0.069 – j 0.337
950	1025.53	0.070 – j 0.168

Table 1
Relationship between F_0, C_E and Z

ATC 600L Series Data Sheet Test Condition Description

Capacitors mounted in series microstrip configuration on 10-mil thick Rogers RO4350® softboard, 22-mils wide 1/2 oz. Cu traces.
FSR = lowest frequency at which S11 response, referenced at capacitor edge, crosses real axis on Smith Chart.
FPR = lowest frequency at which there is a notch in S21 magnitude response.

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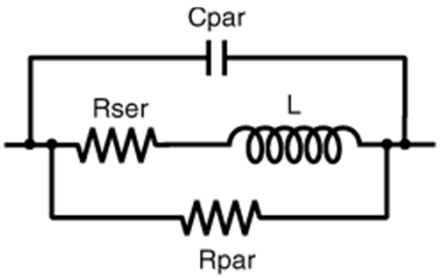
Inductors



- Use
  - Series: Tuning, LE filters, AC block
  - Shunt: Tuning, LE filters, DC return
  - Tuning and filtering: Must maintain $X_L = 2\pi fL$
  - Blocking and by-passing: Desire highest RF impedance possible
- **IPK: An inductor will enter parallel-resonance (max Ω) at a frequency determined by the parasitic capacitance**
  - This is the "self-resonant frequency" (SRF), beyond which the inductor will trend capacitive!
  - Tuning and filtering: Must operate well below the SRF
  - Blocking and by-passing: Optimal near the SRF, but SRF can vary!
    - **ROT: X_L > 500 Ω → L > 500/(2πf) as long as f is not >> SRF**

Part number[1]	Inductance[2] (nH)	Percent tolerance	Q min[3]	900 MHz L typ	900 MHz Q typ	1.7 GHz L typ	1.7 GHz Q typ	SRF typ[4] (GHz)	DCR max[5] (Ohms)	Irms[6] (A)
0403HQ-1N9XJL_	1.9	5	40	1.9	62	1.9	94	11.84	0.012	2.2
0403HQ-2N1XJL_	2.1	5	35	2.1	56	2.1	88	12.40	0.019	1.8
0403HQ-3N4XJL_	3.4	5	40	3.4	66	3.5	96	8.97	0.016	1.9
0403HQ-3N7XJL_	3.7	5	40	3.7	64	3.8	95	8.65	0.018	1.8
0403HQ-5N5XJL_	5.5	5	40	5.5	62	5.7	93	8.60	0.022	1.5
0403HQ-6N6XJL_	6.6	5	40	6.6	60	6.9	92	7.30	0.046	1.1
0403HQ-8N2XJL_	8.2	5	40	8.2	63	8.5	92	6.73	0.040	1.2
0403HQ-9N0XJL_	9.0	5	40	9.1	66	9.5	90	6.85	0.055	1.0
0403HQ-12NXJL_	12	5	40	12.1	60	12.7	90	5.82	0.065	0.80
0403HQ-15NXJL_	15	5	35	15.2	60	16.0	90	5.82	0.188	0.50
0403HQ-18NXJL_	18	5	35	18.2	62	19.6	93	5.15	0.185	0.50

Coilcraft 0403HQ high-Q chip inductor data

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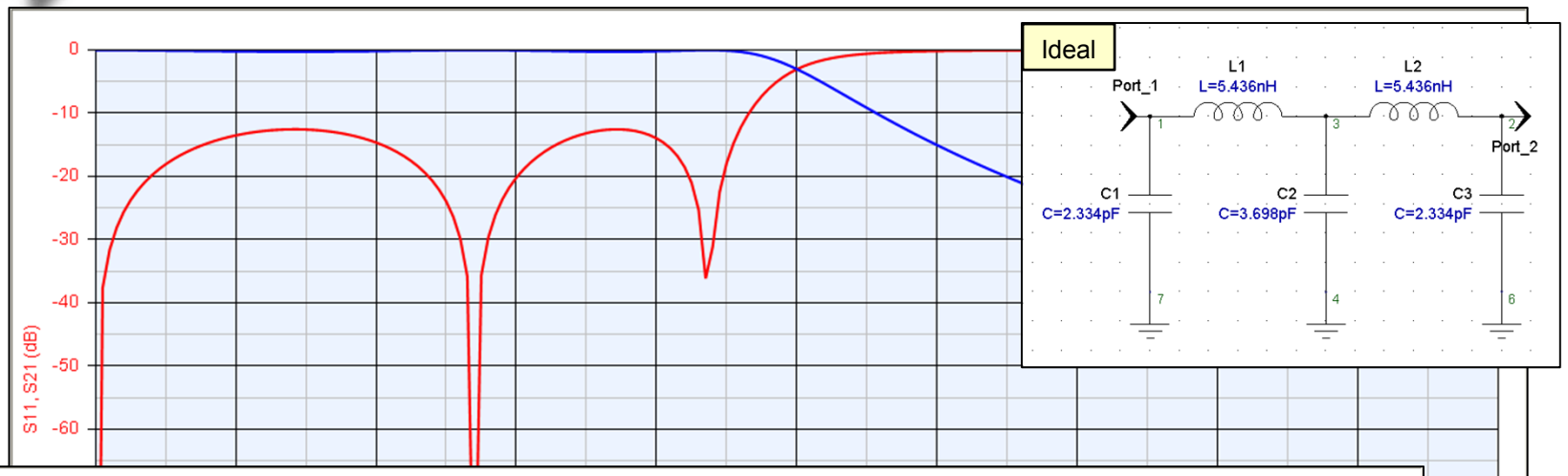
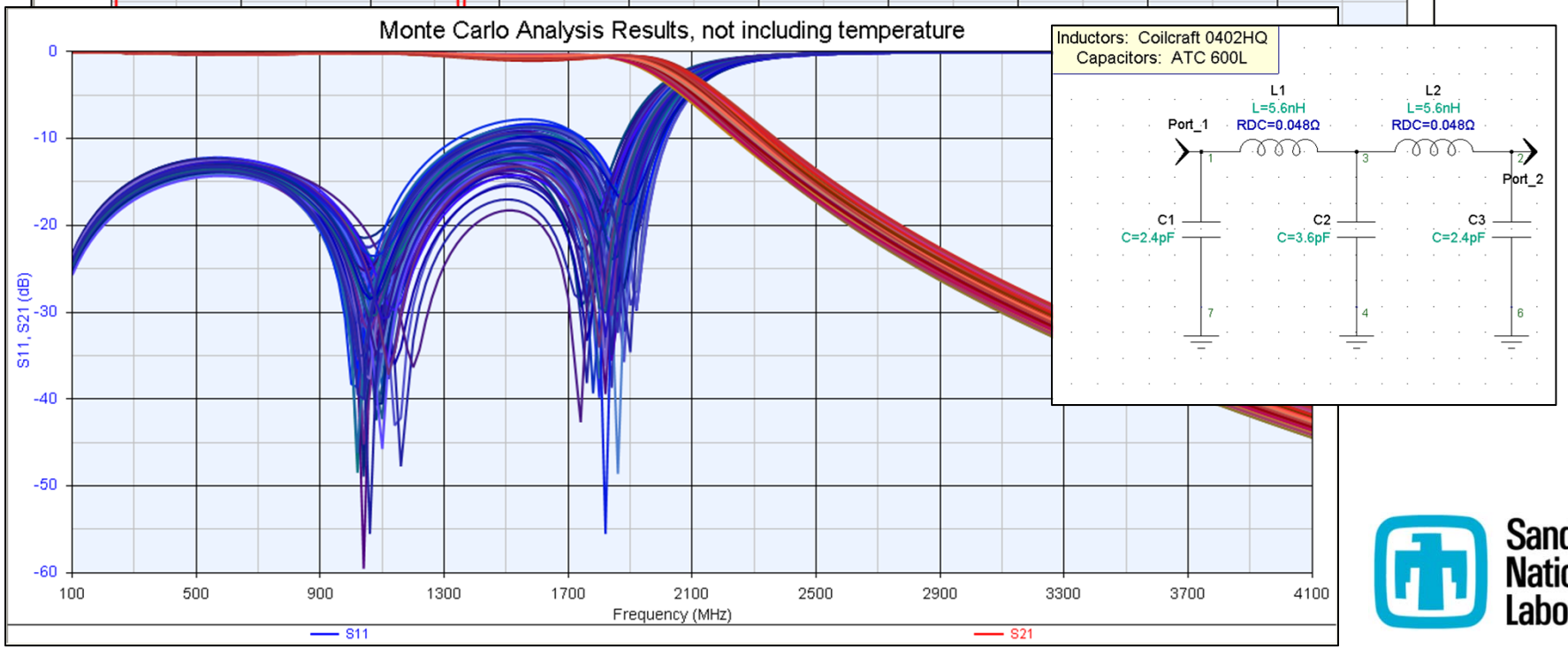
Passives Have Tolerances, Too!
Monte Carlo Analysis





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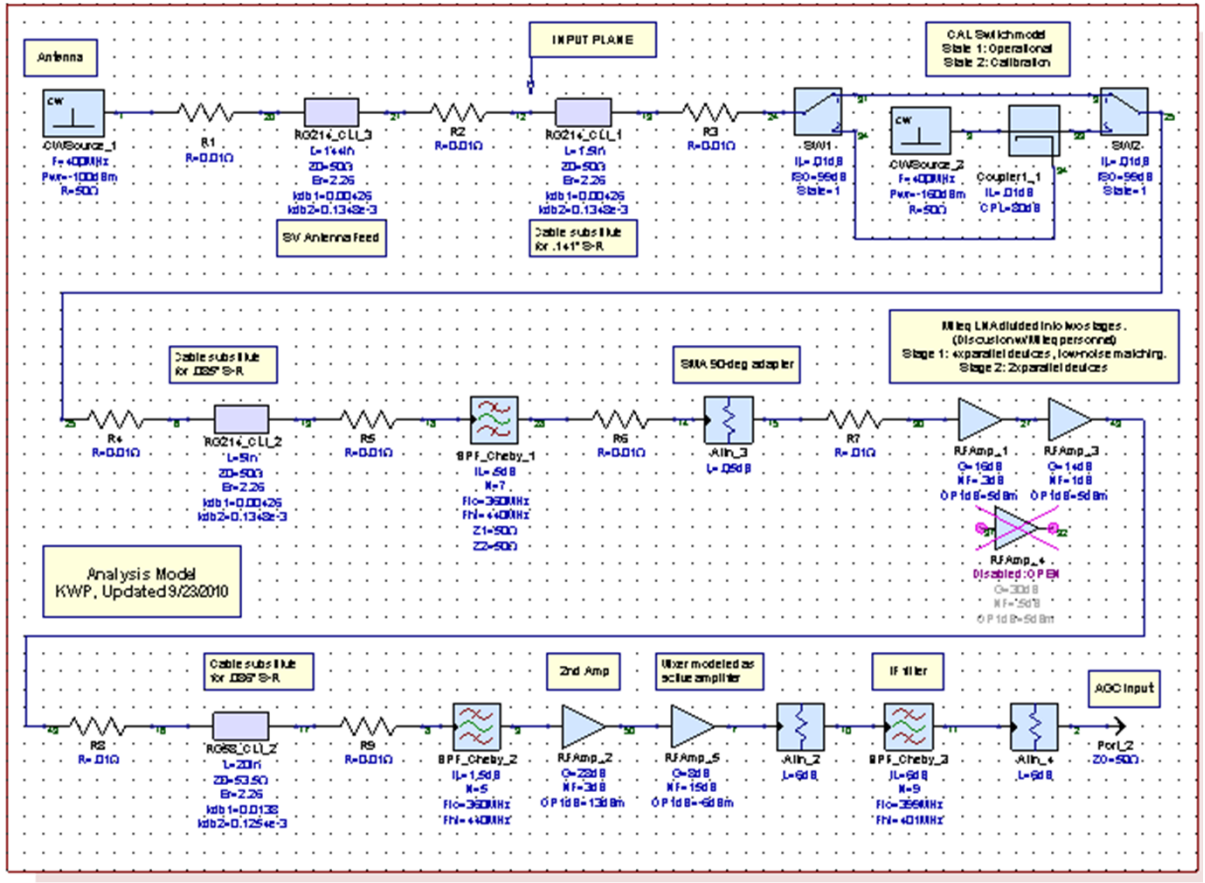
System Concepts

- RF Chain Analysis
  - Cascade analysis is vital to discover the complete picture
    - Input-referred noise figure, gain, IIP3, compression, etc.
    - S-parameters and spreadsheets do not tell the entire picture



Agilent Genesys system simulation file for cascade analysis of a UHF receiver from antenna input to the ADC input.

As with any simulation, it is only as good as the accuracy of the input file, the component models, and the solver algorithms.

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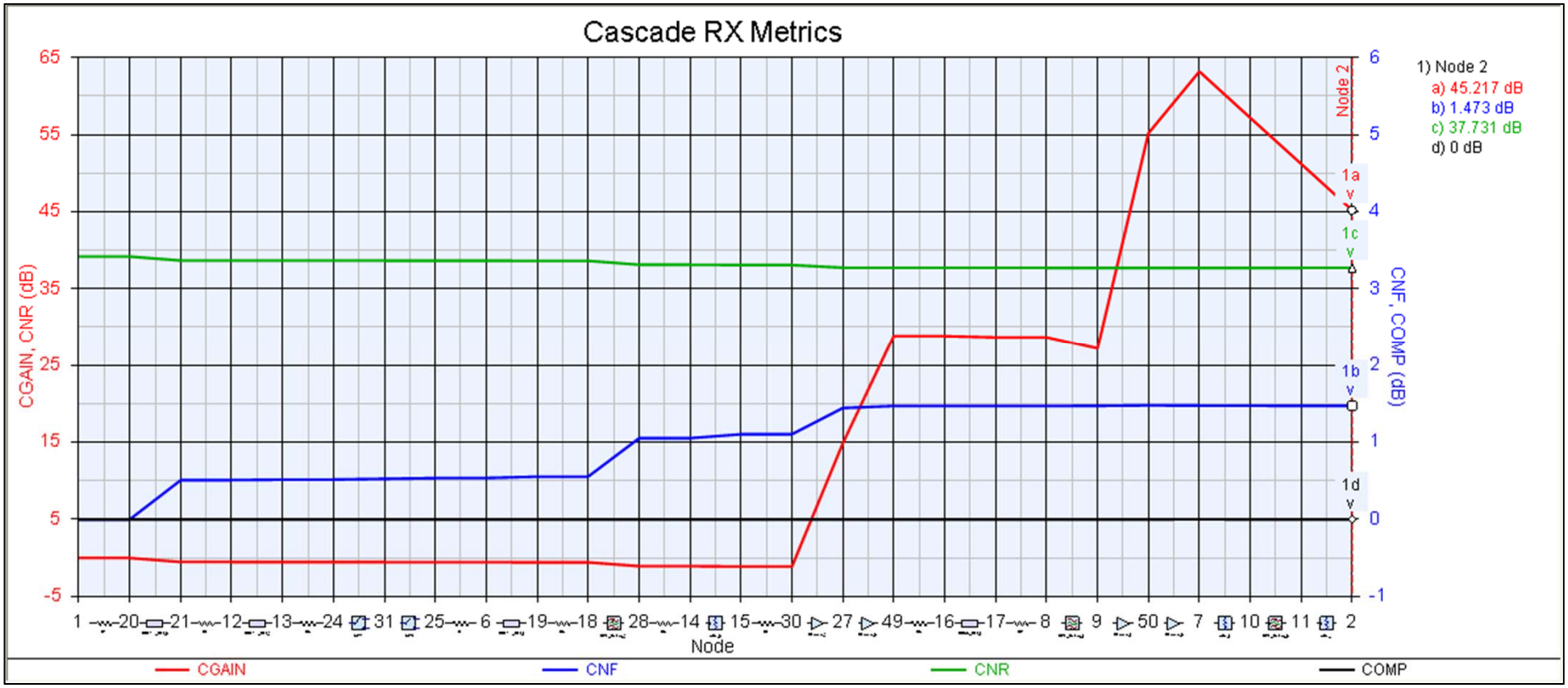
Example Cascade Analysis

Agilent Genesys system simulation results account for power flow in all directions from all sources.

Red: RF Gain; Blue: Input-referred noise figure;
Green: Carrier-to-Noise ratio; Black: Gain compression.



Components in cascade

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System Concepts

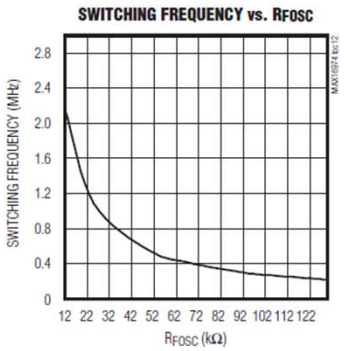
- Other frequency generators are interference to your RF system
  - Digital clocks and logic ICs
    - Fourier components of squarewave clock to dozens of harmonics
    - Example: 19th harmonic of 19.2 MHz digital clock in passband → failed EMI
    - **ROT: Signal BW ≈ 0.35/τ_r**
  - DC switching power supplies
    - 10s of kHz to 10s of MHz depending on the type and application
    - Voltage and current steps, delta functions, ramps, etc. → VERY noisy
  - External signals of all kinds (need EMI shielding and RF port isolation)

MAX16974

High-Voltage, 2.2MHz, 2A Automotive Step-Down Converter with Low Operating Current

Typical Operating Characteristics (continued)

(VSUP = VSUPSW = 14V, VOUT = 5V, FSYNC = GND, fOSC = 400kHz, TA = +25°C, unless otherwise noted. See Figure 1.)



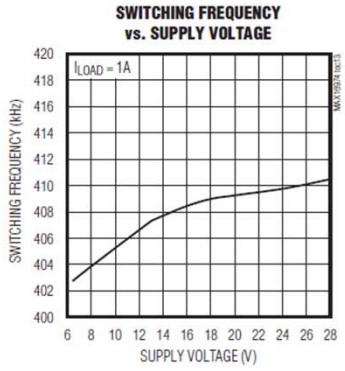


TABLE 1. SPECTRAL (FREQUENCY) COMPONENTS OF A 5 V, 1 GHz, 50% DUTY CYCLE, 100 PS RISE/FALL TIME DIGITAL CLOCK SIGNAL

Harmonic	f	λ	Level	Angle
1	1 GHz	30 cm	3.131 V	−108°
3	3 GHz	10 cm	0.9108 V	−144°
5	5 GHz	6 cm	0.4053 V	−180°
7	7 GHz	4.29 cm	0.1673 V	144°
9	9 GHz	3.33 cm	0.0387 V	108°
11	11 GHz	2.73 cm	0.0259 V	−108°
13	13 GHz	2.31 cm	0.0485 V	−144°

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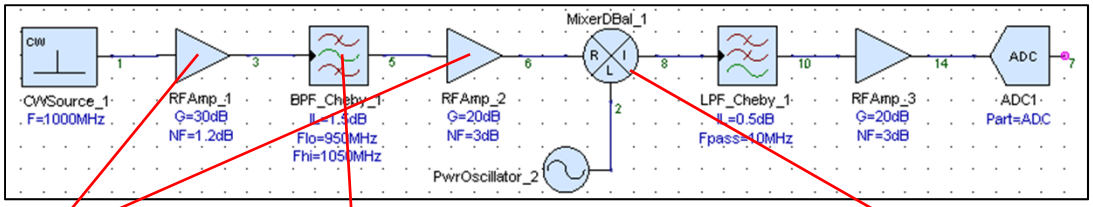
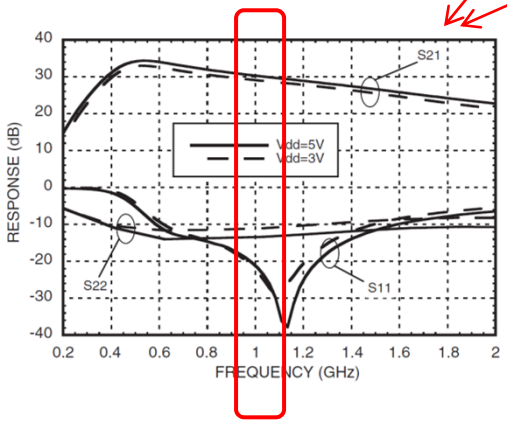
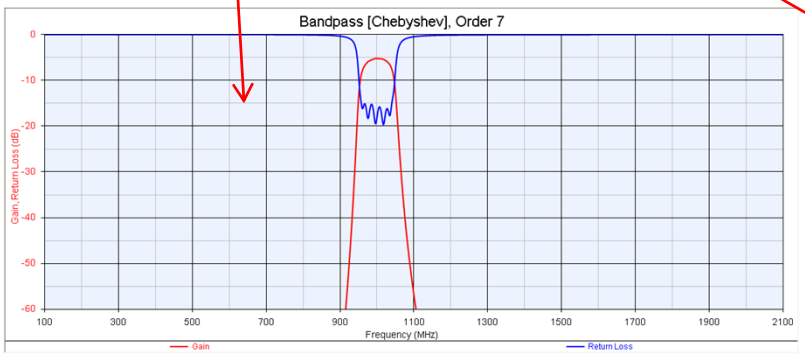
Components in Series

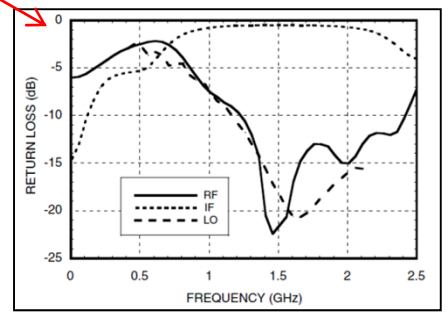
- Caution when using broadband and narrowband devices

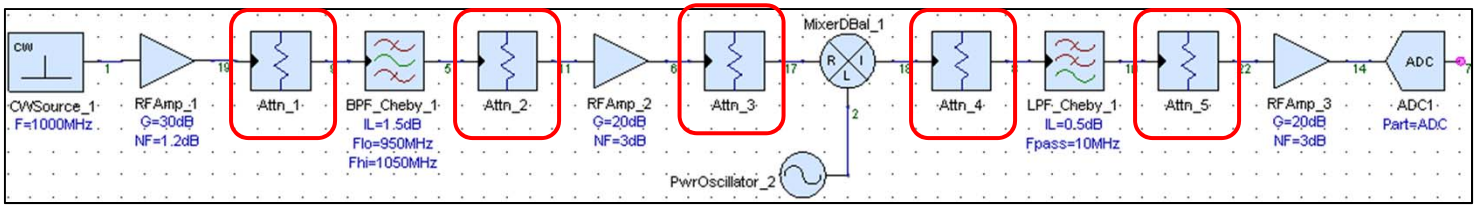


Ideal block diagram









Real block diagram

- **ROT: Use ~ 6 dB attenuators for -12 dB RL broadband**

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Other Interesting System Issues

- Low-Side vs. High-Side Mixing
  - Impact on IF filtering and signal processing
- LO Generation
  - Oscillators, PLLs, multipliers, DDS, etc.
  - Phase noise vs. tuning bandwidth vs. hopping speed
- Measurements of signals in the presence of noise
  - Account for noise power adding to signal power
  - Estimating signal power when SNR << 10 dB
- Etc.

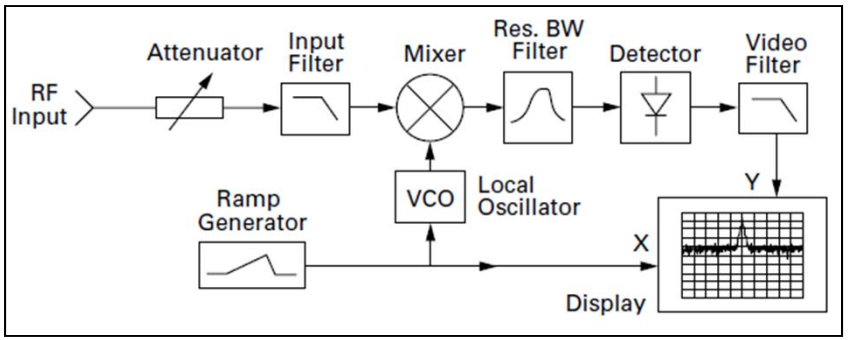
Test Equipment

- The spectrum analyzer and network analyzer are by far the most important pieces of RF test equipment in the lab
- The spectrum analyzer is by far the most complex instrument in the lab, and it is getting MORE complex
  - Concepts you MUST understand (eventually, but sooner = better)
    - Swept vs. FFT ("real time")
    - RBW vs. VBW (vs. sample rate)
    - Detector types
    - Noise, noise figure, and sweep rate
    - Measurement of CW, modulated, and noise-like signals
  - Excellent resources are the various Agilent/HP application notes

- Q: What is the min signal you can measure on a typical Spec An?
- A: Let's find out…
  - In terms of the Displayed Average Noise Level, or DANL

Signal Measurement on Spectrum Analyzer

- **ROT: No ≈ -174 dBm in 1 Hz BW in 50 Ω system at 290K**
- DANL = No + NF + Attenuator
  - A=0, no internal pre-amp: NF ≈ 30 dB → DANL = -144 dBm/Hz
  - A=0, w/ internal pre-amp: NF ≈ 6 dB → DANL = -168 dBm/Hz
    - Pre-amp is usually limited to several GHz
- RF model of swept spectrum analyzer
  - **IPK: RBW sets the total energy detected and displayed in one pixel**
  - **IPK: Thermal noise varies as 10*log10(RBW) for VBW ≥ RBW**
    - Example: RBW = 1 kHz or 1 MHz
      - A=0, no pre-amp: DANL = -114 dBm or -84 dBm
      - A=0, w/ pre-amp: DANL = -138 dBm or -118 dBm
  - **IPK: Use "peak" detector for CW/narrowband, "average" for noise/broadband**



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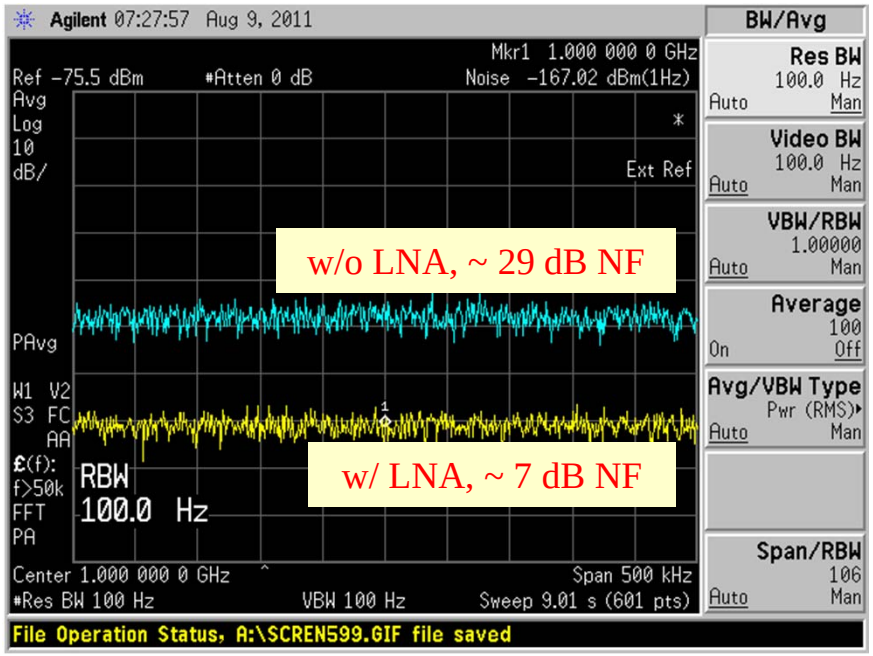
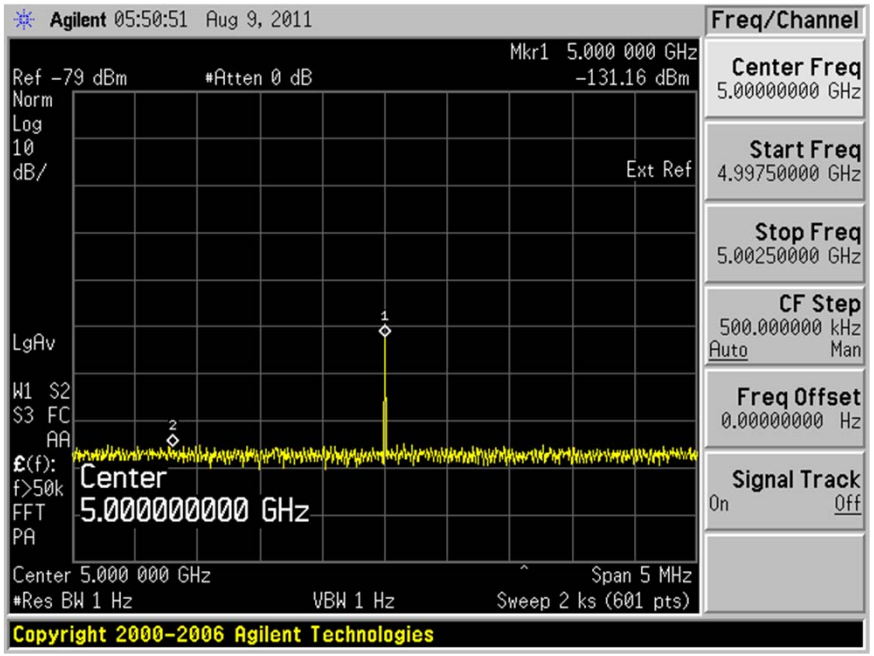
Spec An Noise Floor

Nose PSD measured w/ and w/o LNA



Low SNR CW tone measured with various RBW



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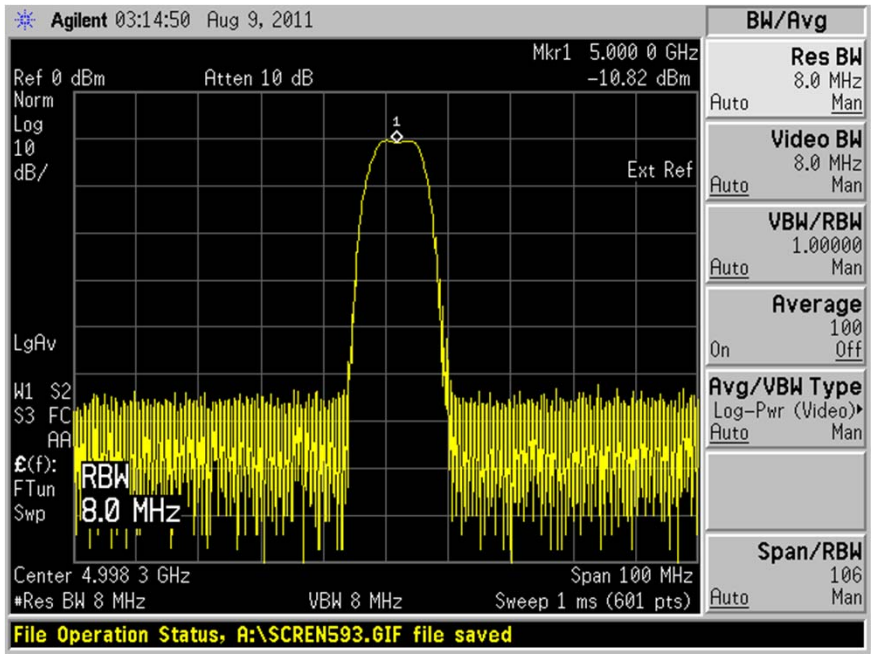
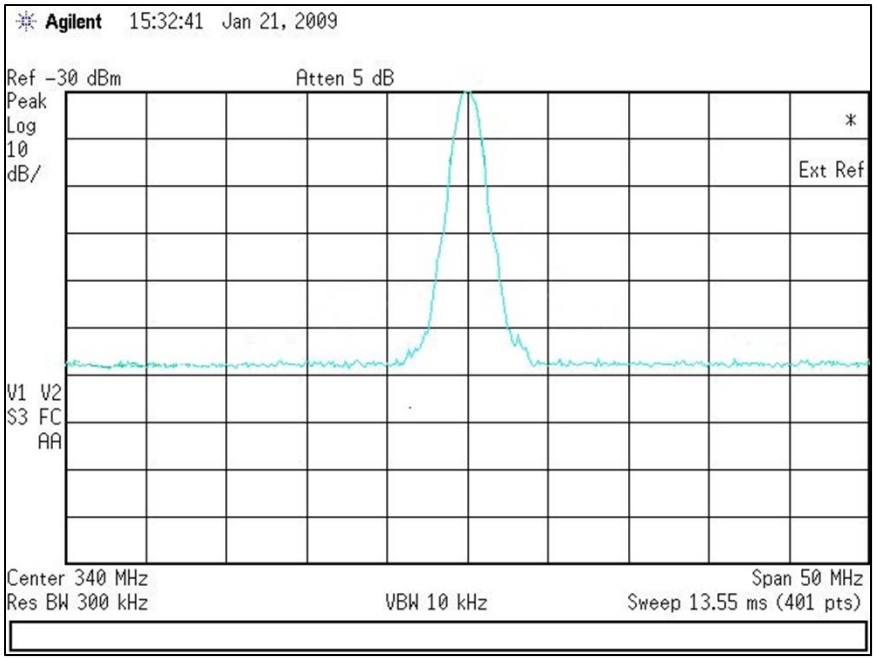
Example of Spec An Measurements

CW signal measured with wide RBWs



Spread-spectrum signal with data filtering



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Summary

- There are dozens (hundreds?) of other topics we could explore…

- Best things you can do to enhance your utility as an RF Engineer
  - Talk to other engineers, ask questions, and observe other designers
  - Simulate/design → build → test → repeat
  - Read and research
  - Go on field tests even if you did not do any of the design
  - Teach/show others what you (think you) know

- Thanks for your time, attention, and enthusiasm!

- Q&A