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Reduction of Distribution Feeders for Simplified PV Impact Studies

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Introduction

PV Interconnection studies that model the impact of the PV to the distribution system can be resource-intensive to simulate the detailed electrical system for high-resolution time-series power flows.

Circuit reduction provides a method for simplifying the complex system to an equivalent representation of the feeder to streamline the interconnection process.

The method preserves any user-specified buses, such as potential PV interconnection locations, to be electrically equivalent to the full model.

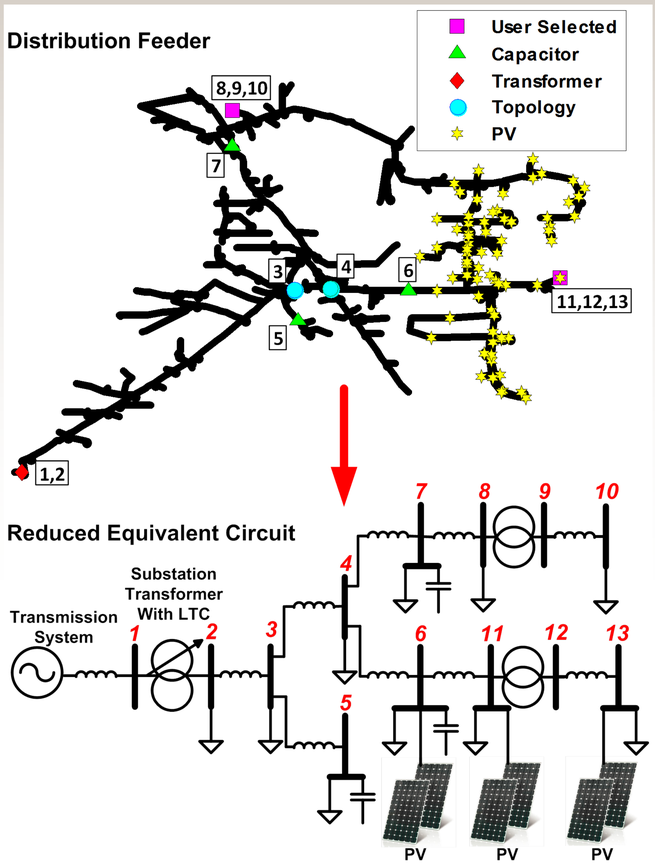
Motivation

The current methods for full interconnection impact studies required detailed and highly complex models of the distribution system.

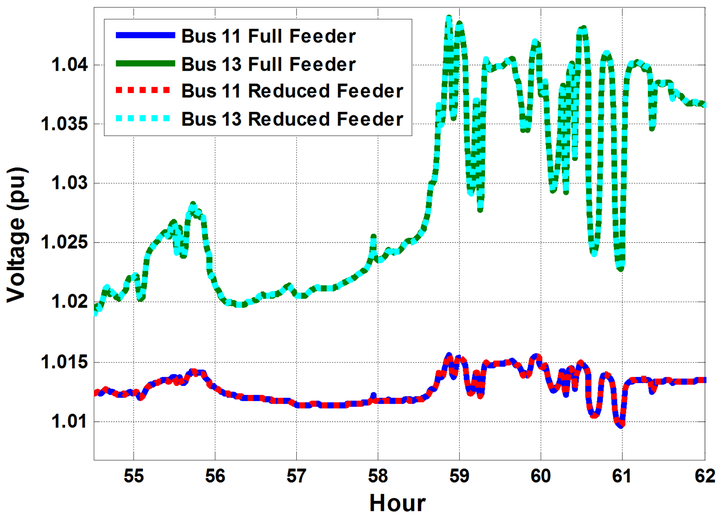
Time-series simulation of a large distribution system at a high time-resolution requires significant computational processing, as do stochastic simulations and multiple-study scenarios.

An equivalent, reduced circuit representation can be used to accurately model the general response of the system while increasing the speed of performing PV interconnection studies by simplifying the complexity of the distribution system.

Circuit reduction also makes it easier to convert a feeder circuit from one software or analysis package, and it provides faster and more accurate interconnection screening criteria by reducing the circuit to a simpler, equivalent representation with only the key circuit parameters.



Time-series analysis with distributed rooftop PV, comparison of full vs. reduced circuit for selected buses of interest.



Magnitude of Reduction from Full Circuit

	Full Circuit	Reduced Circuit	% of Original
Circuit Memory (MB of RAM)	15.5	0.4	2.58%
Time (seconds) to perform a week simulation at 1-second resolution	837.94	15.48	1.85%
Circuit – Number of Lines	1047	9	0.86%
Circuit – Number of Transformers	214	3	1.40%
Circuit – Number of Loads	386	11	2.85%
Circuit – Number of Buses	1262	13	1.03%

Reduction Steps

Step 1: User selects specific buses that should remain in the reduced circuit. The algorithm automatically identifies additional buses of interest such as capacitors, voltage regulators, and junctions required to maintain the topology in the reduced circuit.

Step 2: Remove all buses without objects. This removes all lines that are at the end of a feeder without a load connected to them. It also removes all unnecessary buses that were originally only used for line routing in visualizations and calculating line lengths.

Step 3: Reduce all loads not on paths to buses of interest. All loads are condensed to the nearest upstream bus on a path between the substation and a bus of interest. This often moves loads from their interconnection at the end of a triplex line to the feeder backbone.

Step 4: Perform load bus reduction method presented in the paper to recursively move loads to the adjacent buses.

Implementation

The method was implemented in MATLAB for full automation, with OpenDSS performing the distribution system modeling. MATLAB communicates with OpenDSS through the COM interface to obtain the circuit parameters such as line impedances, line lengths, and load ratings. The circuit reduction is performed in MATLAB and the resulting reduced circuit is saved back out to OpenDSS, where the power flow solutions are simulated for validation.

Current Assumptions

- Three-phase balanced loads
- Fixed-current loads (not fixed P/Q loads)
- Balanced line impedances with no shunt capacitance
- Ignoring the transformer magnetizing current losses

Results and Analysis

Steady-state snapshot and time-series simulations were performed with both the full distribution feeder and the reduced circuit to validate the method.

The reduced circuit is fully equivalent with equal voltages, currents, topology, and impedances.

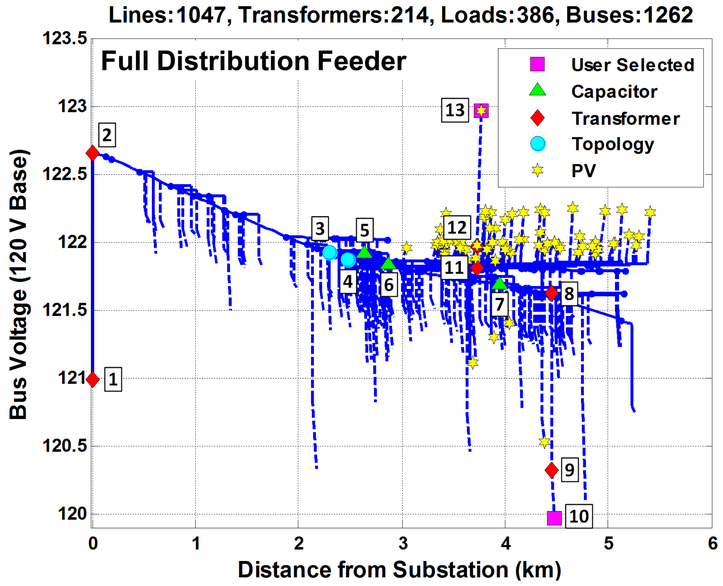
In snapshot analysis comparison between the full distribution feeder and the reduced equivalent circuit of the voltages for buses of interest, error is in the range of $2.22*10^{-6}$ to $3.46*10^{-8}$ in per-unit voltage.

Conclusions

A new method was presented for streamlining the interconnection study process by simplifying the complex system to an equivalent representation of the feeder with fewer buses while maintaining feeder topology as well as the accuracy of key buses of interest.

The equivalent circuit reduction method accurately represents the full circuit for time-series simulations with time-varying load and variable solar generation, and it requires less computation for simulation analyses.

The method is demonstrated with distributed rooftop PV on a 1262-bus feeder with two buses of interest that is reduced to a 13-bus circuit.



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