SAND2013-2987P

Wide-Bandgap Semiconductors for Power Electronics

Bob Kaplar

Sandia National Laboratories

Presented at KLA-Tencor

April 12, 2013

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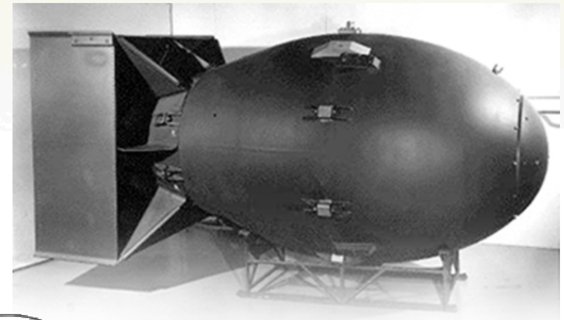
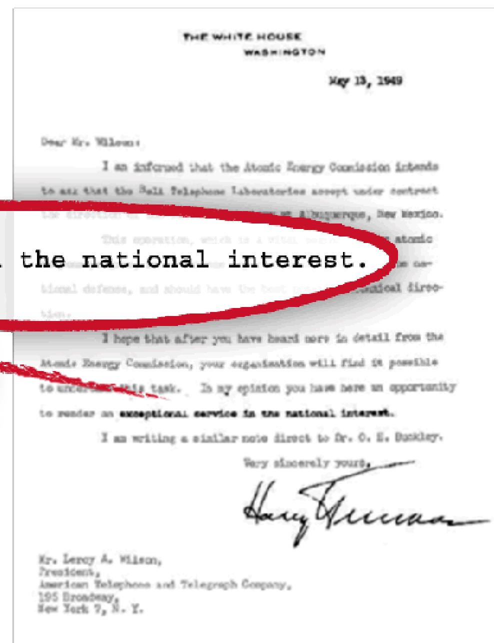
Sandia's History



exceptional service in the national interest.



THE WHITE HOUSE
WASHINGTON

May 13, 1949

Dear Mr. Wilson:

I am informed that the Atomic Energy Commission intends to ask that the Bell Telephone Laboratories accept under contract the direction of [illegible] at Albuquerque, New Mexico.

This operation, which is a vital [illegible] atomic [illegible] na- tional defense, and should have the best [illegible] technical direc- tion.

I hope that after you have heard more in detail from the Atomic Energy Commission, your organization will find it possible to undertake this task. In my opinion you have here an opportunity to render an **exceptional service in the national interest.**

I am writing a similar note direct to Dr. O. E. Buckley.

Very sincerely yours,

Harry Truman

Mr. Leroy A. Wilson,
President,
American Telephone and Telegraph Company,
195 Broadway,
New York 7, N. Y.

Sandia National Laboratories

Sandia's Sites

Albuquerque,
New Mexico

Livermore,
California

Tonopah, Nevada

Waste Isolation Pilot Plant,
Carlsbad, New Mexico

Pantex, Texas

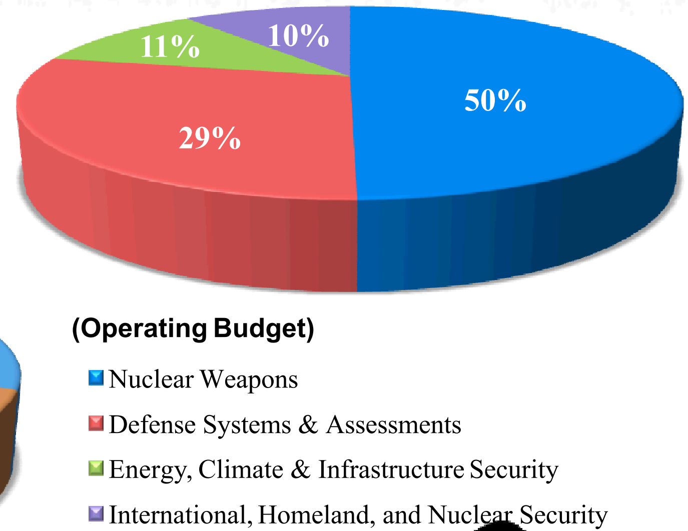
Kauai, Hawaii

Sandia
National
Laboratories

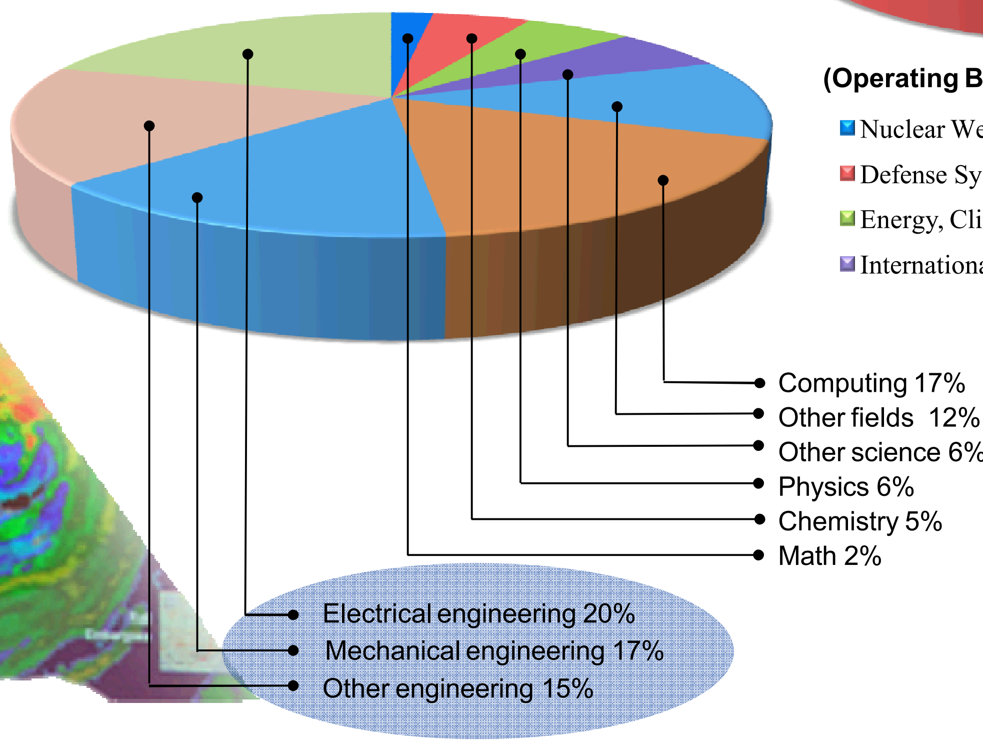
People and Budget

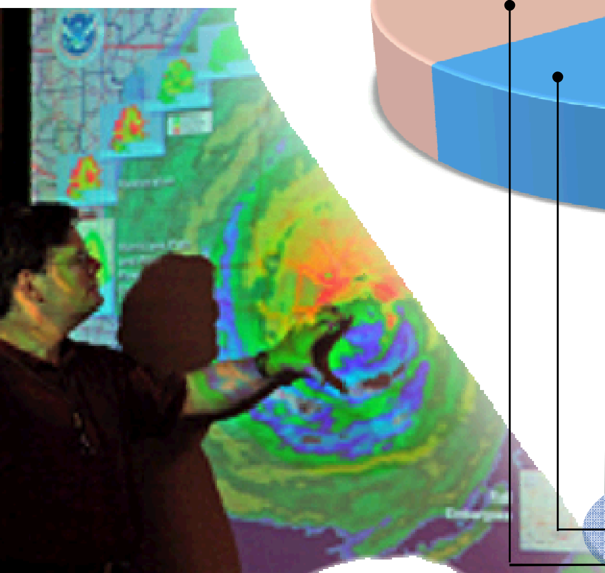
- On-site workforce: 10,605
- Regular employees: 8,859
- Gross payroll: ~$943 million

FY11 Operating Revenue
$2.4 billion



Technical staff (4,344) by discipline





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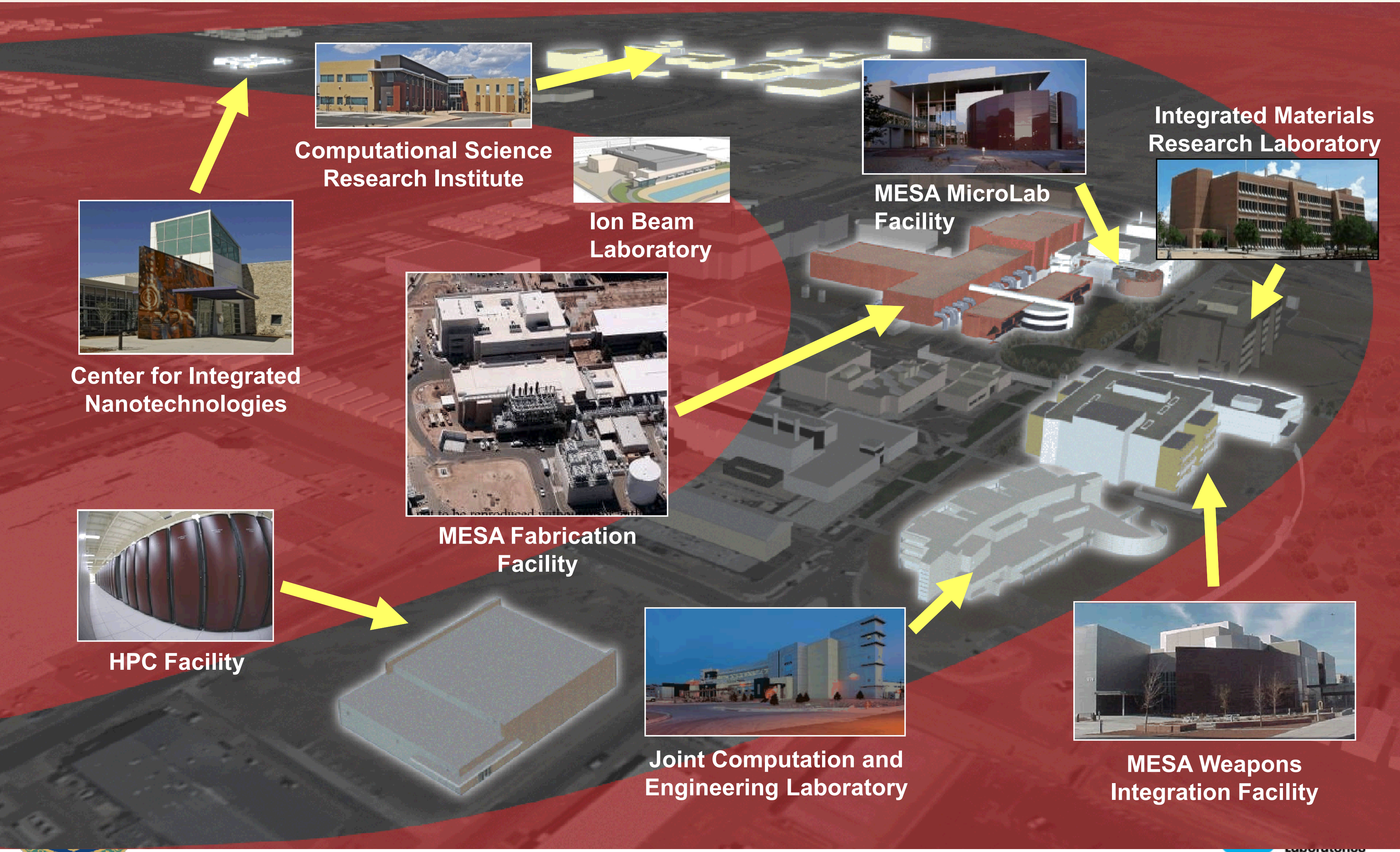
Sandia's Innovation Corridor

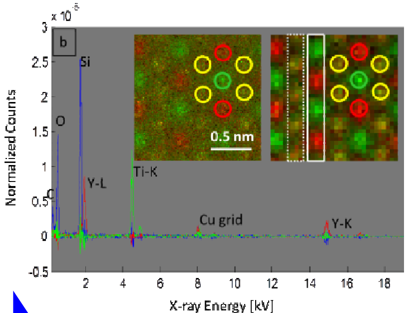


SNL has Extensive R&D Capabilities in Wide Band Gaps – Materials, Devices, and Systems

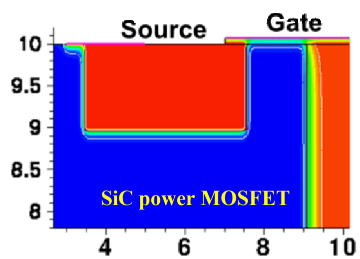
- **60+ years as DOE/NNSA mission lead in electronics**
- **30+ years of compound semiconductor research**
- **20+ years of wide band gap materials & device R&D**
- **Facilities:** ~30,000 ft^2 clean room (MESA facility); Solid-State Lighting EFRC; microgrid testbed (DETL facility); ASIC design & fab; extensive reliability testing and failure analysis

SSLS EFRC

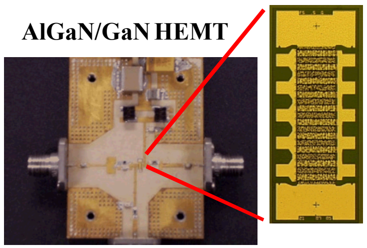
Atomic scale



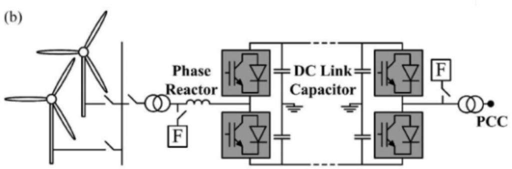
Atomic-resolution characterization



Material and device simulation



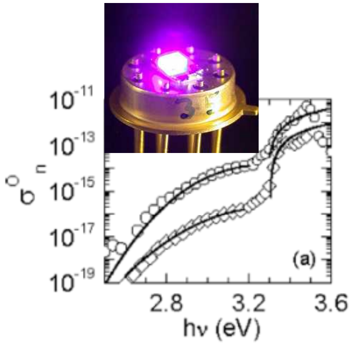
Device fabrication (MESA fab)



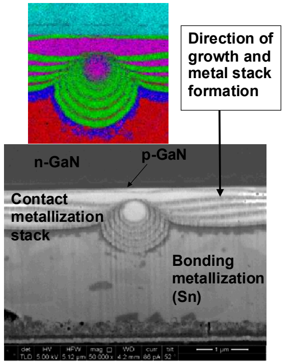
Power circuits and systems

Grid scale

Epitaxial growth



Defect spectroscopy



Reliability physics

Grid-level power networks (DETL)

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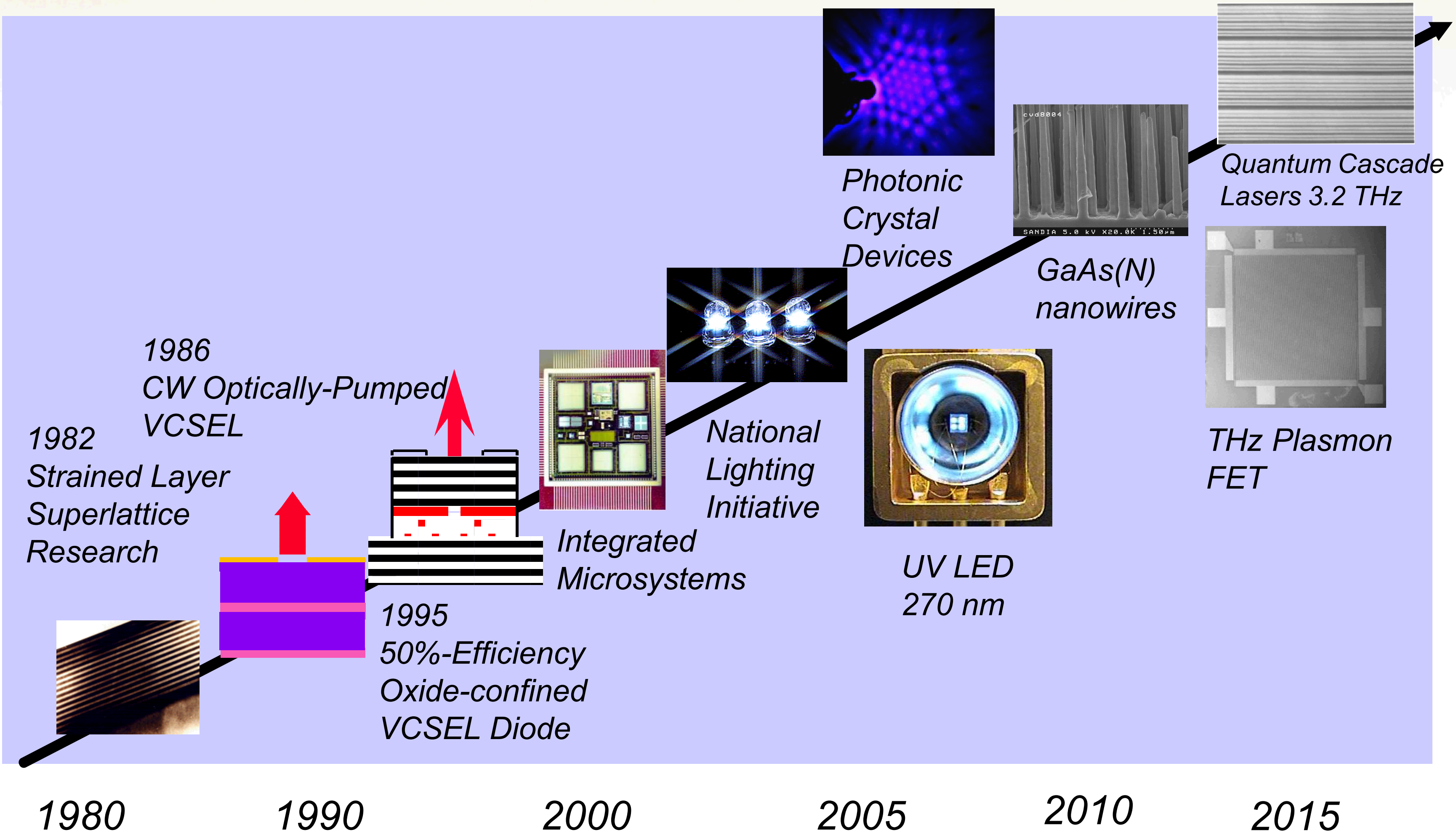
1980-2012: 30+ years of Compound Semiconductor S&T



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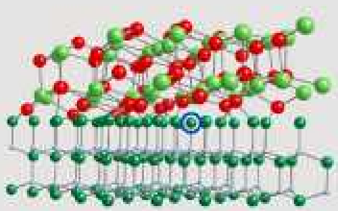
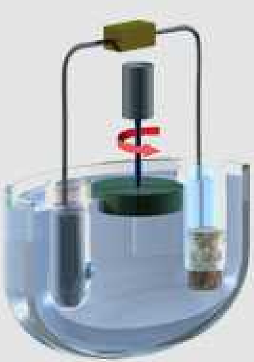
WBG PE Under Sandia's Energy Storage Program

Funded by DOE Energy Storage Program (Dr. Imre Gyuk)
Sandia's Energy Storage PE Program led by Dr. Stan Atcitty

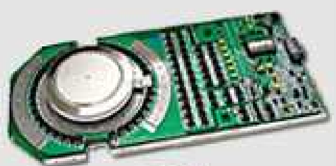
Materials R&D



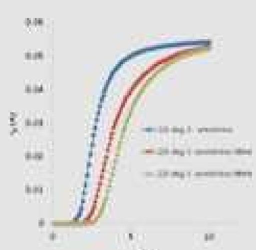
- Gate oxide R&D
- Bulk GaN



Semiconductor devices



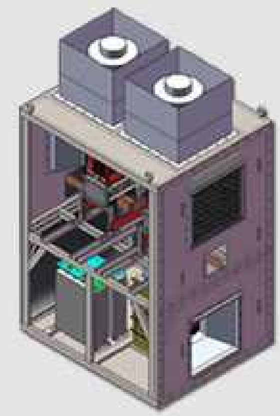
- Post-Si characterization & reliability
- SiC thyristors
- ETO



Power Modules

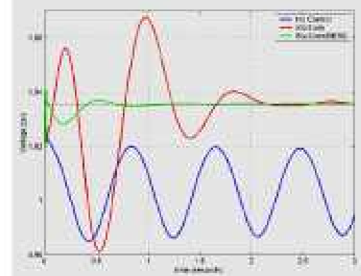
- High temp/density power module

Power Conversion System

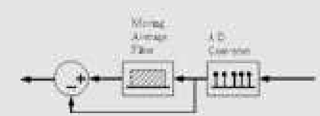


- DSTATCOM plus energy storage for wind energy
- Optically isolated MW inverter
- High density inverter with integrated thermal management
- High temp power inverter

Applications



- Power smoothing and control for renewables
- FACTS and energy storage



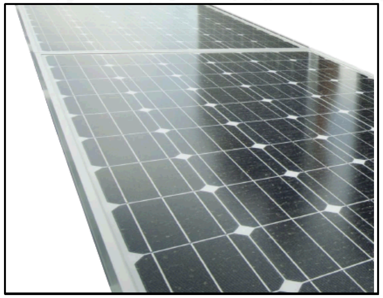
Comparison of Semiconductor Materials

WBG materials allow higher photon energy for optoelectronics, and higher voltage, current, temperature, and frequency for power electronics

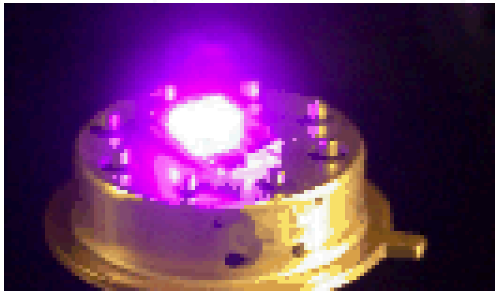
Property	Si	4H-SiC	GaN	Diamond	AlN
Bandgap E_g, (eV)	1.1	3.2	3.4	5.5	6.2
Dielectric constant, ε_r	11.9	10.1	9	5.5	9
Electric breakdown field, E_c (MV/cm)	0.3	2.2	3	10	13
Electron Mobility, μ_n ($cm^2/V\cdot s$)	1500	700	900 (bulk) 2000 (2D)	1900	300
Hole Mobility, μ_p ($cm^2/V\cdot s$)	600	115	150	600	20
Thermal Conductivity, λ (W/cm·K)	1.5	4.9	> 1.3	22	2.9
Saturated Electron Drift Velocity, v_{sat} ($\times 10^7$cm/s)	1	2	2.5	2.7	1.2

WBGs Are Increasingly Critical to Energy Technologies

Transitioning to cleaner and more efficient energy sources will require development and integration of WBG devices



Power electronics and inverters for electric vehicles and the electrical grid



Solid-state lighting

Material	Bandgap (eV)
Si	1.1
4H-SiC	3.2
GaN	3.4
Diamond	5.5
AlN	6.2

4H-SiC, GaN: Wide-Bandgap

Diamond, AlN: Ultra-Wide-Bandgap

WBGs Enable Reductions in Power Loss, Size, and Weight

Device	Brkdwn Voltage	$P_{switching}$ 500 Hz	$P_{switching}$ 5 kHz	$P_{switching}$ 20 kHz	$P_{conduction}$ 100°C
Cree SiC MOSFET	12 kV	4 W/cm^2	40 W/cm^2	160 W/cm^2	100 W/cm^2
ABB Si IGBT	2x6.5 kV	72.5 W/cm^2	725 W/cm^2	2900 W/cm^2	182 W/cm^2

Cree/Powerex/GE

Si IGBT module
13.5 kV, 100 A

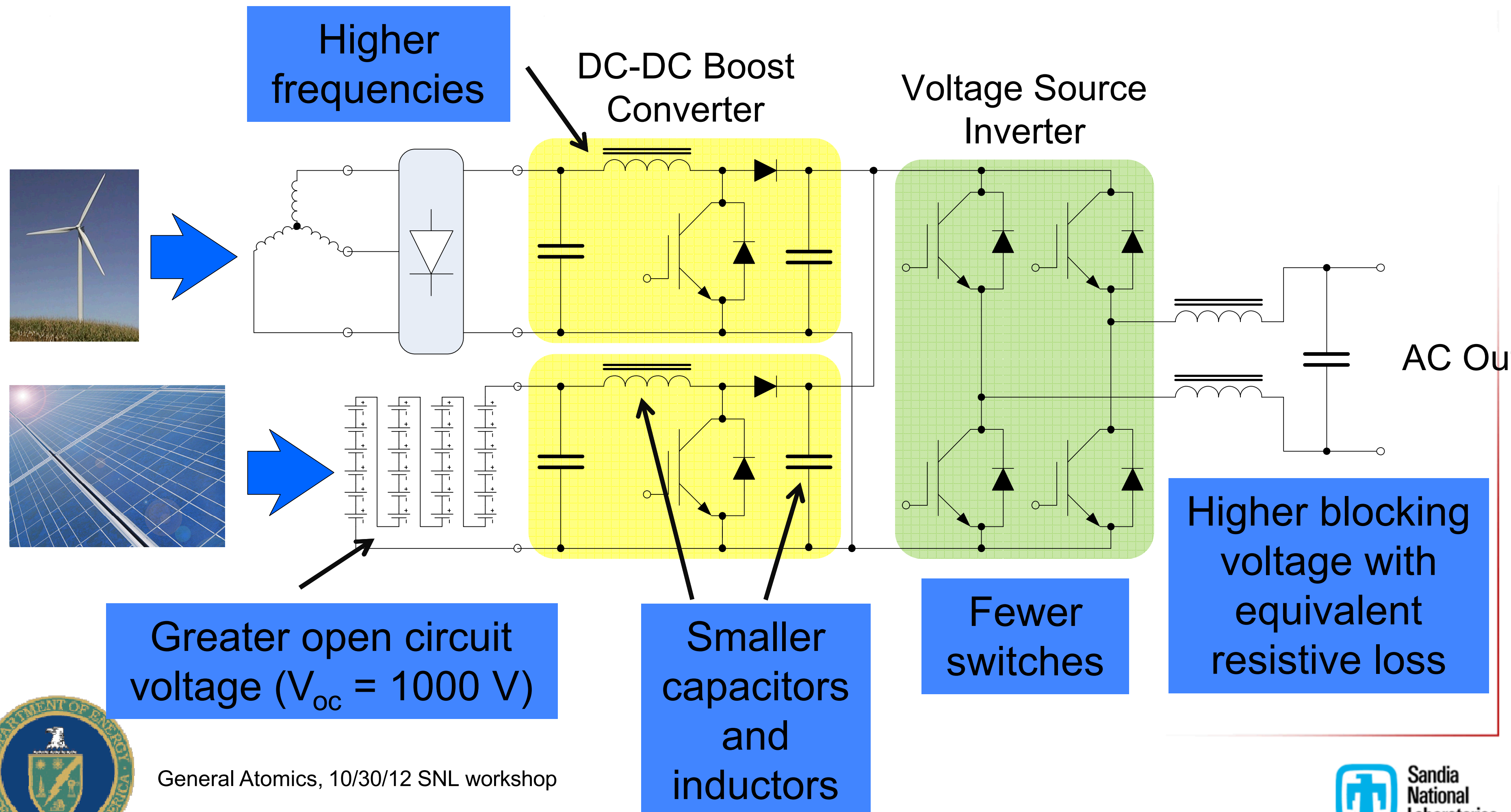
SiC MOSFET module
10 kV, 120 A

SiC MOSFET module is 10% weight and 12% volume of Si IGBT module

M. K. Das et al., ICSCRM 2011

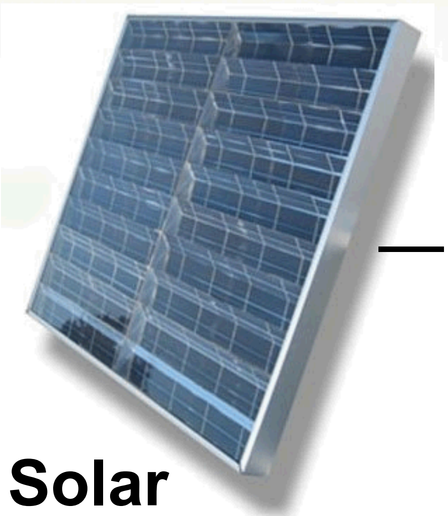
WBGs for Increased Grid Efficiency and Resiliency

A modern, resilient electric grid with integrated renewable power sources requires power electronics and power inverters



General Atomics, 10/30/12 SNL workshop

WBG Power Devices for PV Inverters



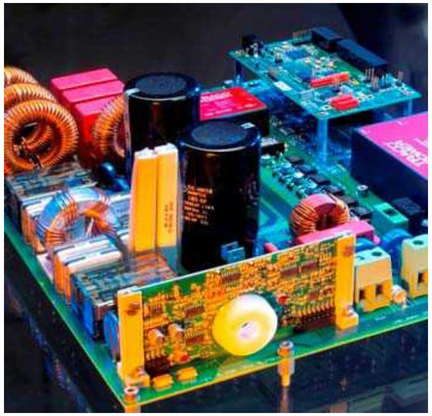
Solar module

—DC—

Inverter

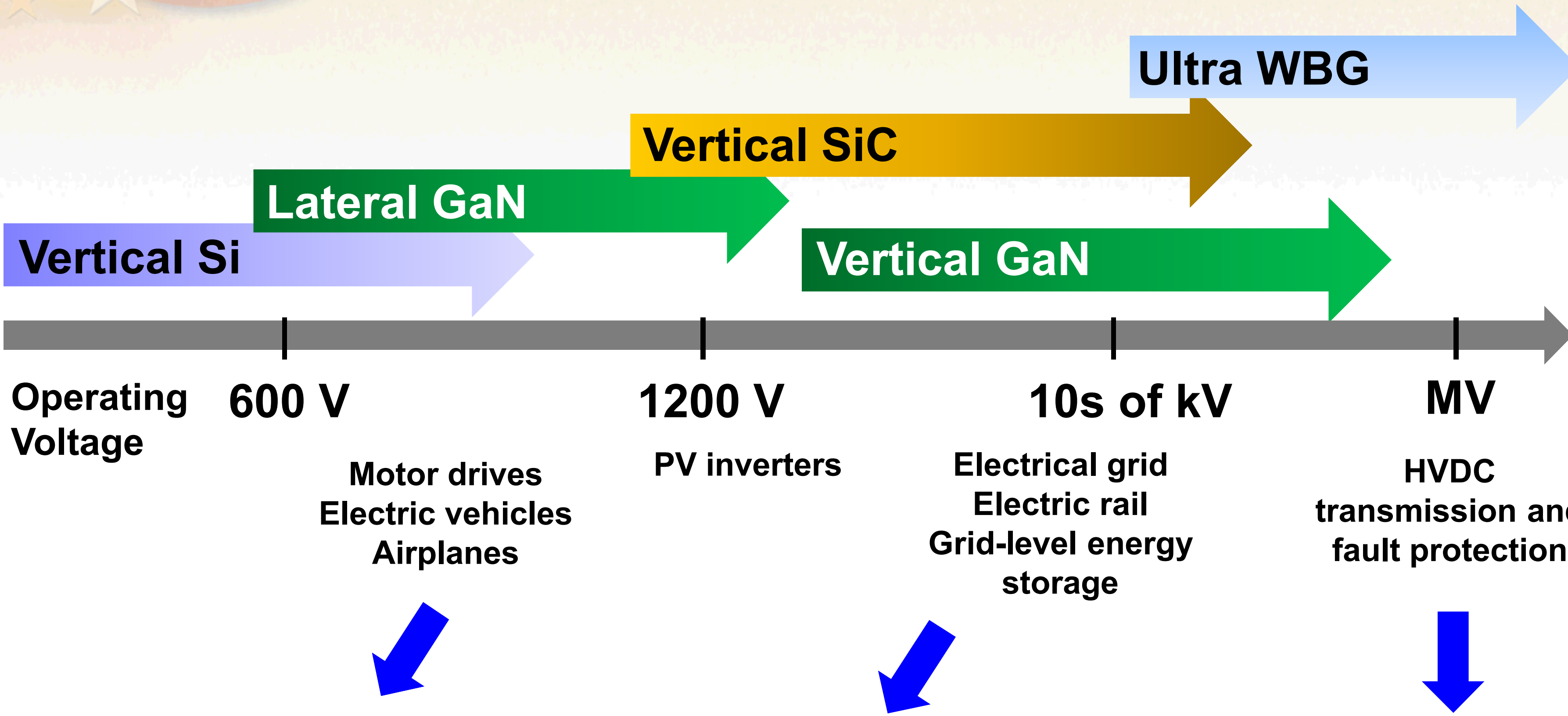
—AC—

Grid



Circuit board from Fraunhofer 97.5% efficient PV inverter using SiC MOSFETs

Application Space for WBG Devices



- Reduce or eliminate passive components (capacitors, inductors)
- Spectral purity extends motor lifetime
- Operate at higher temperatures without liquid cooling

- AC subsystems to 13.8 kV

- Increase grid resiliency
- Less resistive energy loss
- Replace expensive IGBT/IGCT stack

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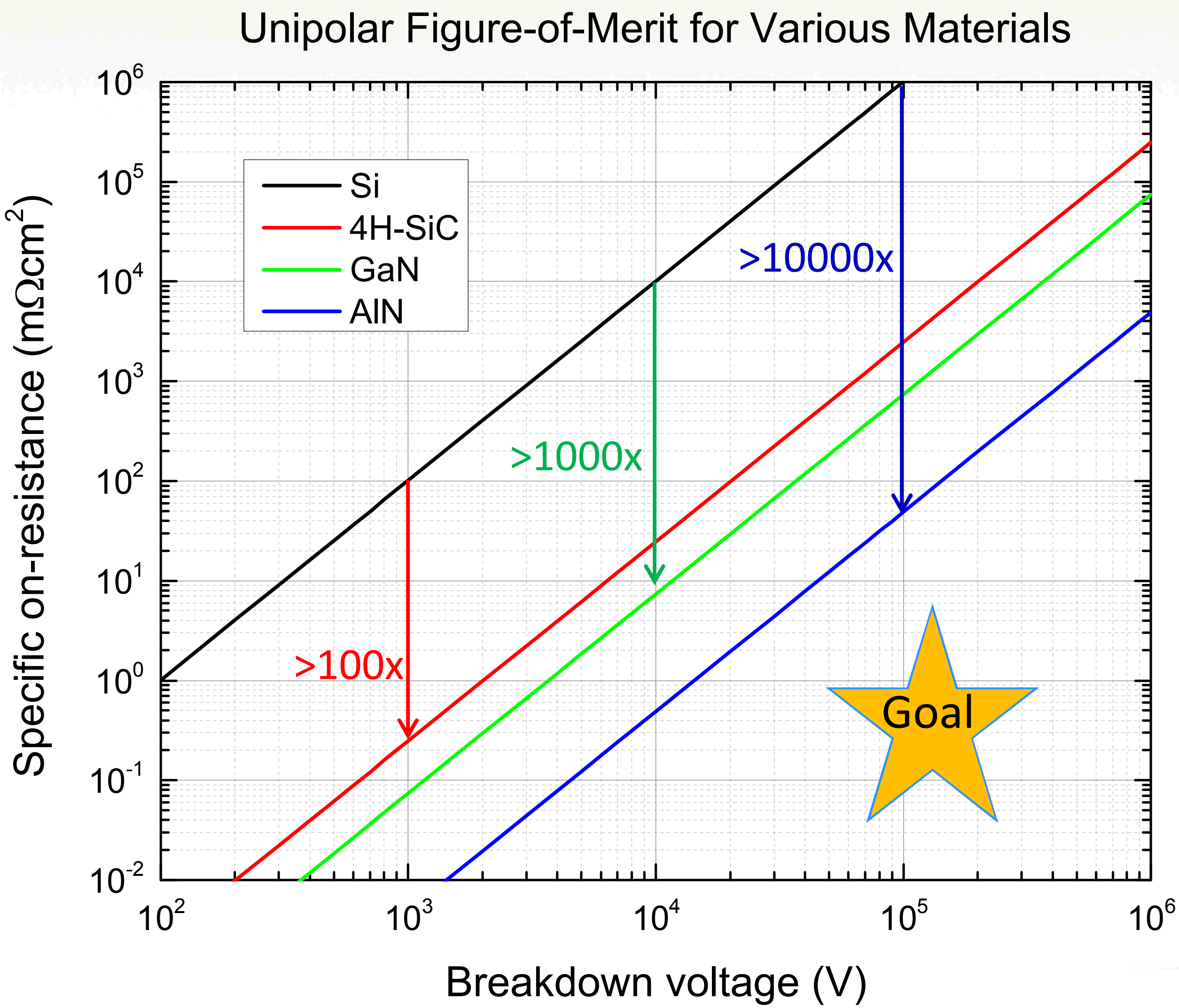
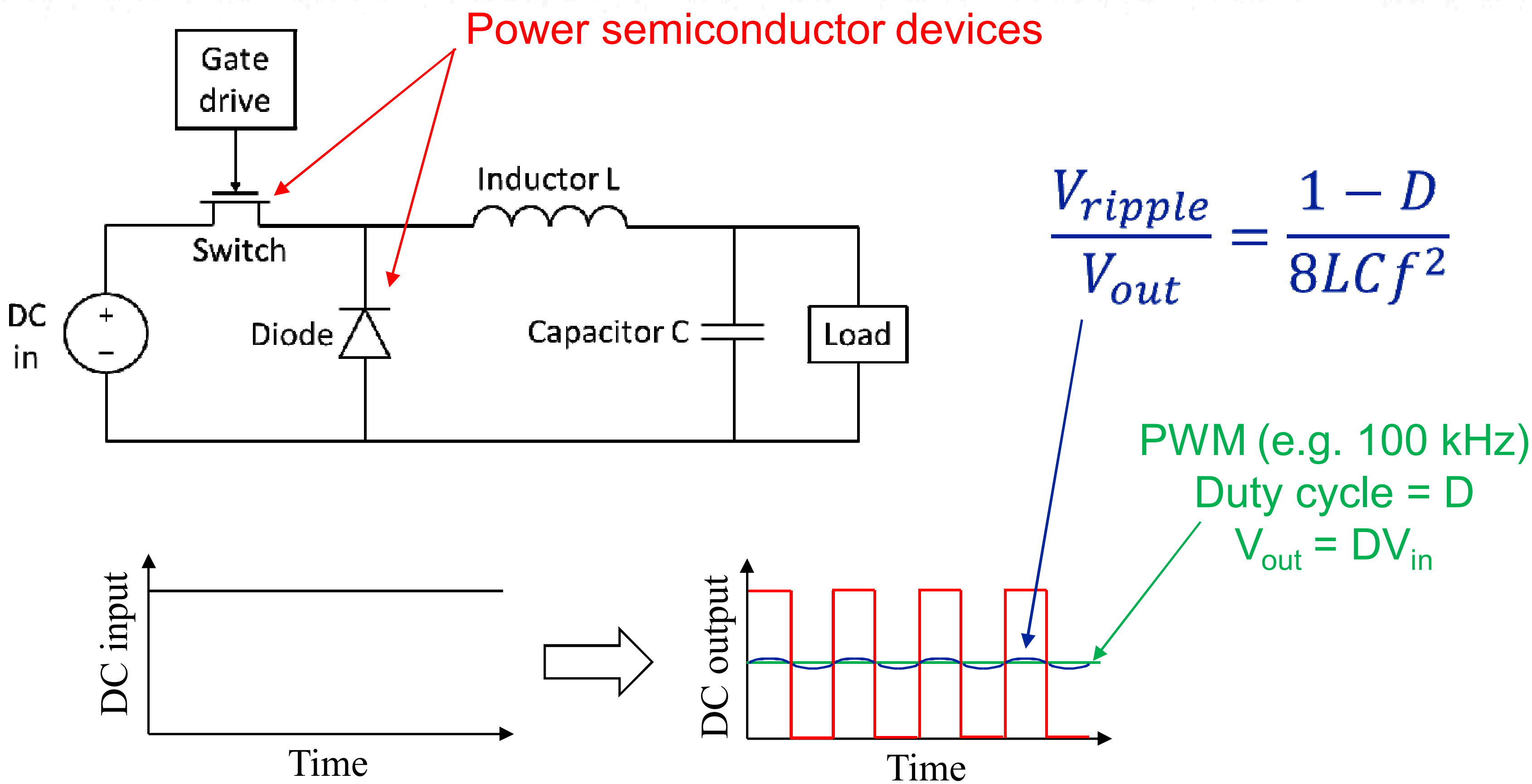
WBGs Offer Orders-of-Magnitude Improvement for PE

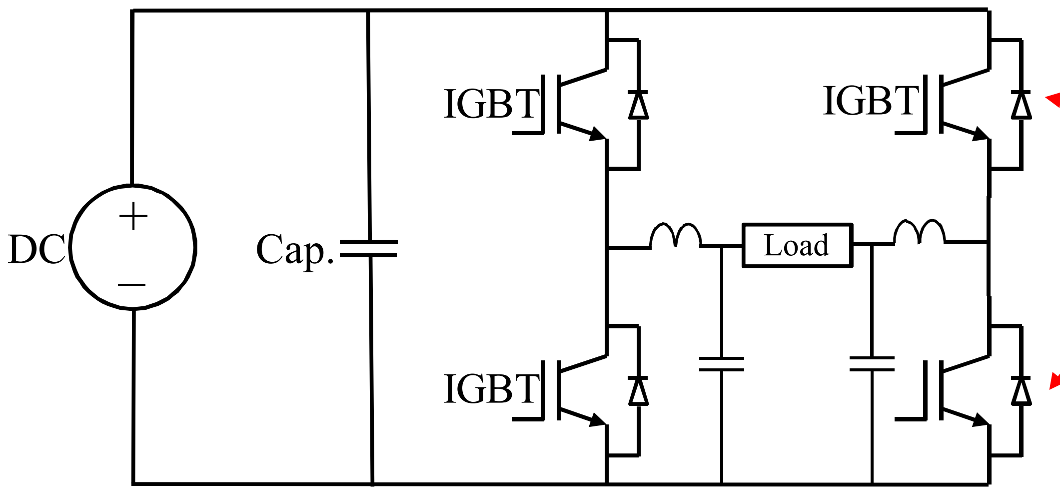


Example Power Electronics Circuit: Step-Down (Buck) DC-to-DC Converter

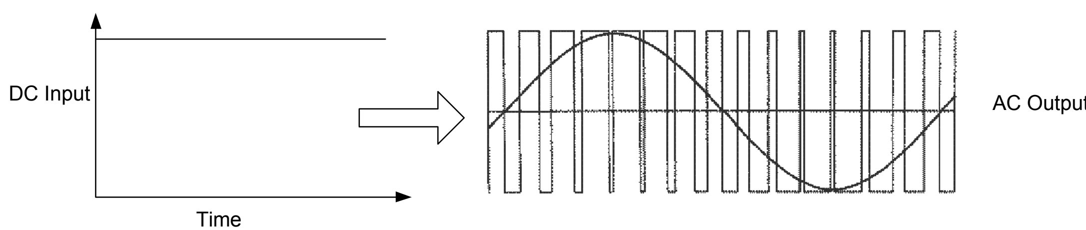


$$\frac{V_{ripple}}{V_{out}} = \frac{1 - D}{8LCf^2}$$

Example of Power Electronics Circuit: Single-Phase Inverter

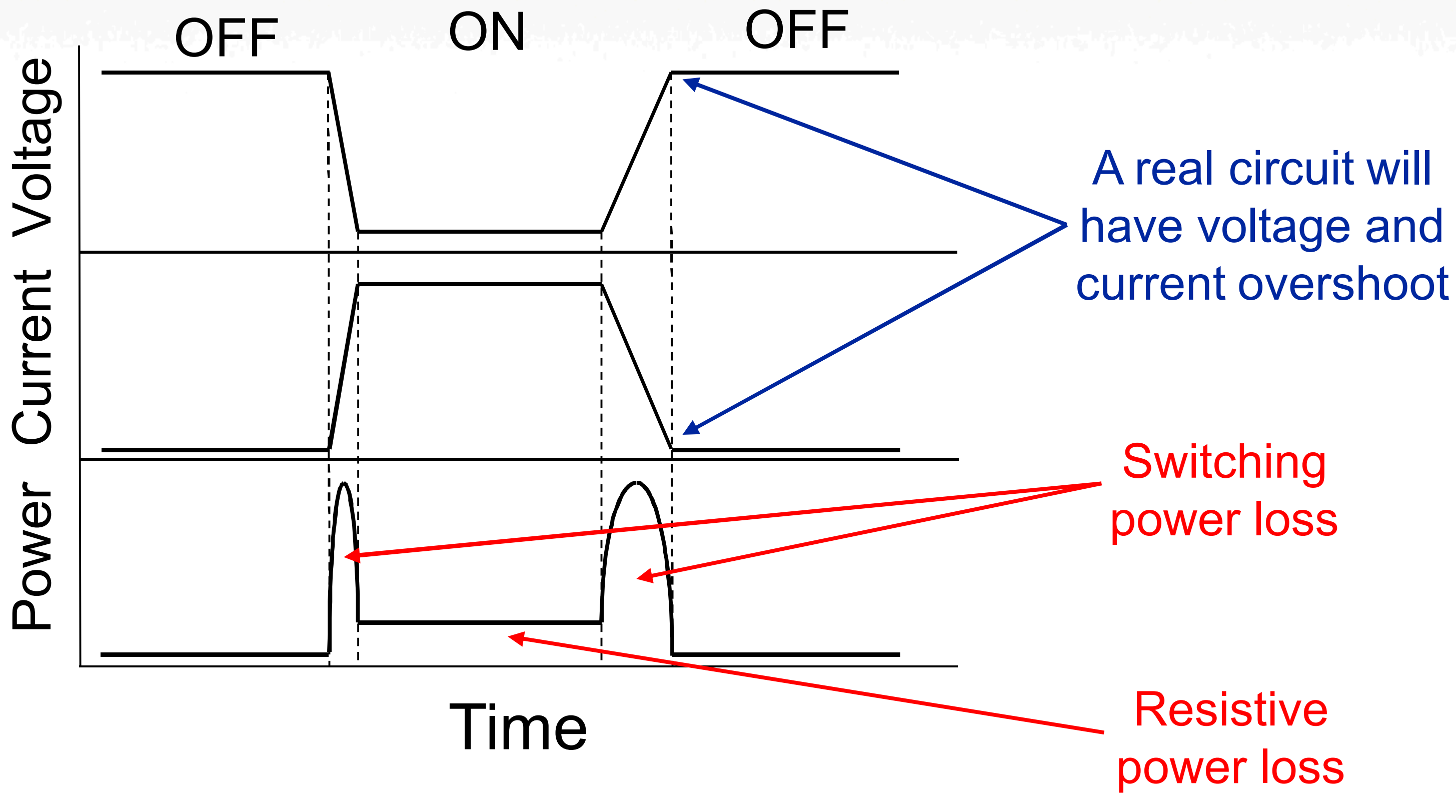


Power semiconductor devices (switches plus free-wheeling diode)



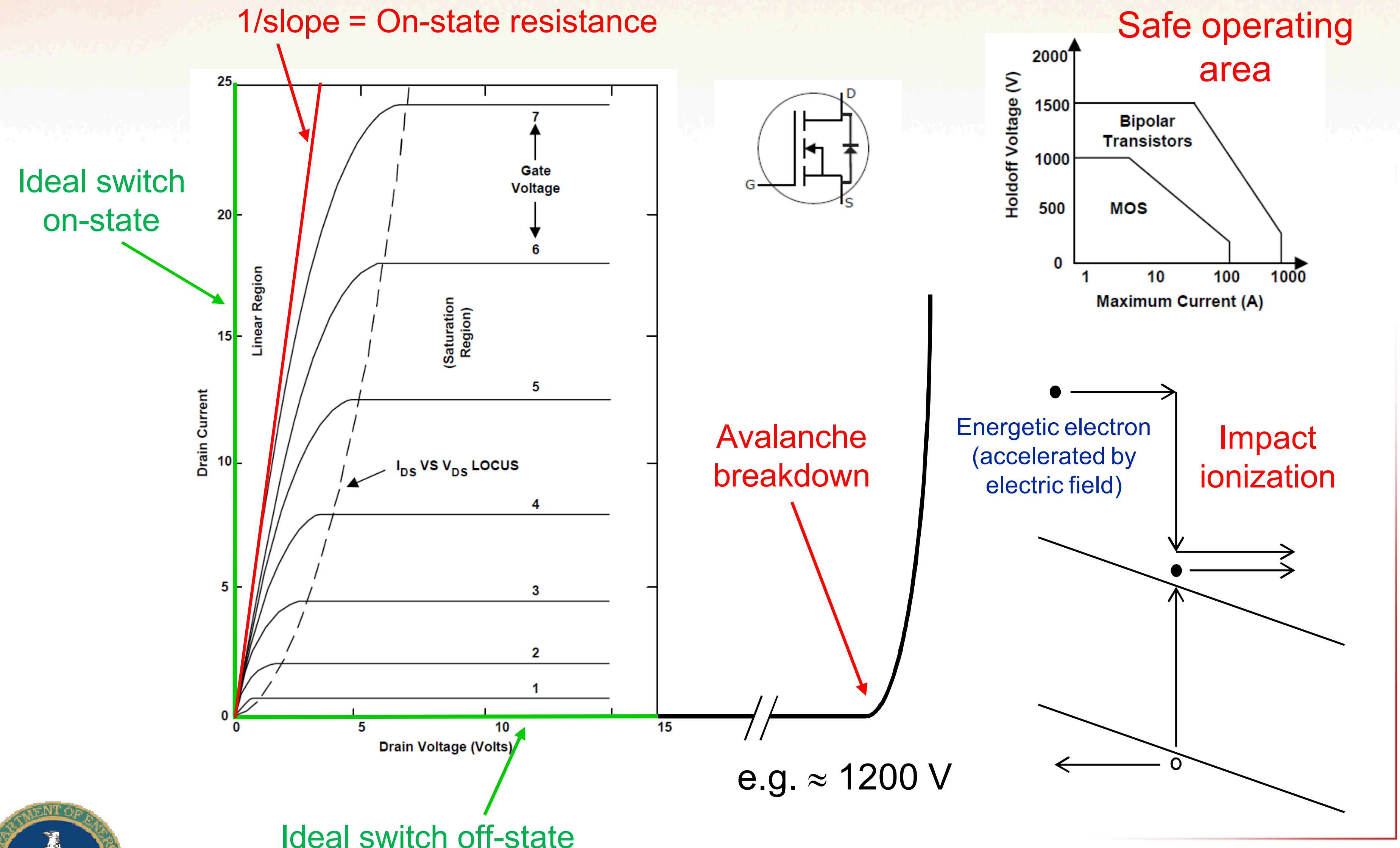
Pulse-Width Modulation (PWM) 10 – 20 kHz

PE Switch Current, Voltage, and Power Waveforms



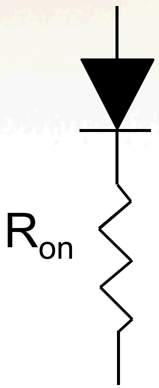
Minimum ON-state loss: Low R_{on}
Minimum OFF-state loss: Low leakage
Minimum switching loss: Fast switching transients

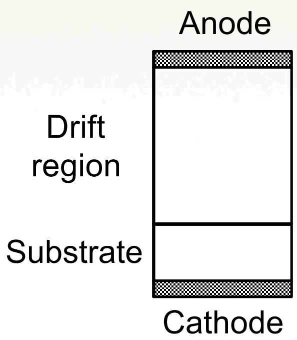
Real Power Devices are NOT Ideal Switches!

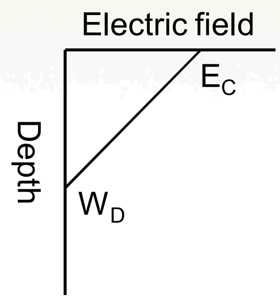


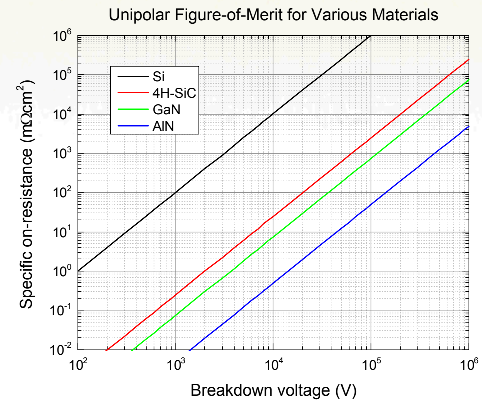
Figures from International Rectifier "Power MOSFET Basics" pamphlet

Unipolar Power Device Figure-of-Merit







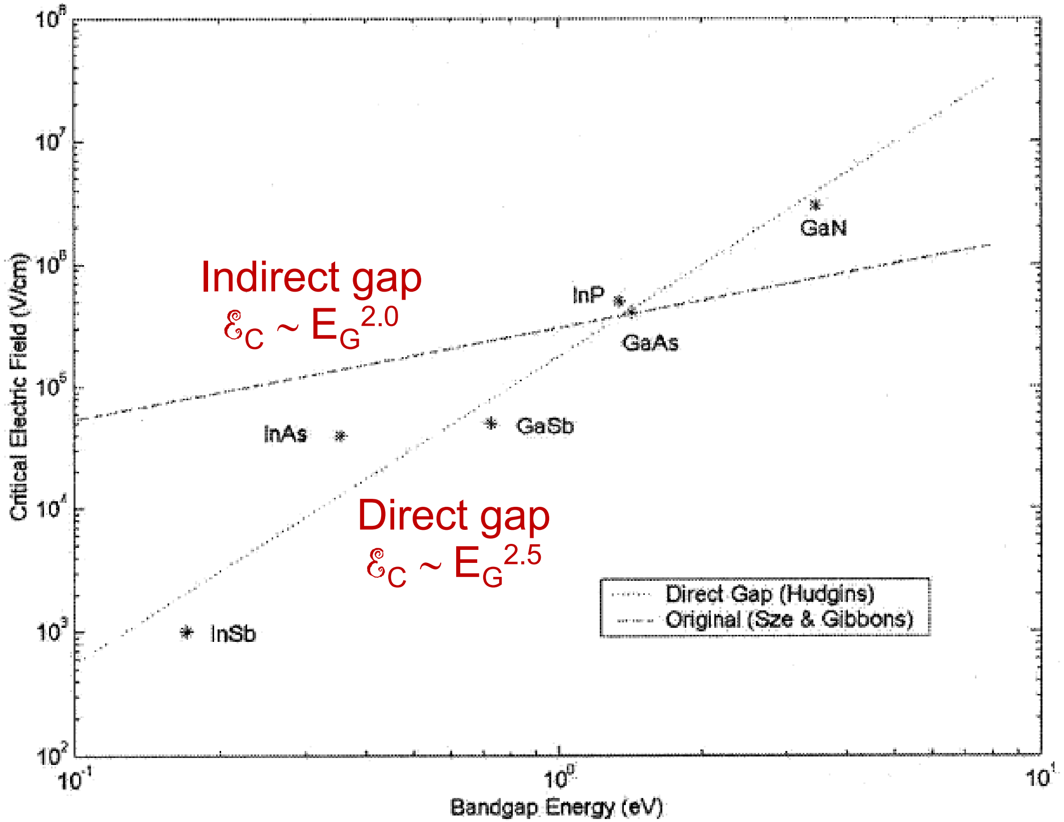


- Off-state: Integrate electric field to get breakdown voltage $V_B = W_D E_C/2$ (1)
- Gauss' law: $\varepsilon E_C = qN_D W_D$ (2)
- On-state: Current transport due to carrier drift, resistance $R_{on} = W_D/\sigma A$
  Conductivity $\sigma = q\mu_n n = q\mu_n N_D$ assuming complete dopant ionization
  Specific on-resistance $R_{on,sp} = R_{on}A = W_D/\sigma = W_D/ q\mu_n N_D$ (3)

- Combining (1) and (2) gives dependence of V_B on N_D and E_C: $V_B = \varepsilon E_C^2/2qN_D$

- Combining (1), (2), and (3) one obtains the unipolar "figure-of-merit":
  $R_{on,sp} = 4V_B^2/\varepsilon\mu_n E_C^3 \rightarrow V_B^2/R_{on,sp} = \varepsilon\mu_n E_C^3/4$

Dependence of Critical Electric Field on Bandgap



Thus, a very strong dependence of FOM on E_G!

- Direct: FOM ~ $E_G^{7.5}$
- Indirect: FOM ~ $E_G^{6.0}$

J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An Assessment of Wide Bandgap Semiconductors for Power Devices," IEEE Trans. on Elect. Dev. **18(3)**, 907 (2003).

Application Classes of Power Devices

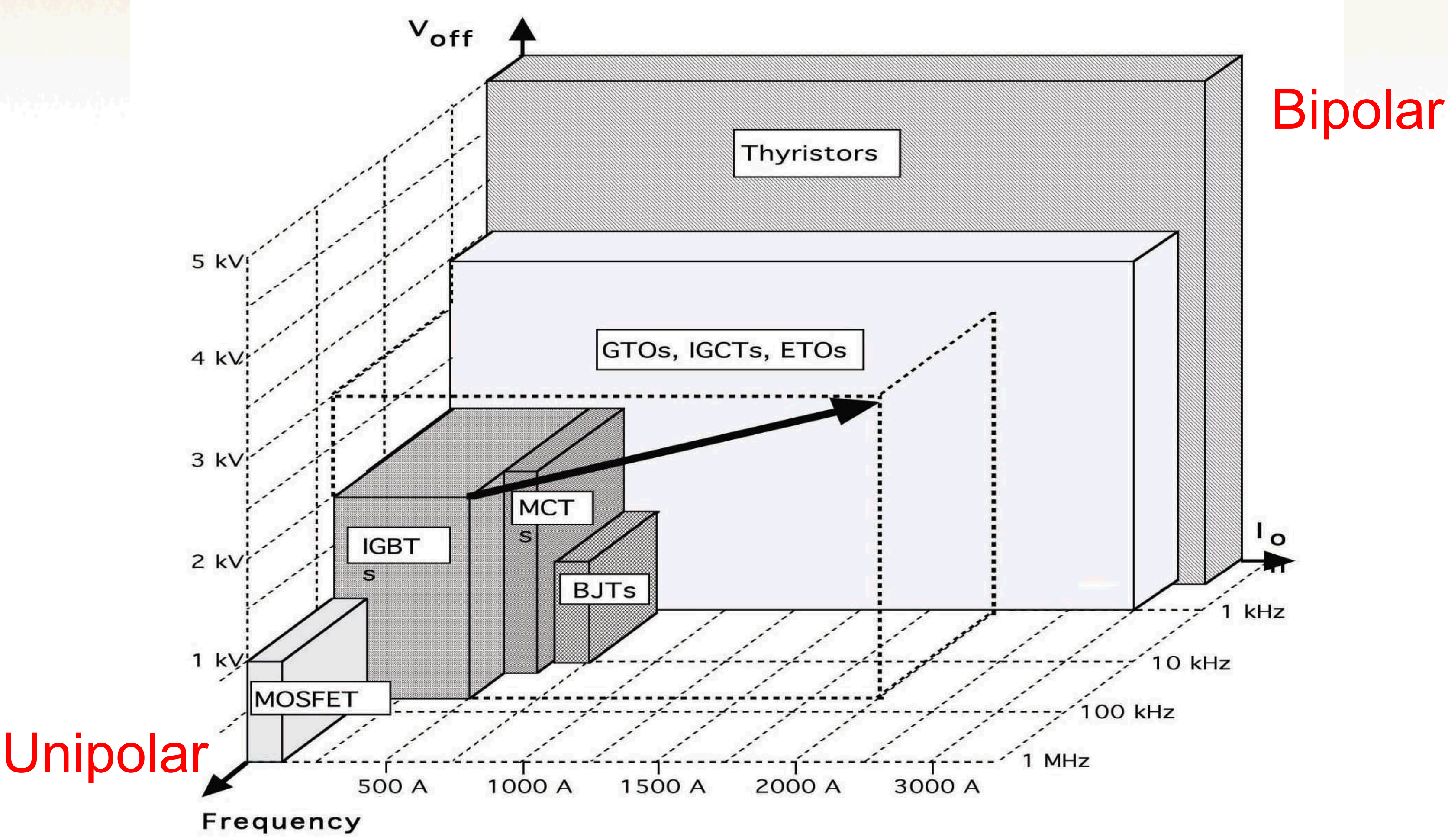
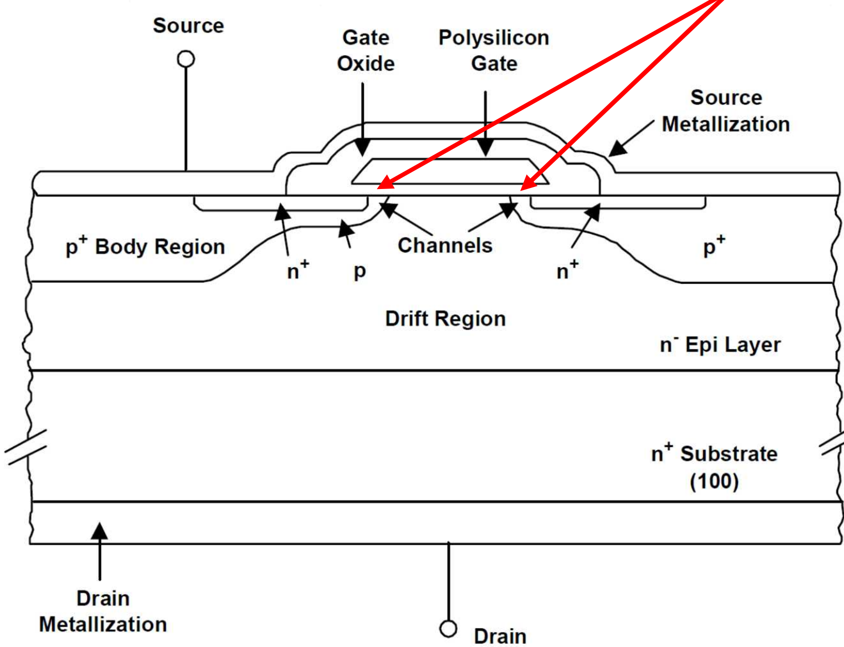
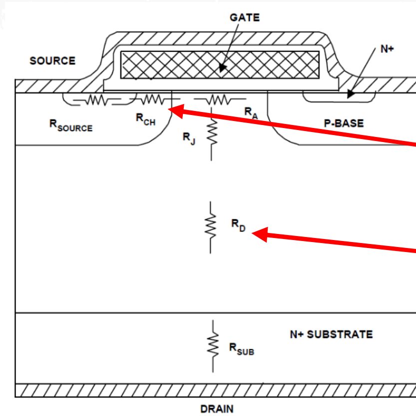


Figure from Mohan et al., “Power electronics: Converters, Applications, and Design” (Wiley, 2003).

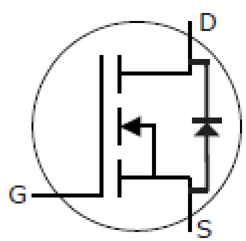
SiC Power D-MOSFET

Critical gate oxide interfacial region





Channel resistance can dominate drift region resistance



Charge injection due to small band offset at SiO_2/SiC interface enhances V_T shift

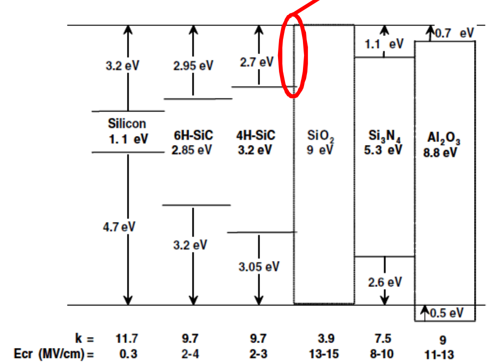


Fig. 1. Dielectric constants, and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offests of these are also shown with respect to SiO_2.

R. Singh, Microelectronics Reliability, v. 46, p. 713 (2006).

Figures from International Rectifier "Power MOSFET Basics" pamphlet

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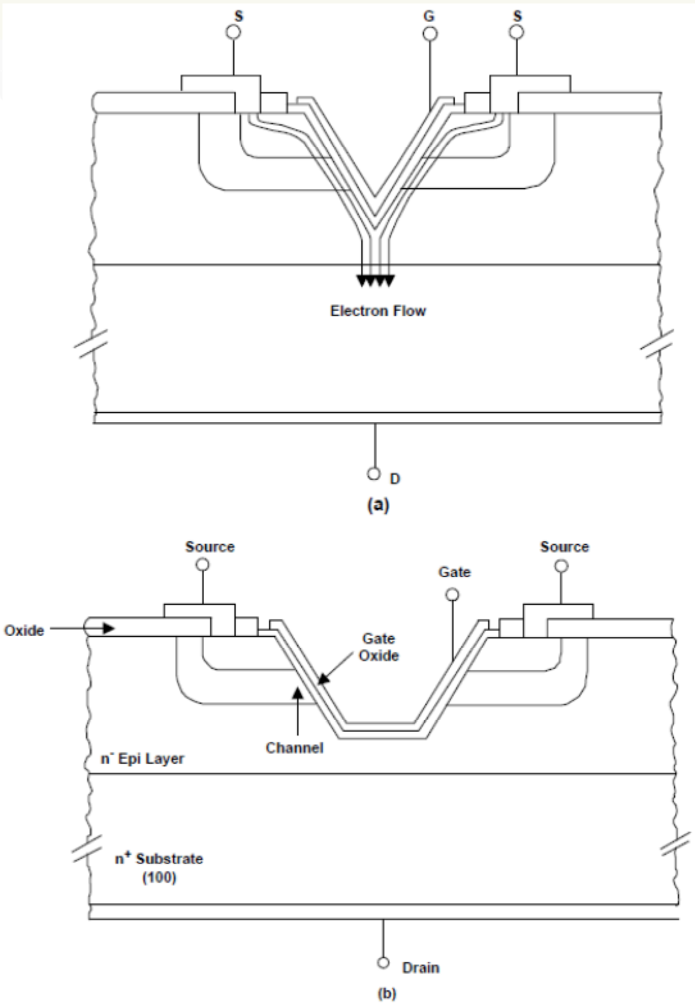
SiC V- and U-MOSFETs



- No double implant
- Channel forms along different crystal plane (generally higher D_{IT} and lower μ)
- Potentially high electric fields at bottom corners
- Earliest SiC power MOSFETs were of this type (or with vertical sidewalls)

Figures from International Rectifier "Power MOSFET Basics" pamphlet

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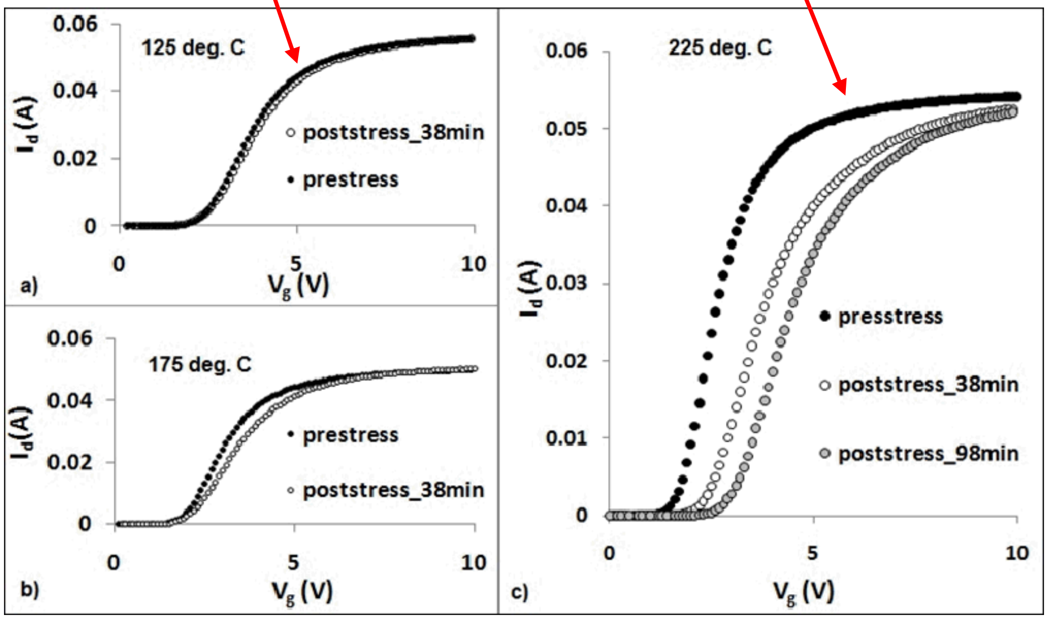
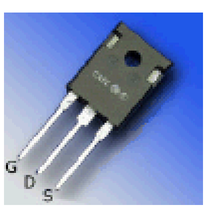
SiC MOSFET Gate Voltage Stress at High T

Minimal degradation at rated temp.

Severe degradation at high temp.

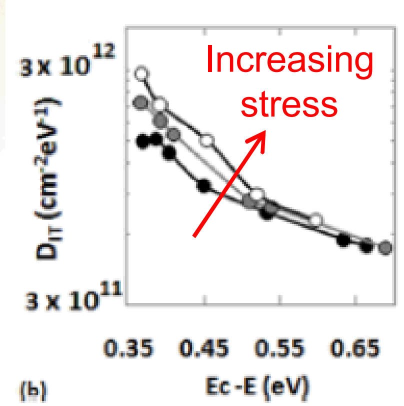


Stress: V_{GS} = +20 V, V_{DS} = 0.1 V

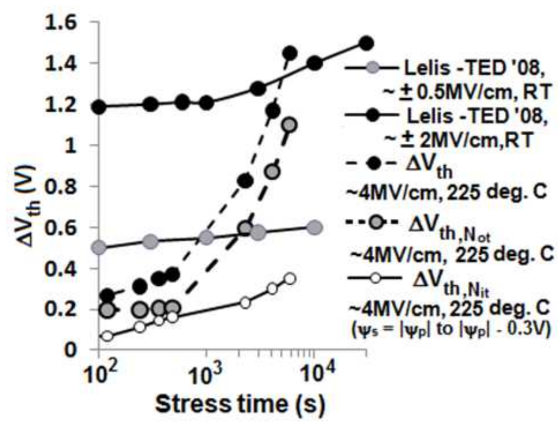


TO-247-3

Commercial 1200 V SiC MOSFET



Interface state density



Evolution of interface and bulk trapping components vs. time

S. DasGupta et al., *Applied Physics Letters* **99**, 023503 (2011)

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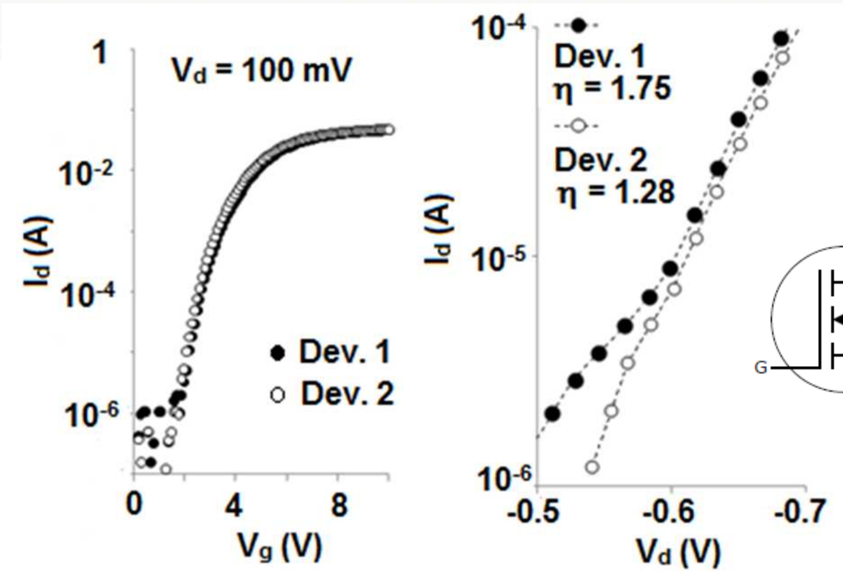
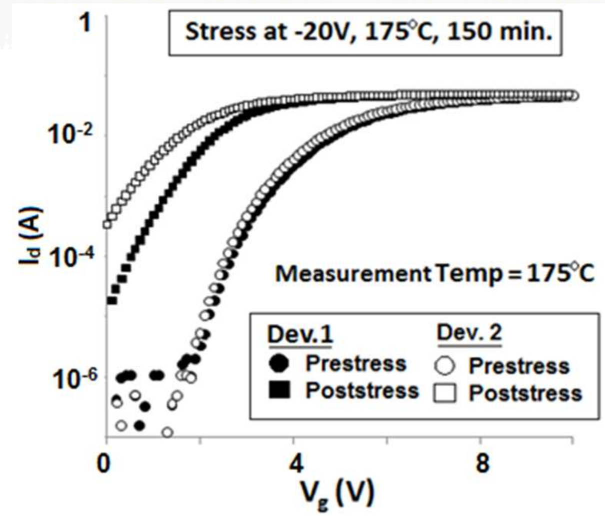
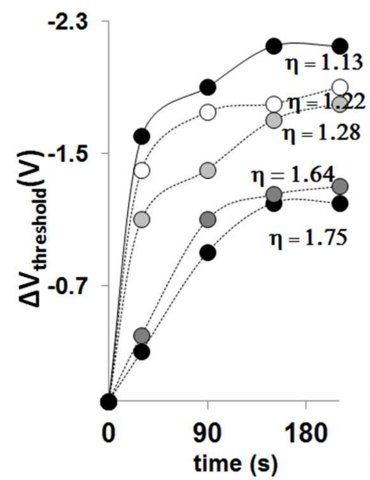
Integrated Free-Wheeling Diode Characteristics and Hole Trapping







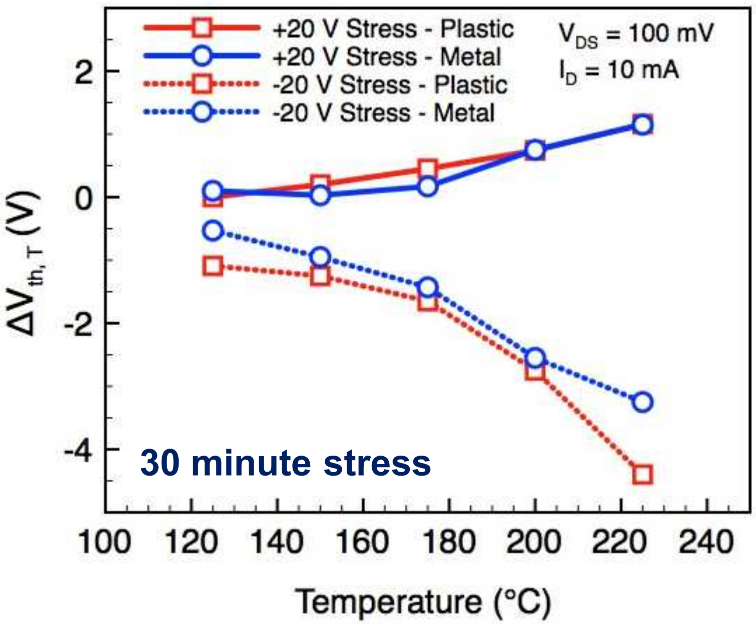
SiC MOSFETs with nearly identical I_D-V_{GS} curves show differences in free-wheeling diode ideality factor; higher η devices show more hole trapping for given stress condition

S. DasGupta et al., *Proceedings of the 50th IRPS*, 3D.3 (2012)

SiC Power MOSFET Threshold Voltage Instability

Plastic

Metal



Threshold voltage shift is independent of packaging type

- Shift in threshold voltage ΔV_T (likely due to charge trapping in the gate oxide) will change R_{ON} and thus the ON-state conduction power loss

- ΔV_T is a function of time t, gate voltage V_G, and temperature T

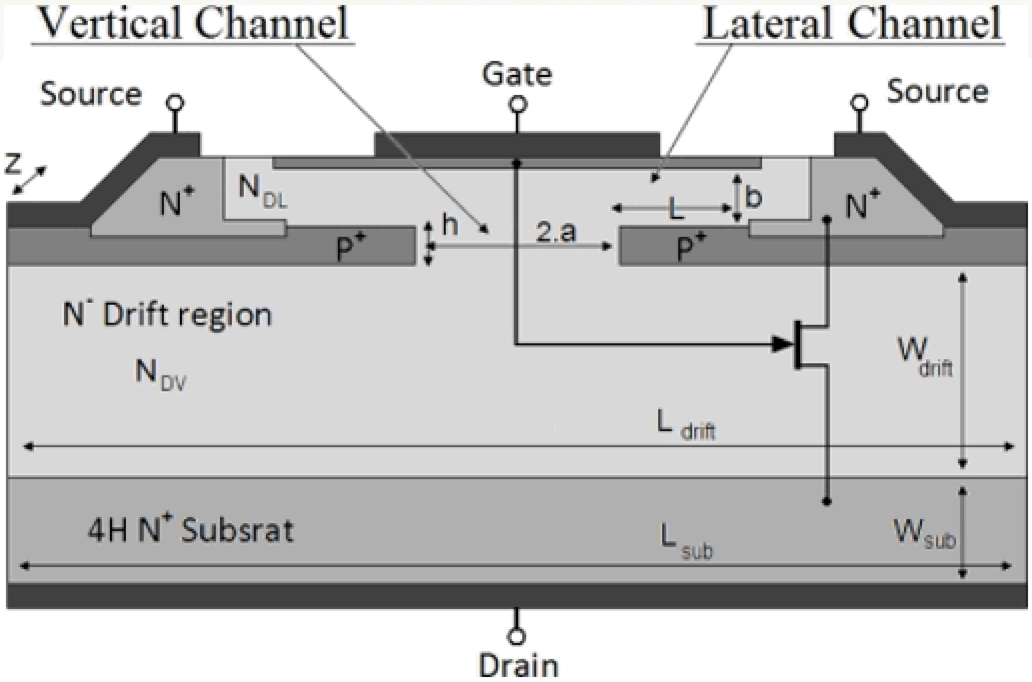
- Assume a power-law dependence on t and V_G, and an Arrhenius dependence on T

- **For *positive* V_G:**
  $\Delta V_T = 8.5\times10^{-3} t^{0.40} V_G^{3.8} \exp(-0.34/kT)$

- **For *negative* V_G:**
  $\Delta V_T = -1.4\times10^{2} t^{0.42} |V_G|^{0.79} \exp(-0.33/kT)$

R. Kaplar et al., accepted to *IMAPS International Conference on High Temperature Electronics Network* (Oxford, UK, July 2013).

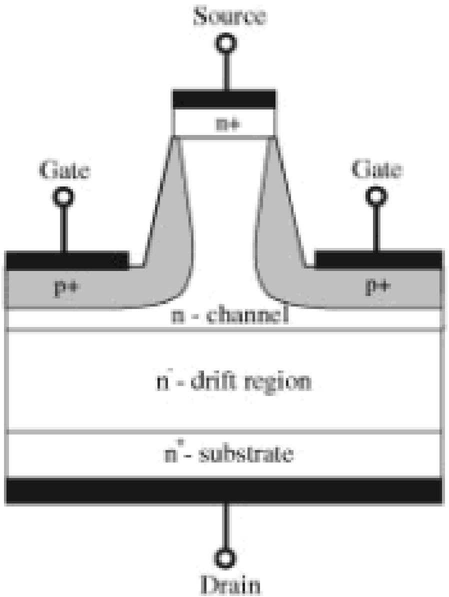
SiC Junction FET



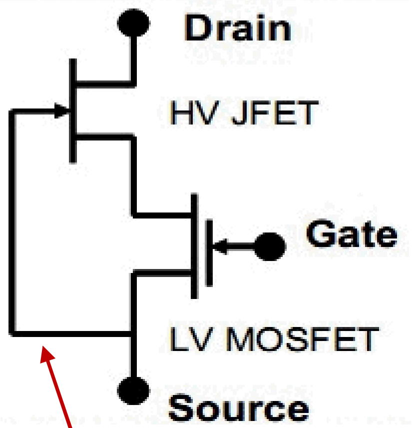
- No gate oxide, so fewer high-temperature reliability concerns
- MOST JFETs are normally-on, which is undesirable for circuits
- Normally-off JFETs suffer from high gate current (fwd. pn junction)

Google images

Cascode Configuration for Normally-Off Operation



High-voltage, normally-on JFET

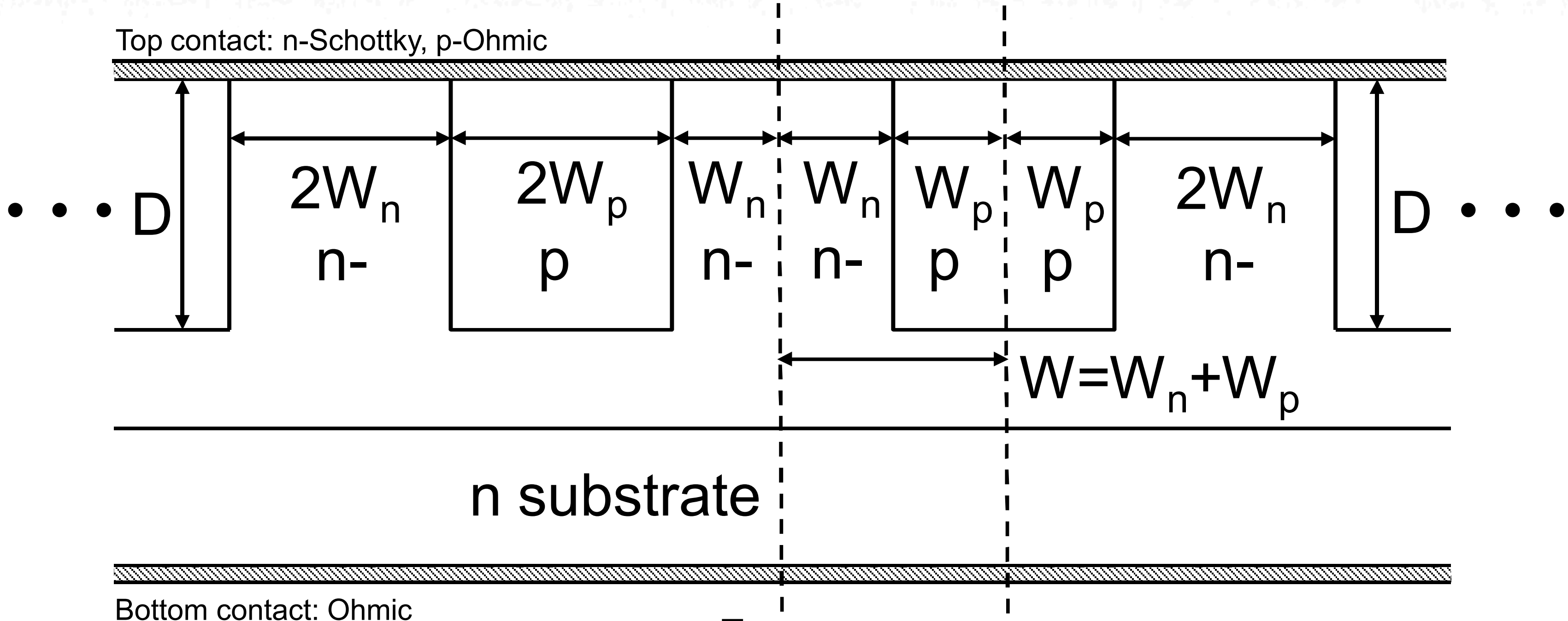


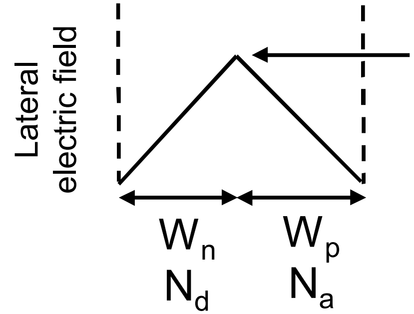
Gate voltage for the HV normally-on device equals negative of the drain voltage of the LV normally-off device; **combination acts as a normally-off HV switch**

Google images

Charge Coupled “Superjunction” for Improved R_{ON} vs. V_{BD}

Vertical dashed lines indicate boundaries of one “cell”

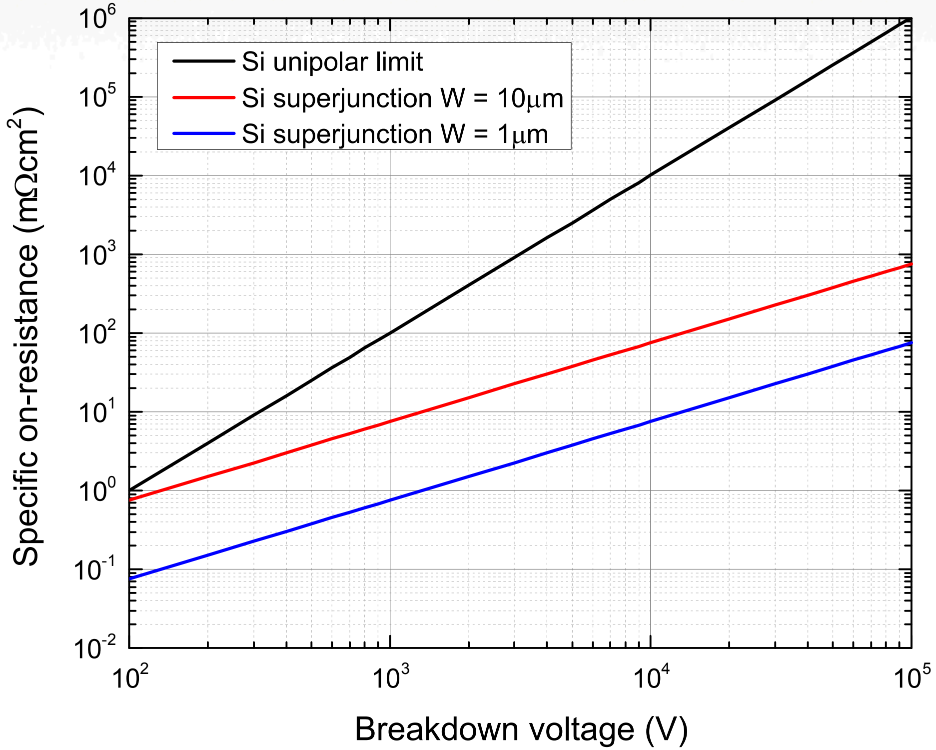




Optimal design dictates that n- and p-regions are both (just) fully depleted (lateral depletion) when $E = E_C$ at the pn junction

Gauss’ law:
$\varepsilon E_C = qN_dW_n = qN_aW_p$

Superjunction can Surpass Unipolar "Limit"



$R_{sp,on} = WV_b/m_n\varepsilon E_C^2$

Note that $R_{sp,on}$ is *linear* in V_B and *quadratic* in E_C

By designing the device appropriately (small W), it is possible to get lower $R_{on,sp}$ for a given breakdown voltage (i.e. to surpass the unipolar "limit")

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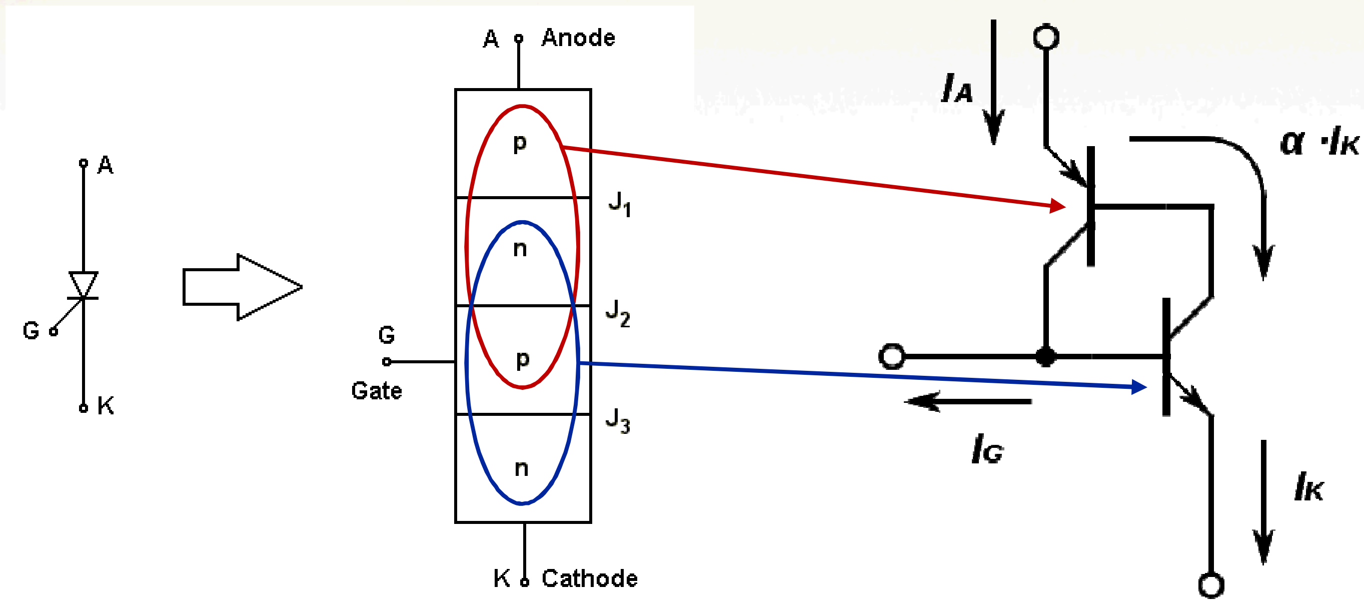
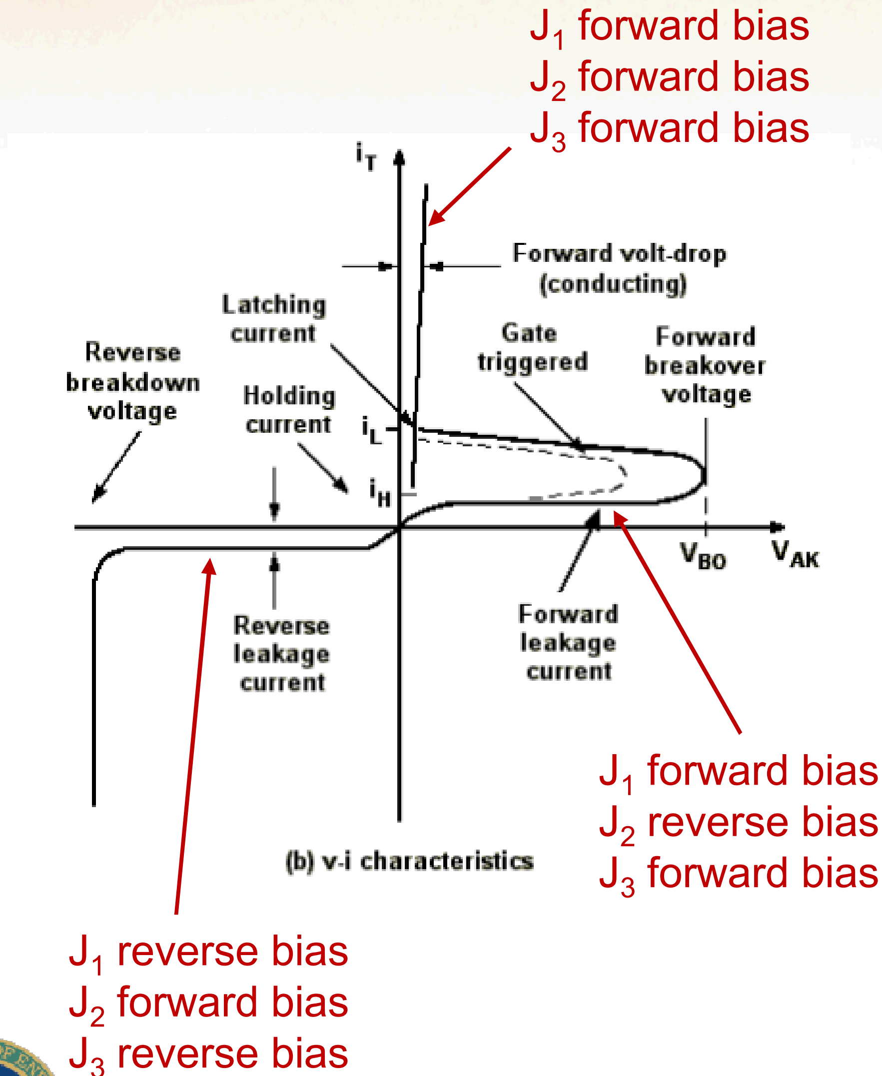
Bipolar Device: Thyristor

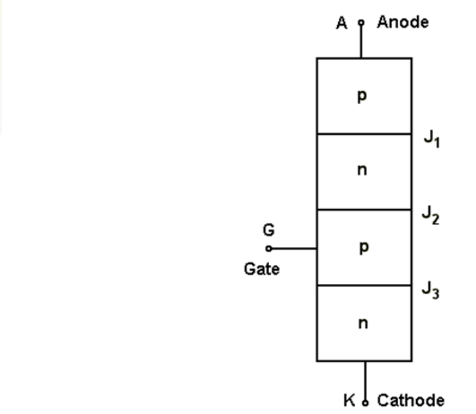


- Three-junction device
- Can be modeled as two coupled bipolar transistors
- Turns on when sum of collector-to-emitter gains approaches 1

Google images

Thyristor IV Characteristics





- Gate is used to inject carriers to switch from forward blocking to reverse blocking
- Difficult to turn off (quasi-controlled "gate turn-off" devices do exist)
- Slow switching due to minority-carrier recombination

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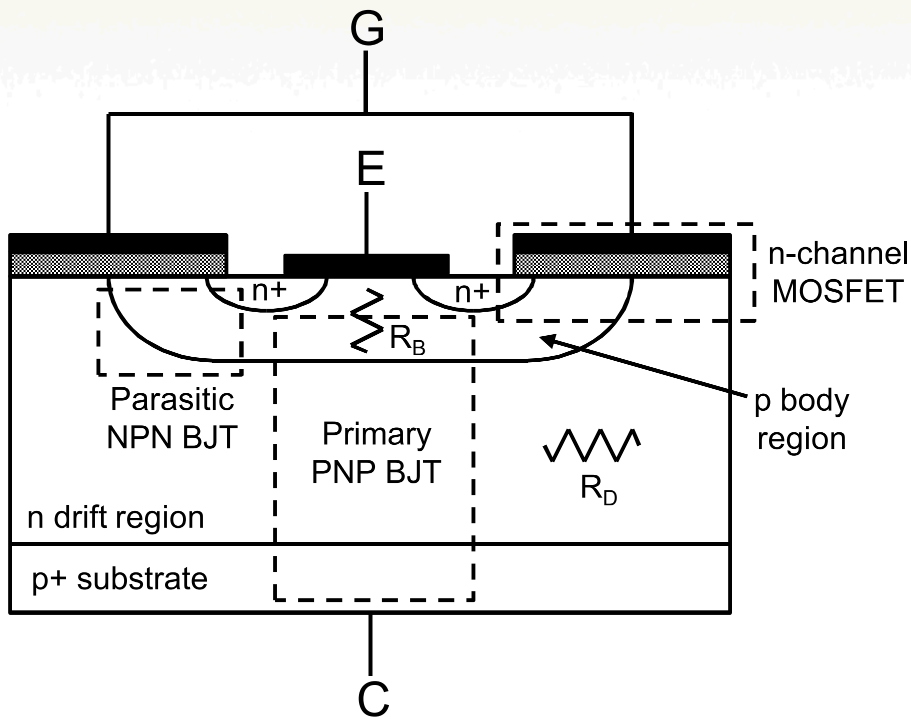
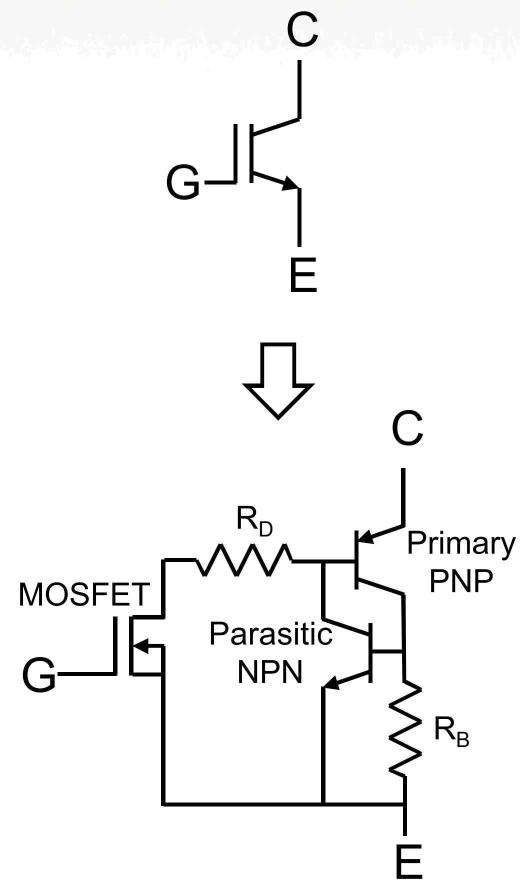
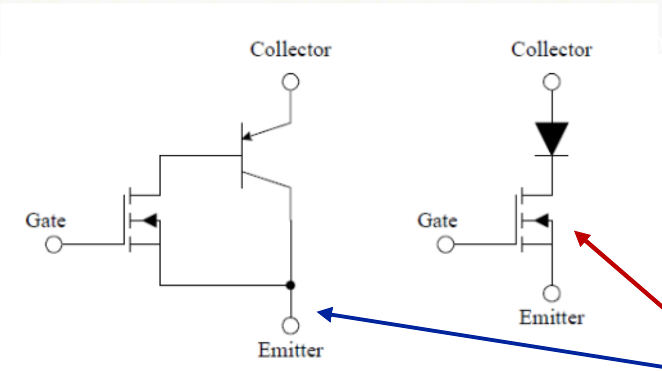
Insulated-Gate Bipolar Transistor (IGBT)

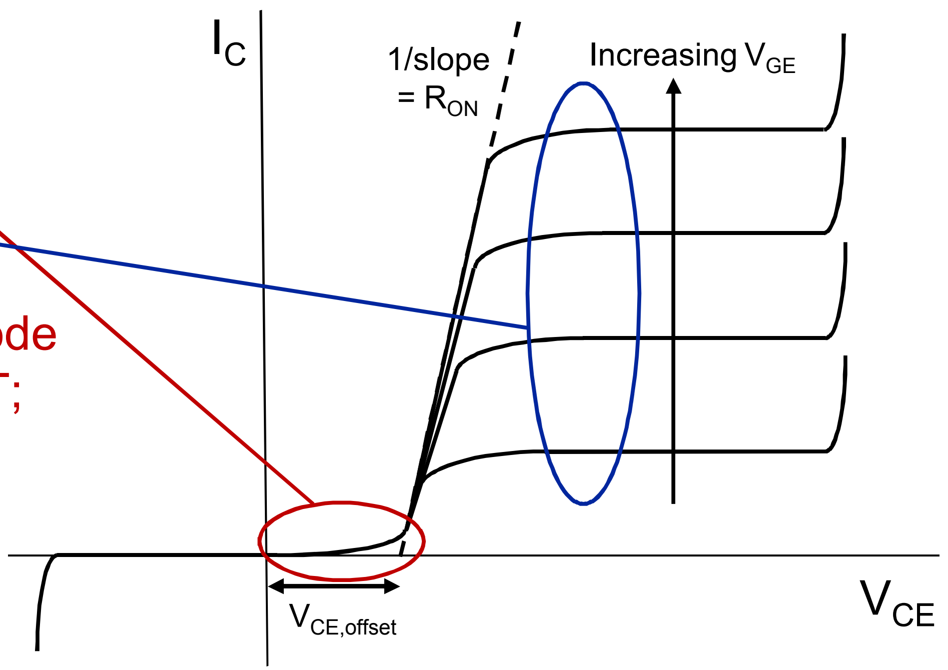




- Hybrid MOS-bipolar device
- Drain current of the MOSFET is the base current of the BJT
- High voltage and current capability with advantage of gate control
- Relatively slow switching

IGBT IV Curves and Equivalent Circuits

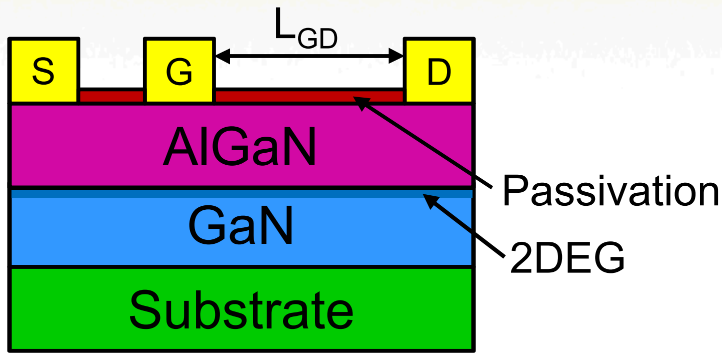


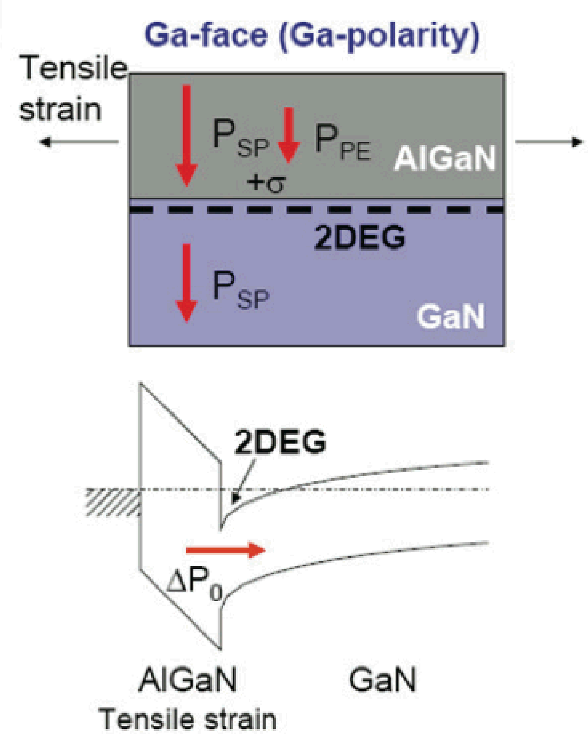


- Low V_{CE}: MOSFET in series with diode
- Higher V_{CE}: MOSFET-controlled BJT; $I_{BJT} = (1+\beta_{BJT})I_{MOSFET}$
- Diode voltage offset is undesirable due to increased power dissipation
- Parasitic thyristor structure can cause latch-up if not properly accounted for

Advanced Power Technology “IGBT Tutorial”

AlGaN/GaN High-Electron Mobility Transistor (HEMT)

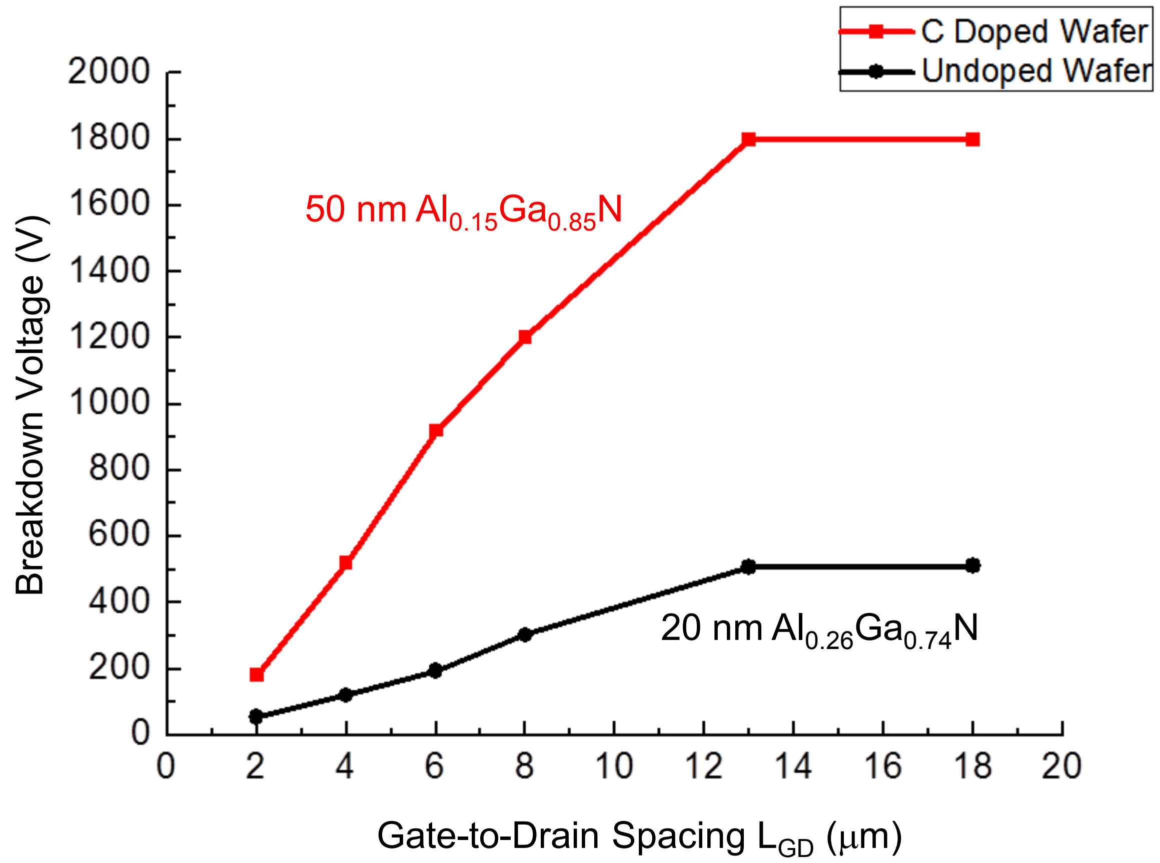




- Power switching HEMT has evolved from AlGaN/GaN microwave HEMT
- Polarization induces high-μ channel without doping (i.e. no scattering)
- Normally-on device (more complex normally-off designs are possible)
- High field is dropped laterally; field is very non-uniform in channel (peaked near gate edge) and field plates are employed to mitigate this problem

Google images

GaN Initiative for Grid Applications (collaboration with T. Palacios at MIT)



Goal is a Grid-level lateral HEMT

L_G = 2 μm, L_{GS} = 1.5 μm, L_{GD} = 1.5 to 40 μm

All devices grown on (111) Si by MOCVD

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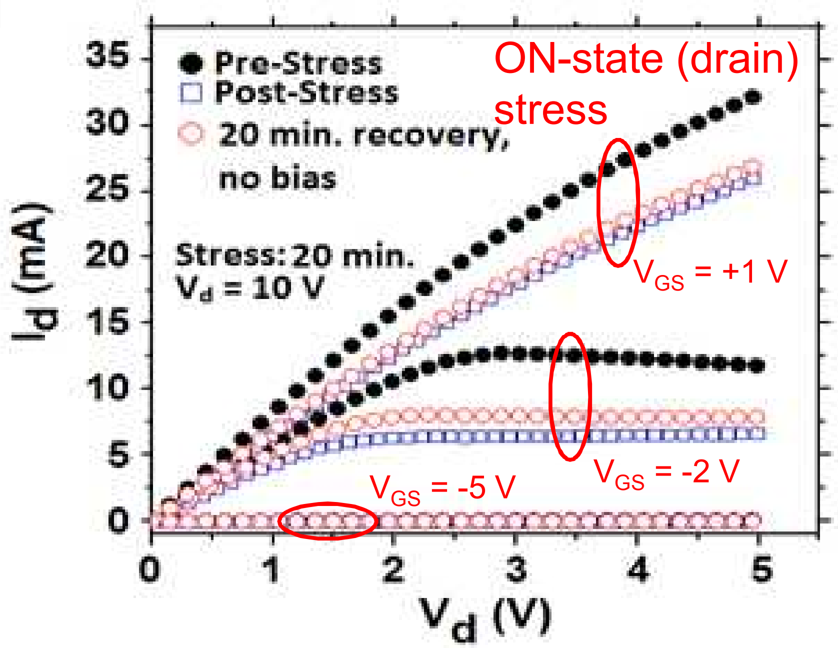
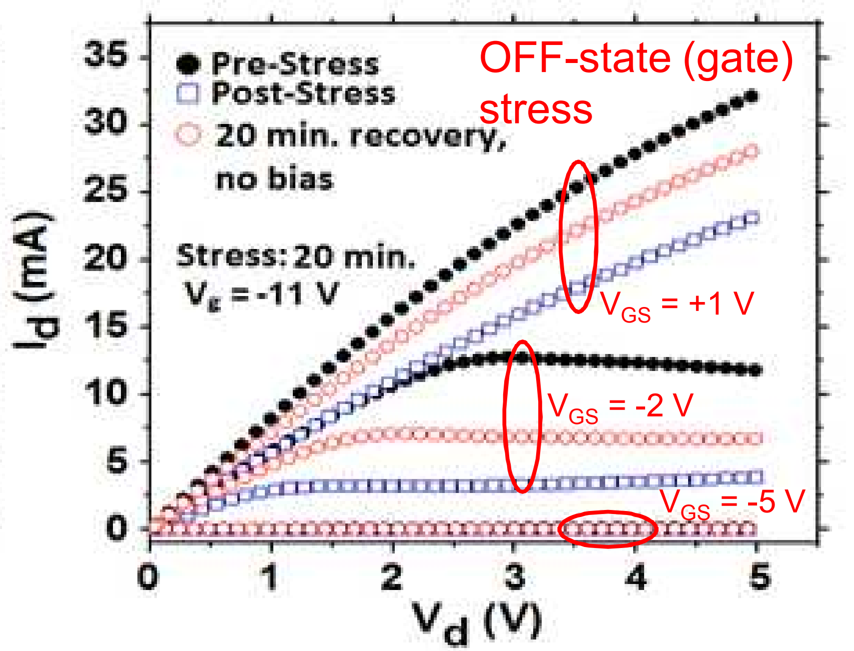
ON-State vs. OFF-State Stress

Passivated $Al_{0.15}Ga_{0.85}N/GaN$ sample



Stress: V_{DS} = 10 V, V_{GS} = 0 V (ON)



Stress: V_{DS} = 0 V, V_{GS} = -11 V (OFF)

ON-state stress (drain bias) results in much slower recovery than OFF-state stress (gate bias)

S. DasGupta et al., *Transactions on Electron Devices* **59** **(8)**, 2115 (2012)

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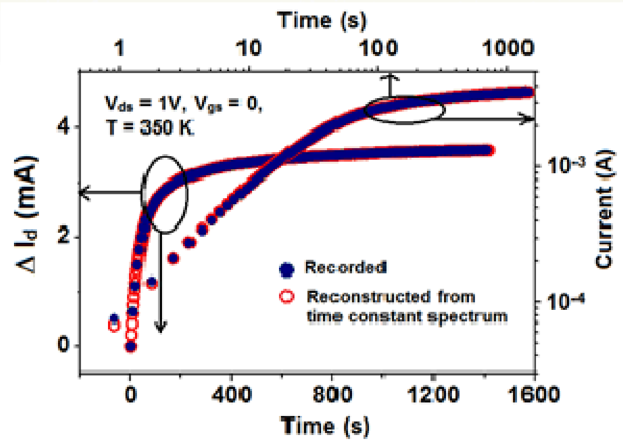
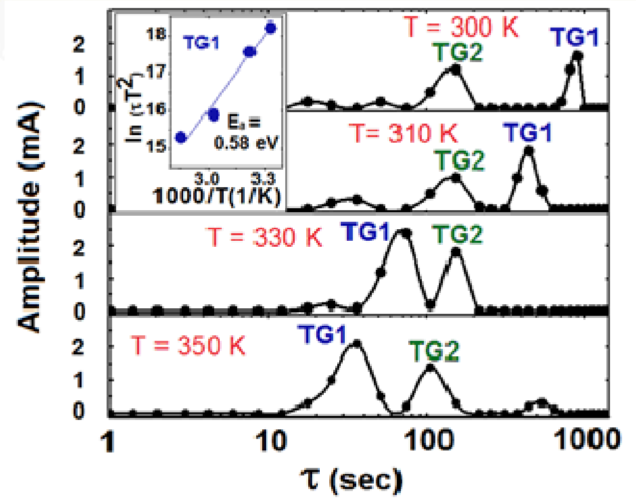
Recovery Current Transient Analysis Following Gate Stress



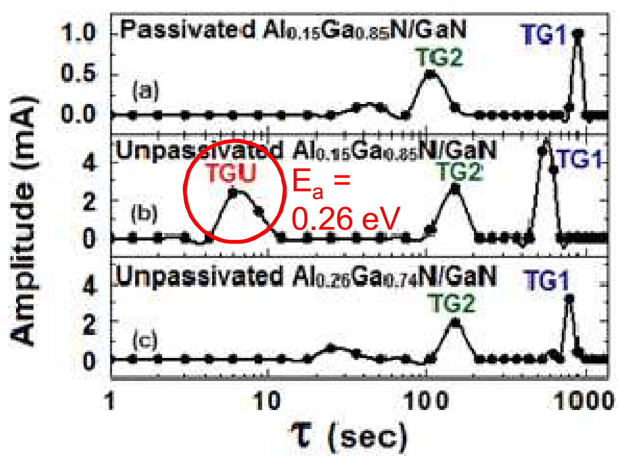
Fitting of recovery transient amplitudes A_i with fixed τ_i:

$$\Delta I_d = \sum_i A_i \left[1 - exp\left(-\frac{t}{\tau_i}\right)\right]$$

Peaks in time constant spectra are indicative of different traps in different samples



Passivated $Al_{0.26}Ga_{0.74}N/GaN$ temperature dependence



Comparison of other samples

S. DasGupta et al., *Transactions on Electron Devices* **59 (8)**, 2115 (2012)

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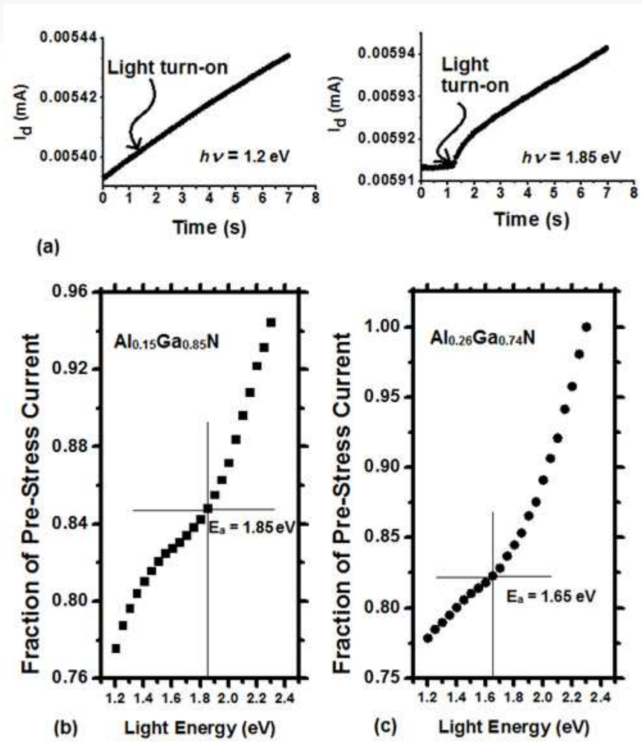
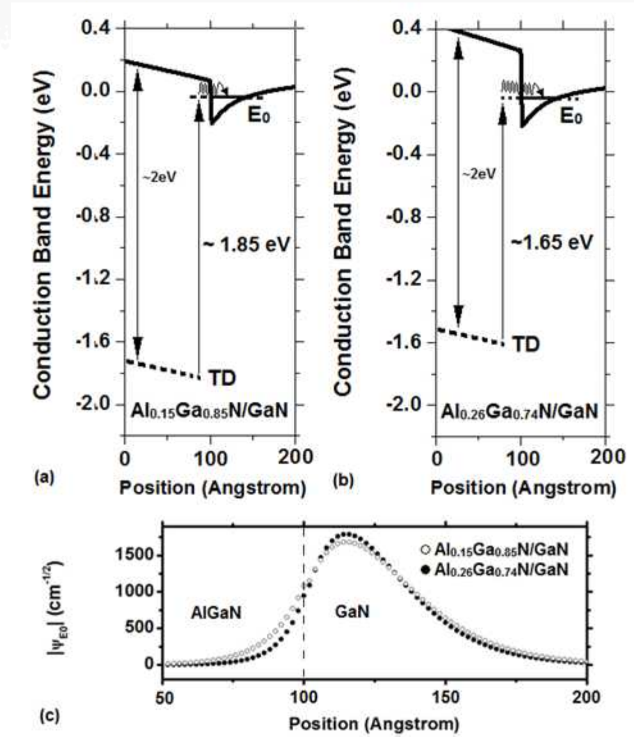
Optical Recovery of Drain-Stress-Induced Trap

15% Al

7 s exposure at each λ

V_{DS} = 1 V
V_{GS} = 0 V

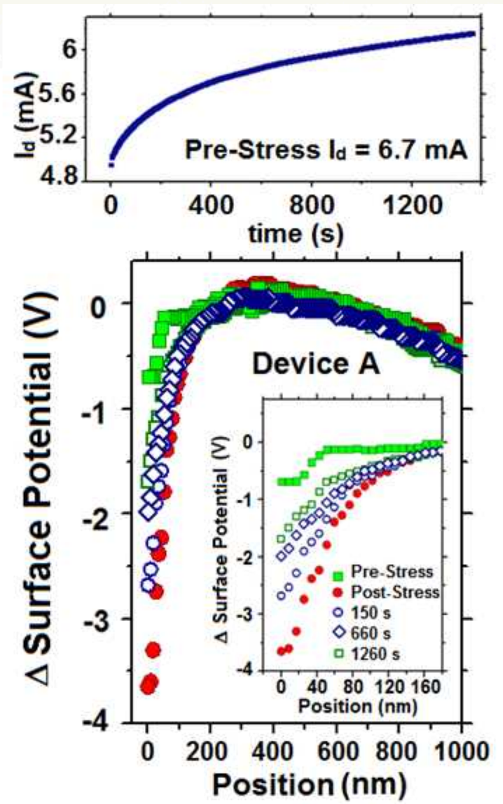




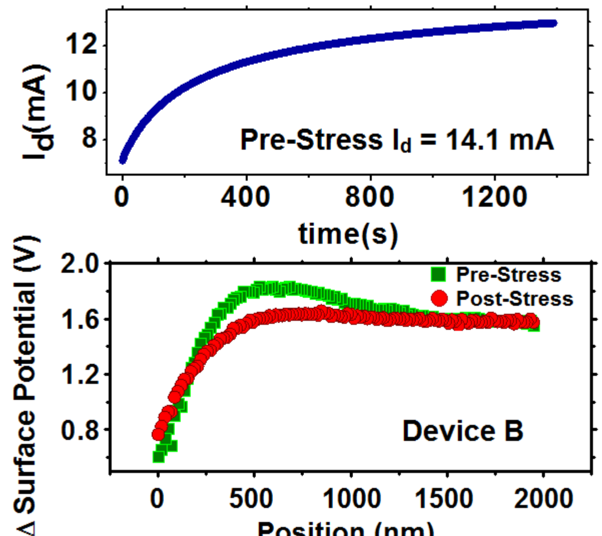
Inflection point (d^2I/dE^2) depends on barrier composition; consistent with transition from a deep level E_C – 2.0 eV in the AlGaN to the 2DEG

S. DasGupta et al., *Transactions on Electron Devices* **59 (8)**, 2115 (2012)

Correlated Surface Potential and Drain Current Following Gate Stress



Device type	AlGaN Barrier	GaN Buffer	Passivation
A (1)	50 nm $Al_{0.15}Ga_{0.85}N$	Carbon doped	ALD deposited $Al_2O_3/SiO_2/Al_2O_3$
B (4)	20 nm $Al_{0.26}Ga_{0.74}N$	Undoped	None



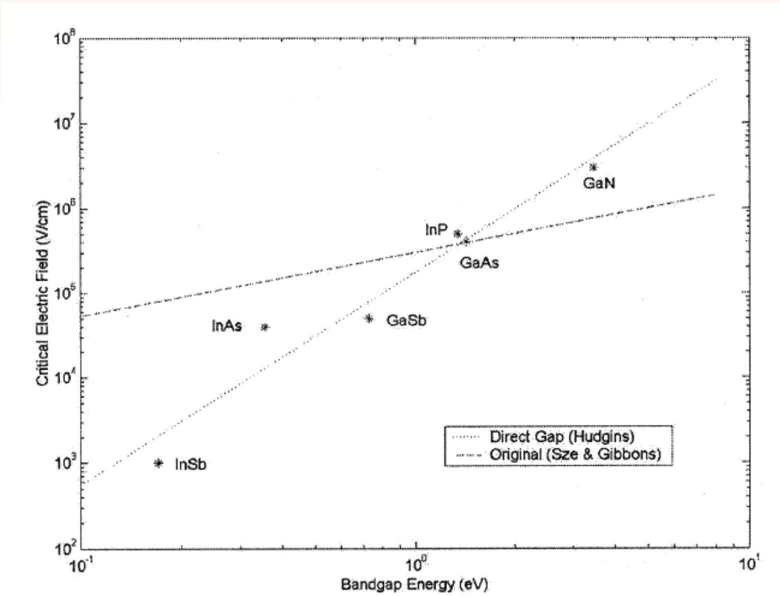
Device A: *Large* change in surface potential near the gate edge

Device B: *Negligible* change in surface potential throughout the drain extension

Results inconsistent with expectations based on buffer doping and surface passivation

S. DasGupta et al., *Applied Physics Letters* **101**, 243506 (2012)

Ultra-Wide-Bandgap Materials for Orders-of-Magnitude Performance Improvement



Hudgins et al., TED **18 (3)**, 907 (2003).

Postulated dependence of $\mathcal{E}_C$ on E_G for direct gap materials:

$$\mathcal{E}_C \sim E_G^{2.5}$$

$E_G(\mathrm{AlN})/E_G(\mathrm{GaN}) = 6.2/3.4 = 1.8$

$\mathcal{E}_C(\mathrm{AlN})/\mathcal{E}_C(\mathrm{GaN}) = 1.8^{2.5} = 4.3$

Remember unipolar FOM:

$$\mathrm{FOM} = V_B^2/R_{on,sp} = \varepsilon\mu\mathcal{E}_C^3/4$$

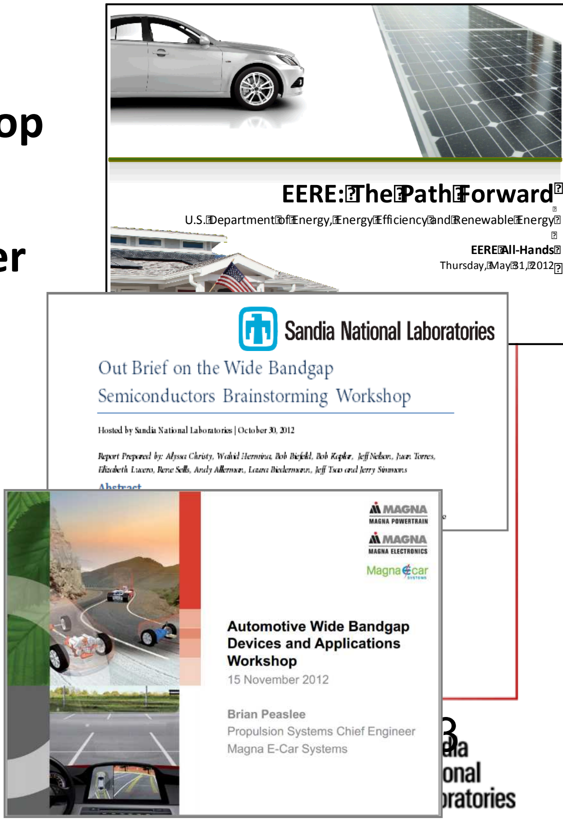
$\mathrm{FOM(AlN)/FOM(GaN)} = 4.3^3 \approx 80$!

This assumes equal electron mobility, which is probably not true; *nevertheless, increase in E_C (cubic dependence) likely outweighs decrease in m (linear dependence)*

Material growth issues are of paramount importance, similar to GaN but less mature

Increasing DOE Interest in WBGs

- **2010 ARPA-E ADEPT Program:** "Agile Delivery of Electric Power Technology," $34.5M
- **Feb 1, 2012:** Chu's Materials for Energy Applications workshop, Berkeley – *WBGs one of four major topics in Chu's talk*
- **May 31, 2012:** EERE—New undersecretary David Danielson announces WBG's as one of his four major initiatives
- **June 26, 2012:** **SNL Workshop on Power Electronics**
- **July 25, 2012:** **WBG Semiconductors for Clean Energy Workshop** (Dave Danielson, DOE/AMO Invitation-only)
- **Sept. 11 and Oct. 23, 2012:** **Robust WBG Semiconductor Power Electronics Workshops** (ANL and the University of Maryland)
- **October 30, 2012:** **SNL WBG Semiconductors Brainstorming Workshop** - *Outlined a Center concept for review from participants*
- **Nov. 15-16, 2012:** **Automotive Wide Bandgap Devices and Applications** (Oak Ridge National Laboratory)
  - *Wide Bandgap devices for the next generation of electric drive systems*



The Need for a National WBG Center

A National Center for Innovation in Wide-Bandgap Semiconductors would

- Spur innovation and enhance competitiveness of U.S. industry
- Improve energy efficiency and incorporation of renewable energy sources
- Enable intelligent, resilient energy grids

This center would build on Sandia's established excellence in

- III-N WBGs for solid-state lighting
- Fabrication, testing, and failure analysis at MESA and CINT
- PV reliability at DETL and microgrid GC LDRD
- Existing power electronics work (energy storage program)

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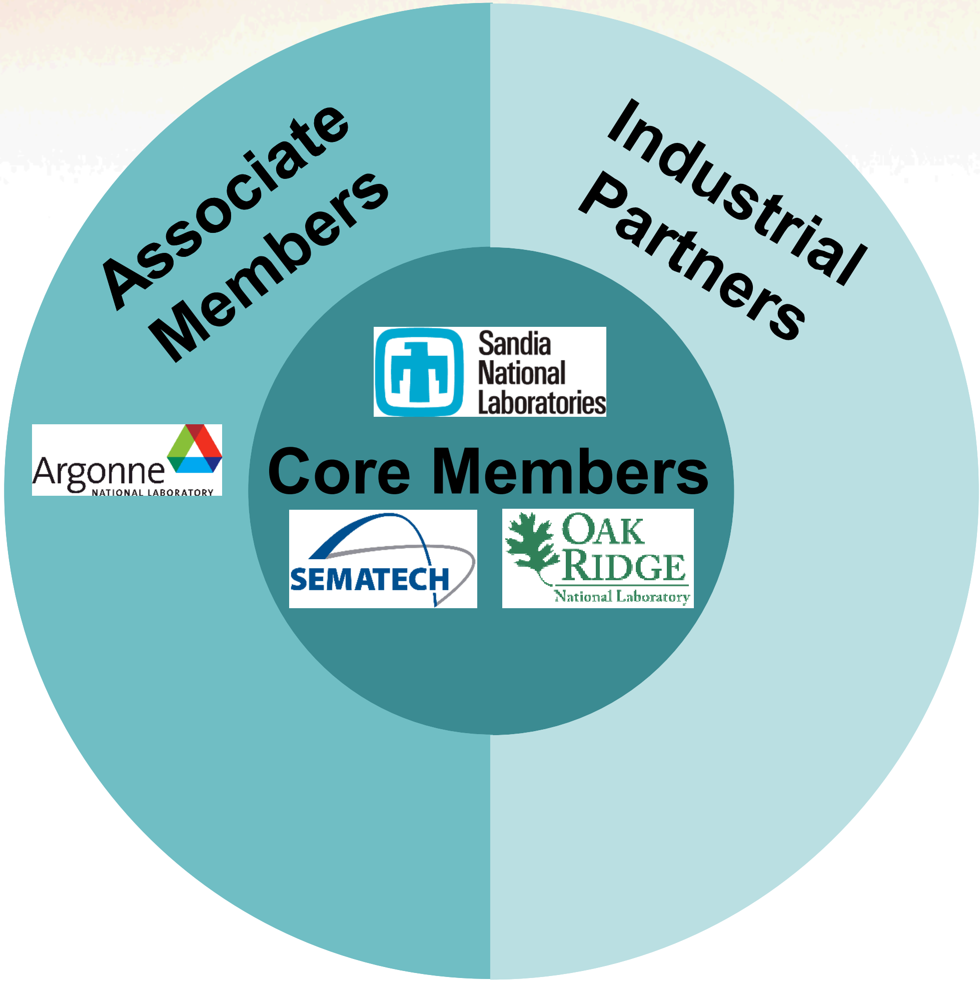
Proposed Center Structure



Core Members (3):
Collectively possess a suite of capabilities unique in its degree of vertical integration and its ability to support collaboration at any level of the technology innovation chain.

Associate Members (~5-10):
Non-profits who will contribute their complimentary capabilities to the Center.

Industrial Partners (~15-20):

- **Industrial Collaborators** drive the Center's response to industrial needs
- **Industrial Users** utilize Center resources to enhance US industrial competitiveness

National Center Technical Scope

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Summary

- WBG power devices promise to increase efficiency and reduce system complexity, but materials and reliability issues have hampered their adoption
- Sandia possesses a full range of WBG capabilities spanning from fundamental materials science to grid-level power systems, and is well-positioned to address these outstanding problems
- WBG power device work to date has been funded by DOE OE and has focused on SiC and GaN power device reliability; parallel work funded by DOE EERE has examined PV inverter reliability
- An opportunity exists to establish a DOE EERE-sponsored "national center" of excellence, in conjunction with other partners (Oak Ridge, Sematech, Argonne, etc.)

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