SAND2013-3932P

Scalable Transistor-Level Circuit Simulation for Radiation Effects Prediction

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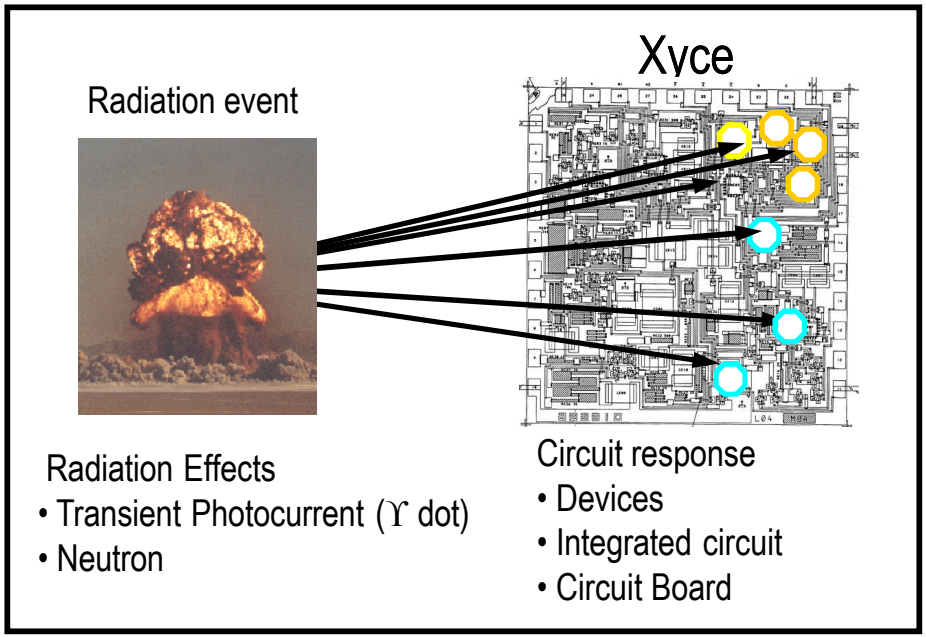
Xyce Motivation:
Support Radiation Effects Prediction

Sandia ensures electrical systems survivability in hostile environments

- Requires electrical modeling:
  - Prompt radiation performance
  - Extended lifecycle (20 to 40 years)

- Requires predictive, physics based models at:
  - Compact model level
    - 1111, 1344, 1355, 1356, 1748
  - Device model level
    - 1111, 1355, 1742, 1748

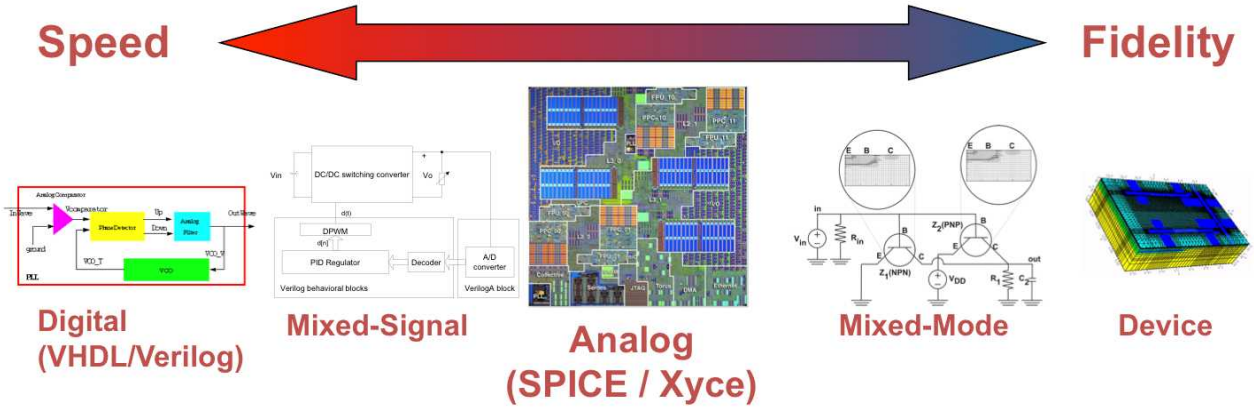


✓ **Advanced mathematical algorithms**

✓ **Massively parallel applications**

Why Transistor-Level Circuit Simulation?

- Essential simulation approach used to verify electrical designs
  - SPICE is the defacto industry standard (PSpice, HSPICE, etc.)
  - Xyce supports NW-specific device development
- Provides tradeoff between fidelity and speed/problem size
  - Xyce enables full system parallel simulation for circuits that are larger than commercial simulators can handle

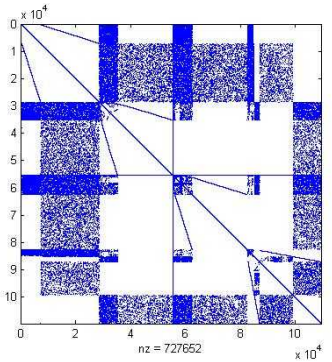


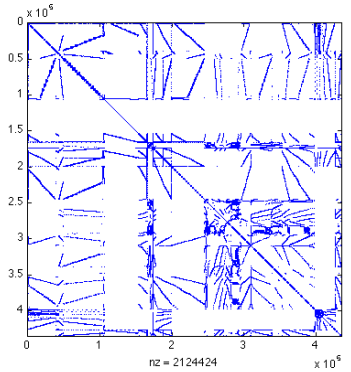
Simulation Challenges

Analog simulation models network(s) of devices coupled via Kirchoff's current and voltage laws

$$f(x(t)) + \frac{dq(x(t))}{dt} = b(t)$$

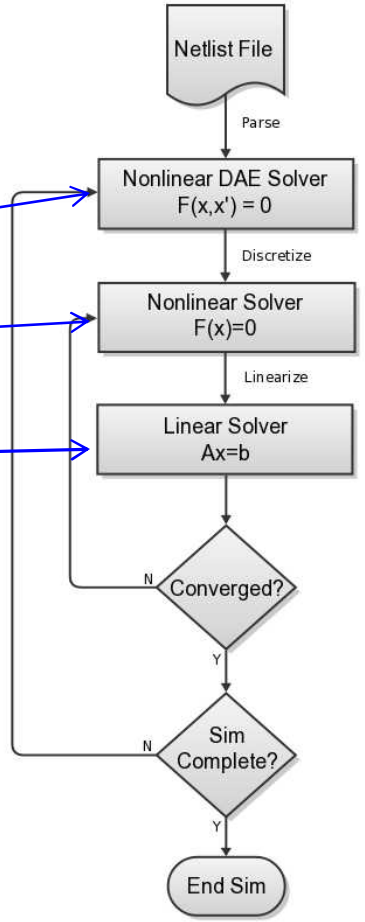
- Network Connectivity
  - Hierarchical structure rather than spatial topology
  - Densely connected nodes: O(n)
- Badly Scaled DAEs
  - Compact models designed by engineers, not numerical analysts!
  - Steady-state (DCOP) matrices are often ill-conditioned
- Non-Symmetric Matrices
- Load Balancing vs. Matrix Partitioning
  - Balancing cost of loading Jacobian values unrelated to matrix partitioning for solves
- Strong scaling and robustness is the key challenge!





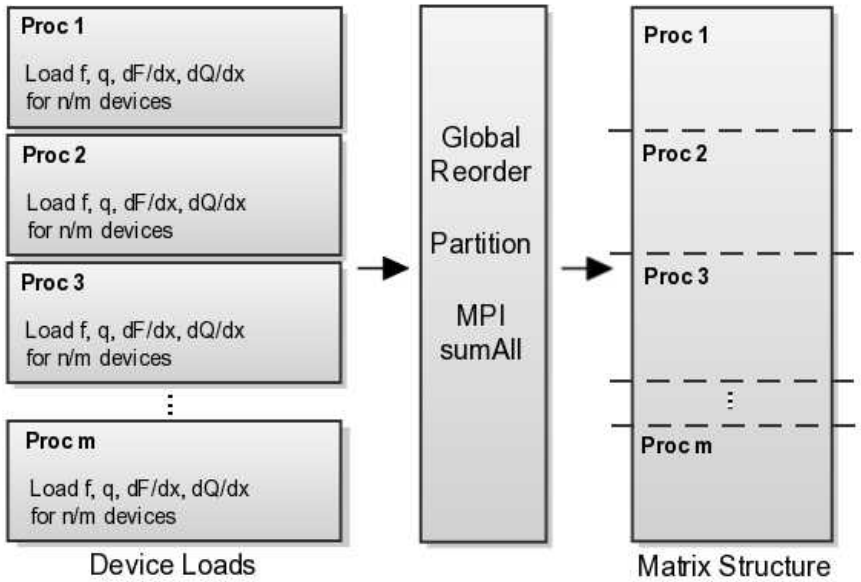
Transistor-Level Simulation Flow

- Circuit simulators solve a system of nonlinear DAEs
  - How this is done depends on analysis type
  - Implicit integration methods
  - Newton's method
  - Sparse matrix techniques
- Transient simulation has phases
  - Compute starting point (DCOP)
  - Start analysis (transient)
  - Sparse linear algebra / solvers
    - •Linchpin of scalable and robust performance



Balancing Multiple Solver Objectives

- Multiple objectives for load balancing the solver loop
  - Device Loads : The partitioning of devices over processes will impact device evaluation and matrix loads
  - Matrix Structure : Graph structure is static throughout analysis, repartitioning matrix necessary for generating effective preconditioners
- Device Loads
  - Each device type can have a vastly different "cost" for evaluation
  - Memory for each device is considered separate
  - Ghost node distribution can be irregular
- Matrix Structure
  - Use graph structure to determine best preconditioners / solvers

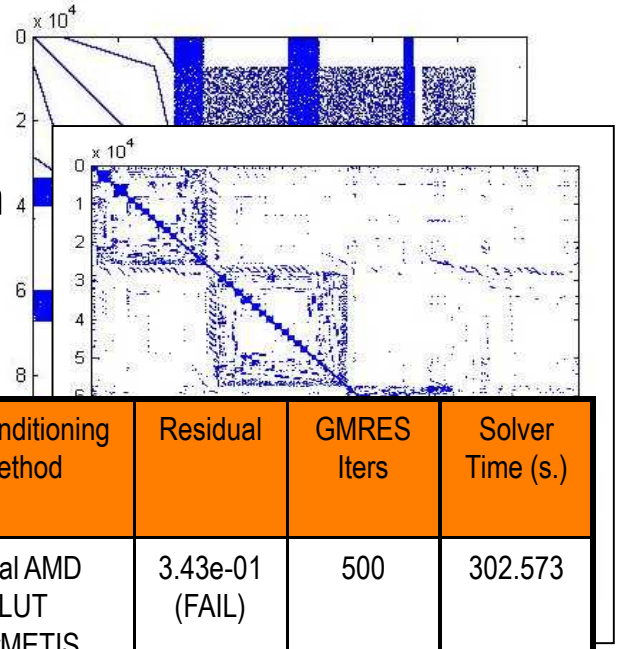


Comparable Parallel Simulation Approaches

- Xyce is a distributed memory, MPI-based analog circuit simulator
  - Hybrid parallelism (MPI+threads) depending on choice of linear solver
- Many commercial simulators have incorporated parallelism
  - Access to multi-processor / multi-core desktops
  - Multithreading key portions
- Multi-Algorithm Parallel Circuit Simulation (MAPS)
  [X. Ye, W. Dong, P. Li, S. Nassif]
  - Multiple numerical integration methods with synchronization
- WavePipe
  [W. Dong, P. Li, X. Ye]
  - Multi-core, shared-memory simulator
  - Emulate hardware pipelining to expedite time integration
- Domain-decomposition Parallel Simulation
  [H. Peng and C.K. Cheng]
  - Divides circuit into linear and non-linear components (subdomains)

History of Linear Solver Scaling

- Initially (circa 1999), Xyce used available PDE-based preconditioning techniques
  - Incomplete LU factorization
  - Limited scaling / robustness
- For small scale circuits, the Dulmage-Mendelsohn permutation (BTF) was leveraged in KLU (2004)
- In 2008, BTF structure was leveraged to create a new preconditioned iterative method
  - Great for CMOS memory circuits
  - Circuits with parasitics are more challenging
- In 2010, initial development of ShyLU, a "hybrid-hybrid" sparse linear solver package
  - Improve robustness



Preconditioning Method	Residual	GMRES Iters	Solver Time (s.)
Local AMD ILUT ParMETIS	3.43e-01 (FAIL)	500	302.573
BTF Block Jacobi Hypergraph	3.47e-10	3	0.139

26x speedup on 16 cores

W. Bomhof and H.A. van der Vorst [NLAA, 2000]
A. Basermann, U. Jaekel, and K. Hachiya [SIAM LA 2003 proc.]

A New Framework for Developing Robust "Hybrid-Hybrid" Linear Solvers

- ShyLU is a sparse linear solver framework, based on Schur complements (*S. Rajamanickam, E. Boman, M. Heroux*):
  - Incorporates both direct and iterative methods
  - Coarse-scale (multi-processor) and fine-scale (multi-threaded) parallelism
  - Can be a subdomain solver / preconditioner or stand-alone linear solver
- This approach solves $Ax = b$ by partitioning it into

$$A = \begin{bmatrix} D & C \\ R & G \end{bmatrix}, x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, b = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix},$$

  where D and G are square, D is non-singular, x and b are conformally partitioned
- The Schur complement is: $S = G - R * D^{-1}C.$

Achieving Scalability and Robustness within Xyce

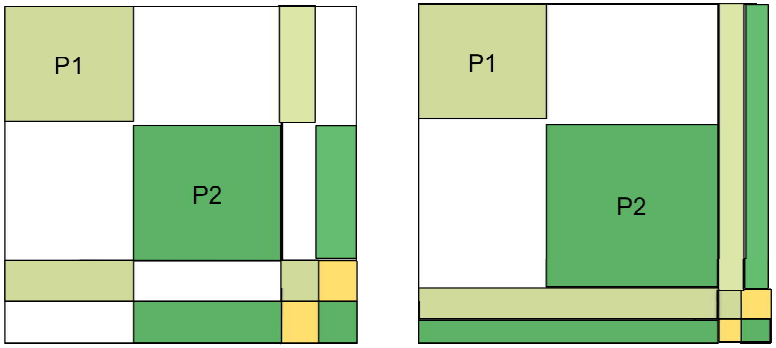
- Solving $Ax = b$ consists of three steps:

1. Solve $Dz = b_1$.
2. Solve $Sx_2 = b_2 - Rz$.
3. Solve $Dx_1 = b_1 - Cx_2$.

D solved exactly using KLU

S solved iteratively via preconditioned GMRES

- ShyLU is used as a stand-alone solver in Xyce
  - Matrices partitioned using hypergraph partitioning (Zoltan)
    - Wide separator – S can be computed locally
    - Narrow separator – S is smaller, but requires communication
  - Preconditioner, S', generated by dropping small entries in S



Xyce Achieves 19x Speedup for Challenging Stockpile Circuit

- Necessary for efficient simulation of a primary logic component for W88-Alt AF&F:
  - 1.6M total devices, ~2M unknowns
  - Xyce w/ KLU solver takes ~ **2 weeks**, w/ ShyLU solver takes ~ **1 day**
  - ShyLU: Optimal # partitions = 64; number of rows in *S* = 1854 (4 MPI procs)

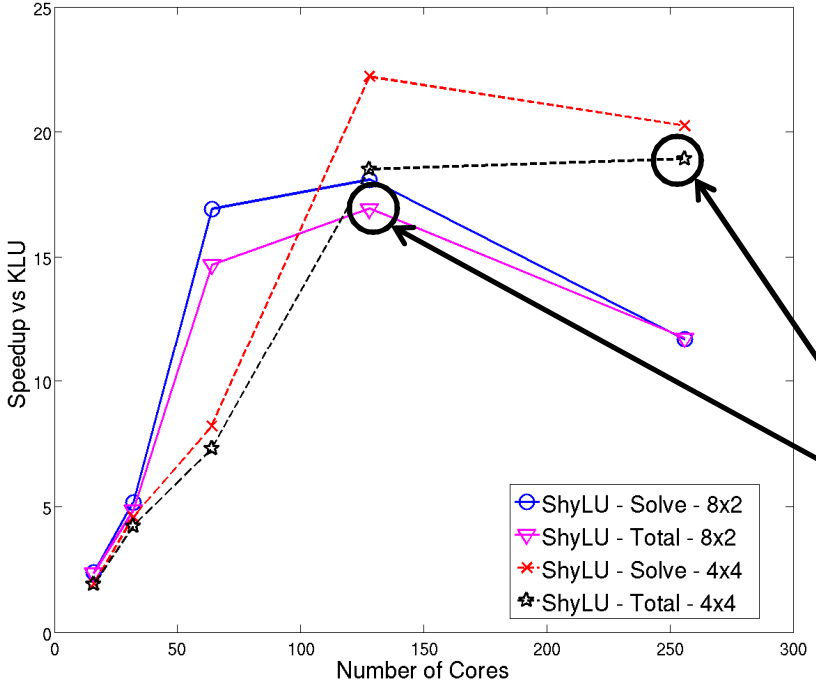


TABLE III
COMPARISON OF TOTAL LINEAR SOLVE TIME (SEC.) OF VARIOUS SPARSE DIRECT SOLVERS FOR OUR TEST CIRCUITS; (-) INDICATES SIMULATION FAILED TO COMPLETE.

	ckt1	ckt2	ckt3	ckt4	ckt5
KLU	**80.8**	162.2	9381.3	7060.8	**14222.7**
PARDISO (16)	128.6	**105.3**	**715.0**	**6690.5**	-
SuperLU	-	10294.1	-	-	72176.8
SuperLU_Dist (16)	-	-	-	-	-

Strong scaling of Xyce's simulation time and ShyLU linear solve time for different configurations of MPI Tasks X Threads per node.

Hybrid Solvers: Recent Comparisons

Recently, several parallel hybrid solvers based on Schur complements have been developed:

- **HIPS** (Gaidamour, Henon)
- MaPhys (Giraud, Haidar, et al.)
- PDSlin (Li, Ng, Yamazaki)
- **ShyLU** (Rajamanickam, Boman, Heroux)

They differ in many ways, e.g, how they approximate Schur complements and how they partition/reorder the matrix.

Numerical tests comparing ShyLU and HIPS were run a 12-core (dual hex) workstation

•HIPS – MPI only

•ShyLU – MPI+threads

ShyLU	4 (2x2)	8 (4x2)	12 (6x2)
ldoor	333s (23)	197s (27)	148s (27)
xyce7	48.3s (15)	36.4s (18)	31.2s (25)

HIPS	4	8	12
ldoor	57s (96)	45s (97)	37s (96)
xyce7	96s (58)	91s (54)	89s (60)

Publications / Presentations

- Publications
  - *"Electrical Modeling and Simulation for Stockpile Stewardship",* ACM XRDS, 2013
  - *"ShyLU: A Hybrid-Hybrid Solver for Multicore Platforms"*, IPDPS 2012
  - *"Parallel Transistor-Level Circuit Simulation",* Simulation and Verification of Electronic and Biological Systems, Springer, 2011
  - *"A Parallel Preconditioning Strategy for Efficient Transistor-Level Circuit Simulation"*, ICCAD 2009
- Presentations
  - *"Sparse Matrix Techniques for Next-Generation Parallel Transistor-Level Circuit Simulation"*

    Heidi K. Thornquist, Parallel Matrix Algorithms and Applications 2012
  - *"Partitioning for Hybrid Solvers: ShyLU and HIPS"*

    Erik G. Boman, Siva Rajamanickam, and Jeremie Gaidamour, Copper Mtn. 2012
  - *"Efficient Preconditioners for Large-Scale Parallel Circuit Simulation"*

    Heidi K. Thornquist, SIAM Computational Science & Engineering 2011
  - *"Advances in Parallel Transistor-Level Circuit Simulation"*

    Heidi K. Thornquist, Scientific Computing in Electrical Engineering 2010
  - *"Large Scale Parallel Circuit Simulation"*

    Heidi Thornquist and Eric Keiter, Circuit and Multi-Domain Simulation Workshop, ICCAD 2009

BACKUP SLIDES

Acronyms

- NW – Nuclear Weapons
- SPICE - Simulation Program With Integrated Circuit Emphasis
- VHDL – VHSIC Hardware Description Language
- VHSIC – Very High Speed Integrated Circuits
- DAE – Differential Algebraic Equation
- DCOP – DC Operating Point
- BTF – Block Triangular Form
- KLU – "Clark Kent" LU
- GMRES – Generalized Minimal RESidual method
- ShyLU – Scalable hybrid LU
- HIPS – Hierarchical Iterative Parallel Solver
- MPI – Message Passing Interface
- AF&F – Arming Fusing & Firing
- ACM – Association for Computing Machinery
- ICCAD – International Conference on Computer-Aided Design
- IPDPS – International Parallel & Distributed Processing Symposium