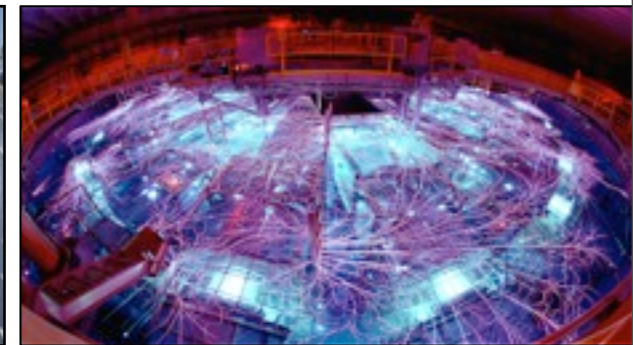
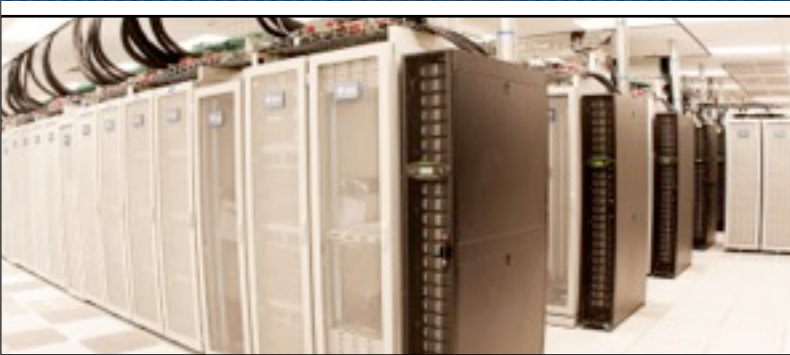


*Exceptional service in the national interest*



# SST Hack-a-thon Component Overview

SST Micro Project Team

Scalable Computer Architectures, Sandia National Laboratories



Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

# SST Micro Components

- Micro is a framework which binds components to a common:
  - Initialization and management infrastructure
  - Timing routines and methods (and conversions between)
  - Exchange of messages
  - Compile and library infrastructure
- Developing a simulation model means selecting which components you want to use
  - Various levels of accuracy
  - Various levels of performance
  - Various levels of stability
  - Not all components work with each other

# Modeling using SST/Micro

- In general studies using Micro will want:
  - Processor core
  - Caches
  - Memory
- SST Micro also provides models for:
  - Network end-points
  - Routers
  - Scheduler(s)
- You cannot easily bind the in-node components with the networking components (... yet).

# GEM5 Processor Core

- SST uses a modified version of the GEM5 simulator to model processor core
  - Cycle-level simulation (although not cycle accurate to x86 cores)
  - Out-of-order x86
  - Runs x86, x86-64, most of SSE2 and a very small part of SSE3
- Needs static Linux compiled binaries
  - Can use your favorite compiler (usually)
  - Run the same binary on the host (good for validation)
  - Creates complications for dependencies

# DRAMSim

- DRAMSim is a cycle-accurate DRAM modeling library from the University of Maryland
  - DDR2 and DDR3 memory modeling
  - Can hack configurations to produce estimates of GDDR-5 memory
- Handles complex processor timing needed to interact with memory

# Cache Models & memHierarchy

- Generally we use caches provided by GEM5
- Developing (nearly finished) our own caches
  - More flexible and better parameterization
  - Allow simulation of cache-to-memory in parallel
  - Allow flexible coherency modeling
  - Parallel GEM5 cores connected by custom caches
  - Improved accuracy and reliability as we can control environment for testing
- Working on the coherency and locking now



Sandia  
National  
Laboratories

*Exceptional service in the national interest*