HETEROGENEOUSLY INTEGRATED SYSTEM ON A CHIP

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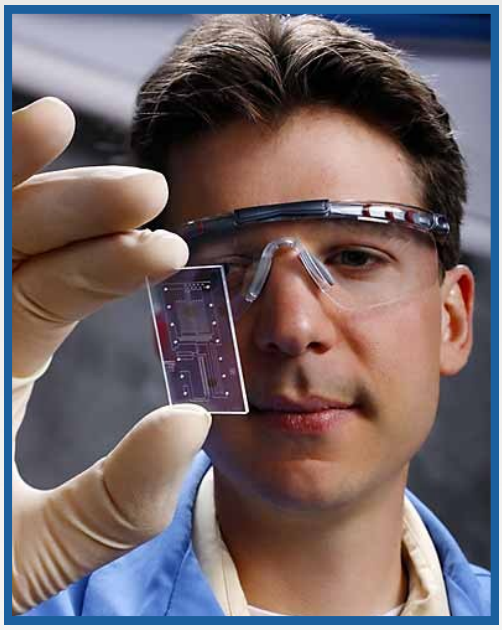
TECHNOLOGY READINESS LEVEL: 7- DEMONSTRATION OF ACTUAL DEVELOPMENT VERSION IN THE OPERATIONAL ENVIRONMENT

US PATENT # 7,335,972

(SD# 7151.1)

TECHNOLOGY SUMMARY



Microsystems packaging requires the assembly and interconnections of microelectronics, MEMS, photonics, fluids, and other microscale devices onto a system-level board or chip to form an integrated microsystems product. Due to the microsystem package providing environmental protection, thermal management, testing, and power distribution, the packaging controls the microsystems performance, cost, size, and reliability.

The present invention relates to microsystems packaging and a method for integrating heterogeneous microsystems devices on to a single chip in a cost effective and efficient manner.

The microsystem-on-a-chip technology comprises a bottom wafer of normal thickness and a series of thinned wafers that can be stacked on the bottom wafer, glued and electrically interconnected. The interconnection layer consists of a compliant dielectric material, an interconnect structure, and can include embedded passives. The stacked wafer technology provides a heterogeneously integrated, ultra-miniaturized, high performing, robust and cost-effective microsystem package. This highly integrated microsystem package can be miniaturized both in volume and footprint and provides all of the needed system level functions.

POTENTIAL APPLICATIONS

- Microelectronics
- Sensors
- Surveillance devices

TECHNOLOGICAL BENEFITS

- Heterogeneously integrated, ultra-miniaturized, cost-effective, high performing microsystem packing that reduces prior art issues
- Eliminates the use of wire bonds and solder joints making the package more robust for applications exposed to extreme shock

TECHNOLOGY INQUIRY?

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