SAND2013-2167P

2013 ERD Memory Planning
March 14, 2013 ERD Telecon
(continued from March 7)

Discussion Topics

- Template for memory section text entries
  - Finish discussion from last week
- Storage Class Memory/Processor In Memory
- Table entries and table status
  - Continue discussion from last week
- Action items
- Feedback from 2011 edition (if there is time)

Proposal: Template for Memory Section Entries

- In red: notes from phone call on 3/06
- Similar to the Logic template that Shamik has proposed:
- Heading (for ReRAM, ferroelectric, possibly others): Overview (250 words)
  - Brief description of common attributes of class structure / mechanism
  - Trade-offs
- Overview (250 words) Changed to 200 words. Might need to edit down further
  - Brief description of device structure / mechanism
  - Do not turn this into a large, intricate physics discussion
- Present status (250 words) Changed to 200 words
  - Best reported results to date
    - Scalability, endurance, retention, write energy, voltage, current, temperature range
    - Array data? (versus single device, theory) – This is discussed in table section
    - Trade-offs: example: temperature vs scalability vs retention
  - Notable recent publications/results since June 2011
- Active research questions (250 words) Changed to 200 words
  - Major challenges to be resolved
  - Critical path – technological and scientific challenges to be solve to move device to the next level
  - Ask experts to prioritize research questions

Proposal: Template for Memory Section Entries

- Other comments from 3/7 phone call
- Writeup should be unbiased even though usually written by a proponent
  - Friendly critic to review each entry
- Need more input and feedback from companies
- Would like to get feedback for writeup and tables prior to chapter lockdown

Reference: Notes on 2011 Roadmap

8-9 pgs

ITRS

Reference: Notes on 2011 Roadmap

- Full page 750-900 words, depending on how many headings
- This typical memory is ~400 words:

4.1.2.1.1. Ferroelectric FET

The Ferroelectric FET (FeFET)[2] memory is a 1T memory device where a ferroelectric capacitor is integrated into the gate stack of a FET. The ferroelectric polarization directly affects charges in the channel and leads to a defined shift of the output characteristics of the FET. A typical FeFET memory element uses inorganic complex oxides or fluorides, such as $PbZr_xTi_{1-x}O_3$, $SrBa_2Ta_2O_9$, $BiMgF_4$, in the gate stack of a silicon FET. A serious difficulty with these materials is interdiffusion and chemical reaction between the stack interfaces at the high deposition temperatures and high oxygen concentrations needed for deposition of the ferroelectric films on a Si substrate[2,3]. In order to avoid the diffusion problem, an insulating buffer layer is inserted between a ferroelectric film and the Si substrate[2], hence, the resulting gate structure consists of a metal-ferroelectric-insulator-semiconductor (MFIS) gate stack. Using an organic ferroelectric film (for example polyvinylidene fluoride - PVDF) as a gate dielectric allows for elimination of the buffer layer, due to lower crystallization temperature of organic materials, and therefore suppression of the diffusion[2,3]. The major challenge of the FeFET memory is the short retention time (typically ~days to ~months), which is the result of two fundamental mechanisms, namely the finite depolarization field present in the stack and the charge injection in the stack due to ferroelectric polarization and a subsequent charge trapping[4,5]. Proposed approaches to increase retention time include improvements of the quality of the FE layer and its interface with the FET structure, e.g. by using all-oxide heteroepitaxial structures[6]. As an ideal case, the use a perfect, single crystal single-domain ferroelectric has been discussed[4,5].

Short retention of the FeFET memory raises question of its potential for application as nonvolatile memory, e.g. for the S-SCM technologies [see the SCM section 4.1.4 below]. On the other hand, DRAM-like applications are envisioned[3] and the FeFET memory may have a potential for M-SCM, if scalability below 50 nm can be demonstrated. Currently, new materials for the FeFET stacks are being actively investigated, such as organic ferroelectrics[3,7], nanotubes[8], nanowires[9], and graphene[10]. The FeFET memory scaling is projected to end approximately with the 22 nm generation, because the insulation layer becomes too thin and the properties of the ferroelectric with respect to thickness dependence of the coercive field will not allow further reduction[11].

Reference: Notes on 2011 Roadmap

- Full page is 670 – 800 words, depending on headings
- Size of typical entries:
  - Ferroelectric heading: 41
  - FeFET: 387
  - Fe ReRAM: 100
  - ReRAM: 450
  - NEMM: 237
- Wide range – can define more strictly this ed

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2013 Storage Class Memory Writeup

- Geoff Burr has volunteered to lead
- Other team members:
  - Matt Marinella
  - Victor Zhirnov
  - ?
- Need to decide section layout & location – separate section?
- Might want to add other similar concepts:
  - Processor-in-memory (for overview, see http://www.cse.nd.edu/~pim/)
  - HP's Nanostores
  - Others?
- Should probably devote a future phone call to this

Discussion Topics

- Template for memory section text entries
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Emerging Memory Section Tables

- Have a system where we have major categories and subcategories?
  - Examples ReRAM, subclasses ECM, VCM, TCM
- Emerging ferroelectric memory
  - Break into two separate entries (e.g., FTJ and FeFET) or create two sub-categories under this name
- Ferroelectric polarization ReRAM
- Nanoelectromechanical memory
  - From the 3/7 discussion and December F2F meeting, sounds like we have decided to remove this (move to transition).
  - Do we need to bring this before the full group first?
- Redox memory
  - 3/7 – we have agreed that creating VCM and ECM subcategories is appropriate – TCM also?

Emerging Memory Section Tables

- Mott memory
- Macromolecular memory
  - Seems like explanation of the mechanism is similar to ReRAM
  - This may be a separate category under the ReRAM heading
- Molecular memory
  - Remove?
  - Ask Rainer Waser about removal/transition
  - Noted that not many new papers are emerging on this topic after the big push from HP, Caltech, UCLA ended.
- Carbon-based memory?
  - NRAM does not have recent peer reviewed papers
  - Stanford stuff – amorphous carbon and nanotube (need to get refs)
  - Carbon bonding mechanism

Emerging Memory Metrics

- What is our standard for listing a metric?
  - Published data on one device that might not be manufacturable? Example – PCRAM energy from nanotube contacts
  - Published array data? Sometimes unavailable
  - We are using different standards for different devices – comparison might not be apples to apples.
  - 3/7: Decided it is worthwhile to put array and single device numbers. Do we want columns for each?
  - Do we want to have theoretical numbers for some cases? Example: flash min write energy is theoretical.

Emerging Memory Section Tables

- Can we get additional feedback from companies, etc before the lockdown of the chapter?
  - Will need to send out draft text & tables earlier…
- What is the ordering of devices? Right now it may be arbitrary but we should probably address this. Possibilities
  - Maturity, potential, performance, research activity?
  - From our own ranking
  - Possibly alphabetical to avoid ranking
  - Decision not yet made…
- Should we create a "nice/easy to read" summary table?
  - This would probably be used in a lot of presentations and give us good visibility
  - Seems like the general feeling about this was positive – should I go ahead and propose a format for this?

Baseline/Prototypical Memory Tech

Table ERD3 Current Baseline and Prototypical Memory Technologies

		Baseline Technologies					Prototypical technologies [A]		
		DRAM		SRAM [C]	Flash		FeRAM	STT-MRAM	PCM
		Stand-alone [A]	Embedded [C]		NOR Embedded [C]	NAND Stand-alone [A]			
Storage Mechanism		Charge on a capacitor		Inter-locked state of logic gates	Charge trapped in floating gate or in gate insulator		Remnant polarization on a ferroelectric capacitor	Magnetization of ferromagnetic layer	Reversibly changing amorphous and crystalline phases
Cell Elements		1T1C		6T	1T		1T1C	1(2)T1R	1T(D)1R
Feature size F, nm	**2011**	36	65	45	90	22	180	65	45
	2024	9	20	10	25	8	65	16	8
Cell Area	**2011**	$6F^2$	$(12\text{-}30)F^2$	140 F^2	10 F^2	4 F^2	$22F^2$	$20F^2$	$4F^2$
	2024	$4F^2$	$(12\text{-}50)F^2$	140 F^2	10 F^2	4 F^2	$12F^2$	$8F^2$	$4F^2$
Read Time	**2011**	<10 ns	2 ns	0.2 ns	15 ns	0.1ms	40 ns [G]	35 ns [J]	12 ns [K]
	2024	<10 ns	1 ns	70 ps	8 ns	0.1ms	<20 ns [H]	<10 ns	< 10 ns
W/E Time	**2011**	<10 ns	2 ns	0.2 ns	1µs/10ms	1/0.1 ms	65 ns [G]	35 ns {J]	100 ns [K]
	2024	<10 ns	1 ns	70 ps	1µs/10ms	1/0.1 ms	<10 ns[H]	<1 ns	<50 ns
Retention Time	**2011**	64 ms	4 ms	[D]	10 y	10 y	10 y	>10 y	>10 y
	2024	64 ms	1 ms	[D]	10 y	10 y	10 y	>10 y	>10 y
Write Cycles	**2011**	>1E16	>1E16	>1E16	1E5	1E4	1E14	>1E12	1E9
	2024	>1E16	>1E16	>1E16	1E5	5E3	>1E15	>1E15	1E9
Write Operating Voltage (V)	**2011**	2.5	2.5	1	10	15	1.3-3.3	1.8	3 [K]
	2024	1.5	1.5	0.7	9	15	0.7–1.5	<1	<3
Read Operating Voltage (V)	**2011**	1.8	1.7	1	1.8	1.8	1.3–3.3	1.8	1.2
	2024	1.5	1.5	0.7	1	1	0.7–1.5	<1	<1
Write Energy (J/bit)	**2011**	4E-15 [B]	5.00E-15	5.00E-16	1E-10 [E]	>2E-16 [F]	3E-14 [I]	2.5E-12 [A]	6E-12 [L]
	2024	2E-15 [B]	2.00E-15	3.00E-17	1E-11 [E]	>2E-17 [F]	7E-15 [I]	1.5E-13 [A]	~1E-15 [M]

Emerging Memory Technologies

Table ERD5 Emerging Research Memory Devices—Demonstrated and Projected Parameters

		A. Emerging Ferroelectric memory	B . Nanomechanical Memory	C. Redox Memory	D. Mott Memory	E. Macromolecular Memory	F. Molecular Memories
Storage Mechanism		Remnant polarization on a ferroelectric dielectric	Electrostatically-controlled mechanical switch	Ion transport and redox reactions	Multiple mechanisms	Multiple mechanisms	Multiple mechanisms
Cell Elements		1T or 1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
Device Types		1) FET with FE gate insulator 2) FE barrier effects	NEMS	1) cation migration 2) anion migration	Mott transition	M-I-M (nc)-I-M	Bi-stable switch
Feature size F	Min. required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	22 nm [A1]	>50 nm [B1, B2]	5 nm [C1]	5-10 nm	5-10 nm	5 nm [F1]
	Demonstrated	0.6 µm [A2]	500 nm [B3, B4]	30 nm [C2], 9nm [C7]	10 µm [D1]	130 nm [E1]	30 nm [F2]
Cell Area	Min. required	$8F^2$	$8F^2$	$8F^2$	$8F^2$	$8F^2$	$8F^2$
	Best projected	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$
	Demonstrated	Data not available	Data not available	$4F^2$ [C2], $8F^2$ [C3]	Data not available	$4F^2$ [E1]	Data not available
Read Time	Min. required	<15 ns	<15 ns	<15 ns	< 15 ns	<15 ns	<15 ns
	Best projected	2.5 ns	<10 ns	<10 ns	< 10 ns	<10 ns	<10 ns [F1]
	Demonstrated	20 ns [A3]	Data not available	<50 ns [C3]	Data not available	10 ns [E1]	Data not available
W/E time	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	2.5 ns [A1]	<1 ns [B1, B2]	<1 ns [C4]	<1 ns [D2]	<10 ns	<40 ns [F1]
	Demonstrated	20 ns [A4]	~5 ns [B3, B4]	0.3ns [C5]	< 20 ns [D3]	15 ns [E2]	10s [F6],0.2 s [F3]
Retention Time	Min. required	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
	Best projected	>10 y [A4]	>10 y	>10 y	Not known	Not known	Not known
	Demonstrated	~3.5 month [A6]	~days	>10 y [C2]	Not known	~year [E3]	1 hour [F6], 2 months [F4]
Write Cycles	Min. required	>1E5	>1E5	>1E5	>1E5	>1E5	>1E5
	Best projected	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16
	Demonstrated	2E11 [A5]	~1E3 [B4]	1E12 [C2]	~1E2 [D4]	~1E5 [E4]	~2E3 [F2]
Write operating voltage (V)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	<0.9 V [A1]	>1 V [B1, B2]	<0.5 V [C6]	Not known	<1 V [E5]	80 mV[F5]
	Demonstrated	±4[A4]	5 V [B3, B4]	0.6/-0.2 [C3]	1.25/0.75 V [D1]	~±2 V [E3]	4V[F6], ~±1.5 V [F2]
Read operating voltage (V)	Min. required	2.5	2.5	2.5	2.5	2.5	2.5
	Best projected	0.7	0.7	<0.2 V [C6]	Not known	0.7	0.3 [F1]
	Demonstrated	2.5 [A3]	1 [B3]	0.15 [C3]	0.2 [D1]	0.5 V [E3]	0.5V [F6],0.5 V [F2]
Write energy (J/bit)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	2E-15 [A7]	1E-17 [B5]	1E-17 [C4]	Not known	Not known	2E-19 [F6]
	Demonstrated	Data not available	Data not available	1E-13 [C7]	5E-13 [D5]	5E-11 [E6]	Data not available
Comments		Potential for non-destructive readout	Inverse voltage scaling presents a problem; Limited endurance	Potential for multi-bit storage; Low read voltage presents a problem	Retention requires additional mechanisms to maintain Mott transition conditions		160 Kbit prototype chip demonstrated [F3]
Research activity [G1]		117	32	593	20	119	57

Transition Table

Table ERD4 Transition Table for Emerging Research Memory Devices

	IN/OUT (Table ERD5)	*Reason for IN/OUT*	*Comment*
Emerging Ferroelectric Memory	**IN**	Replaces former FeFET category and the ferroelectric polarization/electronic effects memory categories	Ferroelectric polarization/electronic effects memory has same difficult problems as FeFET, e.g scalability, retention, endurance fatigue
Redox memory	**IN**	Replaces former nanothermal and nanoionic memory categories	Former 'Nanothermal' and 'Nanoinic' entries often referred to related mechanisms of resistive switching
Mott Memory	**IN**	Separated from the electronic effects memory	
FeFET Memory	**OUT**	Merged with FeFET and the ferroelectric polarization/electronic effects memory	
Electronic effects memory	**OUT**	Replaced by Emerging Ferroelectric and Mott memories	Charge trapping induced resistive switching is not considered in 2011 ERD chapter, as a scaling of this memory technology below 100 nm is difficult for any conceivable material combination [A]
Nanothermal memory	**OUT**	Merged with Nanoionic Memory to form Redox Memory Category	Mechanism related to Nanoionic memory
Nanoionic memory	**OUT**	Merged with Nanothermal Memory to form Redox Memory Category	Mechanism related to Nanothermal memory
Spin Torque Transfer MRAM	**OUT**	Became a prototypical technology	Spin Torque Tranfer MRAM is already included in PIDS chapter since 2009 (TablePIDS8b)

Memory Survey and Taxonomy Tables

- Survey
  - 3/7 – Suggested doing the survey earlier this year; however, would need all entries decided
  - Maybe at July meeting?
  - Any changes to categories or format?
- Taxonomy table
  - Do we want to keep this and update it?

Table ERD10 Potential of the current prototypical and emerging research memory candidates for SCM applications

(The entries in this table result from group discussion at several ITRS meetings. The rationale for these entries is discussed in the individual section on each of the emerging research memory technologies.)

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
Parameter	**FeRAM**	**STT-MRAM**	**PCRAM**	**Emerging ferroelectric memory**	**Nanomechanical memory**	**Redox memory**	**Mott Memory**	**Macromolecular memory**	**Molecular Memory**
Scalability									
MLC									
3D integration									
Fabrication cost									
Endurance									

Scalability	F_{min} >45 nm
MLC	difficult
3D integration	difficult
Fabrication cost	high
Endurance	≤1E5 write cycles demonstrated

Scalability	F_{min}=10-45 nm
MLC	difficult
3D integration	difficult
Fabrication cost	medium
Endurance	≤1E10 write cycles demonstrated

Scalability	F_{min} <10 nm
MLC	difficult
3D integration	difficult
Fabrication cost	high
Endurance	>1E10 write cycles demonstrated

Taxonomy

Table ERD2 Memory Taxonomy

Cell Element	*Type*	*Non-volatility*	*Retention Time*
1T1R or 1D1R [A]	STT-MRAM	Nonvolatile	> 10 years
	Phase change memory	Nonvolatile	> 10 years
	Nano-electro-mechanical memory	Nonvolatile	> years
	RedOx Memory	Nonvolatile	> years
	Mott Memory	Nonvolatile	> years
	Macromolecular memory	Nonvolatile	> years
	Molecular memory	Nonvolatile	> years
1T1C [A]	DRAM	Volatile	~ seconds
	FeRAM [B]	Nonvolatile	> 10 years
1T [A]	FB DRAM [A]	Volatile	< seconds
	FeFET memory [A]	Nonvolatile	> years
	Flash [C]	Nonvolatile	> 10 years
Multiple T [A]	SRAM	Volatile	large

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- Feedback from 2011 edition (if there is time)

Action Items

- Matt & Victor
  - Contact Rainer Waser for opinion:
    - Should carbon based memory should be a topic?
    - Should macromolecular be part of ReRAM?
    - Should we drop/transition molecular?
  - Write a sample entry for FeRAM
  - Propose modified table format
  - Propose in/out table
  - Propose easy to read table?
  - SCM workshop writeup
- Geoff
  - Dedicate a phone call to SCM/PIM, etc

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Memory Section Feedbacks (Paul Franzon)

- End of DRAM scaling problem already happening (e.g., decreasing charge/bit, crosstalk): not addressed as a driver in Table ERD-1, first entry).
- 2024 scaling limits of DRAM (8nm) and NAND (9nm) in Table ERD-3 may be misleading.
- Table ERD-7 for select device parameters: separate read and write current.
- Energy efficiency is important in memory and is hardly addressed in SCM .
- SCM is specific to server class systems. Leaves out issues related to commodity memory and mobile.
- In architecture section: (1) Energy-efficient peripheral and integration circuits are not addressed; (2) Issues in hybrid memory integration for M-SCM could be addressed, e.g. where did 10^9 endurance come from as a threshold?

Memory Section Feedbacks (ChiaHua Ho)

- Table ERD-10: endurance of nanomechanical memory should be "low" instead of "good".
- Detailed comments on Table ERD-5 on the next page.

50nm achieved, 2011 IEDM
Program 3~4V
Read < 1V

Memory Section Feedbacks (ChiaHua Ho)

Cannot find references

Page 6: Table ERD5 (Emerging Research Memory Devices — Demonstrated and Projected Parameters)

		A. Emerging Ferroelectric memory	B. Nanomechanical Memory	C. Redox Memory	D. Mott Memory	E. Macromolecular Memory	F. Molecular Memories
Storage Mechanism		Remnant polarization on a ferroelectric dielectric	Electrostatically-controlled mechanical switch	Ion transport and redox reactions	Multiple mechanisms	Multiple mechanisms	Multiple mechanisms
Cell Elements		1T or 1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
Device Types		1) FET with FE gate insulator 2) FE barrier effects	NEMS	1) cation migration 2) anion migration	Mott transition	M-I-M (nc)-I-M	Bi-stable switch
Feature size F	Min. required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	22 nm [A1]	**50 nm [B1, B2]**	5 nm [C1]	5-10 nm	5-10 nm	5 nm [H1]
	Demonstrated	~~**0.6 µm [A2]**~~	~~180 nm [B2]~~	~~**30 nm [C2]**~~	**200 nm [a]**	250 nm [G1]	30 nm [H2]
Cell Area	Min. required	**$8F^2$**	**$8F^2$**	**$8F^2$**	**$8F^2$**	**$8F^2$**	**$8F^2$**
	Best projected	**$4F^2$**	**$4F^2$**	**$4F^2$**	**$4F^2$**	**$4F^2$**	**$4F^2$**
	Demonstrated	Data not available	Data not available	**$4F^2$ [C2], $8F^2$ [C3]**	Data not available	Data not available	Data not available
Read Time	Min. required	<15 ns	<15 ns	<15 ns	**< 15 ns**	<15 ns	<15 ns
	Best projected	2.5 ns	<3 ns	<10 ns	**< 10 ns**	<10 ns	<10 ns [H1]
	Demonstrated	20 ns [A4]	~~3 ns [B3]~~	<50 ns [C3]	Data not available	~10 ns [G2]	Data not available
W/E time	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	2.5 ns [A1]	<1 ns [B1,B2]	<1 ns [C4]	~~1 ps [b]~~	<10 ns	<40 ns [H1]
	Demonstrated	~~20 ns [A5]~~	~~~1 ns [B3]~~	**0.3ns [C5]**	**< 20 ns [c]**	10 ns [G2]	10s [H6],0.2 s [H3]
Retention Time	Min. required	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
	Best projected	>10 y [A5]	>10 y	>10 y	Not known	Not known	Not known
	Demonstrated	**~3.5 month [A7]**	~~~days~~	>10 y [C2]	Not known	6 month [G4]	1 hour [H6], 2 months [H4]
Write Cycles	Min. required	>1E5	>1E5	>1E5	**>1E5**	>1E5	>1E5
	Best projected	>1E16	>1E16	>1E16	**>1E16**	>1E16	>1E16
	Demonstrated	**2E11 [A6]**	**~10^2 [B4]**	**1E12 [C2]**	**1E8 [d]**	~~>1E6 [G2]~~	>2E3 [H2]
Write operating voltage (V)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	<0.9 V [A1]	Not known [B4]	<0.5 V [E7]	Not known	<1 V [G1]	80 mV[H5]
	Demonstrated	~~±4 [A5]~~	~~1.5 V [B1]~~	0.6/-0.2 [E1]	**< 1V [e]**	~±2 [G2]	4V[H6], ~±1.5 V [H2]
Read operating voltage (V)	Min. required	2.5	2.5	2.5	**2.5**	2.5	2.5
	Best projected	0.7	0.7	<0.2 V [E7]	Not known	0.7	0.3 [H1]
	Demonstrated	~~2.5 [A4]~~	1.5 V [B1]	0.15 V[E1]	Data not available	1 V [G2]	0.5V [H6],0.5 V [H2]
Write energy (J/bit)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	2E-15 [A8]	Not known	1E-15 [E8]	Not known	Not known	2E-19 [H6]
	Demonstrated	Data not available	Data not available	5E-14 [E9]	Data not available	1E-13 [G3]	Data not available
Comments		Potential for non-destructive readout	Inverse voltage scaling presents a problem	2 Mbit prototype chip demonstrated [E1]; Potential for multi-bit storage; Low read voltage presents a problem	Retention induced by maintaining Mott transition conditions		160 Kbit prototype chip demonstrated [H3]
Research activity [1]			**32**				

No mentioned, and ref too old

3V

No mentioned

Simulation data

9nm, 2010 IEDM

Ridiculous projection

Reference no data; another reference showed read-cycle of 1E6

ITRS

Other Considerations

- Add more taxonomy figures in main text.
- Add a list of figures and tables in main text. (A list already exists in the excel table file.)
- Section organization: section 4 includes memory, logic, and MtM (page 5-27) and is long. As a result, subsections like “4.1.3.2.2.1 MIT switch” exist. Make memory, logic and MtM each a section?
- Reference format consistency and redundancy.

Typos

- Typos on page 13: following “4.1.4.4” is “4.1.1.5” and should be “4.1.4.1”; section “4.2” starts with “4.2.4” and should be “4.2.1”. Long section labels may cause confusion.
- Section 4.2.4.5.1 on page 19: line 5 under the section title: “ffunctionalities”.
- More typos pointed out in the following pages.

❑ Typo Corrections

Emerging Research Devices	
Please refer to the ERD summary in the 2008 Update Overview	
Table ERD1	*Emerging Research Devices Difficult Challenges*
Table ERD2	*Memory Taxonomy*
Table ERD3	*Current Baseline and Prototypical Memory Technologies*
Table ERD4	*Transition Table for Emerging Research Memory Devices*
Table ERD5a	*Emerging Research Capacitance-based Memory Devices—Demonstrated and Projected Para*
Table ERD5b	*Emerging Research Resistance-based Memory Devices—Demonstrated and Projected Param*

Table ERD5 *Emerging Research Memory Devices – Demonstrated and Projected Parameters*

- **Table ERD2**

Notes for Table ERD2:

[A] 1T1R—1 transistor–1 resistor 1D1R—1 diode–1 resistor 1T1C—1 transistor–1 capacitor 1T—1 transistor FB DRAM—floating body DRAM FeFET—ferroelectric FET Multiple T—multiple transistor

[B] FeRAM—ferroelectric RAM with one ferroelectric transistor and one ferroelectric capacitor

[C] Floating gate or charge-trapping

one transistor

- **Table ERD5**

Notes for Table ERD5b: → ERD5:

Table ERD4 Transition Table for Emerging Research Memory Devices

	IN/OUT (Table ERD5)	*Reason for IN/OUT*	*Comment*
Emerging Ferroelectric Memory	**IN**	Replaces former FeFET category and the ferroelectric polarization/electronc effects memory categories	Ferroelectric polarization/electronc effects memory has same difficult problems as FeFET, e.g scalability, retention, endurance fatigue
Redox memory	**IN**	Replaces former nanothermal and nanoionic memory categories	Former 'Nanothermal' and 'Nanoinic' entries often referred to related mechanisms of resistive switching
Mott Memory	**IN**	Separated from the electronic effects memory	
FeFET Memory	**OUT**	Merged with FeFET and the ferroelectric polarization/electronc effects memory	
Electronic effects memory	**OUT**	Replaced by Emerging Ferroelectric and Mott memories	Charge trapping induced resistive switching is not consifered in 2011 ERD chapter, as a scaling of this memory technology below 100 nm is difficulty for any conceivable material combination [A]
Nanothermal memory	**OUT**	Merged with Ionic Memory to form Redox Memory Category	Mechanism related to Nanoionic memory
Nanoionic memory	**OUT**	Merged with Nanothermal Memory to form Redox Memory Category	Mechanism related to Nanothermal memory
Spin Torque Transfer MRAM	**OUT**	Became a prototypical technology	Spin Torque Tranfer MRAM is already included in PIDS chapter since 2009 (TablePIDS8b)

electronic

considered

nanoionic

difficult

Notes for Table ERD5b: → ERD4:

[A] H. Schroeder, V. V. Zhirnov, R. K. Cavin, R. Waser, Voltage-time dilemma of pure electronic mechanisms in resistive switching memory cells", J. Appl. Phys. 107 (2010) 054517

Table ERD9 Target device and system specifications for SCM

Parameter	*Benchmark* [A]			*Target*	
	HDD [B]	**NAND flash** [B]	**DRAM**	**Memory-type SCM**	**Storage-type SCM**
Read/Write latency	3-5 ms	~100µs (block erase ~1 ms)	<100 ns	<100 ns	1-10µs
Endurance **(cycles)**	unlimited	10^4-10^5 **[C]**	unlimited	$>10^9$	$>10^6$
Retention	>10 years	~10 years	64 ms	>5 days	~10 years
ON power **(W/GB)**	~0.04	~0.01-0.04	0.4	<0.4	<0.04
Standby power	~20% ON power	<10% ON power	~25% ON power	<1% ON power	<1% ON power
Areal density	~ 10^{11} bit/cm^2	~ 10^{10} bit/cm^2	~ 10^9 bit/cm^2	$>10^{10}$ bit/cm^2	$>10^{10}$ bit/cm^2
Cost **($/GB)**	0.1	2	10	<10	<3-4

Notes for Table ERD3: → ERD9:

[A] The benchmark numbers are representative values, which may have significant variations in specific product
[B] Enterprise class
[C] Single-level cell (SLC) ?

Table ERD10 Potential of the current prototypical and emerging research memory candidates for SCM applications

(The entries in this table result from group discussion at several ITRS meetings. The rationale for these entries is discussed in the individual section on each of the emerging research memory technologies.)

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
Parameter	**FeRAM**	**STT-MRAM**	**PCRAM**	**Emerging ferroelectric memory**	**Nanomechanical memory**	**Redox memory**	**Mott Memory**	**Macromolecular memory**	**Molecular Memory**
Scalability	☹	😐	☺	😐	☹	☺	?	?	☺
MLC	☹	☹	☺	☹	☹	☺	?	😐	☹
3D integration	☹	😐	☺	☹	☹	😐	?	☺	☹
Fabrication cost	😐	😐	☺	😐	☹	😐	?	☺	?
Endurance	☺	☺	😐	☺	☹	☺	😐	☹	?

☹

Scalability	F_{min} >45 nm
MLC	difficult
3D integration	difficult
Fabrication cost	high
Endurance	≤1E5 write cycles demonstrated

😐

Scalability	F_{min}=10-45 nm
MLC	difficult → medium
3D integration	difficult → medium
Fabrication cost	medium
Endurance	≤1E10 write cycles demonstrated

☺

Scalability	F_{min} <10 nm
MLC	difficult → feasible
3D integration	difficult → feasible
Fabrication cost	high → low
Endurance	>1E10 write cycles demonstrated

P. 41 *[7] CMOS Technological Compatibility*—The semiconductor industry has been based for the last 40 years on incremental scaling of device dimensions to achieve performance gains. The principle economic benefit of such an approach is it allows the

principal

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- **6.3 SURVEY-BASED BENCHMARKING OF BEYOND CMOS MEMORY & LOGIC TECHNOLOGIES**
- ***6.3.1 OVERALL TECHNOLOGY REQUIREMENTS AND RELEVANCE CRITERIA***

The second method for benchmarking emerging memory and information processing devices is based on a survey of the Emerging Research Devices Work Group. Some emerging nanoscale devices discussed in this chapter are charge-based structures proposed to extend CMOS to the end of the current roadmap. Other emerging devicesoffer new computational state variables and will likely require new fabrication technologies. A set of relevance or evaluation criteria, defined below, are used to parameterize the extent to which proposed "CMOS Extension" and "Beyond CMOS" technologies are applicable to memory

devices offer

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Memory—Individual Potential for Emerging Research Memory Devic
Related to each Technology Relevance Criterion

Score	
3	Substantially exceeds the appropriate ultimately scaled Baseline Memory Technology (Relevance Criteria 1 – 5) 6) *or* is compatible with CMOS operating temperature 7) *or* is monolithically integrable with CMOS wafer technology 8) *or* is compatible with CMOS wafer technology (i.e., *Substantially Better than* ultimately scaled *Silicon Baseline Memory Technology*)
2	Comparable to the appropriate ultimately scaled Baseline Memory Technology (Relevance Criteria 1 – 5) 6) *or* requires a very aggressive forced air cooling technology 7) *or* is functionally integrable (easily) with CMOS wafer technology 8) *or* can be integrated with CMOS architecture with some difficulty (i.e., *Comparable to Silicon* ultimately scaled *n Baseline Memory Technology*)

scaled *Baseline Memory*

Page 6: Table ERD2 (Memory Taxonomy)

Table ERD2 *Memory Taxonomy*

Cell Element	*Type*	*Non-volatility*	*Retention Time*
1T1R or 1D1R [A]	MRAM	Nonvolatile	> 10 years
	Phase change memory	Nonvolatile	> 10 years
	Nano-electro-mechanical memory	Nonvolatile	> years
	RedOx Memory	Nonvolatile	> years
	RedOx Memory	Nonvolatile	> years
	Macromolecular memory	Nonvolatile	> years
	Molecular memory	Nonvolatile	> years
1T1C [A]	DRAM	Volatile	~ seconds
	FeRAM [B]	Nonvolatile	> 10 years
1T [A]	FB DRAM [A]	Volatile	< seconds
	FeFET memory [A]	Nonvolatile	> years
	Flash [C]	Nonvolatile	> 10 years
Multiple T [A]	SRAM	Volatile	large

Discussion Later

Months ?

Short ?

Notes for Table ERD2:

[A] 1T1R—1 transistor–1 resistor 1D1R—1 diode–1 resistor 1T1C—1 transistor–1 capacitor 1T—1 transistor FB DRAM—floating body DRAM FeFET—ferroelectric FET Multiple T—multiple transistor

[B] FeRAM—ferroelectric RAM with one ferroelectric transistor and one ferroelectric capacitor

[C] Floating gate or charge-trapping