



Position-Dependent Transport of n-p-n Junctions in Axially Doped SiGe Nanowire Transistors

Collin Delker¹, Jinkyong Yoo², Brian Swartzentruber², Tom Harris²

¹Sandia National Labs ²Center for Integrated Nanotechnologies



Office of Science

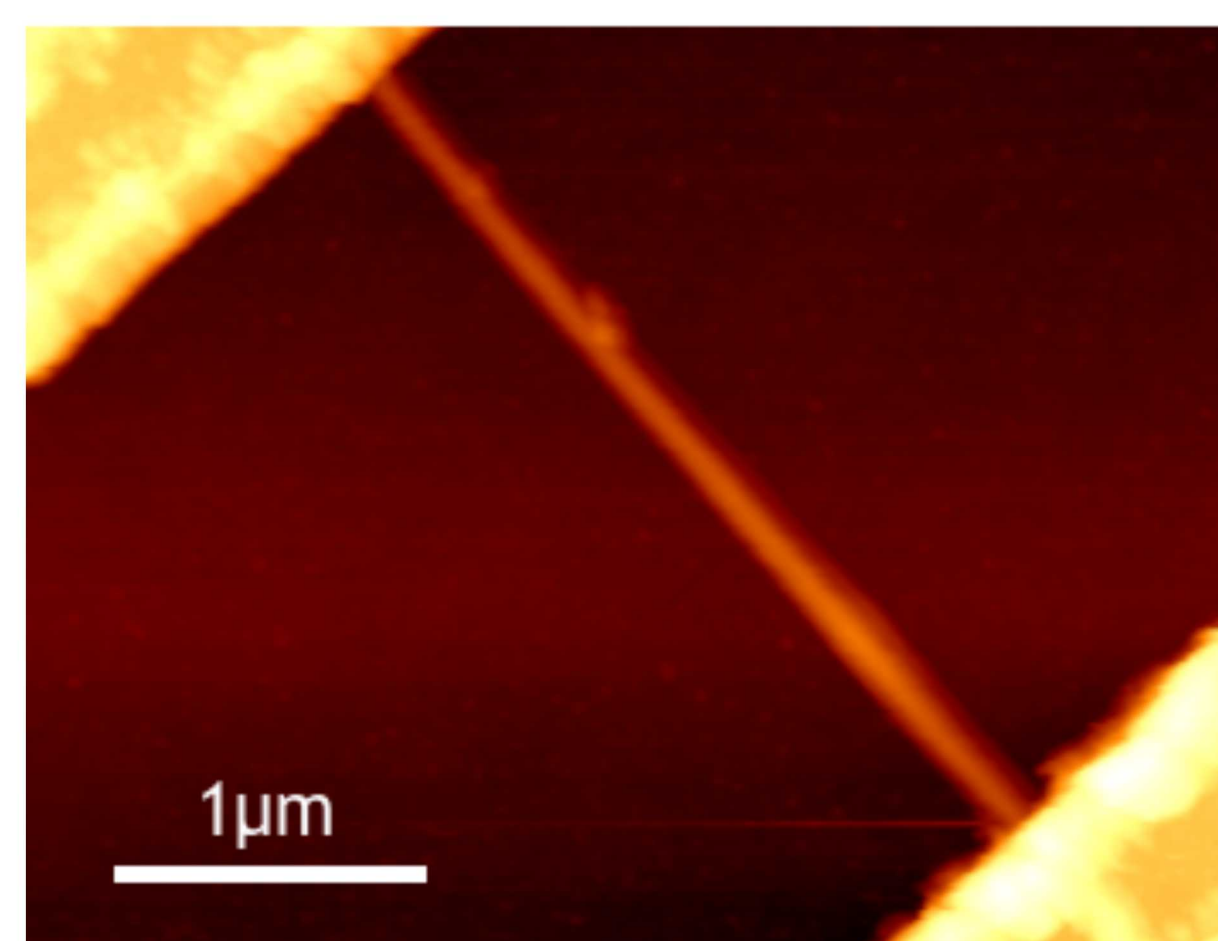
Axial Junction n-p-n Nanowires

Nanowire transistors are attractive architectures for applications in next-generation electronic devices due to their low dimensionality and compatibility with numerous material systems.

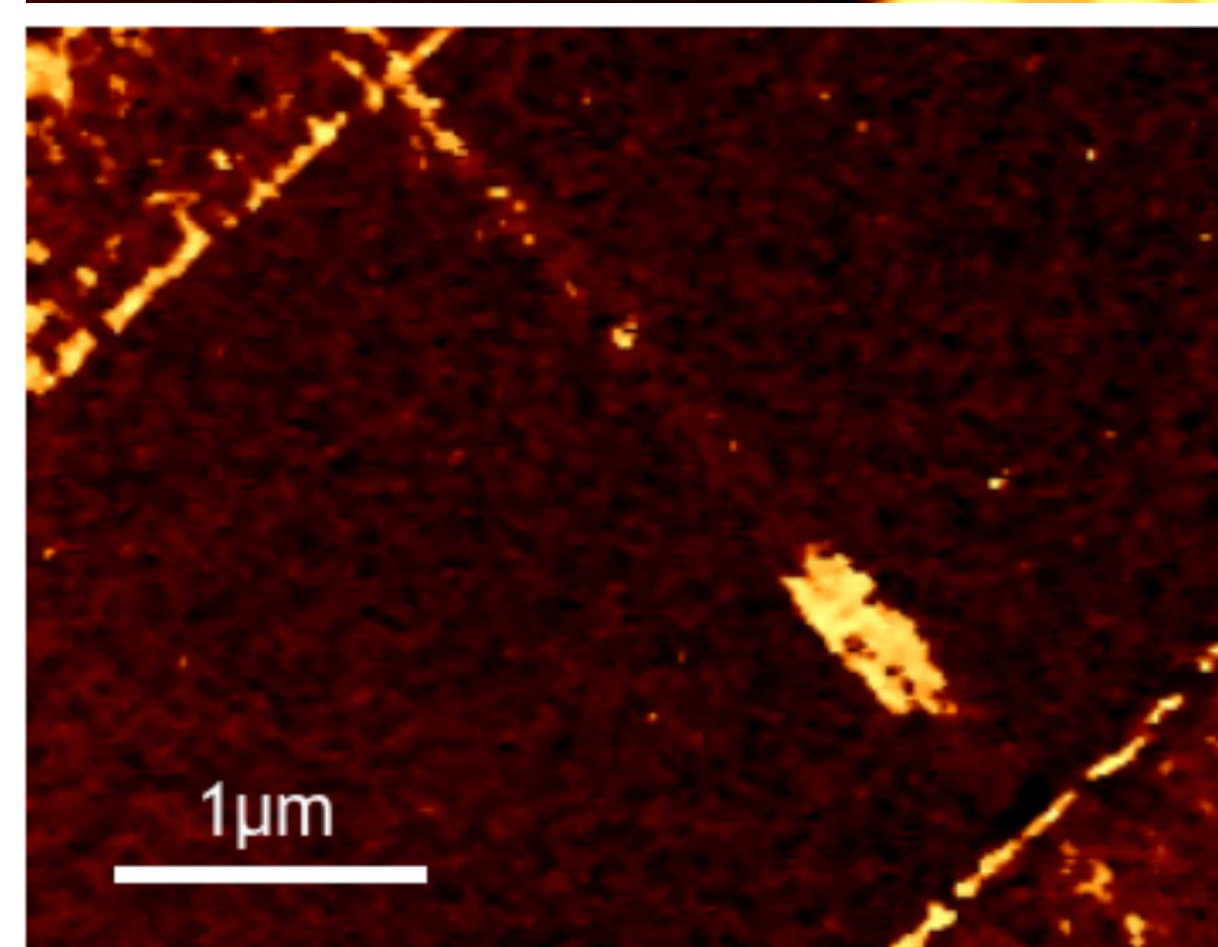
Here we fabricate and characterize SiGe nanowire transistors with an n-p-n doping profile and with a top gate covering only the p-doped section of the nanowire.

The current-voltage characteristics for a series of transistors with varying gate positions reveal that the on/off ratios for electrons is the highest when the gated p-type section is closest to the source contact, whereas the on/off ratios for holes is the highest when the gated p-type section is closest to the drain contact.

Device Fabrication and Identifying the Junction Location

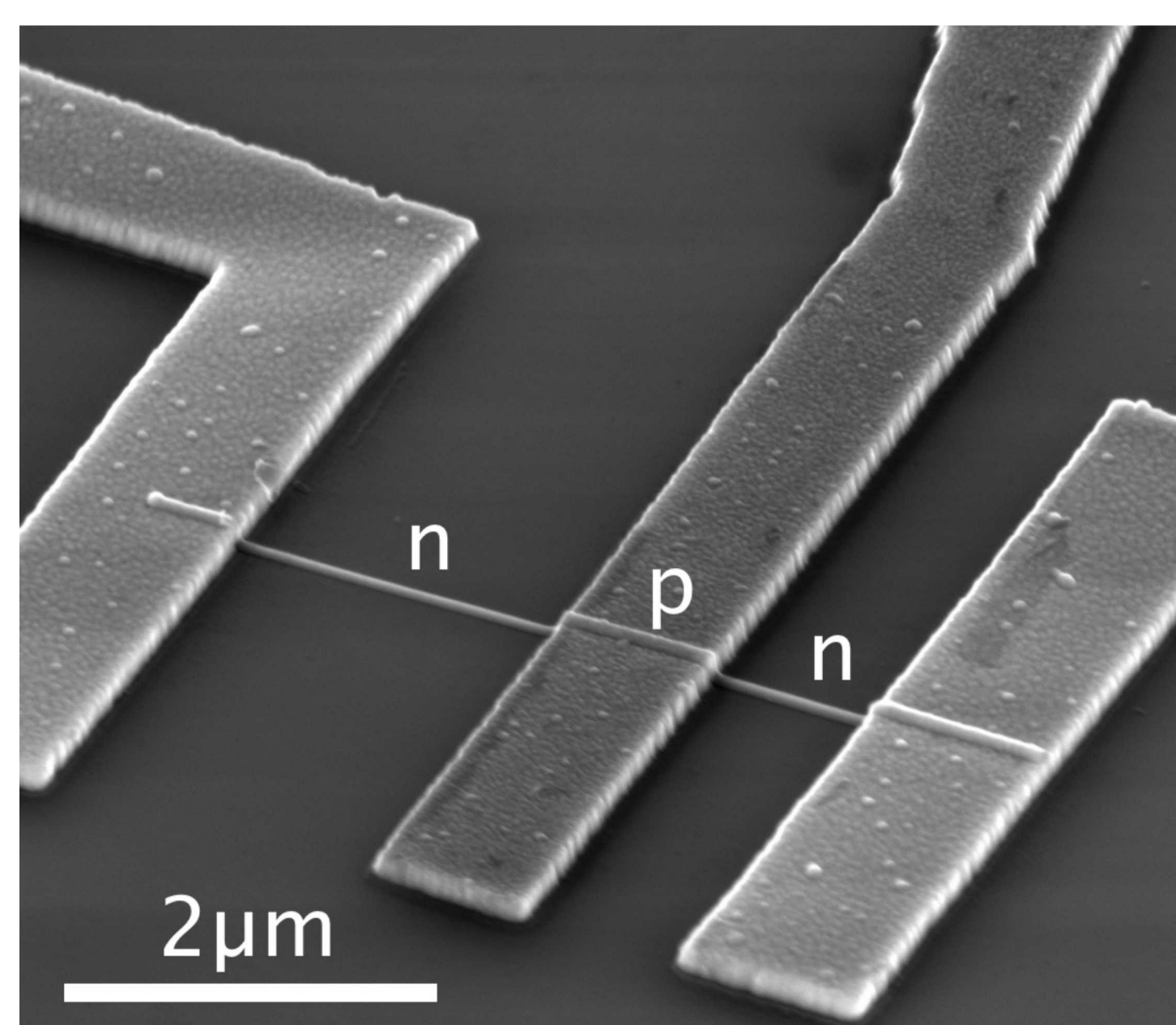


Atomic force microscopy height profile image of a typical n-p-n nanowire showing the wire channel clamped between two metal contacts.

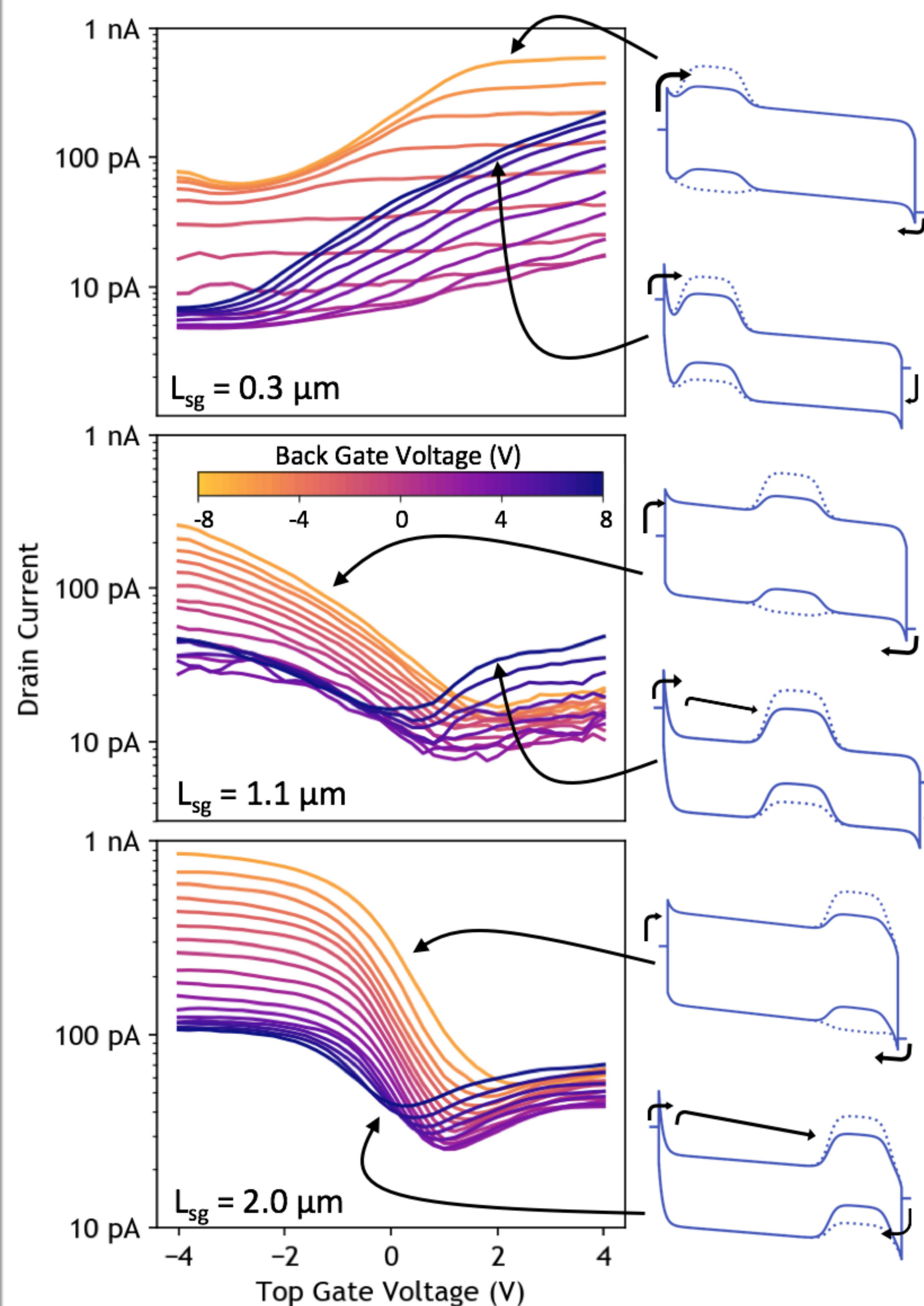


Scanning capacitance microscopy (dC/dV amplitude) image where the brighter region along the wire corresponds to the p-type segment.

SEM image of a completed device with a top gate covering the p-type section. The exposed, n-type sections of the nanowire represent the source-to-gate length and drain-to-gate length regions of the device.



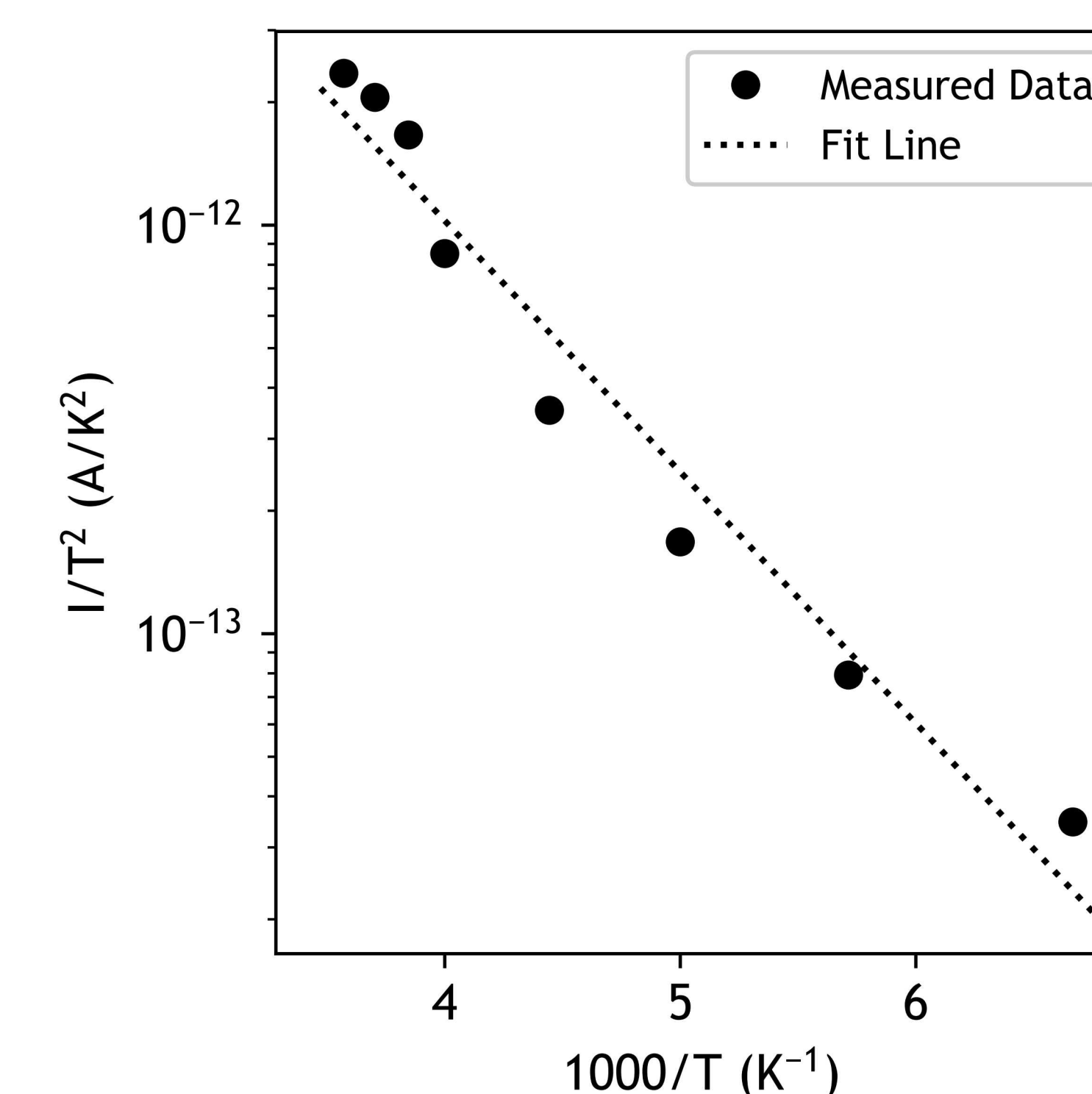
Current-Voltage Transport Characteristics



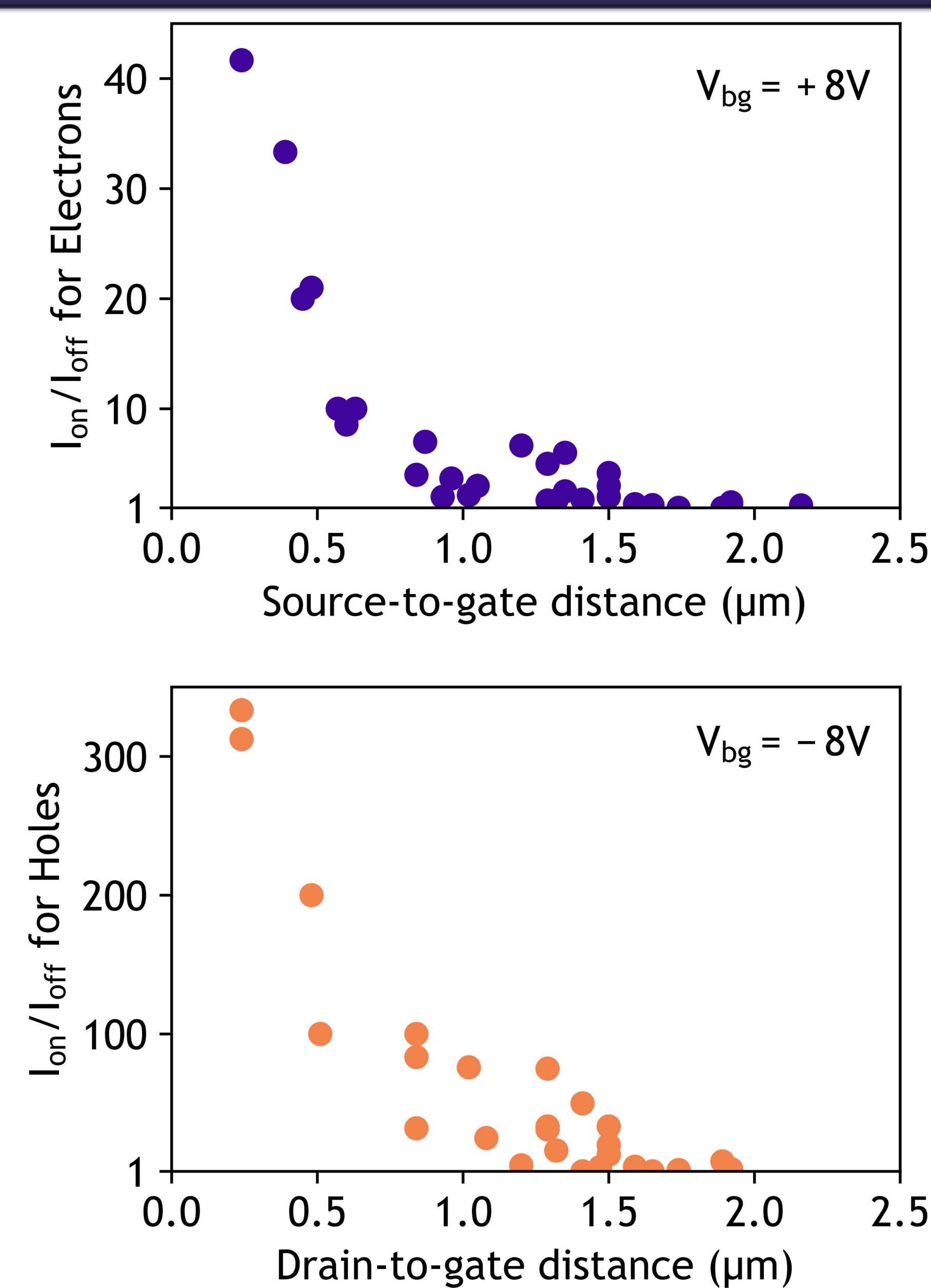
I-V curves and qualitative band diagrams as a function of source-to-gate length (measured from the edge of the source contact to the edge of the gate contact) for three representative devices. The dashed portions of the band diagrams show the bands prior to an applied voltage of the top gate. Back gate voltage values range from -8V (light lines) to +8V (dark lines) in 1 V increments, with $V_{ds} = 1$ V.

Schottky Barrier Height Extraction

We performed low-temperature I-V measurements down to 77K and constructed a Richardson plot, which indicates a Schottky barrier height of 0.65eV for electrons.



On/Off Ratios for Electrons and Holes



On/off ratios for electrons (top) and holes (bottom) as a function of the top gate and p-type section position, with back-gate voltages of $V_{bg} = +8$ V and $V_{bg} = -8$ V for electrons and holes, respectively.

This work was performed, in part, at the Center for Integrated Nanotechnologies, an Office of Science User Facility operated for the U.S. Department of Energy (DOE) Office of Science. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. DOE's National Nuclear Security Administration under contract DE-NA-0003525. The views expressed in the article do not necessarily represent the views of the U.S. DOE or the United States Government.

IEEE ELECTRON DEVICE LETTERS, VOL. 40, NO. 5, MAY 2019

SAND number TBD

