SAND2017-6446C

Loss of Utility Detection Capabilities for Today's Utility Interconnected Photovoltaic Inverters

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***Abstract* — The level of installed photovoltaic (PV) generation has surpassed 35 GW in the United States and the solar penetration continues to increase at a high rate. Almost all installations up to now rely on utility interconnection requirements based on 2003 standards, which made distributed energy resources (DER) devices sensitive to perturbations on the utility, would quickly disconnect, and would not provide utility support when most needed. This is changing, and to minimize adverse effects on the performance of electrical power systems, PV inverters must implement voltage and frequency ride-through capabilities and provide voltage and frequency support features. These new utility support requirements have caused renewed concern of loss of utility capabilities of PV DER devices. This paper focuses on revisions to the utility interconnection requirements and investigates the impacts of these changes on the islanding detection capabilities of PV inverters.**

***Index Terms* — anti-islanding, distributed energy resources, photovoltaics**

I. Introduction

Utility scale photovoltaic (PV) plants drove the total installation for Q3 of 2016 to 4.1 GW and presently over 35 GW of PV based distributed energy resources (DER) has been installed in the United States [1]. Virtually all of the utility interconnected PV systems installed in the continental United States are systems that adhere to IEEE 1547-2003 [2] or IEEE 1547a-2014 [3] utility interconnection standard requirements. To sustain a high level of PV installations, future systems will have to minimize adverse impacts on the grid through voltage and frequency ride-through capabilities and voltage and frequency support functions.

The governing IEEE P1547 [4] utility interconnection standard and the IEEE P1547.1 [5] testing standard are undergoing full revisions, and these revisions are incorporating all of the new electrical power system (EPS) voltage and frequency ride-through capabilities and support functions. Fig. 1 shows the expansion of voltage and frequency limits that impact anti-islanding operation. These new voltage and frequency ride-through capabilities and regulating functions are needed to support the EPS. This also includes power quality, reclosure coordination, and loss of utility detection capabilities of today's DER.

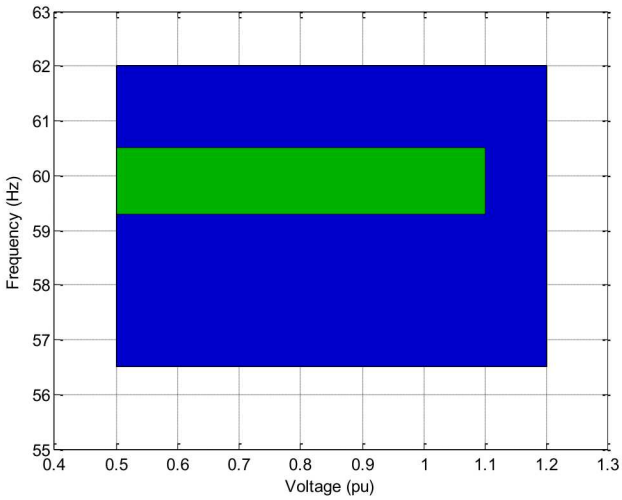

Fig. 1. Increased Voltage and Frequency Impact on Anti-islanding from IEEE 1547-2003 to P1547.

A. Methods of Anti-islanding

Some investigators are expressing concern that the new grid support functions may interfere with the detection of unintentional islands. This paper will focus on the anti-islanding detection requirement, type testing, and the aforementioned impact of grid support functions. The investigation will look into the methods [6] used to detect the loss of utility and prevent an anti-islanding event. It will also investigate how the anti-islanding test procedure of the draft IEEE P1547.1 has changed to account for the new EPS support capabilities, how these may affect the detection, and how long it takes for the DER to respond to the detection upon ceasing to energizing the utility.

B. Integrated Anti-islanding Methods

Anti-islanding techniques are commonly grouped into three categories: passive inverter-resident, active inverter-resident, and non-inverter-resident. These methods have been extensively reviewed and characterized [7-12].

- Passive inverter-resident methods utilize signal processing applied to the inverter terminal voltage, and possibly both the inverter voltage and current, to discern when an island

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or other abnormal grid condition has occurred. Nearly all inverters available today incorporate one or more passive methods, usually in conjunction with active methods. The primary advantages of passive methods are detection speed, low cost, general maintenance of effectiveness regardless of the number of inverters, and freedom from interference of one manufacturers' methods with another's. The primary disadvantage of passive methods is that it is very difficult to select their parameters to simultaneously achieve sensitivity and selectivity (i.e., all islands are detected, without false trips). Nearly all of these methods can be compromised if there are synchronous generators in the island. Examples of passive methods include:

  - Over/undervoltage and over/underfrequency
  - Phase jump detection or vector shift
  - Rate of Change of Frequency (RoCoF)
  - V/Hz relaying
  - Passive impedance detection based on cross-correlation
  - Detection of jumps in voltage THD, or voltage harmonic content at a specific frequency
  - Various forms of signal processing (e.g., wavelet analysis) looking for specific signatures that indicate island formation.

- Active inverter-resident methods involve the use of some deliberate perturbation of or injection into the inverter output current in order to create a condition during islanding that can be detected. Most, but not all, commercially-available inverters today use an active islanding detection method. As a group, these methods tend to be very effective with high selectivity and sensitivity in single-inverter cases, and many retain their sensitivity and selectivity in multi-inverter cases. The primary disadvantages of these methods are that they negatively impact grid stability and power quality, and their capability can degrade when more than one manufacturers' product is present in an island. Active methods are also compromised by the presence of rotating generation, although not as much as passive methods. Examples of active inverter-resident methods include:
  - Phase or frequency shift with positive feedback (e.g., Sandia Frequency Shift)
  - Positive feedback on voltage amplitude, usually triggered by a passive method (e.g., Sandia Voltage Shift)
  - Negative sequence current injection, with or without positive feedback
  - Various forms of Impedance detection, based on perturbation of current phase or magnitude, with or without positive feedback
- Non-inverter-resident methods. As the name implies, these are methods implemented outside the inverter. These methods typically involve one of two mechanisms: a) a change in circuit topology designed to disrupt generation: load balance in an island, or b) communications between the DER site and the grid. These methods tend to be highly effective and provide very good sensitivity and selectivity. Their primary disadvantages are cost and scheduling and logistical issues associated with the installation of the additional equipment, and in addition these methods are often relatively slow to respond. Examples include:
  - Change in circuit topology
    - Capacitor insertion/toggling
    - Grounding or shorting switches
  - Communications
    - Direct transfer trip (DTT)
    - Power line carrier permissive (PLCP)
    - Synchrophasor-based approaches

Table IV describes the most commonly-used methods and their susceptibility to degradation in effectiveness due to the implementation of EPS support functions.

II. Anti-islanding Procedure Changes

The anti-islanding capabilities of inverter based DER are evaluated utilizing a circuit intended to create a condition that minimizes any voltage and frequency shift when the EPS is disconnected. For this to occur, active and reactive power from loads and from generation must be equal and set to resonate near 60 Hz. The islanding test configuration can be connected in either a wye-connection or a delta-connection. If the device under test (DUT) does not require a delta connected load, then it is suggested that the loads be connected in a wye-connected configuration. This configuration will minimize a voltage shift due to the "islanded" circuit not being referenced, which can lead to a false positive where the DUT responds correctly by ceasing to energize the utility or simulated utility in the specified response time, but it does so due to a misaligned circuit load value or a circuit that is not referenced and the voltage symmetry was insufficient to sustain the island. This type of condition may indicate that the DUT ceases to energize the utility but not because the anti-islanding algorithm was sufficient to detect the island condition.

The RLC circuit setup requires several steps to achieve an adequately tuned circuit. The existing test sequence to IEEE 1547.1 requires adjustments to the loads for a proper setting that minimize changes in voltage and frequency the moment the utility is removed. Fig. 2 shows the new RLC islanding circuit that has been introduced. This version has more detail and distinguishes between the types of systems under test and the load configurations. By default, the load configuration will be wye-connected to minimize uncertainty of unbalanced voltages causing a false positive. This test configuration circuit now has the detail needed to ensure the loads remain referenced during the opening of the utility switch (S3) which simulates the loss of the utility.

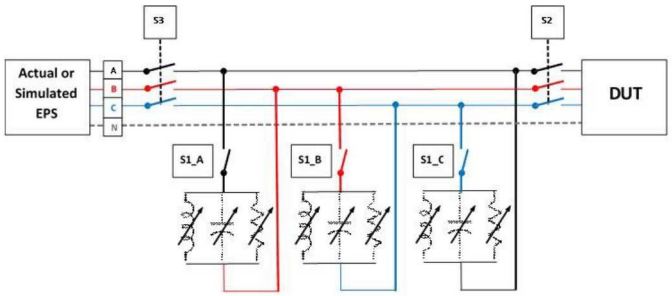

Fig. 2. Wye-connected RLC anti-islanding test circuit.

A. Existing method of RLC Anti-islanding Test Procedure

The test procedure requires that the RLC islanding test be conducted at matched conditions, where the inductance and the capacitance are both set to resonate at 60 Hz and the amount of reactive load equals the active power of the inverter, which will equate to a Q factor close to 1. The resistive load is set to absorb as much power as the DUT is producing. The test procedure then requires up to a ±5% reactive power imbalance in 1% increments. After the 11 tests are conducted from the previous setup, the results are reviewed, and the 1% load setting that yielded the three longest trip times shall be subject to two additional iterations. If the longest run-on times are not consecutive, an additional two iterations are conducted for the nonconsecutive settings in between. For the new version of IEEE 1547.1, it is under consideration to perform the tests at two power levels (95% and 25%) instead of three (100%, 66%, and 33%). Table I shows the number of iterations per power level.

TABLE I
TEST ITERATIONS PER POWER LEVEL

Test condition	Number of tests
Matched	1
Mismatch 1% to 5%	5
Mismatch -1% to -5%	5
3-longest run on times	3
Total number to tests per power level.	14

A test matrix of DER operating conditions has been created to evaluate the DER while operating under different voltage and frequency regulating functions. Table II shows the test conditions that the anti-islanding test procedure should cover to fully assess the capabilities of the DUT. Some of the newly-mandated grid support function capabilities, such as specified power factor, volt-var, and specific reactive power, must be tested independently. Therefore a new sequence of testing is required for each of the functions.

TABLE II
TEST CONDITIONS FOR ANTI-ISLANDING TESTING

Test condition	Functions active during Anti-islanding Test
1	IEEE P1547 default settings
2	SPS, RR, FW
3	VV, RR, FW, VW
4	Watt-Var, RR, FW, VW
5	SVar, RR, FW, VW

Table legend: SPS- specified power factor, RR- ramp rate, FW- frequency-watt, VV- volt-Var, VW- volt-watt, CVar- commanded-Var

This will bring the total number of anti-islanding tests for an EPS supporting DER too approximately: 14 x 2 x 5 = 140 tests. This is a high number of tests that comes at a significant cost when the product is being developed and when the product is undergoing certification. However, there is an alternative.

B. Introduction of New Concise RLC Anti-islanding Test Procedure

Recent changes to the draft anti-islanding test procedure of IEEE 1547.1 will introduce an alternative method for evaluating the loss of utility detection of DER connected to the Area EPS. Part of the reason for the high number of tests with the traditional procedure is that the test sequence sweeps the RLC load parameters over a range in order to find the worst-case condition for the device. The alternative test procedure enables determination of this worst-case condition in fewer steps via the intermediate step of disabling the anti-islanding detection algorithm. The test utilizes a properly tuned RLC circuit that will allow the DER to intentionally island and demonstrate that the RLC circuit has been tuned correctly such that the DER, *with the anti-islanding algorithm disabled*, will have a run-on time longer than the 2 second requirement. Ideally, the DER will run-on long enough for the RLC circuit to be adjusted for a perfect 60 Hz resonance and the power generated-to-resistive load match is close enough to minimize the voltage to change when the utility is removed. The following steps show the procedure for disabling the anti-islanding algorithm:

a) Set all DUT input source parameters to the nominal operating conditions and for the DUT to operate at 95% (+/- 5%) of rated output power in maximum power tracking mode.
b) Set (or verify) all DUT parameters to the default 1547 settings. Grid support functions are set to test condition 1 shown in Table II.
c) Set the actual or simulated EPS to the DUT nominal voltage +/- 5% and frequency.
d) Record all applicable settings.
e) Close switch S1, switch S2, and switch S3, and wait until

the EUT settles at the desired power level.

f) **Disable** the anti-islanding function in the DUT.

g) Open switch S3 and verify that the test setup will support a sustained island and continue to operate for at least the required anti-islanding clearing time.

h) Repeat steps e) through g) for a total of three tests, with each test having a run-on time at least the required anti-islanded clearing time.

i) **Enable** the anti-islanding function in the DUT

j) Close switch S1, switch S2, and switch S3; re-enable operation of the EUT and wait until the EUT settles at the desired power level.

k) Open switch S3 and record the time between the opening of switch S3 and when the DUT ceases to energize and trips, thus de-energizing the test circuit.

l) Repeat steps i) and k) for a total of three tests at this power level.

This test sequence substantially reduces the number of tests while still providing a rigorous type-test of the inverter's anti-islanding method. The new anti-islanding test requirements shown in Table III provide an indication of the number of tests required for this concise anti-islanding test procedure.

TABLE III
NEW ANTI-ISLANDING TEST REQUIREMENTS

Anti-islanding algorithm status	Number of tests
disabled	3
enabled	3

The tests will be conducted at the same two power levels (95% and 25% of rated power). The tests will be conducted with the same EUT operating conditions as presented in Table II. This will bring the total number of anti-islanding tests for an EPS supporting DER to approximately 6 x 2 x 5 = 60, which is less than half the number of tests required under the present test procedure.

The following data show the test results obtained with the anti-islanding algorithm disabled and with it enabled. For each test, the test conditions are identical except for the status of the anti-islanding algorithm.

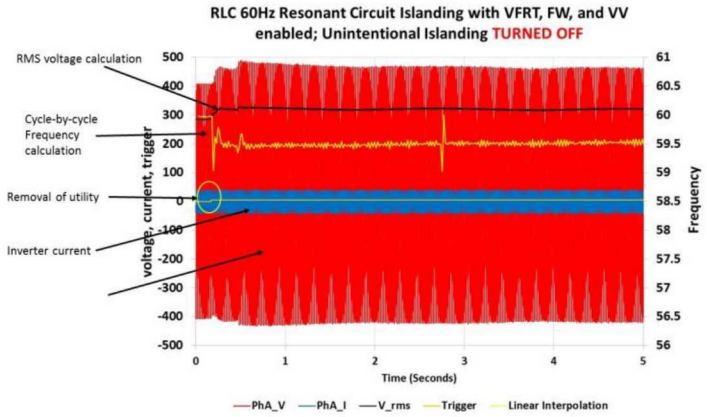

Fig. 3. UI test with algorithm "OFF" demonstrates continuous run-on.

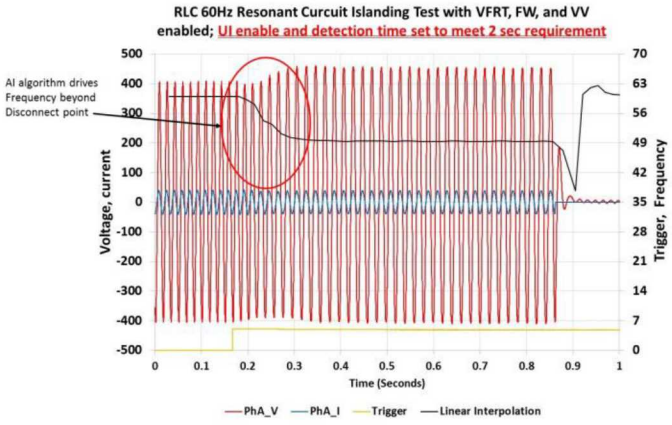

Fig. 4. UI test with algorithm "ON" demonstrates DUT detects loss of utility and ceases to energize within 2 seconds.

C. Introduction to Communication Based Anti-islanding

This anti-islanding test procedure evaluates the DUT's response to permissive signal removal. This test requires the DUT to be operating at rated power. Since EPS support functions do not adversely affect the detection and response time of the DUT to the loss of the permissive signal, there is no need to evaluate using the different operating modes in Table II and at different power levels. The test procedure is simple and only requires the interruption of the permissive signal and documenting the response of the DER. Fig. 5 shows the simplicity of the connection and that this test procedure

TABLE IV
ANTI-ISLANDING METHODS, CHARACTERISTICS, AND SUSCEPTIBILITY TO CHANGES IN PROCEDURE

Power electronic devices		
Method	**Characteristic**	**Susceptibility to EPS support functions**
RoCoF	Commonly-used passive method; trips the inverter when df/dt breaches a threshold	Will be strongly negatively impacted by new ride-through requirements
impedance	Detection with positive feedback	Minor reduction in effectiveness
Impedance	Detection without positive feedback	Minor reduction in effectiveness
Sandia Frequency Shift	implemented as phase or frequency injection	Increase in non-detection zone
perturbation	Feedback on negative sequence current	Increase in non-detection zone
Communication-Based Anti-islanding Methods		
Direct Transfer Trip (DTT)	Opening of utility breaker or isolation device Cost is obstacle unless large installation	No measurable reduction in effectiveness
Power Line Carrier Permissive (PLCP)	Opening of utility breaker or isolation device cost is issue, requires utility commitment	No measurable reduction in effectiveness
Synchrophasor	Several variants, each requiring a utility-supplied reference signal. Cost is issue, requires utility commitment	No measurable reduction in effectiveness

doesn't require any load configurations nor interrupting the actual power flow from the DUT, but the DUT is required to respond to loss of permissive signal and stop energizing the EPS within the required two seconds.

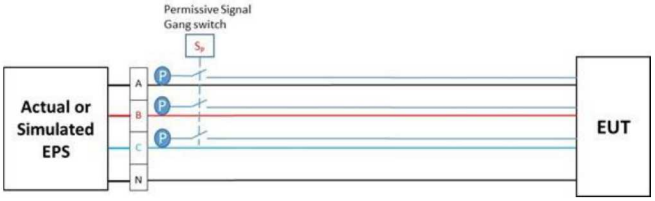

Fig. 5. Permissive signal Anti-islanding Test Configuration.

III. POWER BALANCE REQUIREMENTS

In order for a sustained island to exist, both active and reactive power must be balanced between the aggregate generation and load within the island circuit. Once the utility is disconnected from a section of an EPS, there is nowhere else that power and energy can flow except within the island. It is *after* the island has formed that the powers must be exactly balanced. In the instant just prior to the formation of the island, the degree to which the powers are balanced affects whether a sustained island is possible. In this context, a sustained island is a case where the generation continues to energize the circuit beyond the two second time limit from IEEE 1547.

PV inverters can be approximated by a constant-current model during early stages of an event and by a constant-power model over longer time periods. During the constant power period, the island voltage can be computed as:

$$V_{Island} = V_{EPS}\sqrt{P_{Gen}/P_{Load}} \quad (1)$$

During the constant current period, the island voltage can be computed as:

$$V_{Island} = V_{EPS} \times P_{Gen}/P_{Load} \quad (2)$$

where V_{EPS} is the EPS voltage just prior to formation of the island. P_{Gen} is the aggregate active power generation just prior to formation of the island. V_{Island} is the steady state voltage that the island will stabilize at if the DER does not trip based on voltage or frequency trips or anti-islanding protections. P_{Load} assumes that the aggregate load can be modeled as a resistance, R_{Load}, and is measured just prior to formation of the island.

$$P_{Load} = {V_{EPS}}^2/R_{Load} \quad (3)$$

A similar equation can be used to estimate island frequency by looking at the reactive power balance.

$$F_{Island} = F_{EPS}\sqrt{(Q_L + Q_{Lder})/(Q_C + Q_{Cder})} \quad (4)$$

where F_{EPS} is the EPS frequency just prior to formation of the island. Q_L and Q_C are the reactive powers of the inductive and capacitive loads within the island circuit, also measured just prior to formation of the island. Q_{Lder} and Q_{Cder} represent the reactive power output of the DER and presume constant reactive power operation of the DER before and after formation of the island (a presumption that is being tested at this time).

These equations do not predict the transient response of the system immediately after formation of an island, but it is expected that well behaved DER and island loads will quickly reach steady state equilibrium. These equations also do not

take into account non-idealities of load components such as change in resistance as power level changes, change in capacitance or in inductance with change in voltage, or harmonic currents of magnetic components. The equations are only intended to model the fundamental frequency first order effects.

The quality factor equation from IEEE 1547.1-2005 is modified now to include the reactive power components of the DER:

$$QF = \frac{\sqrt{(Q_L + Q_{Lder}) \times (Q_C + Q_{Cder})}}{P_{Load}} \qquad (5)$$

IEEE 1547-2003 voltage trips that were faster than two seconds range from 0.50 to 1.10 pu. If the island voltage exceeded these limits, the generation would trip on voltage and shutdown before the two second island protection limit. The frequency trips for small generation, less than 30 kW, were fast, 0.16 seconds, at 59.3 and 60.5 Hz. The frequency trips for larger generation could be set as wide as 57.0 to 60.5 Hz.

IEEE P1547 Draft 6 ensures a fast, 0.083 second, voltage trip at 1.20 pu, and momentary cessation at 0.50 pu. The frequency trips range from 56.5 and 62.0 Hz and are fast at 0.083 seconds.

IV. Summary and Future Work Needed to Complete Assessment

Much work has been conducted to group anti-islanding techniques into categories and simulations have been conducted to characterize the susceptibility of these different categories with the implementation of EPS support functions. Capabilities of DER according to the type of anti-islanding methods implemented into the device have undergone some laboratory validation experiments but more are needed to cover the multitude of combinations of categories and the matrix of operating functions.

Conducting laboratory experiments to exercise the new anti-islanding test procedures will continue and are needed to validate that the draft procedures are sufficiently robust and can assess the different types of anti-islanding categories and combinations of EPS support functions. Additional experiments will be conducted to document the variability in loads that can be tolerated and will maintain a load to generation balance that will allow the device under test to continue to operate and stay within the voltage and frequency operating ranges.

ACKNOWLEDGEMENTS

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

The authors would like to thank Jeff Zirzow, who provided much of the test data and Nicholas Gurule for providing the data analysis.

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