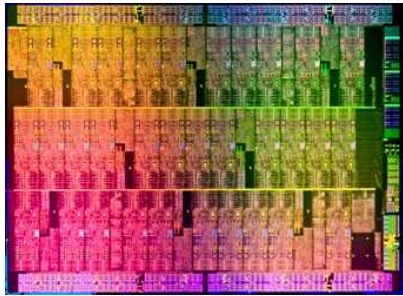# Emerging HPC Systems and Next Generation FE Engineering Analysis Applications

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Pacific Rim Workshop on
Innovations in Civil Infrastructure Engineering
National Taiwan University of Science and Technology
Taipei, Taiwan
January 9-11, 2013

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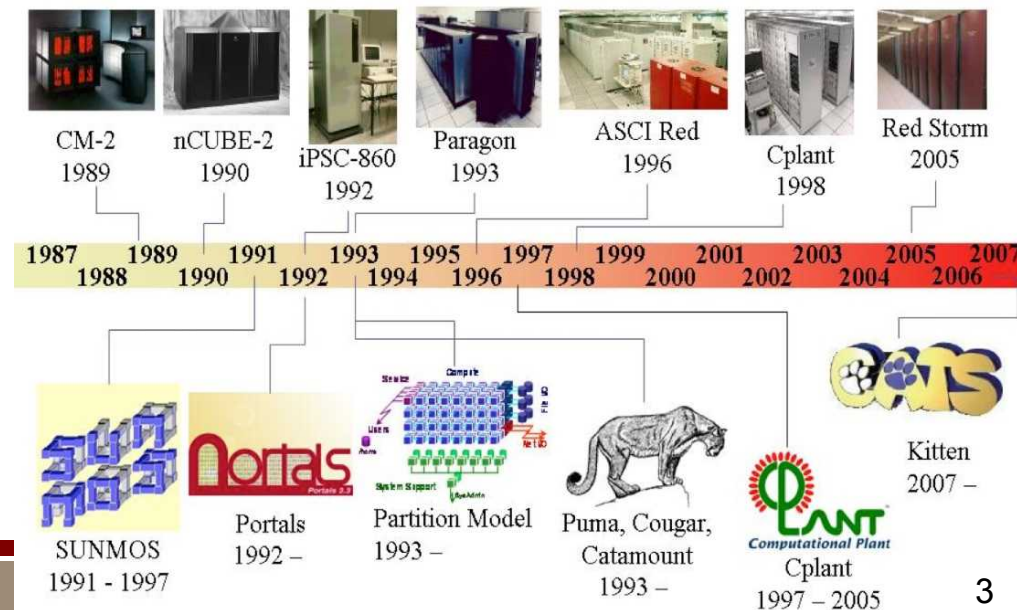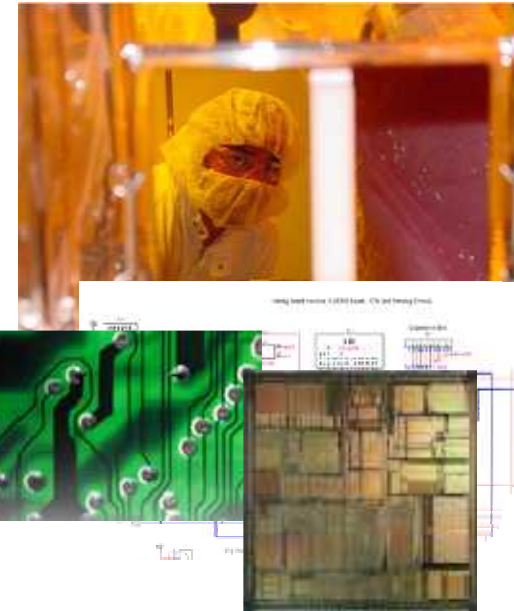
- **Sandia Uses HPC for Traditional Engineering Analysis Applications**
  - **Structural mechanics**
  - **Structural dynamics**
  - **Shockwave physics**
  - **Computational fluid dynamics, combustion, turbulence, heat transfer**
  - **Circuit simulations, device physics, materials science**
  - **Design Optimization, uncertainty quantification**

Sandia has Unique Capabilities for HPC Development

- Microsystems and Engineering Sciences Applications (MESA) Complex – sends more unique designs to IBM Trusted Foundry than any other institution
- Largest concentration of HPC computer architects outside of industry
- History of LWK operating system/runtime system software spans the MPP era
- Helped establish the MPPs with seminal work on bypassing the limits of Amdahl's Law with Weak Scaling

The MPP Era is likely on its last legs

Our goal is to help define the next paradigm for HPC
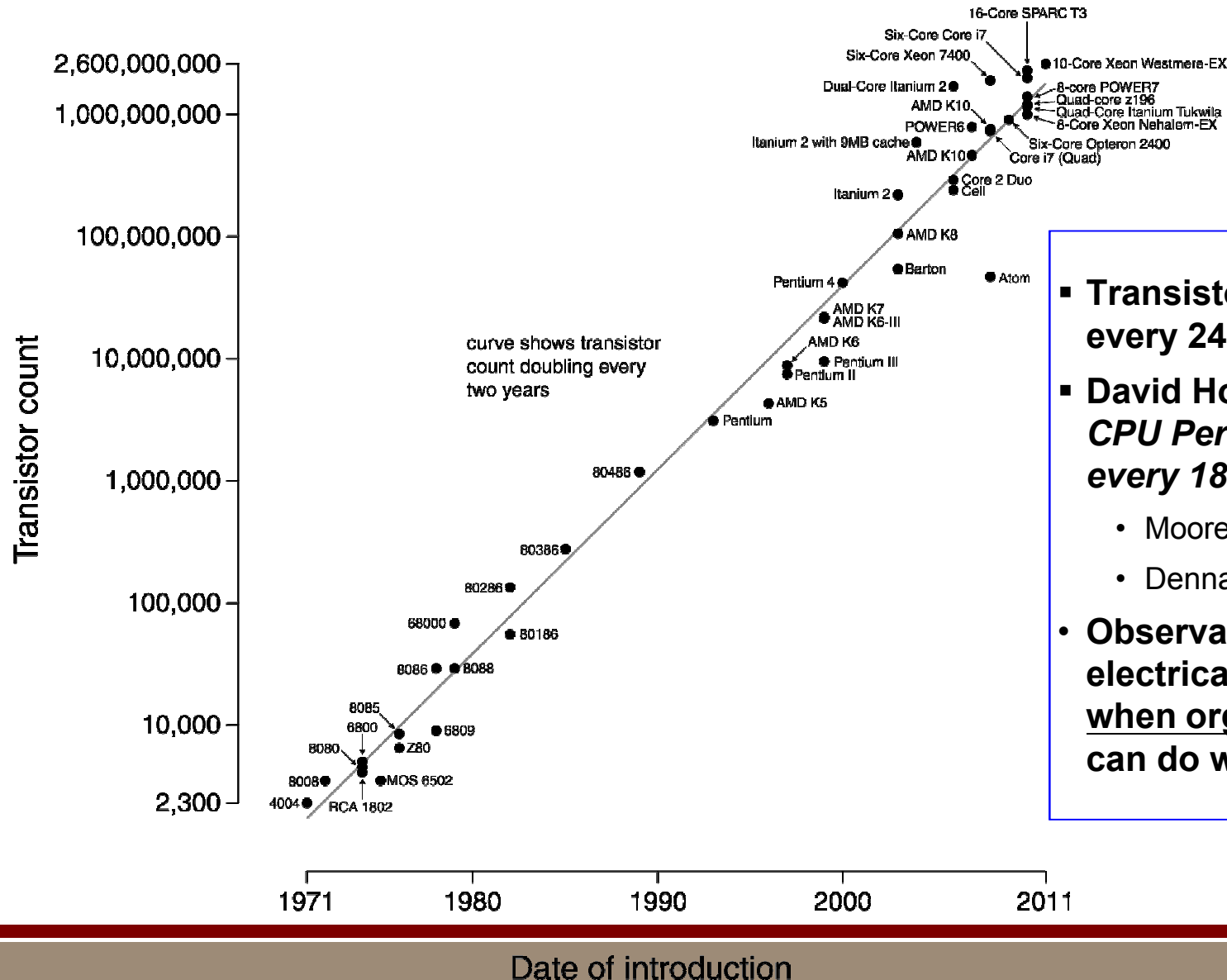

CM-2 1989
nCUBE-2 1990
iPSC-860 1992
Paragon 1993
ASCI Red 1996
Cplant 1998
Red Storm 2005

SUNMOS 1991 - 1997
Portals 1992 –
Partition Model 1993 –
Puma, Cougar, Catamount 1993 –
Computational Plant Cplant 1997 – 2005
Kitten 2007 –

Infrastructure versus Computers

- **Different Time and Length Scales:**

- **Infrastructure "Products"**
  - **Typical Design Lifetime is on the order of 40-50 years**
  - **Typical Sizes on the Order of 10^1 to 10^4 meters, but can me much larger, e.g. a Nation's Power Grid**

- **Computer "Products"**
  - **Typical Design Lifetime is ~4 years for a CPU, ~2 years for a GP-GPU or Cell Phone**
  - **Typical Sizes on the Order of 10^{-8} meters, as of 2012, feature sizes are 22nm = 2.2×10^{-8}**

Moore's Law 1971-2011:

Growth in Transistor Count

Transistor count (y-axis, log scale): 2,300 — 10,000 — 100,000 — 1,000,000 — 10,000,000 — 100,000,000 — 1,000,000,000 — 2,600,000,000

Date of introduction (x-axis): 1971 — 1980 — 1990 — 2000 — 2011

curve shows transistor count doubling every two years

Labeled points: 4004, RCA 1802, 8008, 8080, MOS 6502, 6800, 8085, Z80, 6809, 8086, 8088, 68000, 80186, 80286, 80386, 80486, Pentium, AMD K5, Pentium II, Pentium III, AMD K6, AMD K6-III, AMD K7, Pentium 4, Barton, Atom, AMD K8, Itanium 2, Cell, Core 2 Duo, Core i7 (Quad), Six-Core Opteron 2400, AMD K10, POWER6, Itanium 2 with 9MB cache, AMD K10, Dual-Core Itanium 2, Six-Core Xeon 7400, Six-Core Core i7, 16-Core SPARC T3, 10-Core Xeon Westmere-EX, 8-core POWER7, Quad-core z196, Quad-Core Itanium Tukwila, 8-Core Xeon Nehalem-EX

- **Transistor count doubles every 24 months**
- **David House, Intel:** *CPU Performance doubles every 18 months due to*:
  - Moore's Law
  - Dennard Scaling
- **Observation of what electrical engineers, <u>when organized properly</u>, can do with silicon**
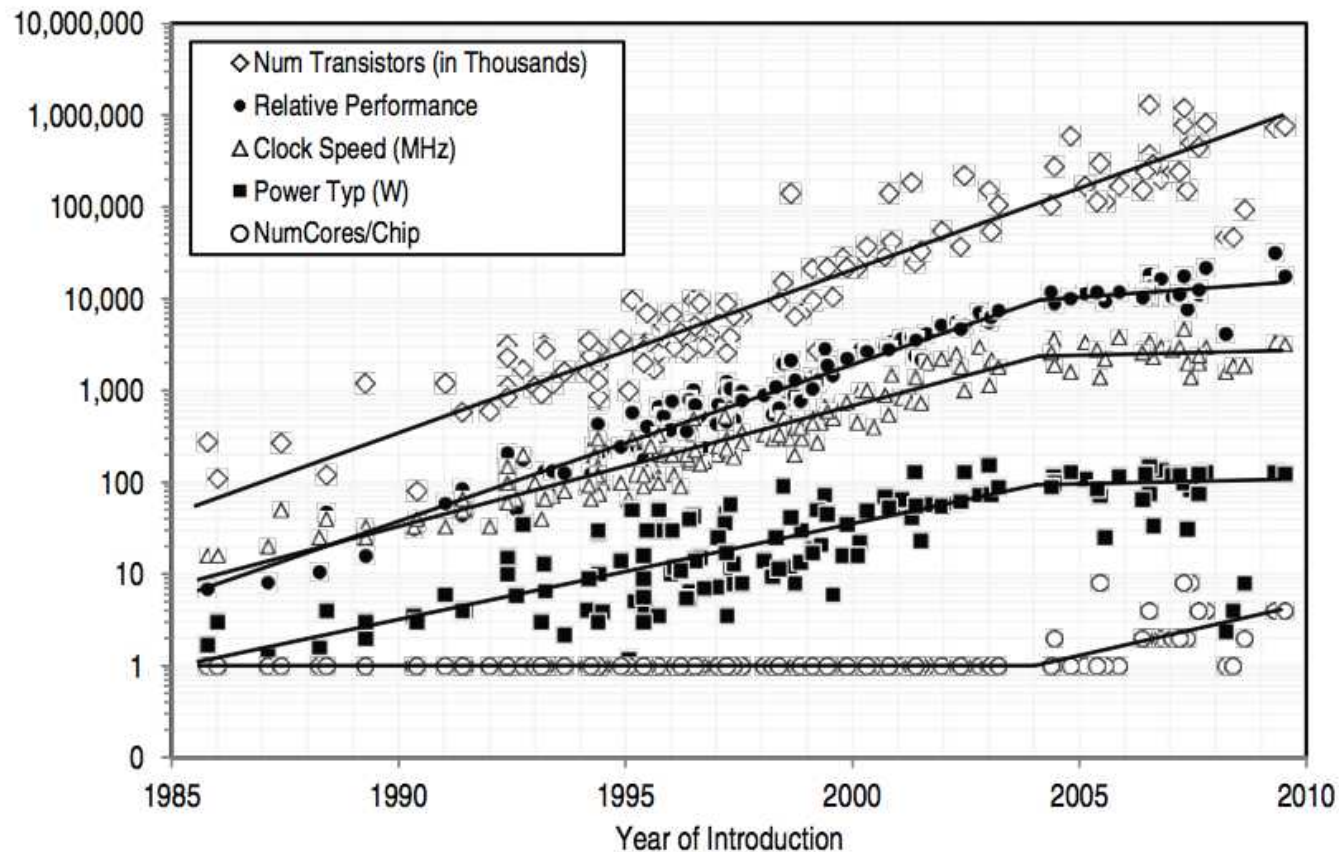
Moore's Law and the Loss of Dennard Scaling

FIGURE 2.1 Transistors, frequency, power, performance, and cores over time (1985-2010). The vertical scale is logarithmic. Data curated by Mark Horowitz with input from Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith, Chris Batten, and Krste Asanoviç.

The Future of Computing Performance: Game Over or Next Level, Samuel Fuller and Lynette Millet, Eds., National Academy Press, 2011

Classes of Computing Platforms

- **Workstations: SMP systems with ~4CPUs**
  - **Typical**
- **Cloud Computing**

- **Clusters and MPP Integrated Systems**
  - **Typical**
- **Advanced Architectures**

Cielo, the ASC Program's Capability Computing Platform

|	
Operational Time Frame	2011
Theoretical Peak Performance	1,374 TF
HPL (Linpack) Performance	1,110 TF using 142,272 cores
Cabinets	96
# Compute Nodes	8,944
# Compute Cores	143,104
Compute Processor	Dual AMD Opteron™ 6136 eight-core "Magny-Cours" Socket G34 @ 2.4 GHz
Compute Memory	286 TB DDR3 @ 1333 MHz
Compute Memory BW	763 TB/s
Service Nodes	272 AMD Opteron™ 2427 six-core "Istanbul" Socket F @ 2.2 GHz
External Login Nodes	Qty 4 Dell PowerEdge R815 Servers
User Disk Storage	7.6 PB User Available Capacity
Parallel File System	Cray DVS and Lustre
Parallel File System BW	~160 GB/s
High Speed Interconnect	Cray Gemini 3D Torus in a 16 x 12 x 24 (XYZ) Topology
Bi-section BW	6.57 x 4.38 x 4.38 (XYZ) TB/s
System Foot Print	~3,000 sq ft including Storage
Power Requirement	3,980 KW running HPL
Operating System	Cray Linux Environment
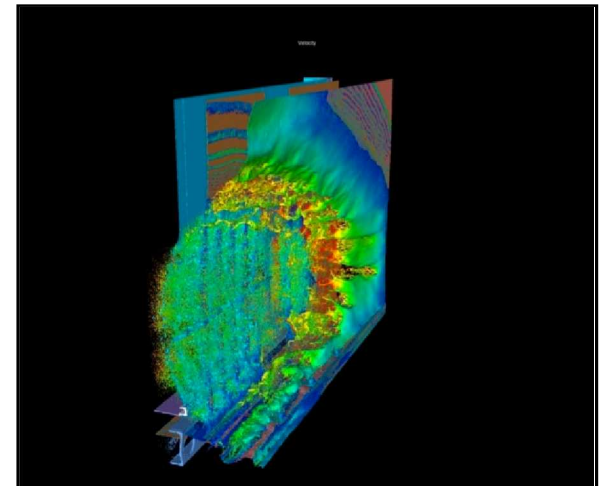
A 32,768 CTH simulation run on Cielo helps designers understand the response of structures under severe blast loading conditions

Engineering Analysis Applications vs Materials Science Applications

- Differences in demands on and requirements from computer architectures

- Materials Science applications can benefit from special purpose computer architectures, e.g. MD-Grape, MyAnton

- Engineering Analysis applications, e.g. Finite Element Mechanics, CFD, Combustion, Nuclear Reactor design Applications, etc. stress data movement local - memory, and global - interconnect

What is Different about Exascale?

- Exascale is ~ a decade out in time

- Exascale is ~ 5 Moore's Law generations out

- With this many generations of evolution, Exascale hardware can be radically different from Petascale hardware

- Given this longer time-frame we have an opportunity for true Co-design

- In contrast, if our focus was our 2015 system, hardware is largely locked in
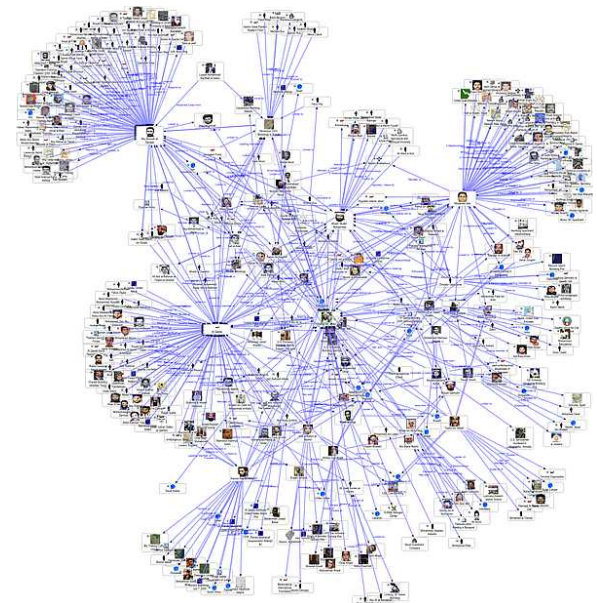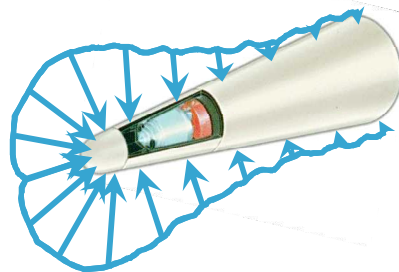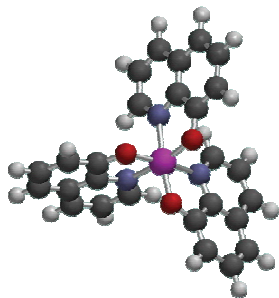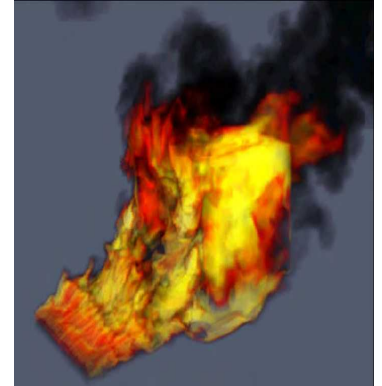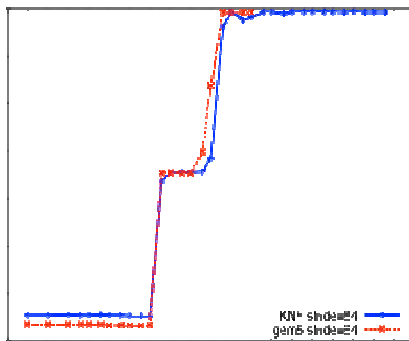
Define and Develop the Co-design Methodology for HPC
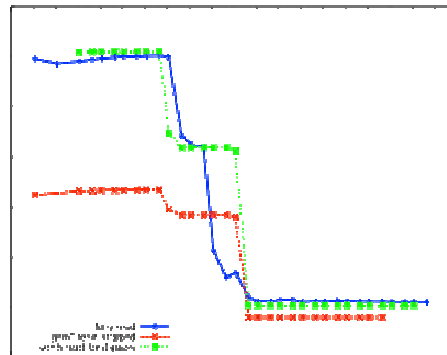
- **Key Co-design Capabilities**
  - Simulators
  - Proxy Applications
  - Agile system software
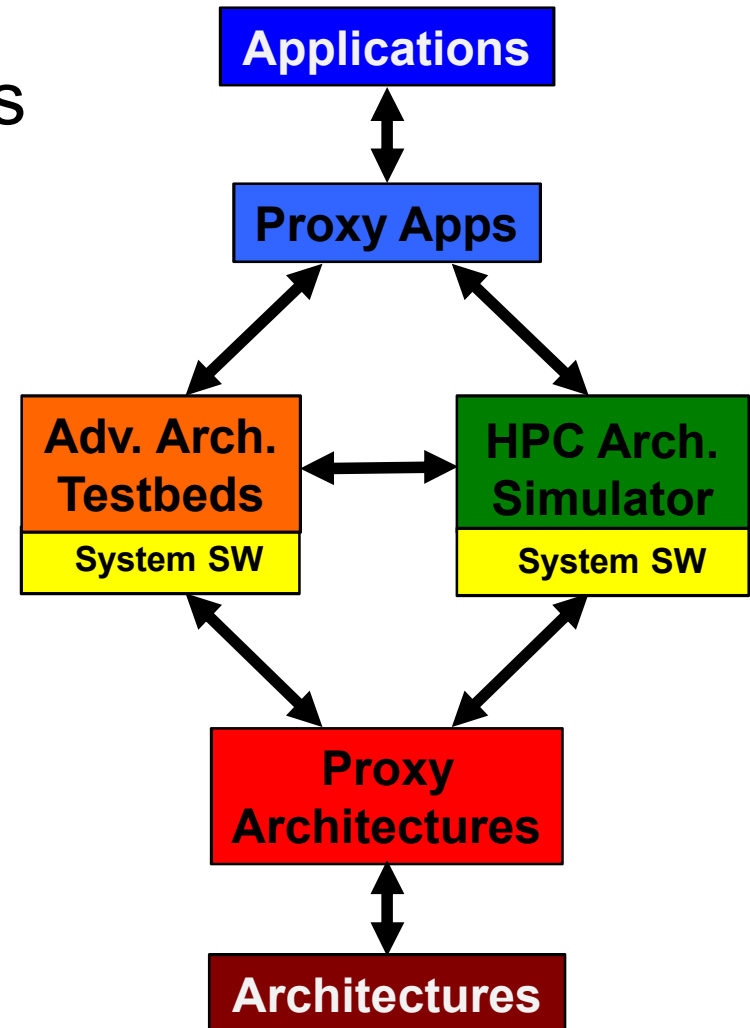 - Testbeds
  - Proxy Architectures

Latency

Bandwidth

Backup Slides

Applicability of Heterogeneous Architectures to our Application Portfolio

- ⑩ HPC community focused on heterogeneous architectures with COTS processors and accelerators to solve the energy/performance challenges; e.g. China's *Tianhe-1a*, ORNL's *Titan*
- ⑩ Future heterogeneous architectures will be more tightly integrated and have unified memory systems, but limited memory capacity and bandwidth & latency performance
- ⑩ We need to understand what fraction of our NW workload can use these heterogeneous architectures
  - ⑩ Likely good match for PEM and single physics applications; e.g. LAMMPS
  - ⑩ Likely poor match to EPIC applications with multiphysics; e.g. Reentry, Combustion
  - ⑩ Likely poor match to our Cybersecurity, Graph applications