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Redox transistors based on TiO_2 for analogue neuromorphic computing

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ABSTRACT

The ability to train deep neural networks on large data sets have made significant impacts onto artificial intelligence, but consume significant amounts of energy due to the need to move information from memory to logic units. In-memory "neuromorphic" computing presents an alternative framework that processes information directly on memory elements. In-memory computing has been limited by the poor performance of the analogue information storage element, often phase-change memory or memristors. To solve this problem, we developed two types of "redox transistors" using TiO_2 (anatase) which stores analogue information states through the electrochemical concentration of dopants in the crystal. The first type of redox transistor uses lithium as the electrochemical dopant ion, and its key advantage is low operating voltage. The second uses oxygen vacancies as the dopant, which is CMOS compatible and can retain state even when scaled to nanosized dimensions. Both devices offer significant advantages in terms of predictable analogue switching over conventional filamentary-based devices, and provide a significant advance in developing materials and devices for neuromorphic computing.

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ACRONYMS AND DEFINITIONS

Abbreviation	Definition
RRAM	Resistive Random Access Memory
OVRT	Oxygen vacancy redox transistor
MIEC	Mixed ionic and electronic conductor
CMOS	Complementary metal oxide semiconductor
$V_O^{\cdot\cdot}$	Oxygen vacancies
YSZ	Yttrium-stabilized zirconia
OCV	Open-circuit voltage
V_W	Write voltage
V_{th}	Threshold voltage
mV	Millivolt
CMOS	Complementary metal oxide semiconductor
V_R	Read voltage
V_{REF}	Reference voltage
RF	Radio frequency
DC	Direct current
eV	Electron-volt

1. INTRODUCTION

The ability to train deep neural networks on large data sets has significantly improved artificial neural networks and artificial intelligence[1], with diverse applications including autonomous vehicles, materials discovery, and medical diagnostics. One significant limitation of deep neural networks is high energy consumption owing to the need to shuttle enormous quantities of data between memory and processor in conventional digital computing architectures[2] which are not optimized for data-intensive operations. In-memory "neuromorphic" computing presents an alternative framework that reduces power consumption by processing information in parallel directly on non-volatile analogue resistive memory elements[3–5]. The analogue information states are stored as the analogue electronic conductances of memory elements, and energy-intensive multiply-and-accumulate matrix operations are conducted in parallel within a crossbar array using Ohm's Law and Kirchoff's Law. System-level energy analyses[2,6,7] suggest that in-memory computing using crossbars will consume as few as 10^{-14} Joules per multiply-and-accumulate operation, hundreds of times more efficient than the best digital approaches.

In-memory computing architectures for both inference and training deep neural networks have been proposed[7,8] and experimentally realized[6,9–13]. These systems are limited by the unpredictability of the analogue non-volatile resistive memory[14–16] element, or artificial synapse, at the heart of the technology. Non-volatile memory including resistive memory[5,14–16], phase-change memory[7,17,18], flash memory[19,20], and ferroelectric memory[21,22] have been investigated. However, none have been able to meet the necessary requirements and integrated into a large, energy-efficient crossbar array.

The goal of this LDRD is to explore the use titanium dioxide in three-terminal redox transitors memory cells as artificial synapses in neuromorphic computing. As will be described later, redox transistors are a three-terminal memory device that stores analogue information states using the concentration of ions in a host material.

1.1. Two-terminal resistive memory

Most work on in-memory neuromorphic computing has utilized two-terminal resistive random access memory (RRAM). In these memory devices, analogue resistance information states are stored as point defects within a nanosized filament[14–16]. Devices with cation defects like copper or silver are termed conducting-bridge random access memory or electro-chemical metallization memory [23–27], while devices with anion defects (typically oxygen vacancies) are termed valence-change memory[14] or simply RRAM. An applied voltage between the top and bottom contacts results in joule heating and defect migration. In valence-change memory, long information retention arises from a high activation energy for defect mobility (typically >1 eV), which makes these defects and resulting information state frozen at room temperature. High write speeds can be achieved from internal joule heating to temperature as high as 800K in the filament when oxygen vacancies are over 10^{10} times more mobile assuming an Arrhenius activation energy of 1 eV [28]. Due to these advantages, most experimentally-realized crossbar arrays for in-memory computing utilize resistive memory[6,9–13].

Despite intense research over the past two decades, RRAM suffer from stochastic, nonlinear, and unpredictable switching[29–31]. Because joule heating is localized near the filament, only the oxygen vacancies in and near that filament are mobile. As a result, analogue states are stored in *discrete* numbers of defects in the filament, which can be as small as 2 nm[32]. Due to kinetic theory, discrete atoms are probabilistic and intrinsically stochastic; as a result, filament-containing resistive memory also switch stochastically and irreproducibly between cycles[29–31,33–35]. Non-reproducible switching present immense challenges for analogue memory, which necessitate the ability to accurately distinguish

between neighboring analogue resistance states. State-of-the-art analogue RRAM show that only ~60% of switching attempts even change the resistance state in the correct direction[6,10,25,36], slightly better than random (50%). Training is even more difficult, and energy-efficient training may not be feasible for filamentary RRAM devices.

1.2. Three-terminal redox transistors

Due to the challenges of controlling memristive filaments, many researchers have recently investigated three-terminal redox transistor. A similar concept was originally proposed by Widrow in the 1950s[37] and includes several related implementations over the decades[38]. However, recent innovations in solid-state batteries, fuel cells, and organic electrochemical transistors have reignited interest and technological development into redox transistors[39–48]. They use a variety of materials, including lithium transition metal oxides, 2D materials, and electroactive polymers. This work specifically builds three-terminal redox transistors using TiO_2 (anatase) metal oxides.

1.3. Titanium Oxide

TiO_2 (anatase) is a transition metal oxide that serves as the main material of interest in this work. Because redox transistors are based on the insertion of ions, TiO_2 can serve as a host for both lithium ions[49] and for oxygen vacancies; this document will report on the use of TiO_2 for both those ions. For the lithium ion version (section 2), the key innovation is the reduction in the electrochemical voltage to near-zero as a result of fast ion transport and the elimination of the open-circuit voltage. For the oxygen vacancy version (section 3), the key innovation is the use of CMOS compatible materials with long retention times due to an intrinsic energy barrier. Both versions have lower electrochemical write energies than RRAM due to the absence of internal joule heating.

The electronic structure of TiO_2 is a wide bandgap semiconductor with a bandgap above 3 eV. However, it can be intrinsically doped with oxygen vacancies[50], as well as extrinsically with materials like lithium[51]. Both oxygen and lithium are n-type dopants which increase the carrier concentration and electronic conductivity, which will be used to store analogue information states in redox transistors. In both cases, electrons that are donated by lithium or by oxygen vacancies are localized onto the Ti site as Ti^{3+} or, in Kroger-Vink notation, as Ti'_{Ti}. The electronic structure is complex, but it is generally believed that these form large polarons[52]. While most electronic devices typically seek high conductivity, in the case of neuromorphic computing we seek lower conductivity in order to minimize the read currents and to enable the fabrication of larger crossbar arrays[53].

1.4. Published works

Three peer-reviewed papers were published or, at the time of this document, submitted for publication, and a fourth one under preparation. They are:

1) Y. Li, E. J. Fuller, S. Asapu, S. Agarwal, T. Kurita, J. J. Yang, A. A. Talin. "Low-voltage, CMOS-free synaptic memory based on Li_XTiO_2 redox transistors." *ACS Applied Materials Interfaces*, **11**, 38982-38992 (2019)[54]
2) Y. Li, J. van de Groep, A. A. Talin, M. L. Brongersma. "Dynamic tuning of gap plasmon resonances using a solid-state electrochromic device." *Nano Letters*, **19** 7988-7995 (2019)[55]
3) Y. Li, E. J. Fuller, S. Yoo, C. H. Bennett, D. S. Ashby, R. D. Horton, M. S. Bartsch, M. J. Marinella, W. D. Lu, A. A. Talin. "Filament-free resistive memory enables deterministic analogue switching." Submitted and under peer review at *Advanced Materials*[56]

2. LITHIUM INSERTION INTO TITANIUM OXIDE FOR LOW-VOLTAGE ELECTROCHEMICAL MEMORY

We first devise a lithium-based synaptic memory cell based on TiO_2 (anatase). This created the first inorganic redox transistor that uses the same material for both the gate and the channel, enabling no open-circuit, built-in voltage. Combined with a low-voltage selector switch, this device presents one of the lowest possible voltages for any memory technology, as low as 200 mV. Significant portions of this section was reprinted or adapted with permission from Y. Li, E. J. Fuller, S. Asapu, S. Agarwal, T. Kurita, J. J. Yang, A. A. Talin. "Low-voltage, CMOS-free synaptic memory based on Li_XTiO_2 redox transistors." *ACS Applied Materials Interfaces*. **11**, 38982-38992. Copyright (2019) American Chemical Society."

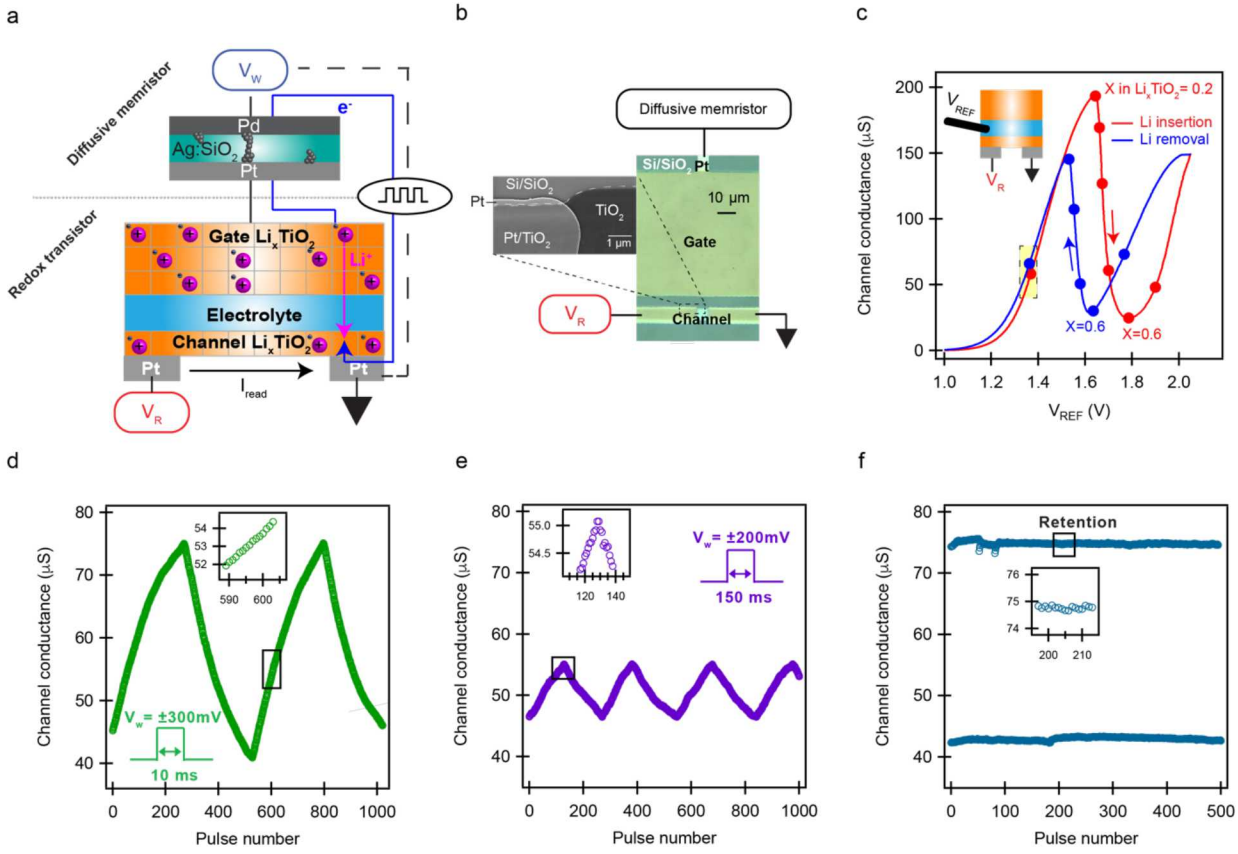

Figure 1 LixTiO2 electrochemical synapse. (a) Synaptic memory cell containing a Li_xTiO_2 redox transistor and a diffusive memristor selector. V_W is used to conduct weight updates by moving electrons and ions from the gate and the channel. V_R is used to read the conductance of the channel. (b) Optical image and scanning electron micrograph of the redox transistor. The suspended channel that is grown directly above the Si/SiO_2 substrate is 10×8 μm² in size. (c) The channel conductance as a function of the V_{REF} as we electrochemically insert and remove lithium from the channel using the $Li_{0.7}FePO_4$ reference electrode at a constant current of 1 nA. V_{REF} is the electrochemical potential of the $Li_{0.7}FePO_4$ reference electrode relative to the Li_xTiO_2 channel. Red indicates lithium insertion and blue indicates lithium removal. The shaded region indicates the operational range of the synapse. (d-e) Potentiation (increased conductance) and depression (reduced conductance) weight updates of a synaptic memory cell. The lower voltage in (e) requires longer times and a lower range. (f) The redox transistor retains state when V_W is set to 0, the diffusive memristor shuts off, and the lithium dopants are trapped in the channel. Each pulse during the retention measurements represents ~ 1 s. Reproduced with permission from ref. [54]; copyright 2019, American Chemical Society.

2.1. Symmetric Li_XTiO_2 redox transistor with near-zero OCV

Our synaptic memory cell is illustrated schematically in Fig. 1a. The cell contains an inorganic redox transistor and a diffusive memristor selector[24,57]. In this section, we discuss the redox transistor, which uses Li_XTiO_2 films (~30-nm-thick) with the anatase crystal structure as the gate and channel in a planar geometry (Fig. 1b). We use a solid polymer electrolyte ($LiClO_4$ dissolved in polyethylene oxide) that provides a path for Li^+ ions to flow between the gate and the channel while forcing the electrons to travel through an external circuit that connects that gate and the channel electrodes.

As an analogue memory device, the synaptic weight is stored in the electronic conductance of the channel electrode, which is read by applying a small voltage bias (~50 mV) and measuring the current across the "source" and "drain" electrodes connected to the channel. Synaptic weight updates are conducted by applying a write voltage (V_W) pulse to drive Li^+ and electron movement between the gate and channel. The insertion (extraction) of Li^+ and e^- reduces (oxidizes) the TiO_2 host to alter the electronic conductance of the channel. The concomitant transfer of both Li^+ ion and e^- maintains overall charge neutrality in the gate and channel electrodes to minimize electrostatic charges[58]. Like a battery, the built-in potential in the solid electrolyte between the gate and channel electrodes, or the OCV, is dictated by the thermodynamic difference in the Li chemical potential between the gate and the channel. To minimize the voltage, our device not only using the same materials as gate and channel, but also minimizes the change in the channel OCV to ±70 mV that occurs when the lithium concentration X changes during weight updates.

To evaluate the redox transistor as a synaptic weight storage medium, we study the electronic conductance of the channel as a function of the lithium concentration X. A nearby $Li_{0.7}FePO_4$ electrode (V_{REF}) is used to control X in both the gate and the channel and to serve as the electrochemical reference electrode[59] (Fig. 1c). This provides a reproducible method to measure the change in the electronic conductance of the Li_xTiO_2 channel as a function of X and the electrochemical voltage V_{REF} (Fig. 1c). We find that Li insertion (red) increases the channel conductance when V_{REF} < 1.6V (equivalent to a Li_XTiO_2 voltage >1.8 V vs Li/Li^+). The bulk channel resistance decreases because lithium acts as an n-type donor, increasing the concentration of Ti'_{Ti} (Ti^{3+}) polarons[60–62]. Upon further increase in the electrochemical voltage, the conductance drops sharply, before rising again at V_{REF} ~ 1.9V. The rapid drop in conductance between 1.6 and 1.9 V has been associated with an anatase-to-Li-titanate phase transition[63], and will be discussed in detail later. Beyond 1.9V, the channel conductance increases again as lithium inserts into the Li-titanate solid solution and increases the n-type carrier concentration. The trends are reversed upon lithium removal (blue). The measured voltage represents the sum of the OCV and the overpotential; the voltage hysteresis, common in electrochemical systems[58], arise because the overpotential, which also depends on X, is positive upon lithium insertion and negative upon lithium removal.

After establishing the electronic conductance as a function of X, we conduct preliminary experiments to evaluate the feasibility of this redox transistor to operate as a synapse with the gate and channel electrodes at a lithium concentration X~0.1, where it has a relatively high lithium diffusivity[64]. This prelithiation was achieved by applying 1.3V on V_{REF} while grounding all other electrodes (see Experimental Section for details). At X~0.1, the redox transistor also allows for a doubling of the channel conductance (from 40 to 80 μS) with a 70-mV change in the OCV (Fig. 1c). To keep the material operating within the anatase solid solution regime, it is important to ensure that the sum of V_W and the prelithiation voltage (1.3V) does not substantially exceed onset of the phase transition at 1.6V.

2.2. Low-voltage, Si-free electrochemical synapse

To realize a practical neuromorphic accelerator some level of integration with Si CMOS will almost certainly be necessary. However, a reduction in the number of single-crystalline silicon devices required to achieve function is beneficial because these devices cannot be stacked in three dimensions and requires additional power. Because of the large number of synapses in an array, passive arrays that do not use a Si-based transistor in each synapse would be advantageous for low power and high packing density[5].

We show how our inorganic redox transistor can also be integrated with a passive diffusive memristor selector and maintain its low-voltage operation. The diffusive memristor[24,57] is a two-terminal low-voltage threshold switch[65] based on Ag filament formation in a SiO_2 matrix that is connected in series with the gate of the redox transistor (Fig. 1a). The diffusive memristor becomes electronically conducting (ON) when the applied voltage exceeds a threshold voltage V_{th}; according to a transmission electron microscopy study[66], the Ag in the oxide forms an elongated filament that connects the two terminals, allowing an electronic pathway to the redox transistor's gate in order to conduct weight updates. When the applied voltage falls below V_{th} the elongated Ag filament collapses into a "circular" cluster that minimizes the surface energy[66]. This shorter circular cluster no longer spans the distance between the two terminals; thus, the memristor reverts back to its high-impedance equilibrium OFF state, preventing the redox transistor from self-discharging and allowing it to retain its state. Here, V_{th} is ~170 mV, for both positive and negative polarizations, and the ON/OFF ratio exceeds 10^7 with a ~1 mV/decade ON switching slope[24,57]. The high ON/OFF ratio at low threshold voltage enables selectivity during programming of the redox transistor and retention after programming, which we discuss in detail later.

To conduct weight updates at room temperature, we apply ±300 mV for 10 ms (Fig. 1d) or ±200 mV for 150 ms to V_W (Fig. 1e); as we show later, the switching time depends on the applied voltage. At V_W=±300 mV, we observe ~250 analogue states with linear and symmetric programming characteristics. Our synapse is also able to conduct weight updates with a total voltage of ±200 mV, only seven times the thermal voltage, an extremely low value for analogue memory. The conductance range of the channel is limited here because the 200-mV applied voltage is only slightly higher than the 170-mV threshold voltage of the diffusive memristor.

The diffusive memristor selector enables the redox transistor to retain its state, as demonstrated in Fig. 1f, for at least 500 pulses that each last ~1 s. This reflects the high OFF impedances of the selectors, which effectively isolate the gate from the channel. The ability of the redox transistor to retain state confirms that non-volatile changes in the channel conductance arise from the migration of lithium between the gate and the channel, as opposed to the redistribution of lithium within the channel, which would be volatile at room temperature. We further measure retention over longer time periods using analogue switch selectors, which have larger OFF resistances.

2.3. Array-level programming considerations

Functional array integration, as shown schematically in Fig. 2a, is a significant challenge for any emerging neuromorphic computing technology[16,67]. To reduce latency during training, it is desirable to address elements for programming through voltages sent along the rows and column at the edges of the network. In this way, neural network weight updates can be executed in a single, parallel operation within a clock cycle. One proposed method of parallel programming is a "half-select" scheme. In this scheme, the row and column voltages (V_R and V_W) at the edge of the crossbar select the synapses that will undergo weight updates, while not disturbing the other synapses. For example, we would select redox transistor **1,1** in Fig. 2a for a weight update using a positive V_{R1} and a

negative V_{W1} applied at the edges of the crossbar. However, in the process, the "half-selected" devices **1,2** and **2,1** must not be disturbed. To do so, the **N,M** selectors must remain OFF unless both V_{RN} and V_{WM} are applied: the application of either V_{RN} or V_{WM} is below the threshold voltage of the diffusive memristor, allowing the redox transistor to retain its state, while the application of both V_{RN} and V_{WM} (with opposite polarities) results in a voltage difference that is than the threshold voltage so the redox transistor can conduct weight updates.

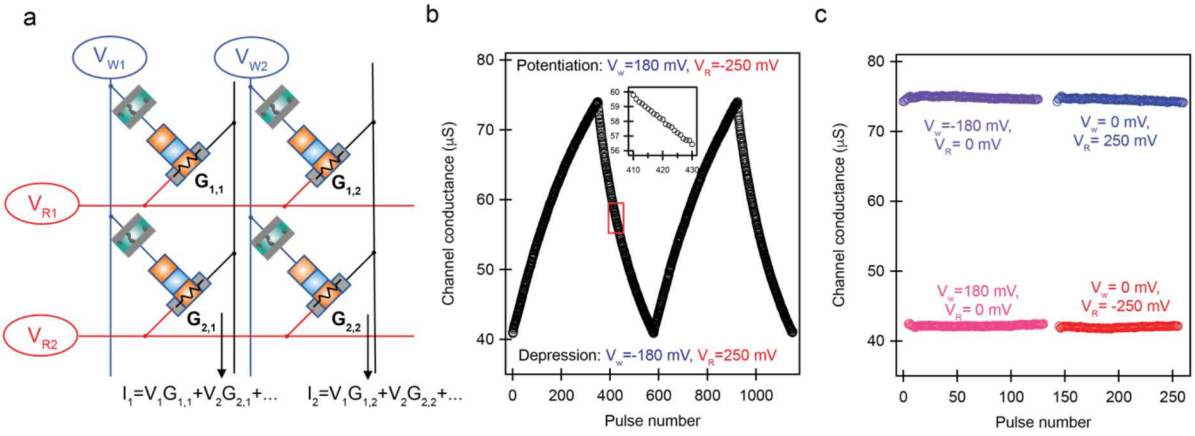

Figure 2: **Compatibility of the synaptic memory cell with a V/2 crossbar programming scheme.** (a) A proposed crossbar programming scheme incorporating the redox transistor and the diffusive memristor selector. The row and column voltages at the edge of the crossbar array are used to select which cells to program; however, half-selected cells that share a row or column with selected cells cannot be disturbed. The diffusive memristor needs to provide the selectivity. To improve the readability, we placed the two Pt electrodes adjacent to the channel in the schematic for each redox transistor. (b) The V/2 programming scheme, which entails applying a positive V_W and a negative V_R (for potentiation) or a negative V_W and a positive V_R (for depression). (c) The synaptic memory satisfies the half-selection rule by retaining state when either V_R or V_W, but not both, is applied. Each pulse here lasts ~ 1 s, and the measurements were conducted at room temperature. Reproduced with permission from ref. [54]; copyright 2019, American Chemical Society.

In Fig. 2b, we show the results of a V/2 weight update write scheme at room temperature using the circuit placement described in Fig. 1a. We apply approximately half the write voltage via V_W ($\pm$180 mV) and the other half via V_R ($\mp$250 mV), for 10 ms. Our results show that this V/2 programming scheme linearly potentiates and depresses the synapse similarly to applying $\pm$300 mV via V_W (Fig. 1e). Importantly, half-selected devices that experience only V_W or V_R are not disturbed (Fig. 2c). Our V/2 half-select demonstration relies upon our elimination of the OCV: otherwise, a large OCV will always latch the selector ON, precluding the cell from retaining state. We note that the weight updates can be conducted with the "source" biased to $V_R = \mp$200 mV and the "drain," or the terminal on the channel opposite to V_R, always grounded (Fig. 1a, 2a). This allows the devices to be integrated into a dense array without requiring a select device to disconnect or float the "drain" during writing. In contrast, V/2 weight updates on organic redox transistors required an extra read-select transistor that floats the "drain" during write and grounds the "drain" during read[43]. The reason is because the organic channel is unstable against the large electronic currents induced by a high V_R~400 mV between the "source" and "drain" electrodes during write[43]. Not only is V_R lower here, but the inorganic Li_XTiO_2 channel is more stable against these applied read voltages and currents, allowing us to eliminate this extra read-select transistor.

Due to the electrical polarization between the "source" and "drain" electrode during weight updates incurred by $V_R = \mp$250 mV, we anticipate some spatial redistribution of lithium. However, because the lithium in the channel equilibrates when V_R is removed, such transient changes should

not affect the long-term, non-volatile channel conductance. Since weight updates are non-volatile (Fig. 2c), the redistribution of lithium has a minor effect on the channel conductance, and that the primary source of weight updates is the migration of lithium between the gate and the channel. Since all devices in this work are processed below 500° C and do not require single-crystal silicon, a three dimensional stacking scheme could be envisioned[16] assuming that an electrolyte that is stable at 500° C[68] can be integrated, and is subject for future investigations. A stable 500° C electrolyte will also allow the construction of a gate/electrolyte/channel structure stacked on top of each other with no OCV, where the gate and channel are made of the same crystalline materials like $LiCoO_2$ and TiO_2 that require a high-temperature anneal.

We evaluate the linearity and noise characteristics of our combined non-volatile analogue memory cell in a crossbar by inputting the conductance data obtained from experiment into the crossbar simulation program CrossSim[69]. CrossSim simulates a three-layer network, and was used in previous work[47,48,70,71]. Fig. 3a shows the statistical distribution of the experimental data used for CrossSim. Our simulation results in Fig. 3b show high classification accuracy using the MNIST versions of handwritten digits[72]. The combination of the redox transistor with the diffusive memristor selector yields ~92% accuracy, close to the numerical limit. We anticipate that improvements on switching speed and material crystallinity may improve linearity further to reach ideal accuracy as has been demonstrated with previous metal oxide devices[47].

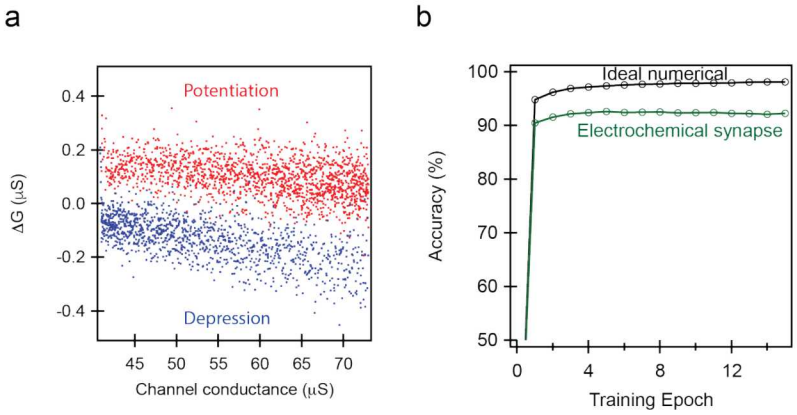

Figure 3: Linearity and noise characteristics of the redox transistor and its effects on the accuracy of backpropagation. (a) Reproducibility of ΔG, or the change in conductance upon a weight update, with every pulse under different channel conductance states, using the data from Fig. 2b. Each dot represents one weight update. (b) Crossbar simulations using the data in (a) show that the memory cells is able to attain over 90% accuracy to train a backpropagation network on the MNIST data set. Reproduced with permission from ref. [54]; copyright 2019, American Chemical Society.

2.4. Experimental methods

Fabrication of TiO_2 redox transistors:

The redox transistors were grown on Si <100> wafer with 300-nm thermal oxide (Fig. S2). First, a photolithography process using Microchem LOR5B lift-off resist and Shipley S1813 photoresist (spin-coat at 4000 rpm each) was used to define the Pt contacts. The patterns were exposed using a photomask and a Karl Suss contact aligner, and developed using Microposit MF319 ammonium hydroxide developer for ~45 s. 5-nm Ti adhesion layer and 50-nm Pt contacts were grown using electron-beam evaporation at ~1 Å s^{-1}, and excess metal was lift-off using Microchem Remover PG, a N-methylpyrrolidone based solvent. We conduct a second photolithography step on top of the Pt patterns to define the TiO_2 patterns, identical to the photolithography for the metal contacts except

for the TiO_2 deposition; here, the gate is 1000 × 100 μm^2 and the channel is 1000 × 10 μm^2, of which the middle 8 × 10 μm^2 is grown directly on the thermal oxide and forms the suspended channel (Fig. 1b). TiO_2 was grown using reactive DC sputtering from a 3-inch Titanium target (99.97% target purity from Kurt J. Lesker) with a total power of 300 W (460 V and 0.65 A) for 30 min at a deposition rate of 1 nm min^{-1}. The baseline pressure of the sputter chamber (Kurt J. Lesker) was ~2 × 10^{-7} torr, and sputtering was conducted at 4 torr environment consisting of 33% oxygen and 67% argon. The sample was annealed at 500° C for 1 hr in air to crystallize the material into the anatase crystal phase. To measure the crystal structure and the deposition rate, we reactive sputter a thin film of TiO_2 under the same conditions for 1 hr on a Si <100> wafer, and annealed at 500° C for 1 hr in air.

We next add a macroscopic $Li_{0.7}FePO_4$ reference electrode about 5 mm away from the TiO_2 electrode. The $Li_{0.7}FePO_4$ was obtained by chemically delithiating $LiFePO_4$ nanoparticles from Mitsui Engineering and Shipbuilding using a stoichiometric amount of aqueous potassium persulfate via the reaction $LiFePO_{4\,(s)} + 0.15\ K_2(SO_4)_{2\,(aq)} \rightarrow Li_{0.7}FePO_{4\,(s)} + 0.15\ Li_2SO_{4\,(aq)} + 0.15\ K_2SO_{4\,(aq)}$. K_2SO_4 was purchased from Sigma Aldrich and mixed with deionized water. The mixture was given 24 hr at rest for the reaction to complete. The water-soluble sulfates were removed by centrifuging the mixture three times in deionized water and drying under vacuum. The dried $Li_{0.7}FePO_4$ powder was mixed with carbon black (Timcal C65) and polyvinylidene fluoride (MTI) at a ratio of 70wt%:20wt%:10wt%. Afterwards, the solids were mixed with N-methylpyrrolidone (Alfa-Aesar), and this suspension was manually painted onto a Pt current collector near the TiO_2 patterns to form the reference electrode. Special care was taken to ensure that the $Li_{0.7}FePO_4$ electrode is electrically isolated from the TiO_2 patterns.

To complete the redox transistors, we use a polymer electrolyte consisting of 30 wt% $LiClO_4$ (Sigma-Aldrich) with polyethylene oxide MW 600,000 (Sigma-Aldrich), both of which are dissolved in methanol. This viscous mixture was drop-cast to cover both the TiO_2 patterns and the $Li_{0.7}FePO_4$ reference electrode; the solid polymer electrolyte containing the $LiClO_4$ salt dissolved in polyethylene oxide forms after the methanol dries. To remove residual water, we keep the mixture in an Ar glovebox on a hot plate at 80° C for at least 24 h prior to operation.

Data acquisition measurements:

The experiments in Figs. 1-2 (except for Fig. 1c) were conducted using a National Instruments Data Acquisition Device (-6358) controlled using the LabView program. Analogue outputs were connected to V_{IN} (for analogue switch only), V_W, and V_R, while the final current collector for the channel was connected to a virtual ground created by the inverting input of an operational amplifier. An operational amplifier (AD820) was used to create an operational trans-conductance amplifier circuit using a 1 MOhm resistor between the inverting input to the output, and the operational amplifier output was connected to an analogue input of the DAQ to measure the read current through the channel. For the analogue switch experiments, V_{IN} was 2.0 V and applied concurrently with V_W; V_{IN} was not used in the diffusive memristor experiments.

Crossbar simulations

The crossbar simulations were conducted using the potentiation and depression data sets in Fig. 3a-b. More details can be found on the CrossSim[69] site and in previous work[47].

3. OXYGEN VACANCY REDOX TRANSISTOR (OVRT)

Three-terminal redox transistors based on Li+ and H+, including the one presented in section 2, have successfully solved the stochasticity and linearity challenges of two-terminal memristors. However, they suffer from two significant shortcomings. First, such devices use nonstandard materials including lithium transition metal oxides and polymers, all of which cannot be integrated into preexisting fabs. Second, these devices contain a very low intrinsic energy barriers against loss of state: with ion migration activation energies below 0.5 eV, any electrostatic or electrochemical potential difference between the gate and channel will result in rapid loss of state. In contrast, resistive memory cells containing oxygen vacancies contain much larger activation energies, effectively enabling them to "freeze" the state for many years at near-room temperature. Li+ and H+ based ECRAM instead uses electronic switches to try to retain state, but this method does not scale to nanosized dimensions. To remedy these issues, we produced the three-terminal devices based on oxygen vacancy instead of Li+ or H+. This is also known as the bulk-RRAM cell[56] because, like standard filament-based RRAM, it also uses oxygen vacancies.

3.1. Oxygen vacancy redox transistor concept

Like earlier redox transistors, the three-terminal OVRT uses electrochemical ion insertion and extraction to modulate the bulk dopant concentration in the channel to provide predictable switching between hundreds of analogue states. Unlike past redox transistors that utilize Li^+ or H^+, the present device shuttles oxygen vacancies ($V_O^{\cdot\cdot}$) to achieve non-volatility and CMOS compatibility. At moderately elevated temperatures, ion transport is achieved through write voltages (V_W) applied to the gate (Fig. 4a). To retain state, the device is rapidly cooled to room temperature, where ion flow is suppressed (Fig. 4b) but the channel remains electronically conductive (Fig. 4c). An essential component is a solid electrolyte with an appropriate $V_O^{\cdot\cdot}$ activation energy to maximize the difference in the ionic resistivity between elevated and room temperatures for fast weight updates and low memory loss. Figure 4d plots the ionic resistivity of Yttrium-stabilized Zirconia (YSZ), which has an Arrhenius activation energy ~1.1 eV. The thermally-activated ion migration within the electrolyte is crucial towards long state retention: not only does this provide state retention when the gate and channel are electronically shorted (Fig. 4b), but, as we show in more detail later, this ionic switch provides retention times that are independent of device area. In contrast, past redox transistors that operate at constant temperature need an external electronic switch to electronically isolate the gate from the channel[39,43,45,47,48,54], and the retention time in this configuration decreases proportionally with the redox transistor area.

Thermally-activated $V_O^{\cdot\cdot}$ migration also provides fast writing and long retention in filament forming memristors like the resistive random access memory (RRAM). Unlike OVRTs, however, RRAM elements concentrate the electrical current and the resultant joule heating into filamentary hotspots within the MIEC[14,16,28,73] during high-voltage "writes" (Fig. 4e). Localized joule heating as high as 500°C (ref. [28]) enable $V_O^{\cdot\cdot}$ migration, very fast write times, and long retention times after the device cools. However, concentrating the electric field and joule heating to filamentary hotspots results in highly non-uniform $V_O^{\cdot\cdot}$ distributions, leading to nonlinear and unpredictable weight updates and a limited number of analogue states[5].

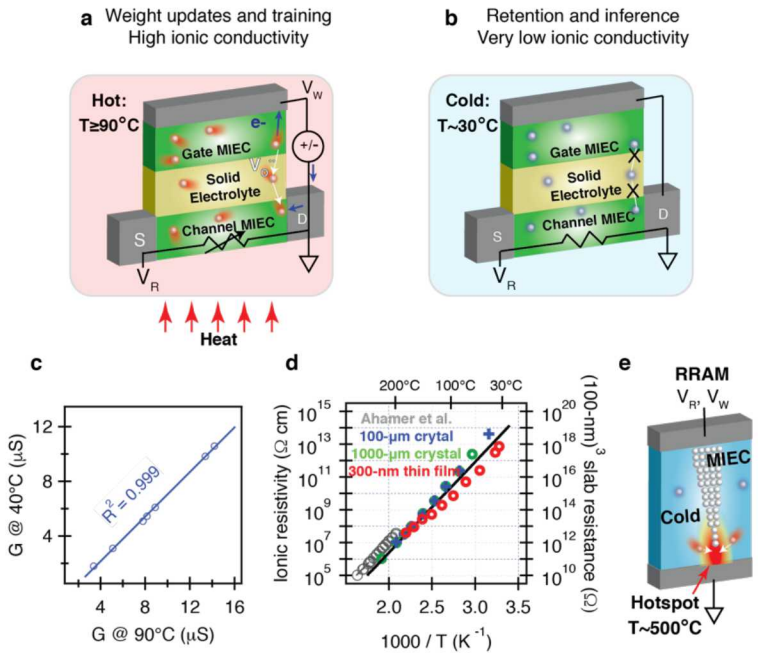

Figure 4: Oxygen vacancy redox transistors (OVRTs) store information through the bulk oxygen vacancy ($V_O^{\cdot\cdot}$) concentration in the MIEC channel. (a) To conduct weight updates, OVRTs electrochemically shuttle $V_O^{\cdot\cdot}$ between the gate and the channel via the electrolyte at elevated temperatures, modifying the bulk compositional $V_O^{\cdot\cdot}$ concentration in the channel, which controls the electronic conductance. (b) To retain state, the device is rapidly cooled to near room temperature, where the ionic conductivity drops significantly, effectively blocking $V_O^{\cdot\cdot}$ from migrating between the gate and channel without needing a switch to electrically isolate the gate and the channel. (c) The channel conductance (G) has a linear and predictable relationship when it is cooled from 90°C to 40°C; each point represents a different oxygen vacancy concentration. (d) The ionic resistivity of the Yttrium-stabilized Zirconia (YSZ) electrolyte follows a thermally-activated Arrhenius process with an activation energy of ~1.1 eV; our ionic resistivity measured through electrochemical impedance spectroscopy follows the high-temperature trends measured by Ahamer et al[74]. (e) While resistive RAM also harness $V_O^{\cdot\cdot}$ to store information, they concentrate electric fields and joule heating to form filamentary hotspots, which generally result in nonlinear and unpredictable state changes. In contrast, the OVRT uses external heat sources and thus has minimal spatial variation in temperature or electric fields, resulting in uniform $V_O^{\cdot\cdot}$ distributions in the bulk as a result of configurational entropy.

In contrast to RRAM, the OVRT uses external heating sources that provide nearly homogeneous temperature increases (Fig. 4a); in the absence of significant temperature gradients, configurational entropy drives $V_O^{\cdot\cdot}$ to distribute as a uniform solid solution within the channel's bulk in many MIECs[58]. The ion-conducting, electron-insulating electrolyte also controls the number of $V_O^{\cdot\cdot}$ transferred to equal half the number of electrons moved in the external circuit in accordance with electroneutrality[58]. Memristors that lack electrolytes do not achieve precisely controlled $V_O^{\cdot\cdot}$ concentration, even when they contain three terminals[75]. The OVRT also requires no electroforming or reset process.

3.2. Weight updates in OVRT

We fabricate CMOS-compatible OVRTs on Si substrates (Fig. 5a) with 100-nm thermal oxide by first evaporating the bottom Pt contacts, then sputtering the TiO_2 (anatase) channel, YSZ electrolyte, $TiO_{2-\delta}$ gate, and Ti top contact (see Experimental Methods for more details on fabrication). OVRTs resemble solid oxide fuel cells[76]; the primary difference is the presence of source-drain

contacts on the channel electrode to read the electronic conductance, and the absence of gas evolution and reduction reactions.

We demonstrate analogue memory functionality by conducting weight updates using 2-μs write pulses at 180 °C (Fig. 5b). Our results show over 100 analogue states with linear and symmetric switching. Despite using a solid electrolyte, our write speed is orders of magnitude faster than that of oxygen-vacancy based synaptic transistors using ionic liquid electrolytes[38,40]. The channel resistance range of 2-10 MΩ nears the desired range for large, energy-efficient crossbar arrays[43,53], and can achieve even higher resistances through square channel geometries.

Fig. 5c shows the mean write time as a function of the temperature for three devices, within the operational temperature range of CMOS circuits. Assuming that the write time is proportional to the total ionic resistance, we estimate an ion conduction activation energy of ~1.5 eV (Fig. 5c); this suggests that the device write time is not controlled by the electrolyte ionic resistance, which has a 1.1 eV activation energy (Fig. 5c).

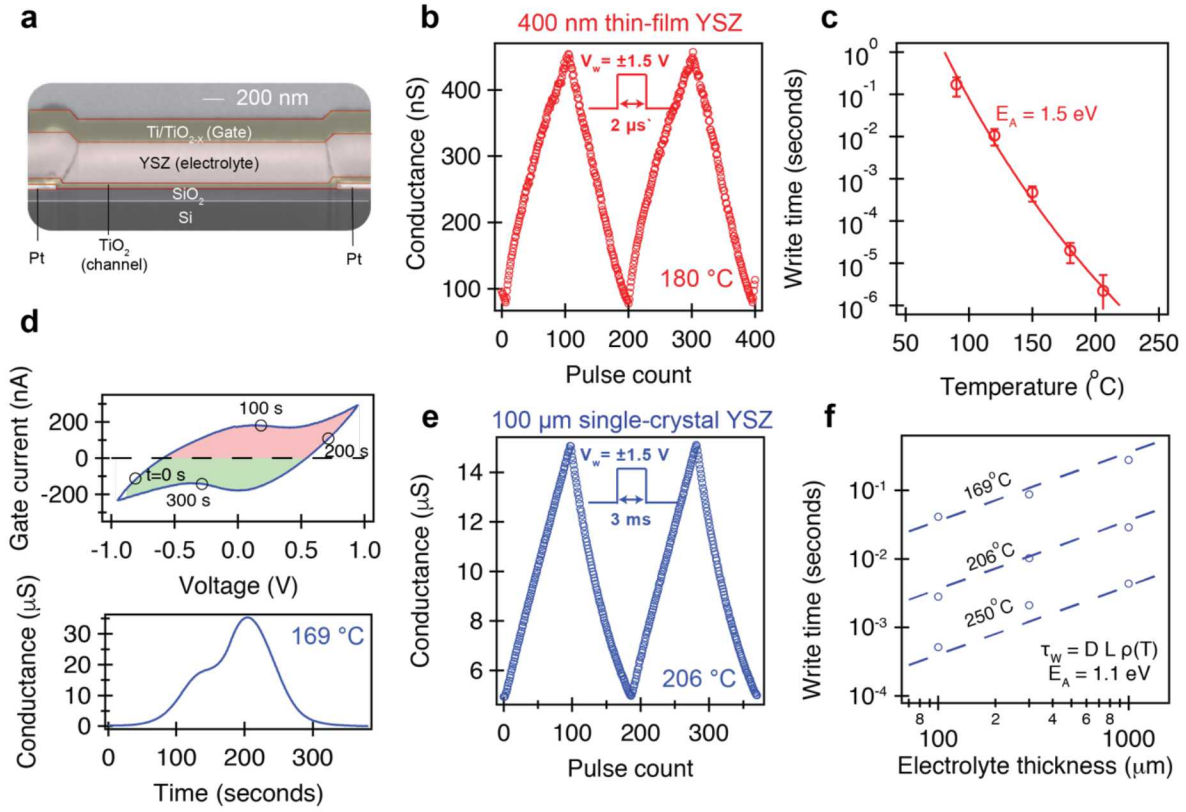

Figure 5: The OVRT shows a large number of analogue states, high channel resistance, and predictable switching. (a) Cross-section scanning electron micrograph of the OVRT with a thin-film YSZ electrolyte. Reading is performed by measuring the conductance of the channel gap between the two Pt contacts. Writing is performed by applying a voltage and controllably shuttling oxygen vacancies between the gate and the channel. (b) Weight updates of the thin film redox transistor with a 400-nm-thick electrolyte show linear and predictable switching, over 100 analogue states, high channel resistances, and write speeds as fast as 2 μs. (c) The write time decrease at higher temperatures. Assuming that the write time is proportional to ionic resistance, it fits to an activation energy of ~1.5 eV, which is higher than the 1.1 eV of YSZ (Fig. 4d). The error bars are based on twice the standard deviation for the three devices measured. (d) Cyclic voltammetry between the gate and the channel indicates that the channel conductance can be modulated as it is electrochemically oxidized and reduced by oxygen vacancies. (e) Weight updates of the redox transistor fabricated on 100-μm single-crystal YSZ shows linear and symmetric switching with over 100 analogue states. (f) The effect of electrolyte thickness and temperature on the write time needed to achieve 100 analogue states within a 3× change in conductance.

All results are fitted using a common fit parameter D = 80 ± 20 nF cm^{-2} (95% confidence interval), and are consistent with ion transport across the thick YSZ substrates being the rate-limiting process.

To better understand the OVRT, we construct model devices on single-crystal YSZ substrates with thicknesses between 100 and 1000 μm. In these devices, $TiO_{2-\delta}$ gate/channel and Pt contacts are grown on opposites sides of the electrolyte substrate. To characterize the electrochemical reactions that enable OVRT performance, we conduct cyclic voltammetry to shuttle $V_O^{\cdot\cdot}$ between the gate and the channel while measuring the electronic conductance of the OVRT's channel (Fig. 5d). At positive gate currents the channel conductance increases as $V_O^{\cdot\cdot}$ is inserted into the channel, where Ti^{4+} ions are reduced to Ti^{3+} creating two mobile polarons for every $V_O^{\cdot\cdot}$ inserted, (written as Ti'_{Ti} in Kroger-Vink notation). At negative gate currents, the process is reversed. The electronic conductivity of our channel increases with temperature (Fig. 4c), characteristic of small polaron conduction[50]. The low electron mobility, typical of polaronic conductors, facilitates the realization of high channel resistances despite the high electron concentrations, which are needed for high chemical capacitance[77,78] and long information retention. The channel conductance (G) has a linear and predictable relationship when cooled from high temperature (Fig. 4c). We propose a simple method to convert channel conductance to the synaptic weight value which corrects for the temperature dependence of the channel electron conductivity in the supplemental information.

We conduct weight updates using 1.5 V pulses (3 ms) at 206 °C (Fig. 5e); higher temperatures and write times are needed due to increased electrolyte thickness and resistance. The channel conductance is higher than the thin-film devices because the gate and channel were more reduced during fabrication (i.e., higher δ in $TiO_{2-\delta}$). The projected electrical energy per weight update is ~10^{-17} J for a scaled (100 nm)^2 OVRT without accounting for the energy of heating (see Methods for quantification).

In Fig. 5f we plot the write time as functions of electrolyte thickness and temperature. The results are fitted to the simple model $\tau_W = DL\rho(T)$, where D = 80 ± 20 nF cm^{-2} (95% confidence interval) is the common fit parameter to all data points, $\rho(T)$ is the temperature-dependent resistivity from Fig. 4d, and L is the thickness of the YSZ electrolyte used. Our results show that write time can be shortened by decreasing the thickness L and by increasing the temperature T. Unlike with thin-film devices, the rate-limiting step here is bulk resistance of the YSZ electrolyte, which is over 800 times thicker compared to the $TiO_{2-\delta}$ layers. The excellent fit across all fabricated devices suggests minimal device-to-device variation. We speculate that this arises from our use of the bulk oxygen vacancy concentrations, rather than filamentary defects, to set the resistance state.

3.3. Information retention of OVRTs

Next we consider the long-term retention of the device and how it relates to the electrolyte properties and overall charge capacity of the cell. Unlike past works that use an electronic switch to isolate the gate from the channel[39,43,45,47,48,54], we plot the memory loss over time (Fig. 6a) when the gate and channel are shorted (Fig. 4b). Initially, the device was charged to a high-conductance state. Our results show that the channel conductance decay time strongly depends on temperature. At room temperature, the device conductance changes by less than 0.3% after one week.

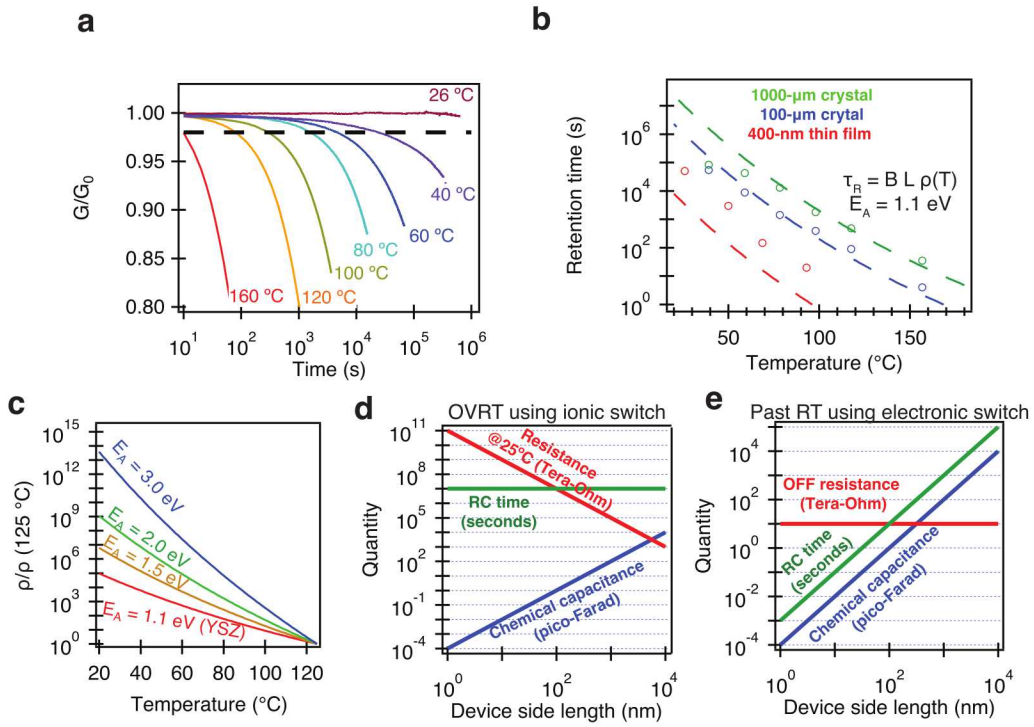

Figure 6: Retention of the OVRT at various temperatures when the gate and channel are shorted without an electronic switch. (a) Channel conductance decay of the redox transistor on single-crystal YSZ over time at different temperatures as the gate and channel are shorted. Retention time increases significantly at lower temperatures as the electrolyte resistance rises. (b) The retention time $\boldsymbol{\tau_R}$, defined as 2% change in conductance, as a function of temperature (T) and electrolyte thickness (L), with a single fit parameter B = 1.4 ± 0.5 μF cm^{-2} (95% confidence interval) fitted to all the single-crystal results (c) Projected retention time based on $\boldsymbol{\tau_R}$ normalized to the value at 125°C. Higher oxygen vacancy activation energies increase the rate that $\boldsymbol{\tau_R}$ increases at lower temperatures. (d) RC time constants for OVRTs that utilize thermally-activated ionic switch do not depend on the device size because the ionic resistance increases at the same rate that the chemical capacitance decreases. We assume the gate, electrolyte, and channel are each 100-nm-thick, the specific chemical capacitance is 1000 F cm^{-3}, and the ionic resistance is 10^{14} Ωcm from Fig. 4d. (e) The RC time decreases significantly with device size if an electronic switch is used to retain state, as done in past works on Li^+ and H^+ redox transistors (RT). As chemical capacitance of the RT decreases with size, the switch's resistance does not decrease with the RT size and assumed to be 10^{13} Ω here, resulting in drastic decrease in $\boldsymbol{\tau_R}$.

In Fig. 6b we plot the retention time τ_R, defined as the time necessary for the channel conductance to drop by 2%, as a function of temperature for various electrolyte thicknesses. The trendline fit is given by $\tau_R = BL\rho(T)$, with B as another fit parameter related to the chemical capacitance with a value of 1.4 ± 0.5 μF cm^{-2} (95% confidence interval). We observe two significant deviations: first, the thin-film device retains state longer than predicted based on the thickness, consistent with the earlier observation that oxygen vacancy transport in the thin-film electrolyte may not be rate limiting. Second, the 1-mm-thick devices have shorter retention than expected at lower temperatures; this is likely due to the incorporation of oxygen from the gas phase into the channel, which is not accounted for our model for τ_R. Despite deviations, our results demonstrate the ability of OVRTs to retain state for periods of days to weeks due to low $V_O^{\cdot\cdot}$ mobility at or near room temperature. Based on our simple model, longer retention times can be achieved by using materials with higher Arrhenius activation energy for $V_O^{\cdot\cdot}$ mobility (Fig. 6c), which increases the temperature dependence of the ionic resistivity.

We next consider how the OVRT retains state when scaled to smaller lateral dimensions while the gate and channel are shorted. We assume that the retention time is proportional to a RC time constant (τ_{RC}), where C is the chemical capacitance[78] of the gate and channel while R is the total ionic resistance of the device. While the chemical capacitance decreases proportionally with the area, the ion resistance increases at the same rate, leading to a τ_{RC} which is independent of device size (Fig. 6d). A τ_{RC} of 10^7 s, ~ 4 months, is obtained for a volumetric specific chemical capacitance of 1000 F cm^{-3} (ref. [44]), ionic resistivity of 10^{14} Ωcm at room temperature (Fig. 4d), and gate, electrolyte, and channel thicknesses of 100 nm each.

In contrast, redox transistors based on Li^+ and H^+ that operate at constant temperature have retention times that decrease for smaller devices. In these devices, the ionic conductivity is always high, so retention necessitates by blocking electronic current between the gate and channel using electronic switches, such as transistors[39,45,47,48] or diffusive memristors[43,54]. As a result, R_{OFF} is constant and depends on the properties of the switch while C decreases proportionally with the area of the redox transistor (Fig. 6e). Assuming that R is ~10^{13} Ω based on low-leakage transistors[79], this scheme provides long retention times for relatively large devices (>10 μm)^2 as previously demonstrated[39,43,45,47,48,54]. However, τ_{RC} decreases drastically for smaller devices, yielding only ~10 s for scaled (100 nm)^2 devices, many orders of magnitude lower than for a scaled OVRT (Fig. 6d). Scaled diffusive memristors[24] can potentially provide higher electronic OFF resistances, but it is unclear if the OFF resistances can be sufficiently high for CMOS-compatible versions[80].

3.4. Experimental methods

Fabrication of *redox transistors on single-crystal YSZ*: Single-crystal YSZ substrates, 1 cm square and 100, 300, and 1000 μm thick, were purchased from MTI (www.mtixtl.com) and used without further processing. These substrates have a nominal concentration of 8 mol% Y_2O_3 in ZrO_2. Reactive DC sputtering using a Kurt J. Lesker CMS18 system was used to deposit TiO_2 from a 76-mm-diameter Ti metal target (99.99%) using a sputter power of 300 W in a 4 mtorr gas environment consisting of 33% O_2 and 67% Ar. Sputtering was conducted on both sides on the substrate: the TiO_2 film on the channel side is 60-nm-thick; the TiO_2 film on the gate side is 120-nm-thick. The sputter rate was about 0.5 nm min^{-1}. The film was then annealed at 600°C in air for 1 hr to crystallize the anatase phase. A 5-nm Ti adhesion and 50-nm Pt contacts were grown on the 60-nm-thick channel by electron beam evaporation at an evaporation rate of ~ 1 A s^{-1}. Two contacts separated by 250 μm were grown using a stainless-steel shadow mask on the channel side, forming the "source" and "drain" contacts. The area of the channel between the contacts is 8000 μm long and 250 μm wide.

Next, we reduced the gate and part of the channel from TiO_2 to $TiO_{2-\delta}$ in a reducing environment containing 2 bar of pure H_2 at 400 °C for 1 hr using a Setaram PCTPro gas sorption tool. The channel regions under the Pt contacts were not reduced because the Pt blocks oxygen from leaving TiO_2, while the gate TiO_2 side as well as the part of the channel not blocked by the contacts were reduced. After reduction, the channel conductance was determined to be ~100 μS using the previously-fabricated contacts. An unpatterned Ti/Pt contact was again grown by electron beam evaporation on the 120-nm-thick $TiO_{2-\delta}$ gate as the gate contact to complete the device.

Fabrication of redox transistors with thin-film YSZ on Si/SiO_2 substrate: We first fabricated the Pt contacts on the channel side using optical photolithography. Photoresist was spun on a 150-mm silicon wafer containing a 100-nm-thick dry thermal oxide layer. The photoresist was patterned using a Karl Suss contact aligner and developed with a MF-319 developer. The channel was 1600 μm long

and 2 μm wide. Afterwards, 5 nm of Ti and 50 nm of Pt were evaporated, and the remaining metal was removed by lift-off in PG Remover to define the contacts. Next, 60 nm of TiO_2 was evaporated by reactive sputtering as described previously and annealed at 600 °C for 1 hour to crystallize into anatase to create the channel. 400 nm of YSZ was grown by RF sputtering on a 76-mm YSZ target (8 mol% Y_2O_3 in ZrO_2, Plasmaterials LLC) using a sputter power of 240 W and a growth rate of ~0.25 nm min^{-1}. The sample was then annealed at 700 °C for 2 hours.

120 nm of amorphous, oxygen-deficient $TiO_{2-\delta}$ layer was grown above the YSZ. This oxygen-deficient film was grown by changing the sputter gas composition from 67% Ar and 33% O_2 to 87% Ar and 13% O_2; the deposition rate was ~10 nm min^{-1}. This oxygen-deficient film is conductive, whereas the oxidized anatase film is not. Finally, a 20-nm Ti layer was sputtered above $TiO_{2-\delta}$ by changing the sputter gas to 91% Ar and 9% O_2; the sputter rate was ~5 nm min^{-1}. These two final layers were not annealed to preserve the oxygen-deficient gate $TiO_{2-\delta}$ layer.

We note that these two methods yielded different channel conductance ranges because they differed in the amount of oxygen vacancies that was incorporated. The direct sputtering of nonstoichiometric $TiO_{2-\delta}$ was done for the thin-film devices because the YSZ films delaminate in the presence of two bars of hydrogen. Reducing the annealing temperature to be compatible with a back-end-of-line process is an important avenue of future work on OVRTs.

Electrochemical cycling and retention: The OVRT on single-crystal YSZ was characterized on a hot plate in an Ar glovebox (Fig. 2d). The temperature of the hot plate was calibrated using a thermocouple adhered to a reference YSZ substrate using silver paint. One probe was connected to each of three contacts; a Bio-logic SP-300 bipotentiostat was used to study the sample, whereby potentiostat channel 1 was used as V_W to apply voltage and current between the gate and one of the contacts on the channel, and potentiostat channel 2 was used to measure the electronic conductance of the channel by applying a constant 100-mV bias and recording the channel. Upon heating while the gate and channel are under open-circuit conditions, the conductance of the channel on single-crystal YSZ drops as oxygen vacancies in the exposed channel equilibrate with the less-conductive, more oxidized TiO_2 under the contacts that was not previously reduced by hydrogen. Above 150 °C, an open-circuit voltage of -400 mV was measured, suggesting that the gate was more reduced than the channel. We cycled the gate and channel using cyclic voltammetry in Fig. 2d at 170 °C.

Retention measurements: Long-term retention measurements in Fig. 3 were made using a SP300 bipotentiostat. The single-crystal samples were heated to 160 °C using a Nextron heated probe station and charged to 20 μS by applying a gate voltage of 1V and measuring the channel read current. Afterwards, the device was quickly cooled (<30 s) to the desired measurement temperature. Once it was cooled, we shorted the gate and channel by applying 0 V to the gate and measured the channel conductance as a function of time. The thin-film devices were measured identically, except that potentiation was conducted at 90 °C instead of 160 °C.

Electrochemical impedance spectroscopy: The ionic conductivity of the YSZ electrolyte were measured using electrochemical impedance spectroscopy on a hot plate in the glovebox. We apply alternating currents on opposite sides of single-crystal YSZ with Pt contacts from a frequency of 10^5 Hz to frequencies as low as 10^{-4} Hz at 50°C with an amplitude of 100 mV. For the thin-film devices, impedance measurements were conducted on a device with thin films of Pt (50 nm), YSZ (300 nm), and Pt (50 nm).

Data acquisition measurements: The experiments in Figs. 2b-c, e-f, as well as all other experiments where pulses were less than 1 second, were conducted using a National Instruments Data Acquisition Device (DAQ-6358) controlled using the LabView program on a hot plate in a glovebox. An analogue switch (MAX327CPE) served as the extrinsic selector during weight updates; this selector was ON by applying 2V concurrent with the write pulses, and OFF at all other times to retain state during weight updates. Analogue outputs from the DAQ were connected to V_W, V_R, and the V_{IN} of the analogue switch, while the final contact for the channel was connected to a virtual ground created by the inverting input of an operational amplifier. An operational amplifier (AD820) was used to create an operational trans-conductance amplifier circuit using a 1 MΩ (for the single-crystal YSZ devices) or 100 MΩ (for the thin-film YSZ devices) resistor between the inverting input to the output, and the operational amplifier output was connected to an analogue input of the DAQ to measure the read current through the channel.

The write speed for the single-crystal devices was quantified by through the write pulse length needed to obtain 100 weight updates between the highest and lowest operational conductance state of the device. The write time for the thin-film devices were quantified in the same manner, but the error bar represents twice the standard deviation for the write time quantified across the three devices measured.

4. CONCLUSIONS

We successfully demonstrated two types of electrochemical redox transistors based on TiO_2 (anatase), one using lithium as a dopant and the other using oxygen vacancies. Both devices operate on the basis of electrochemically moving dopant ions in and out of the TiO_2 channel and modulating its resulting analogue conductance value. They solve the challenge of resistive memory by providing a way to predictably and linearly changing the analogue state. The OVRT is the more promising of the two devices because it enables the use of CMOS-compatible materials and can potentially be scaled into nanosized dimensions. These provide significant advance towards creating materials and devices for neuromorphic computing.

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