U.S. DEPARTMENT OF ENERGY | Sandia National Laboratories | The Ohio State University | CHPPE | GeneSiC SEMICONDUCTOR

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Medium-voltage Power Electronics for Grid-tied Energy Storage Applications

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Project Motivation

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Motivation:

- Facilitate large-scale energy storage to improve resiliency and modernize the power grid.

Goal:

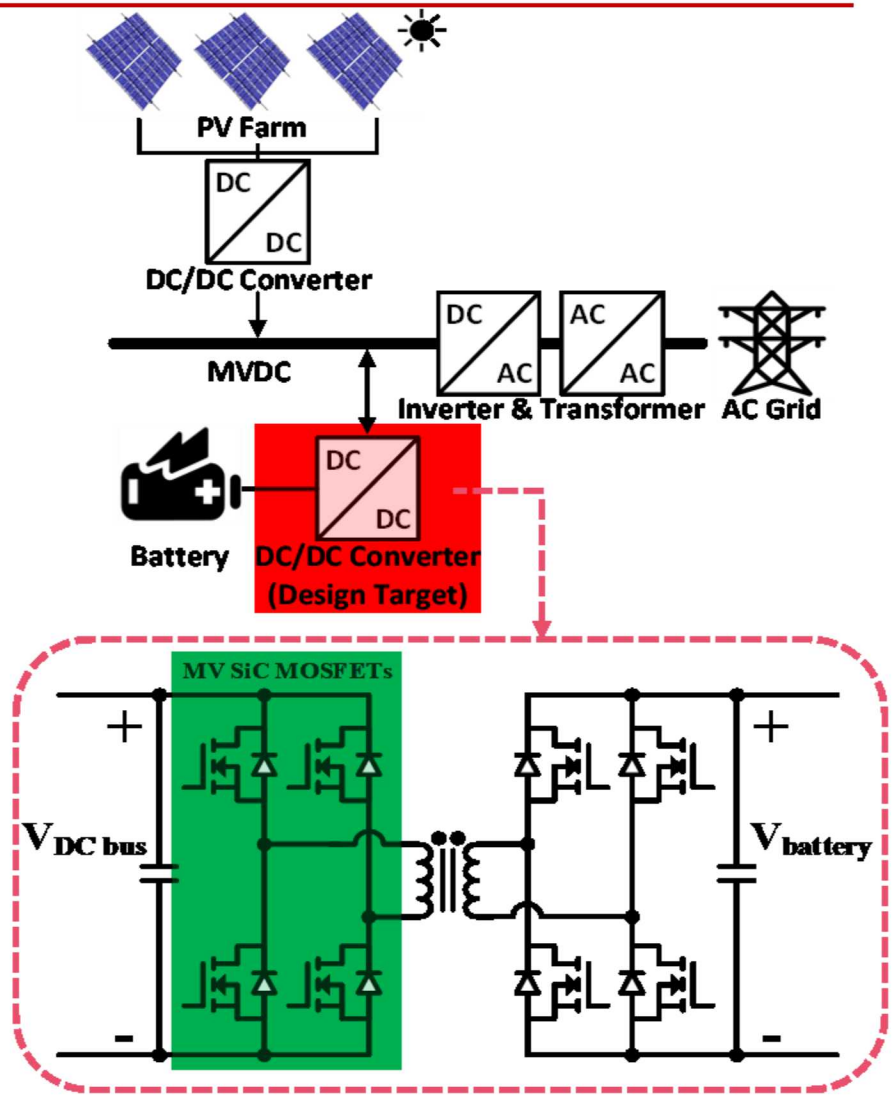
- Increase MW-scale energy storage capabilities using wide bandgap SiC devices.

Challenges:

- Lack of inexpensive commercially available SiC devices above 3.3 kV.
- Testing higher voltage WBG devices for application reliability.

Proposed Methodology:

- Build a MV DC/DC power electronic converter with WBG devices to test their performance and reliability for energy storage integration.



PV energy harvesting system with storage and proposed DC-DC converter design

Project Timeline

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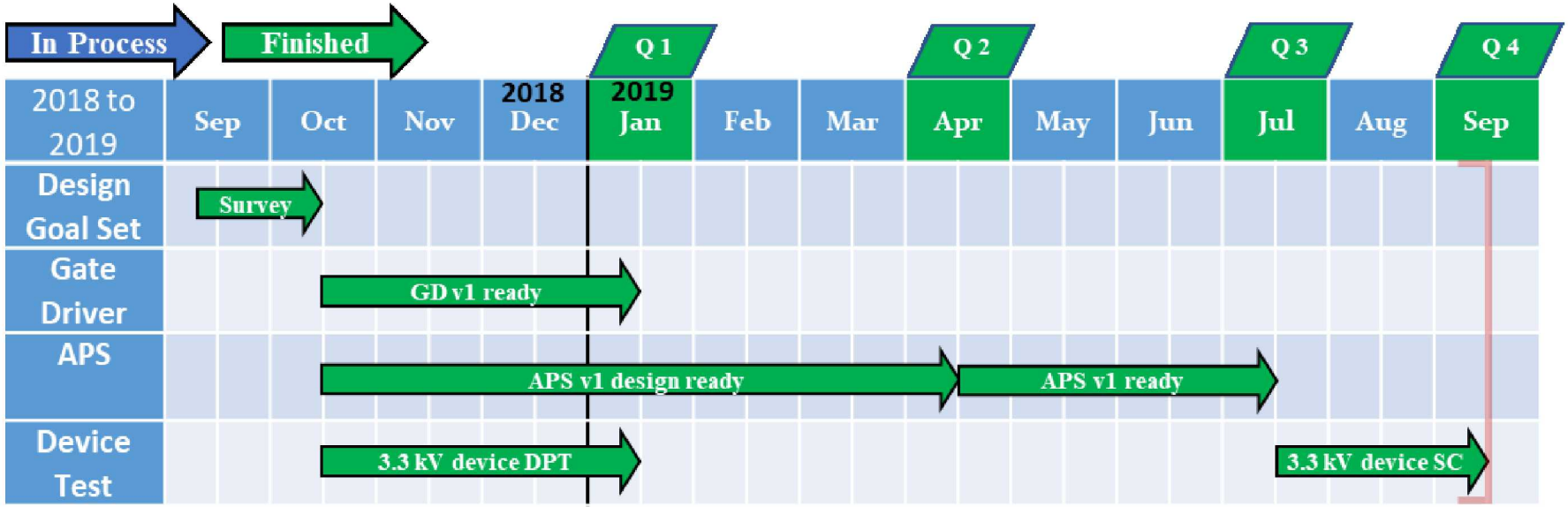
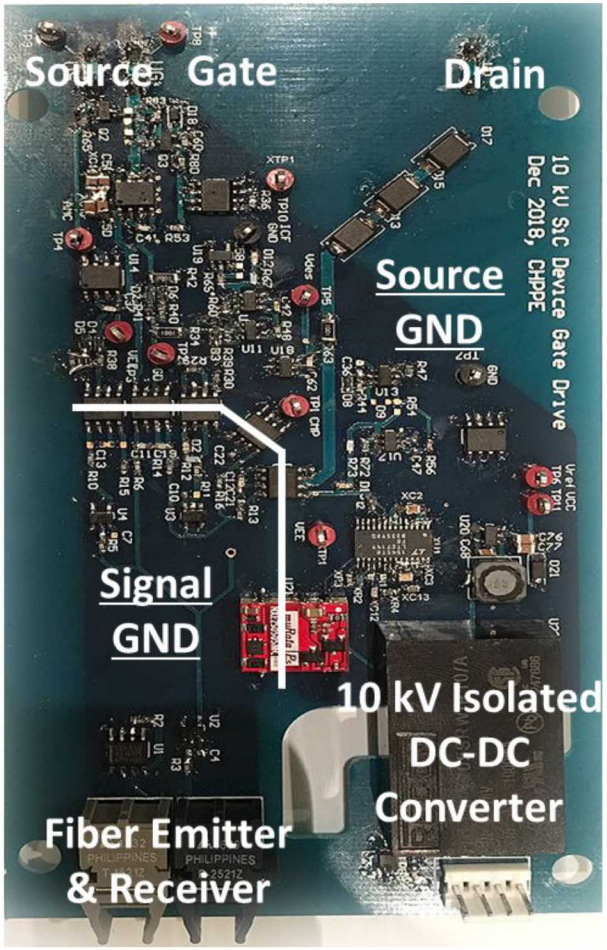
Key Milestones:

- **Year 1: Gate drive and auxiliary power supply design for medium-voltage SiC devices. [Finished]**
- **Year 2: Medium-voltage discrete SiC device evaluation and modeling.**
- **Year 3: Power module fabrication and DC/DC converter development.**



Year 1 milestones

Completed Gate Driver Design for 6.5 kV Device



6.5 kV device gate driver

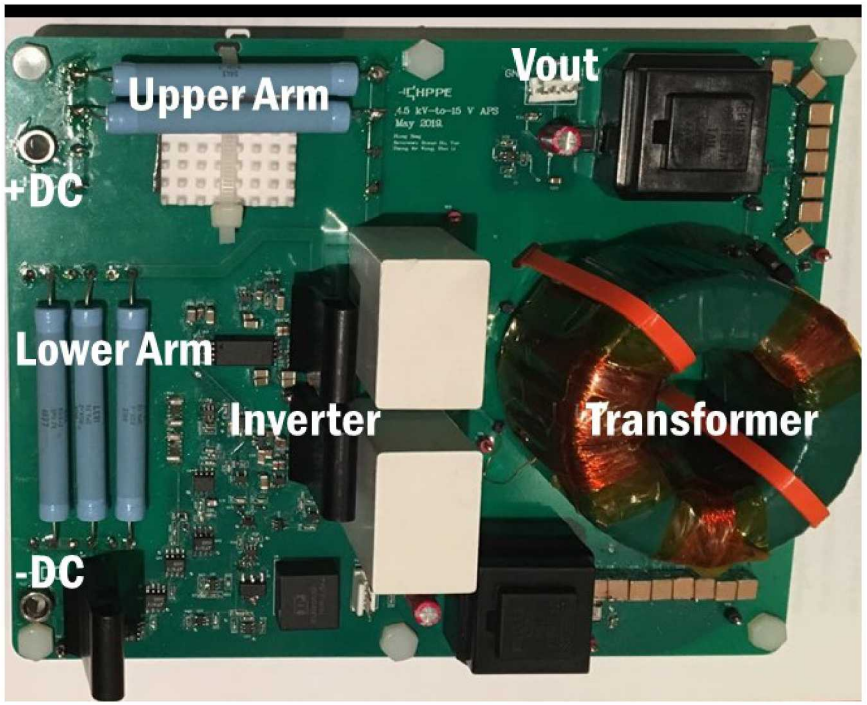
Specifications	Nominal Values
Output Voltage	+18 V / -4 V
Source Current	9 A
Sink Current	9 A
Insulation Voltage	6.5 kV
CMTI	150 kV/μs
Maximum Power	6 W

Functions:

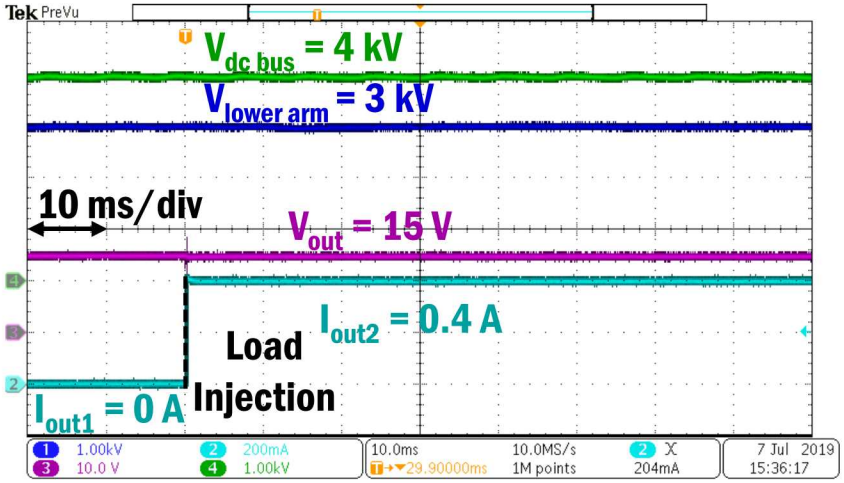
1. **Overcurrent Protection**
2. **Overvoltage Protection**
3. **Soft-off During Fault**
4. **Optical Diagnostics**

Auxiliary Power Supply Design Successfully Tested

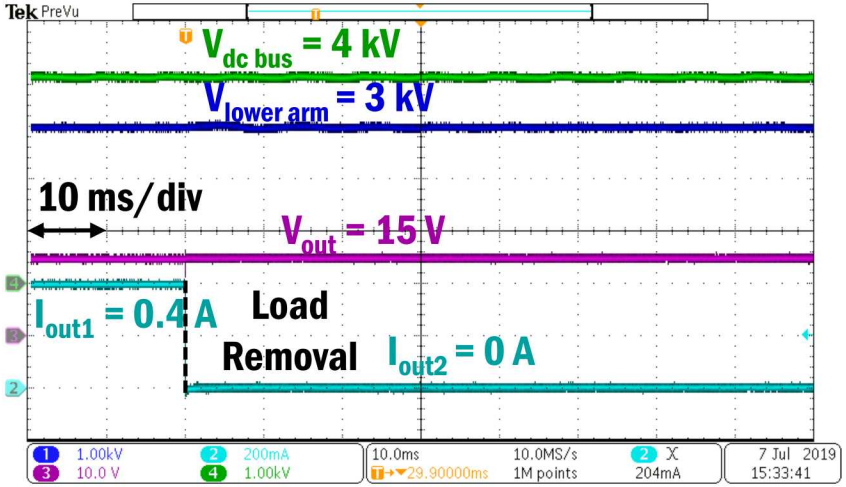
Specifications	Nominal Values
Input Voltage Range	3-4.5 kV
Output Voltage	15V
Maximum Output Power	10 W
Board Dimensions	152 x 188 mm^2



MVDC bus auxiliary power supply



Load injection transient at 4 kV DC bus



Load removal transient at 4 kV DC bus

Switching Loss Evaluation of GeneSiC 3.3 kV SiC MOSFET

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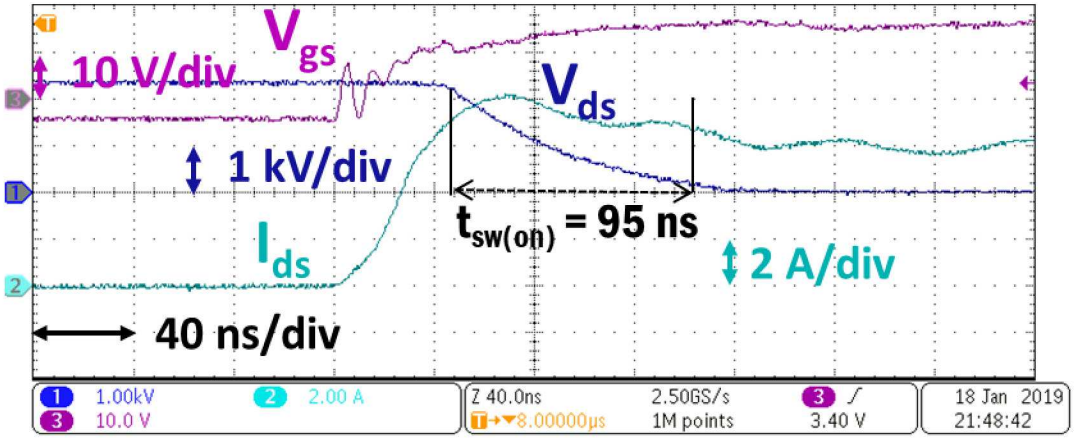
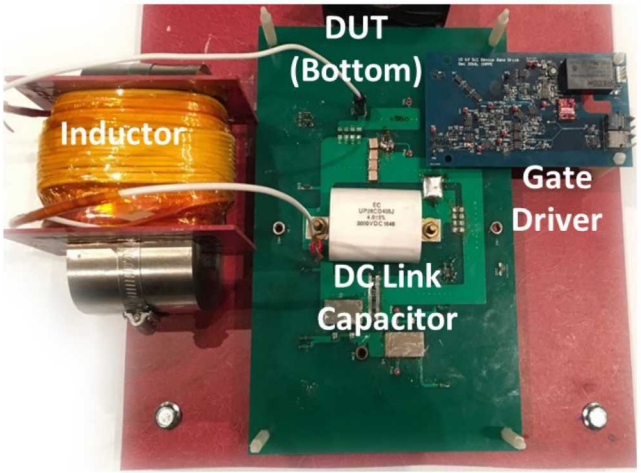
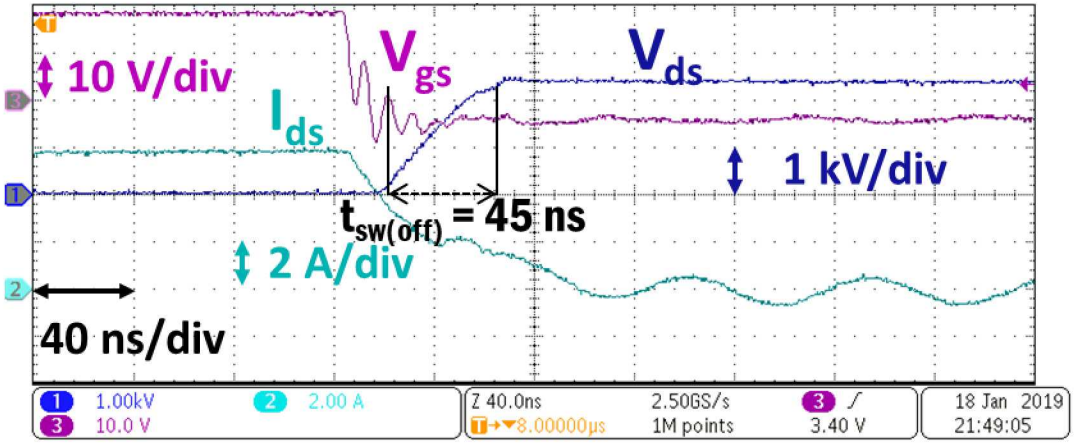
Specifications	Results
$t_{sw,on}$	95 ns
$t_{sw,off}$	45 ns
dV/dt_{on}	25 kV/μs
dV/dt_{off}	53 kV/μs
$E_{sw,on}$	850 μJ
$E_{sw,off}$	150 μJ



Device switches on (V_{dc} = 2.4 kV, I_{ds} = 6 A)

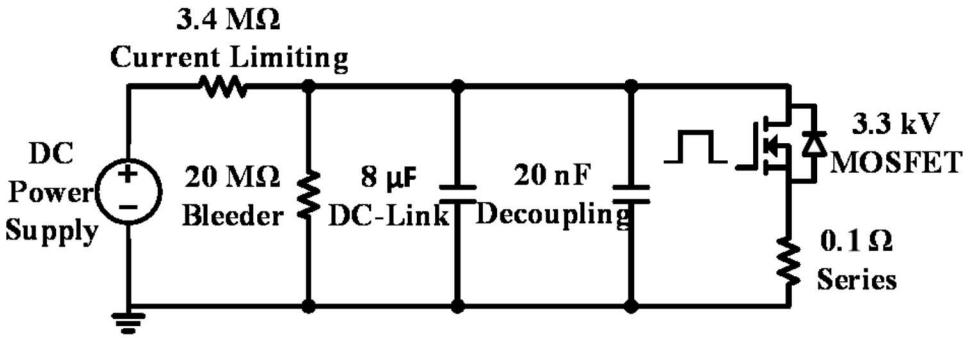


Double-pulse test setup

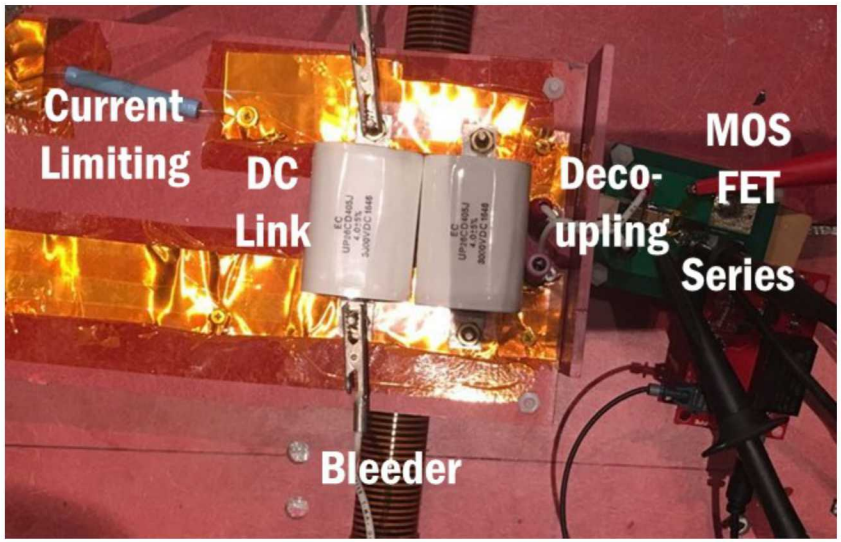


Device switches off (V_{dc} = 2.4 kV, I_{ds} = 6 A)

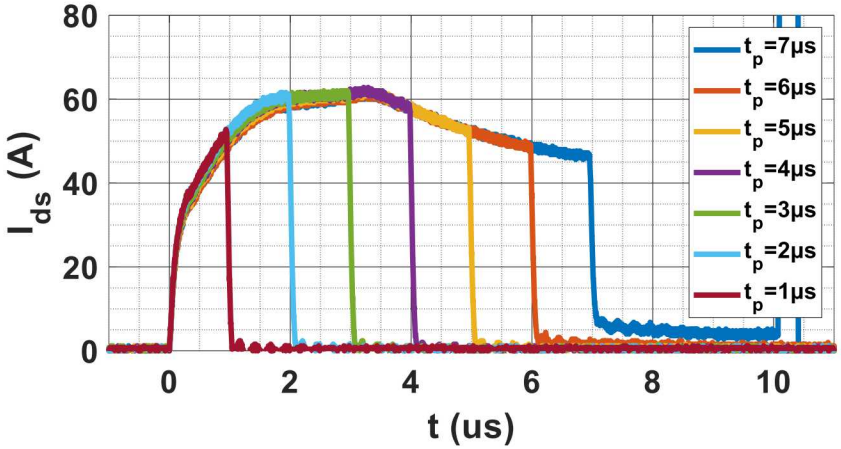
Short-Circuit Evaluation of GeneSiC 3.3 kV SiC MOSFET



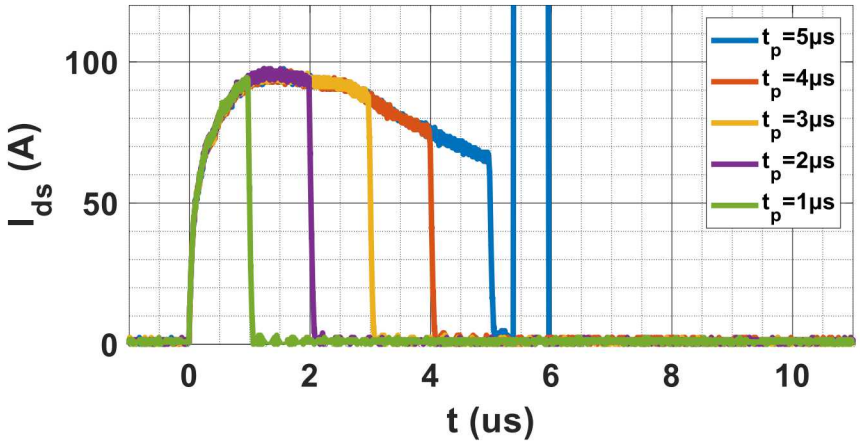
Short-circuit test circuit diagram



Short-circuit test setup



Short-circuit current in a long-channel designed MOSFET



Short-circuit current in a short-channel designed MOSFET

Summary

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Accomplishments:

- Built and tested gate driver and auxiliary power supply design for SiC devices.
- Measured switching losses in 3.3 kV SiC devices.
- Tested the short-circuit capabilities of the 3.3 kV SiC devices.

In Progress:

- Continue device evaluations to build device model for Year 2.

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