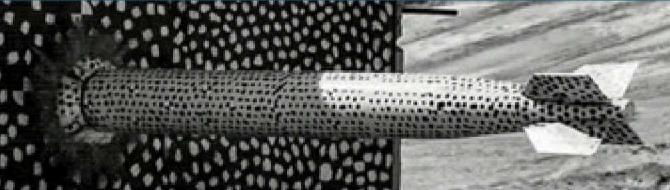


# Si Diode Speed Enhancements



*PRESENTED BY*

Q. Looker, M. Sanchez

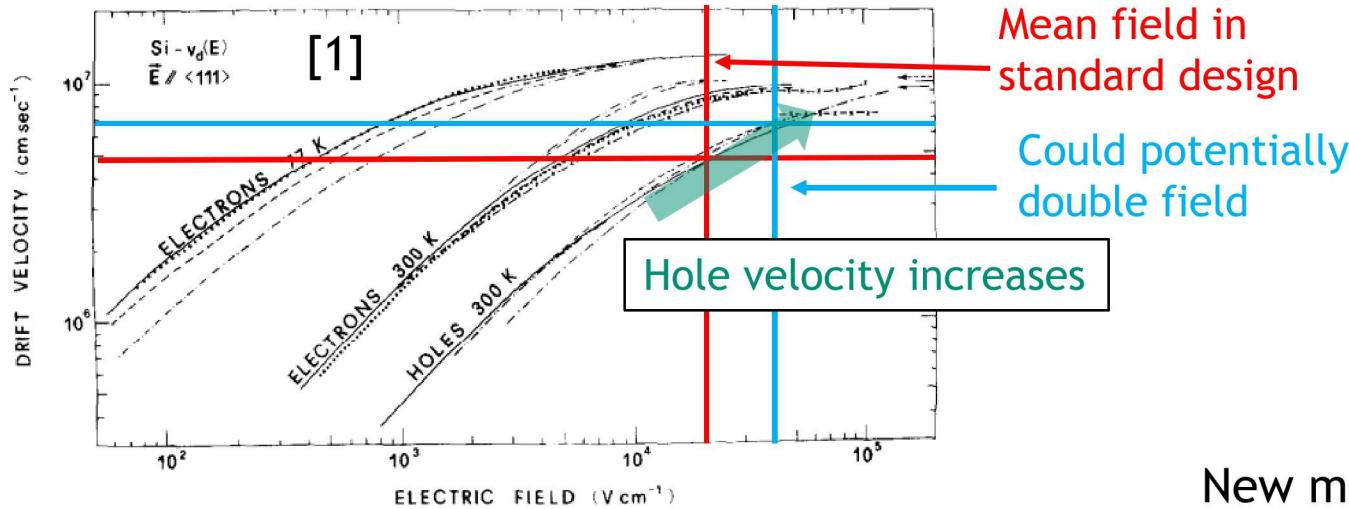


SAND2019-15004PE

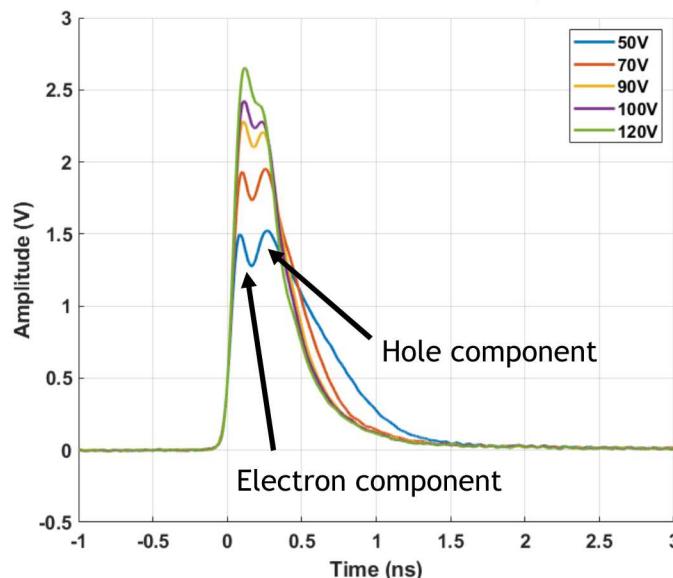


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# Increasing Electric Field Magnitude Can Speed Up Existing Designs

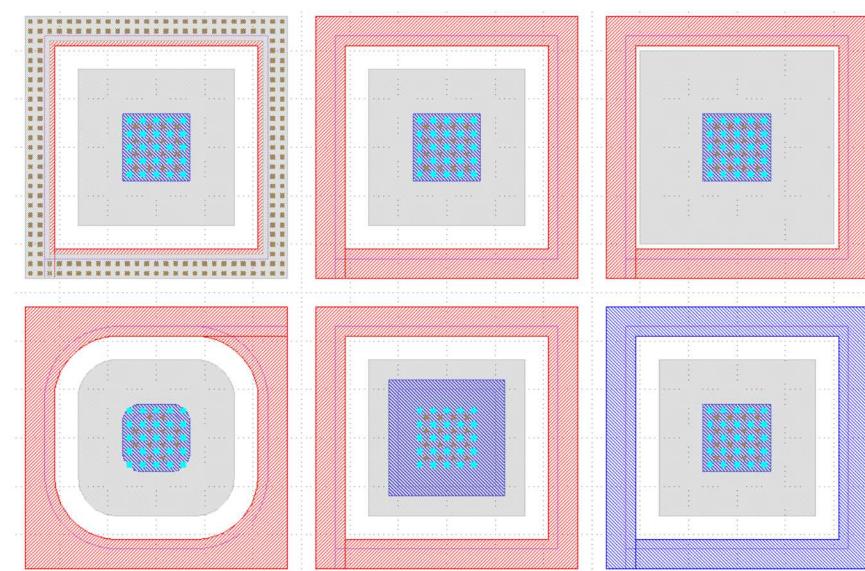


Pulsed Laser Measurement on 25  $\mu\text{m}$  Thick Si



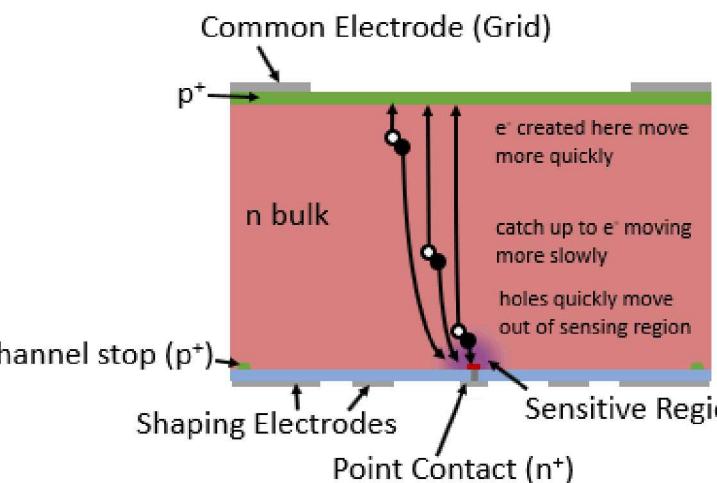
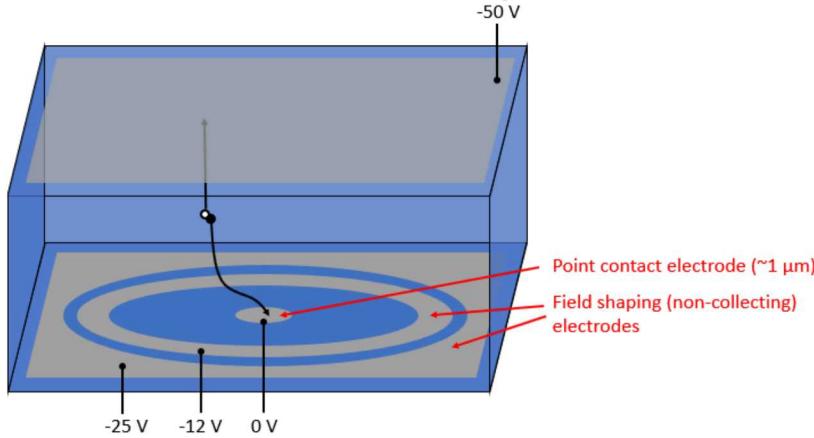
- Increasing applied bias increases carrier velocity
- Applied bias limited by diode breakdown voltage

New mask design with pixel design variants

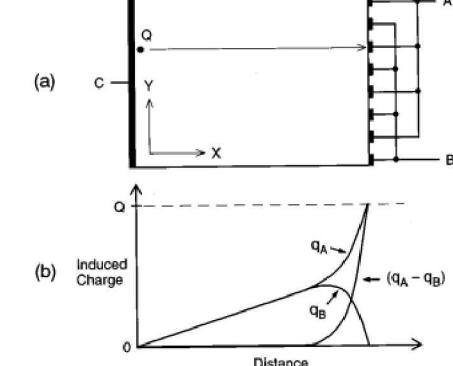
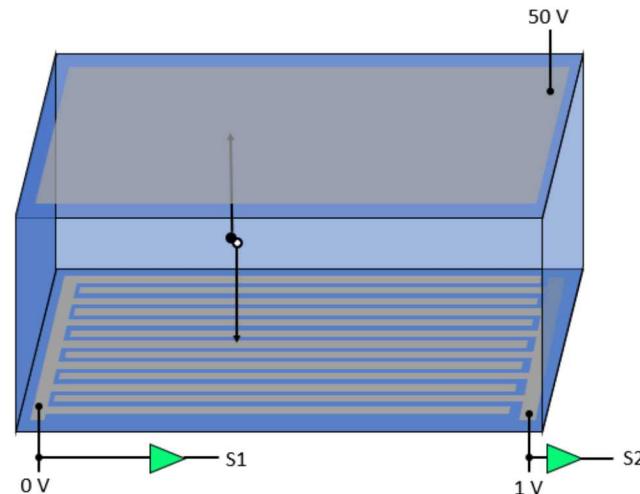


# 3 Alternate Electrode Configurations Could Potentially Compress Charge Collection Time

## Point Contact Concept



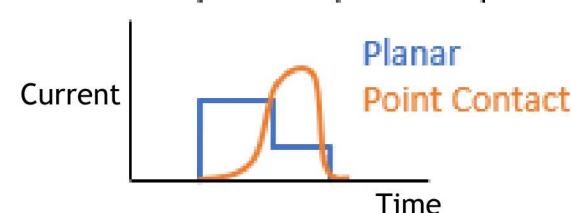
## Coplanar Grid Concept



P. Luke, APL 65, p.2884 (1994)

- Can operate as typical pixel when  $PV=S1+S2$
- Can increase dynamic range when  $PV=S1$ .  $S2$  shunted to VRST.
- Can reduce sensitive volume when  $PV=S1-S2$ , similar to point contact

## Anticipated Impulse Response



# A New Fabrication Process Could Yield a More Optimal Geometry

4

Doped polyfill column structures described in Parker 1997, Kenney 1999, Kok 2006, etc.

