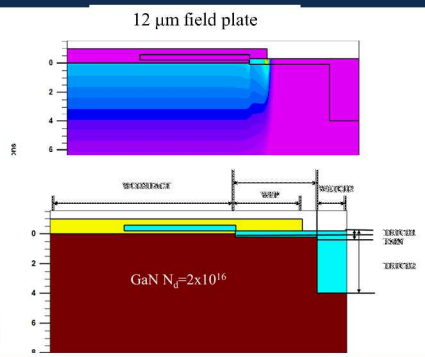
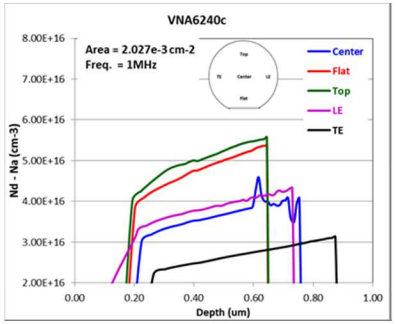
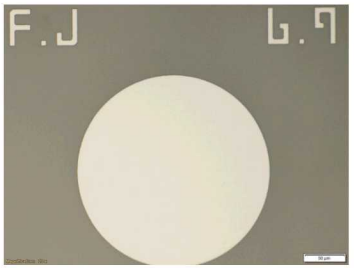
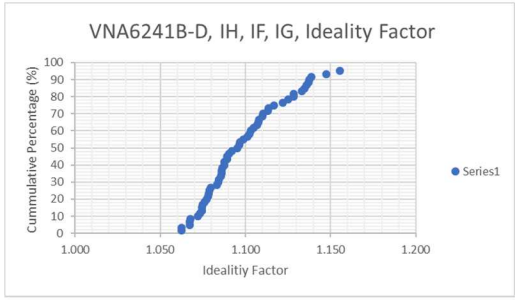
SAND2019-13922PE









Stable GaN-Based Schottky Contacts: Device Fabrication Update

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Program Update
Monterey, CA
November 5-8, 2019

The authors gratefully acknowledge the support from Capt. (Ret.) L. Petersen of ONR, as well as the interactions with our collaborator Prof. T. Weatherford (NPS)

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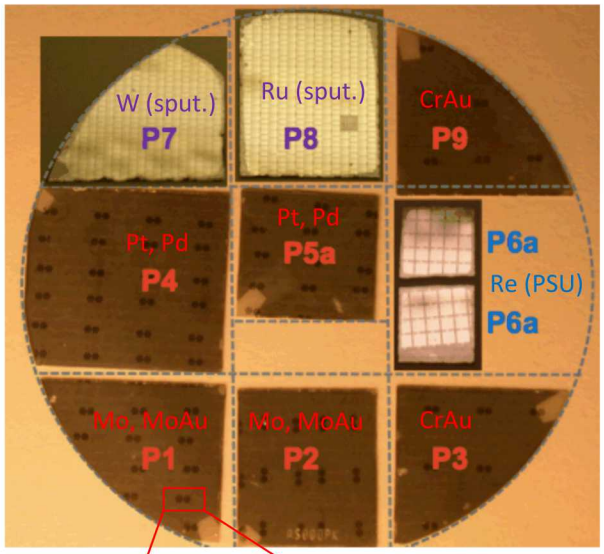
Pd Schottky Diodes: TCAD Simulation, Material Growth, Fabrication, and Characterization

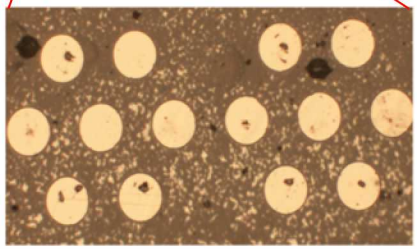
SANDIA NATIONAL LABORATORIES

Outline

- Progress – Previous Years
- 3rd Generation Device Design
- TCAD Simulations
- Improvement of Schottky junction
- Investigation of Surface Passivation Methods
- Packaging Development
- Paths Forward

Progress – Previous Years (Gen 1)

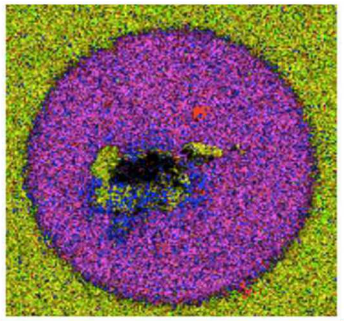




150 μm diameter

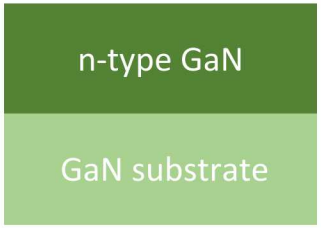
- Original sample set was intended as a quick way to survey a variety of Schottky metals and surface cleans
  - Simple shadow mask process (mostly)
  - Mo, Pt, Pd, W, Ru, CrAu, MoAu, Re
  - Not an optimized design

- Some samples showed catastrophic failures
  - Believed to be due to excessively high local current density
  - "Extrinsic" failure mode not of interest for fundamental physics understanding
  - Motivates a more comprehensive fabrication process

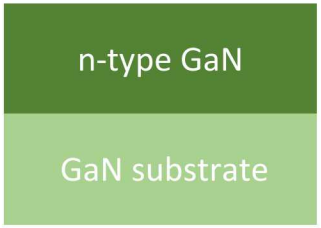


Gen 2 Process Flow

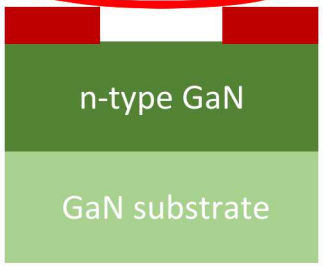
1) GaN growth



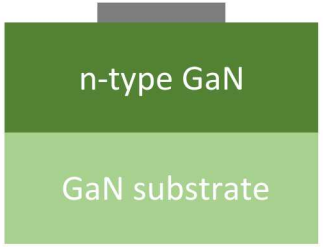
2) Solvent clean



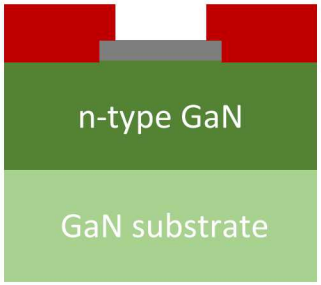
3) Lithography and surface preparation



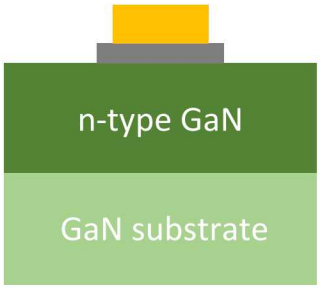
4) Schottky metal deposition and liftoff



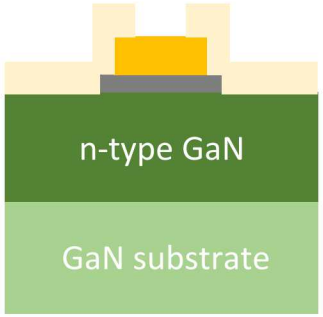
5) Lithography



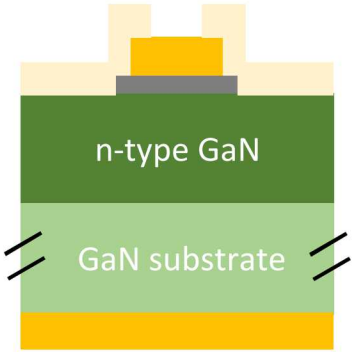
6) Bond pad metal deposition and liftoff



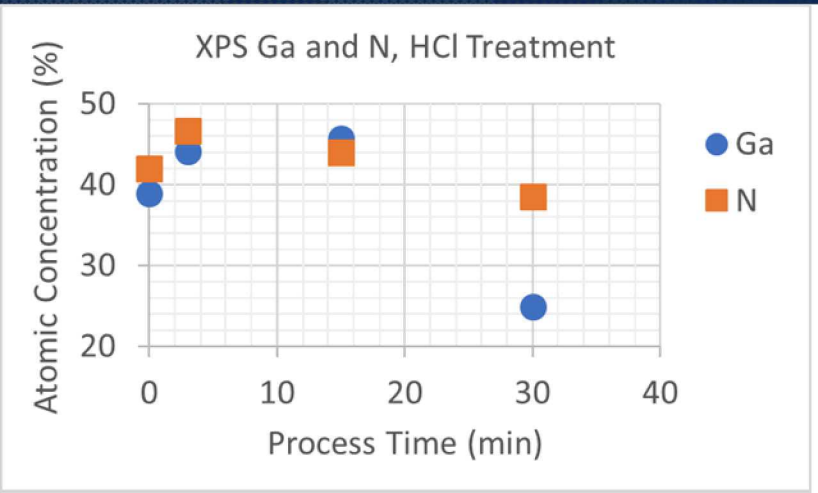
7) Dielectric passivation and window etch

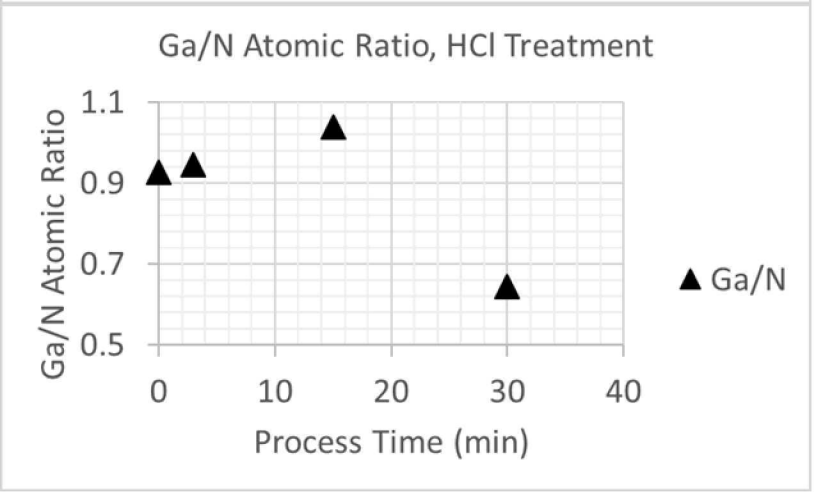


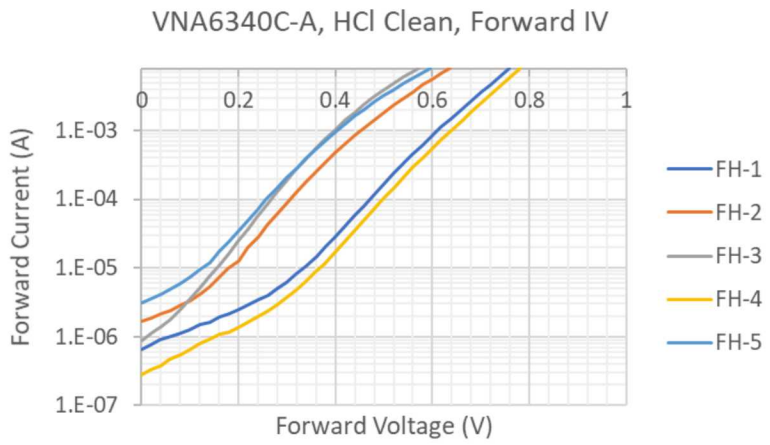
8) Substrate thinning and backside metal deposition

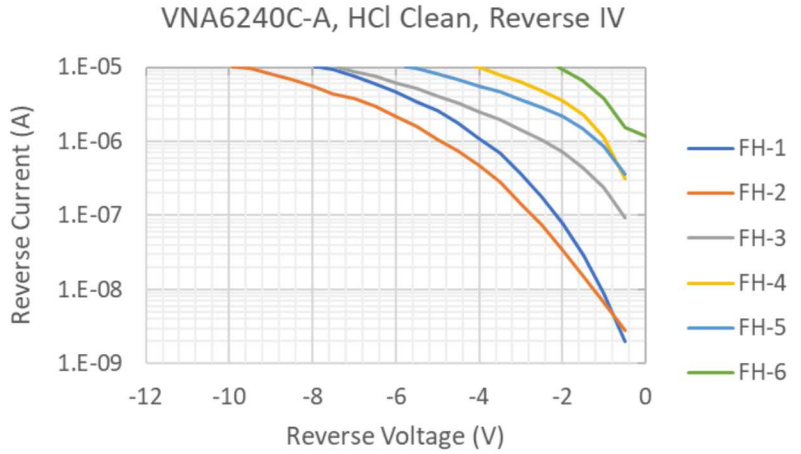


80 C HCl Treatments Before Pd Deposition





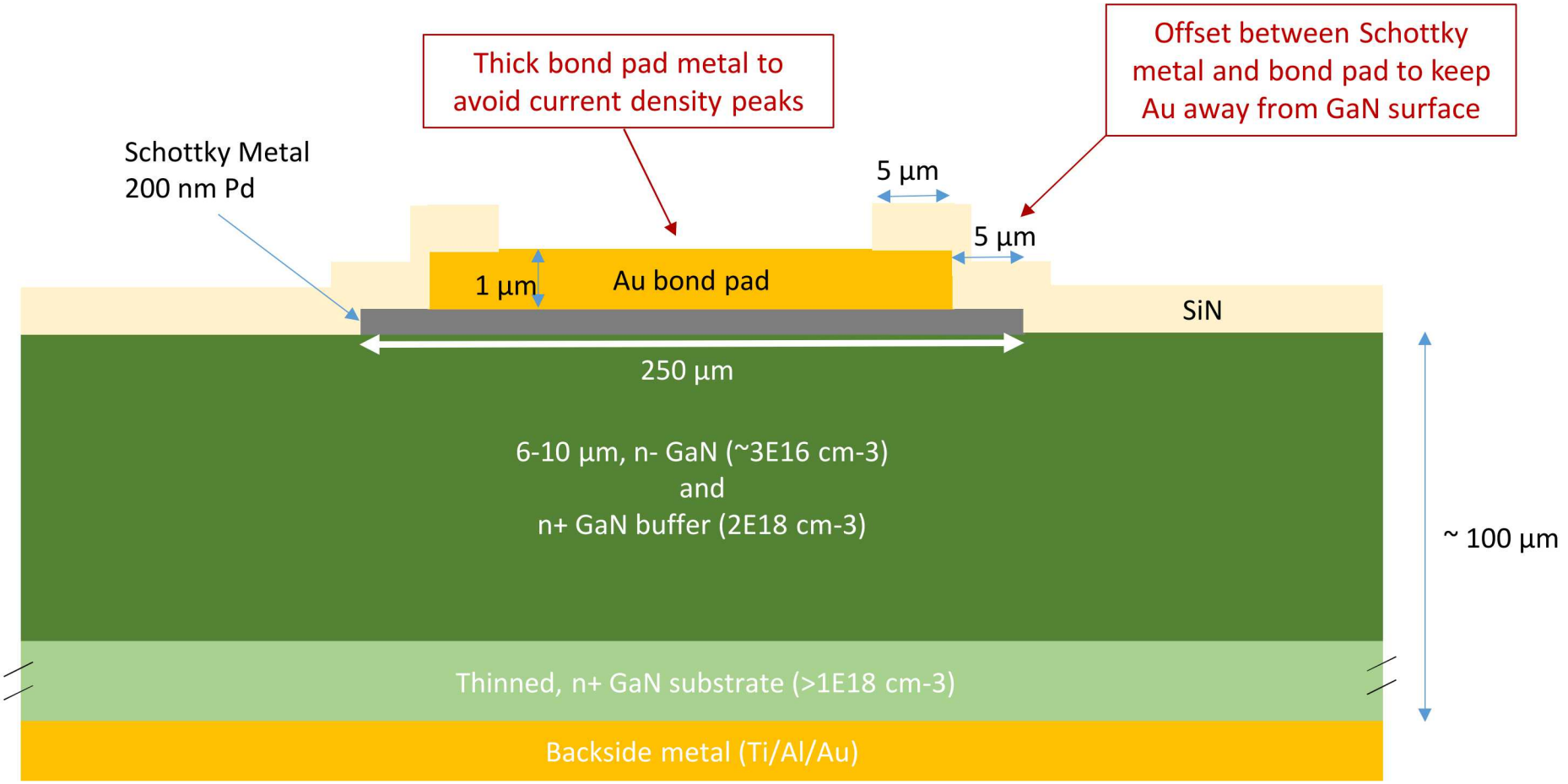




- Similar Ga and N on surface except at 30 min. Ga/N ratio evolves with HCl etch time.
- Devices leaky in forward and reverse bias operation

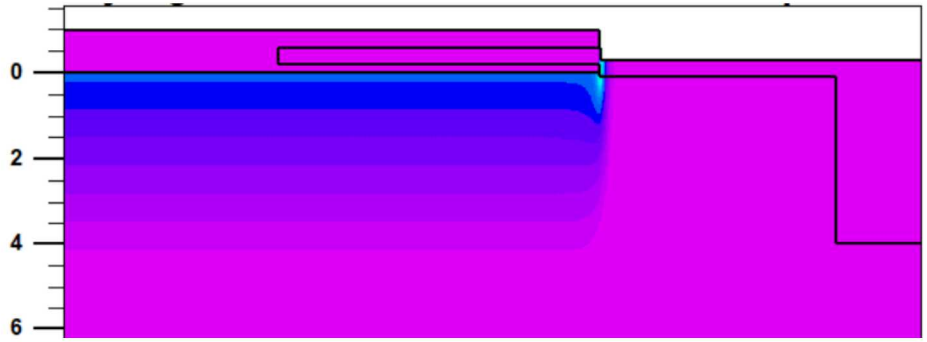
Based on work by P. Reddy, B. Sarkar, F. Kaess, M. Gerhold, E. Kohn, R. Collazo, and Z. Sitar, APL 110, 011603 (2017)

Cross-Section of 3rd Generation Schottky Diode Design

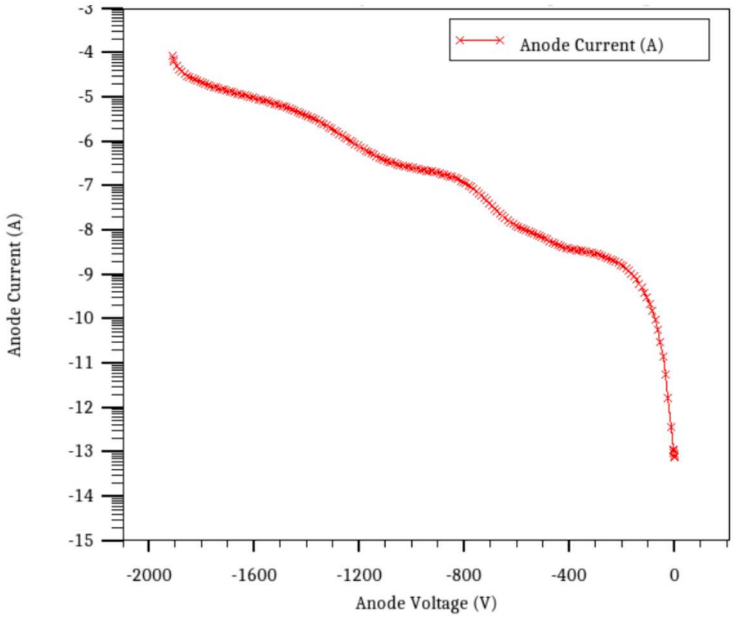


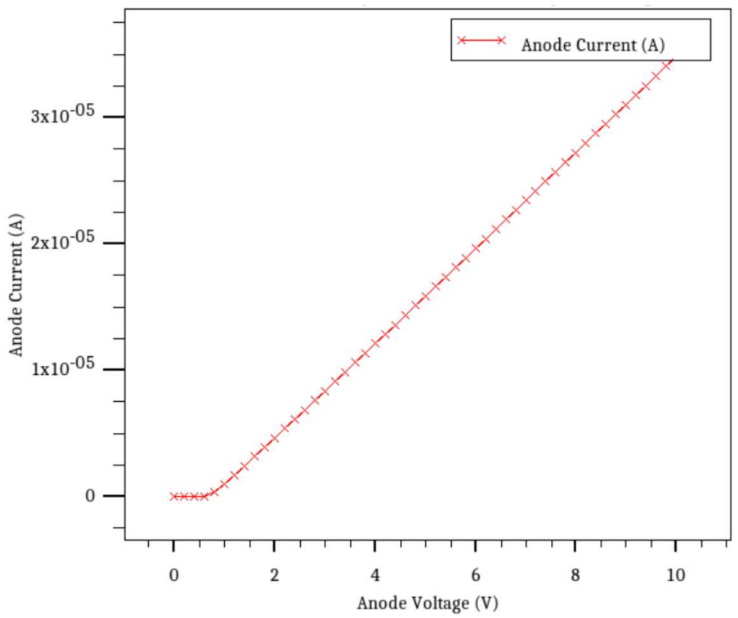
Investigating Field Plates to extend reverse breakdown voltage

Silvaco TCAD Simulations

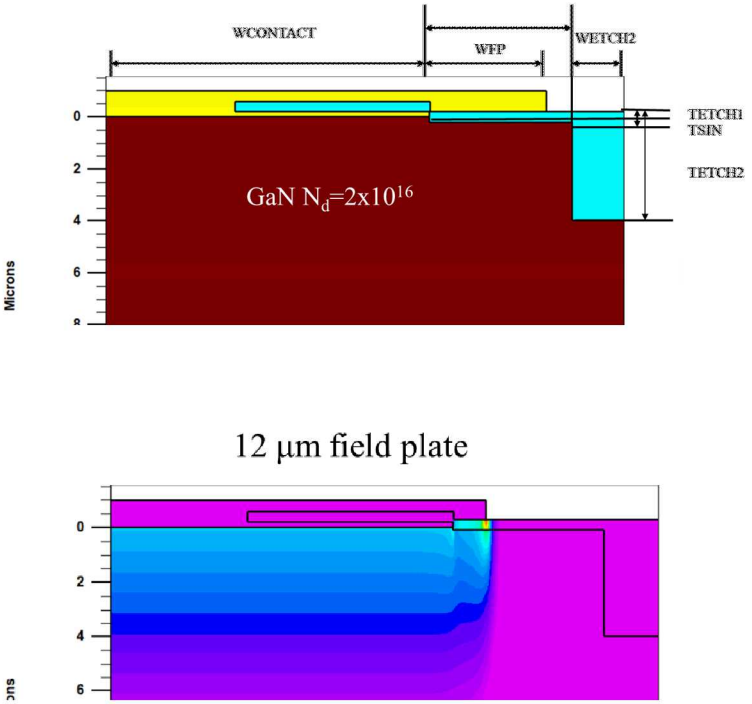


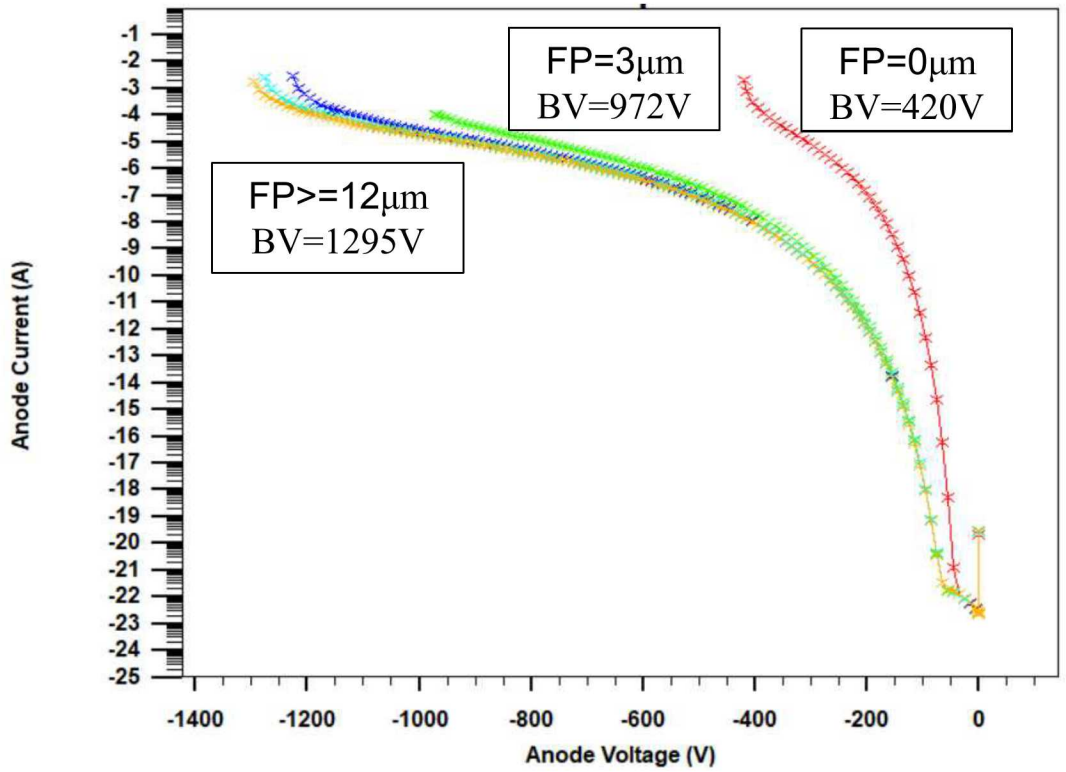
Used different TCAD models to try and match experimental results Universal Schottky Tunneling model and Phonon Assisted Electron Tunneling models showed closest match





Silvaco TCAD Simulations – Field Plates

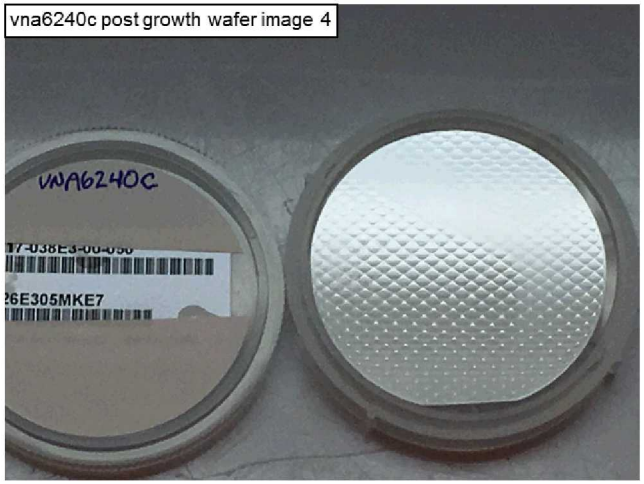




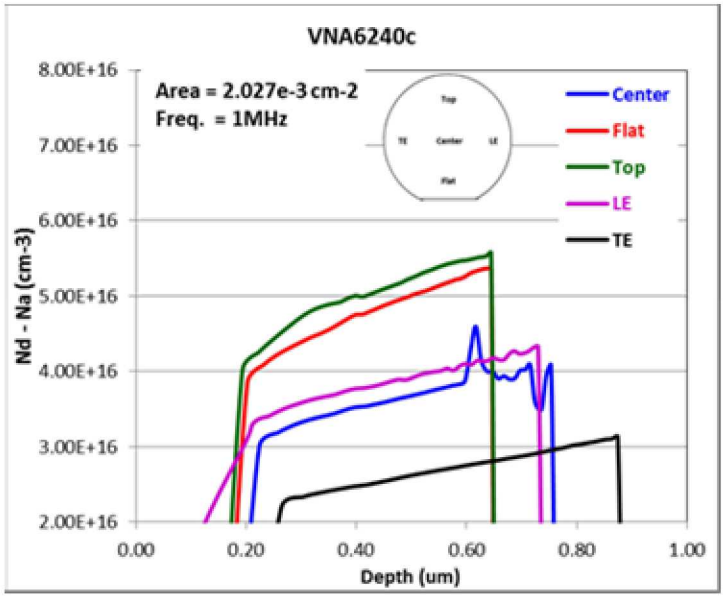
- Simulated effects of Field Plate dimension and isolation etch
- Field plates can extend reverse breakdown voltage significantly
- Field plates longer than ~ 15 µm do not significantly extend Vbr (400 nm dielectric)
- Device isolation feature doesn't improve simulated performance

MOCVD Wafer Growth

- Wafers grown on HVPE GaN substrates from Mitsubishi (no dot-core structures)
- Drift layer carrier concentration ranges from 2-5 E16 cm^{-3} across the 2” wafer (example data shown to the right)
- Similar material being supplied to PSU under this project.



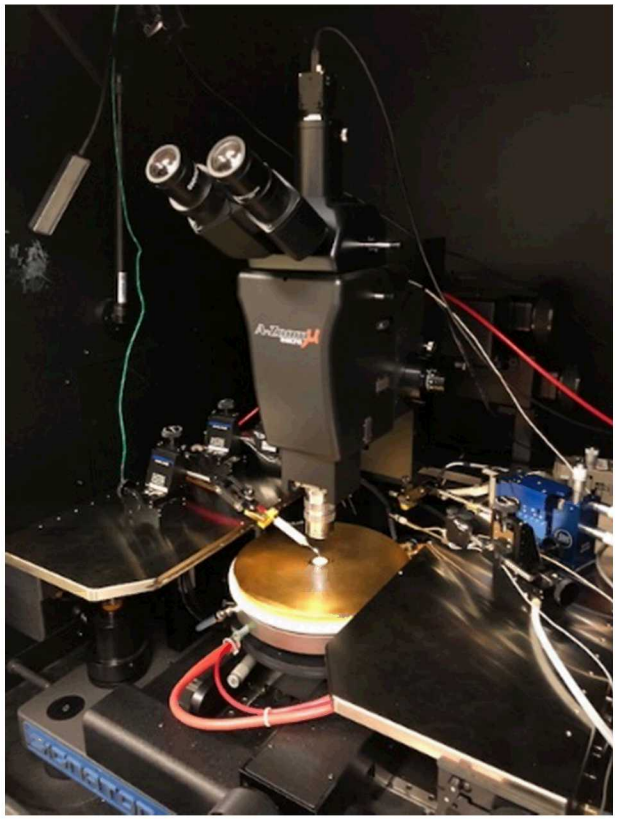
Optical images (pattern is from reflection of light fixtures)



Typical Capacitance-Voltage data for net carrier concentration in n-GaN layer

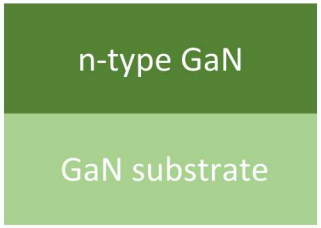
Characterization of Diodes

- Characterized processed wafers using High Voltage probe station
  - Used manual and auto-prober for characterizing these samples
- Tested devices under FC-70 (Fluorinert) to avoid surface breakdown (not necessary for these devices)
- Used manual probe station for shadow mask samples
- Used auto-prober to test larger numbers of devices on wafers with 2nd generation mask set.

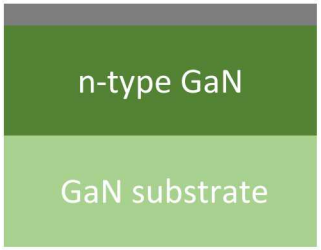


Gen 3 Process Flow

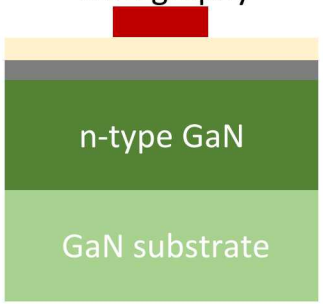
1) GaN growth



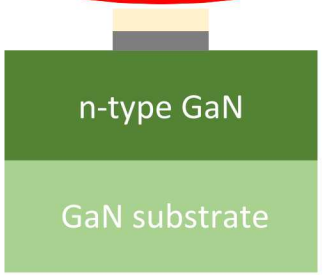
2) Ozone Clean, HF, DI, blanket deposit 200 nm Pd



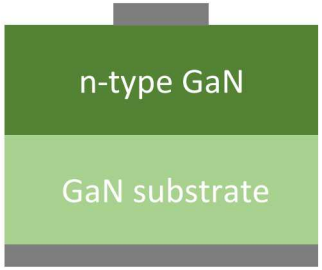
3) SiN Deposition, Lithography



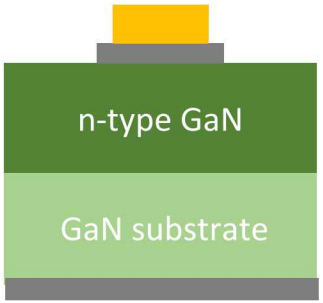
4) Etch SiN, Etch Pd



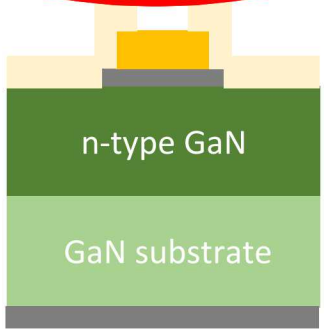
5) Remove SiN, Backside Ti/Al, Test



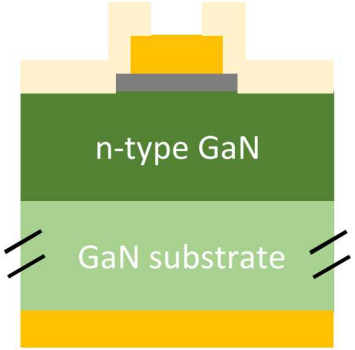
6) Bond pad metal deposition and liftoff



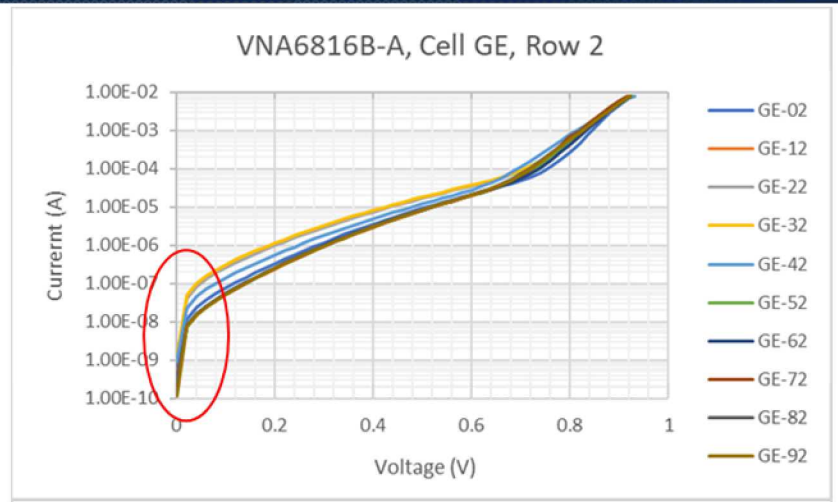
7) Dielectric passivation and window etch

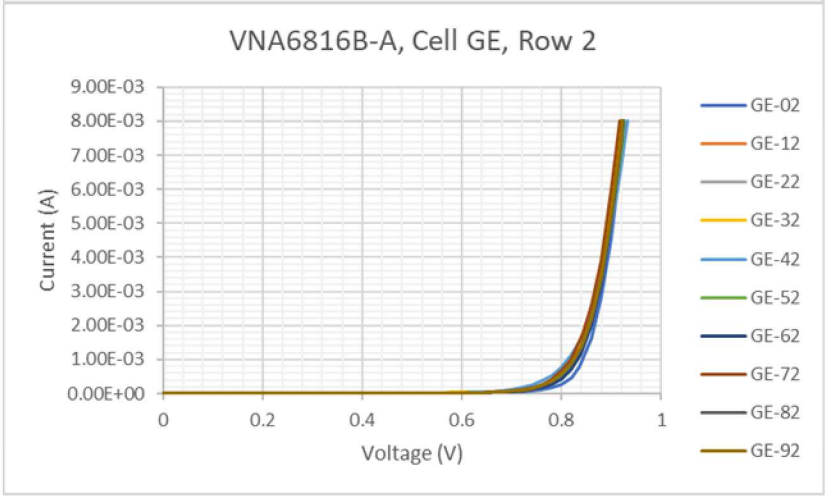


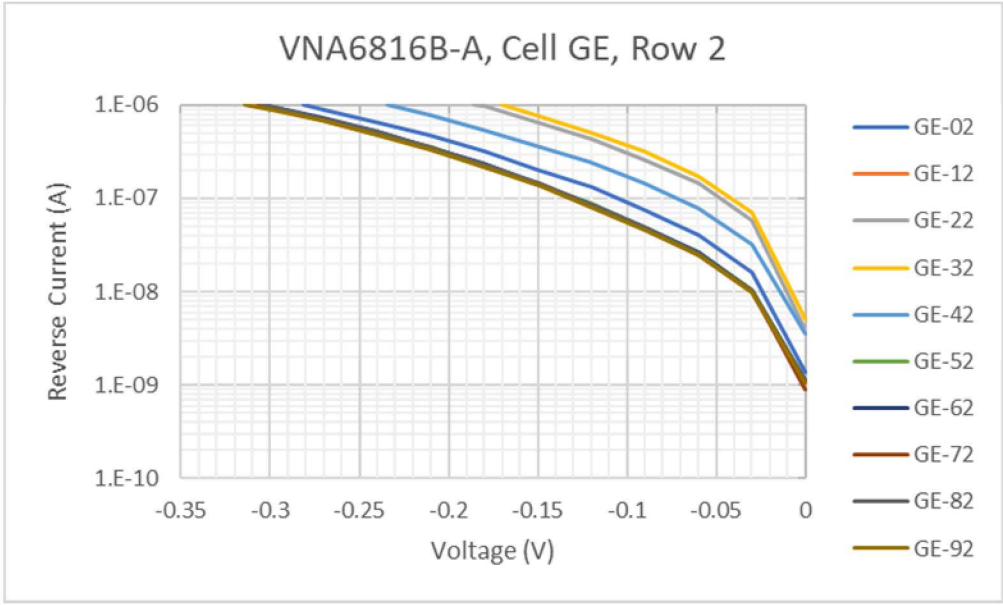
8) Substrate thinning and backside metal deposition



1) Pd Only – Dry Etch Removal of Pd

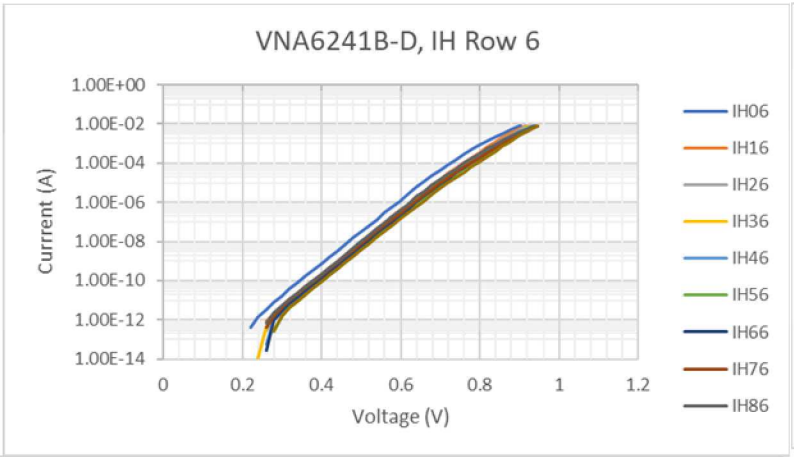


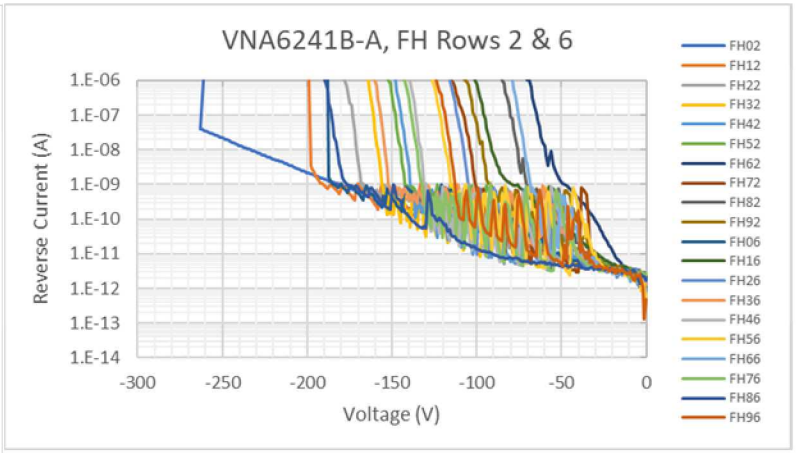


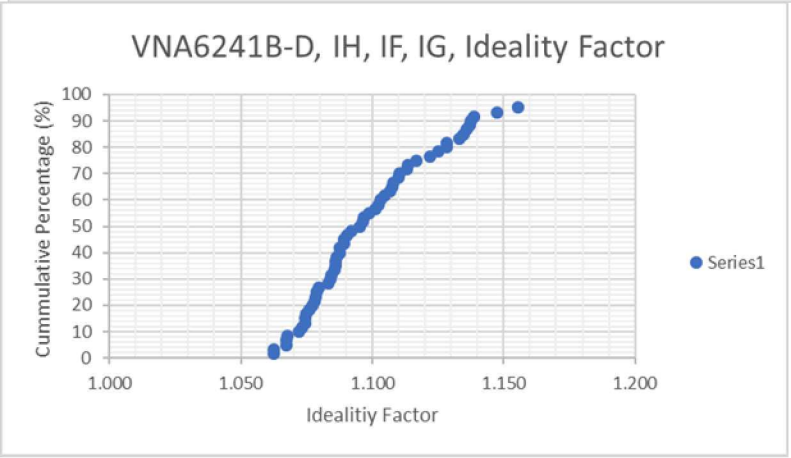


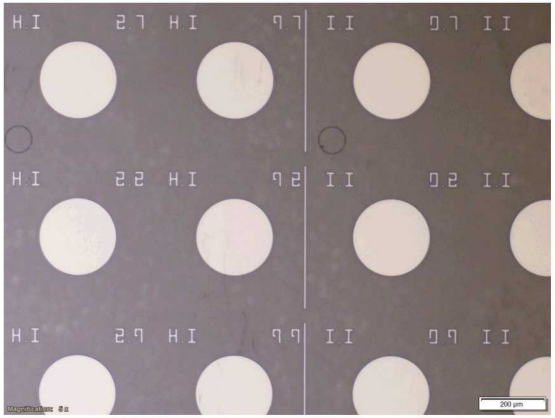
- Dry Etch of Pd using SiN mask investigated (A. Ozbek, and B. Baliga, IEEE EDL 32 (3), 2011)
- Modest forward leakage currents
- High reverse leakage currents

2) Pd Only – Dry Etch + Wet Etch (AR) of Pd



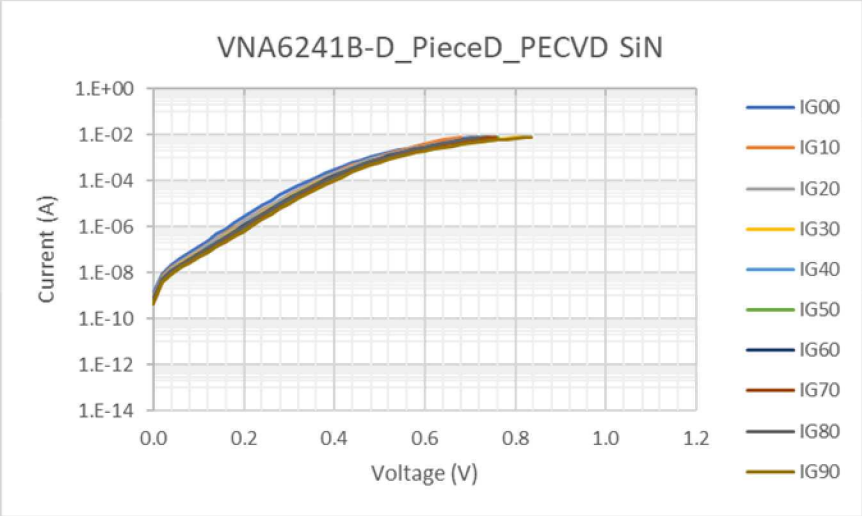


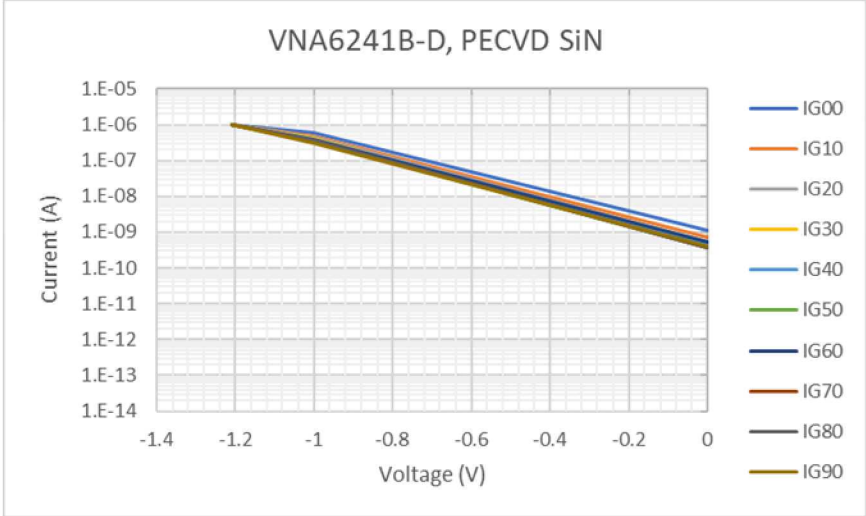


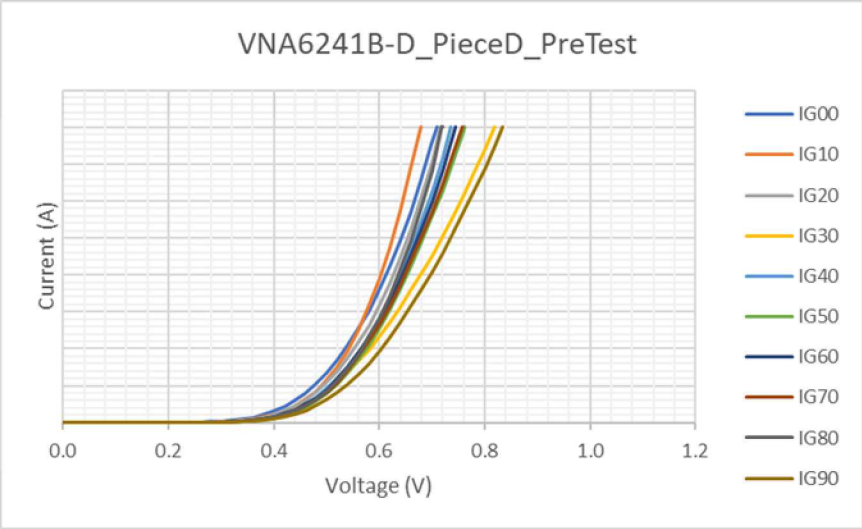


- Dry etch + wet etch (Aqua Regia) using SiN mask
- Low forward leakage currents with decent ideality factors and uniformity
- Low reverse leakage currents

3) Full Process – PECVD SiN

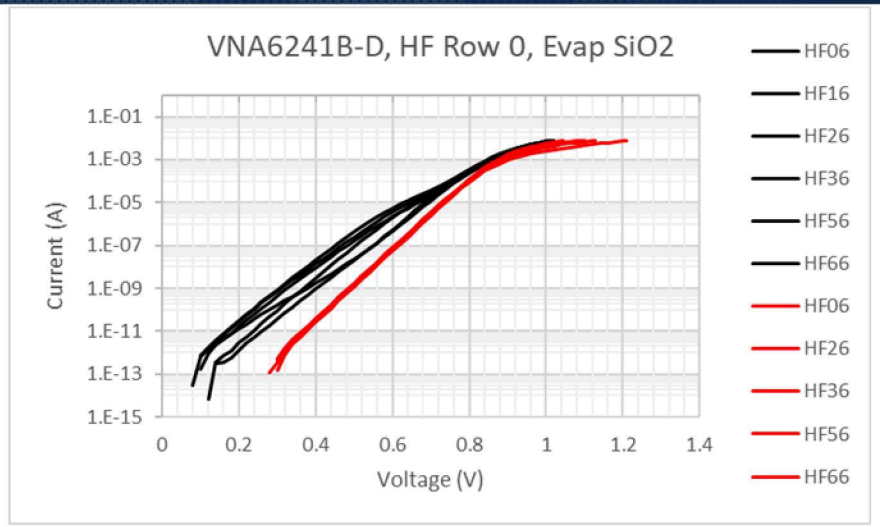


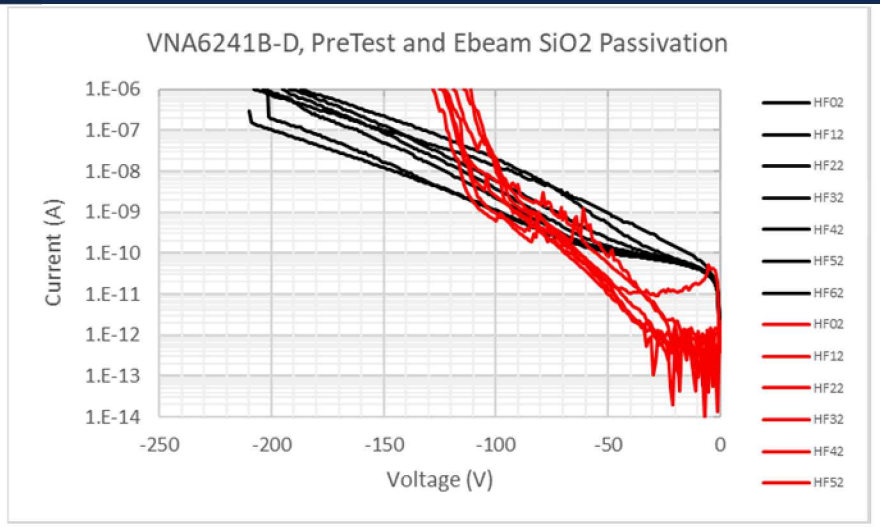


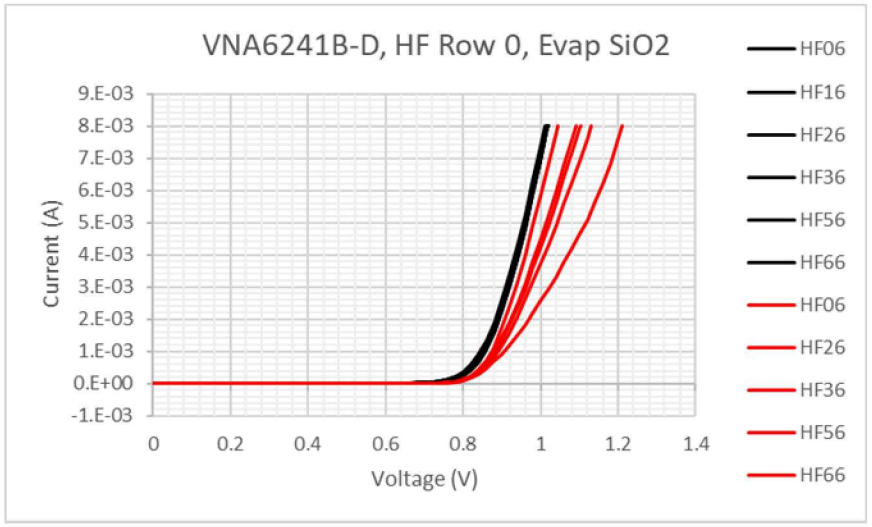


- Dry etch + wet etch (Aqua Regia) using SiN mask
- Finish process with Au bond pads, PECVD SiN passivation
- Test before wafer thinning showed very high forward and reverse leakage currents
- Verified cause is SiN passivation

4) Full Process – Ebeam SiO2

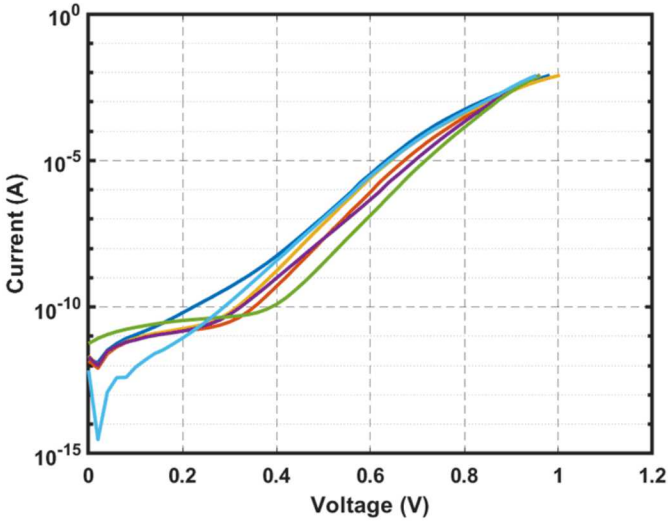


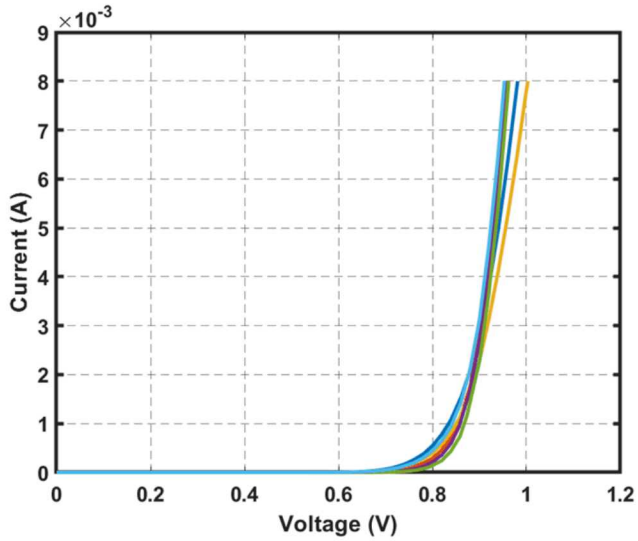


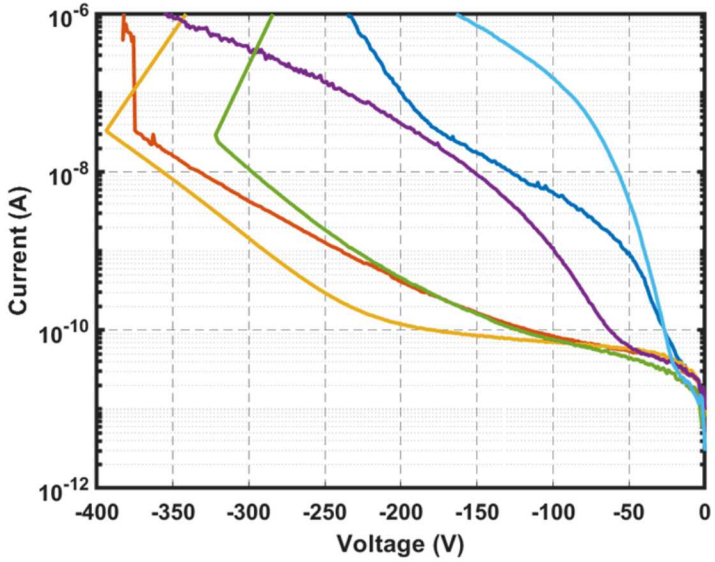


- Dry etch + wet etch (Aqua Regia) using SiN mask
- Finish process with Au bond pads, Evaporated SiO2 passivation
- Test before wafer thinning showed slightly higher forward leakage
- Improved performance
- Investigating other non-plasma passivation methods

5) Full Process – Ebeam SiO2 and Field Plates



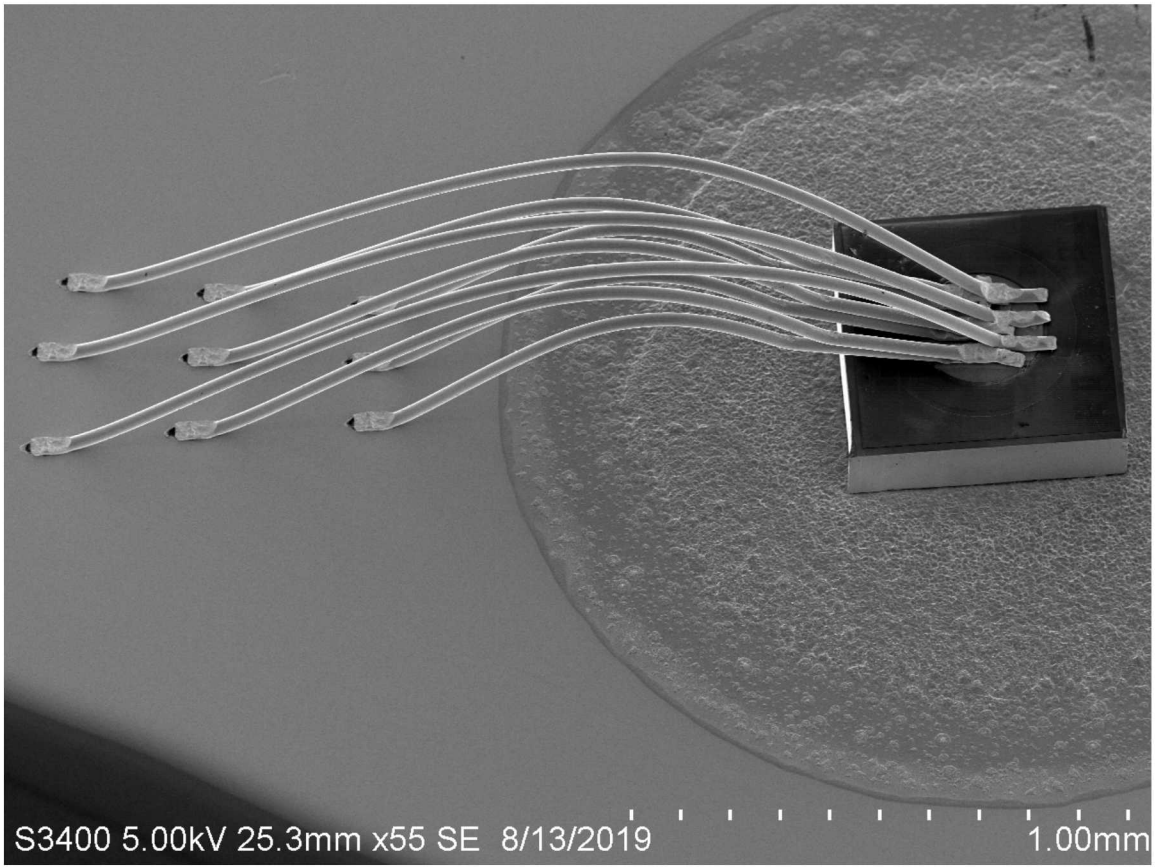




- Applied field plates connected to Au bond pad after SiO2 passivation
- Forward leakage current reduced with field plates.
- Reverse leakage current dramatically reduced with field plates.
- Voltage at -1 uA of leakage 300-400 V on better devices

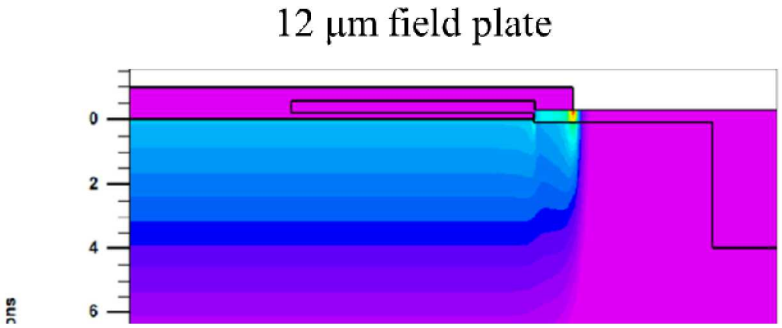
Packaging Development

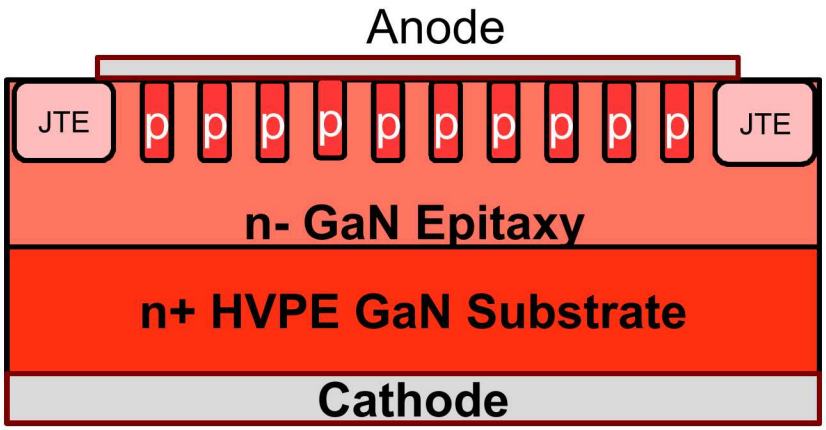
- Engaged Sandia production packaging team to develop multi-wire bond for 3A forward current
- Current capacity of 25 µm diameter wire ~ 0.5 A
- Successfully bonded 9 wires onto same size contact pad on test devices
- Will use same process for latest iteration of SNL Schottky diodes



Future Directions

- Continuing efforts to improve Schottky diode performance
- Continue to study high-current performance stability
- For improved reverse bias performance, Junction Barrier Schottky (JBS) diodes are preferred
- Being developed in existing DOE program for insertion into electric vehicles





Summary

- Previous experiments with different metals (shadow mask) drove decision for Pd as our choice for the metal contact (Gen1)
- Gen2 devices used lift-off technique to form metal contacts
  - Devices showed substantial leakage in forward and reverse operation
  - XPS study performed to improve performance (still leaky)
- Gen3 devices used ozone clean and blanket Pd metal deposition
  - Much improved results in forward and reverse
  - Ideality factors between 1.05 and 1.15
- PECVD SiN passivation in final wafer process caused significant leakage in forward and reverse
- Alternative passivation method (e-beam SiO2) improved results
- Field plates further improve results
- TCAD models developed to approximate experimental results
- Wafers in process and packaging for high-current testing
- Future efforts toward JBS diodes for higher reverse breakdown