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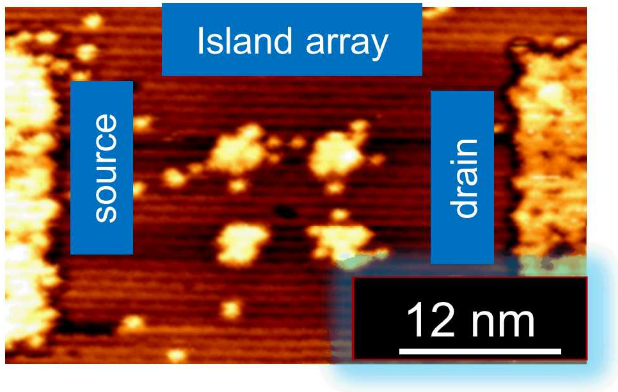

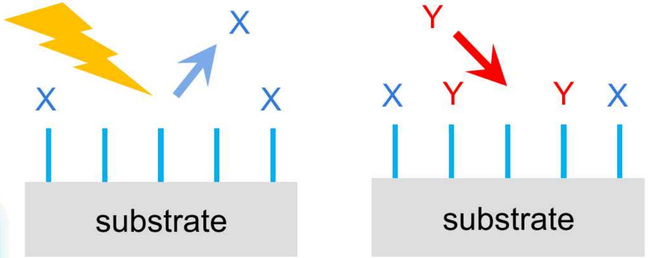

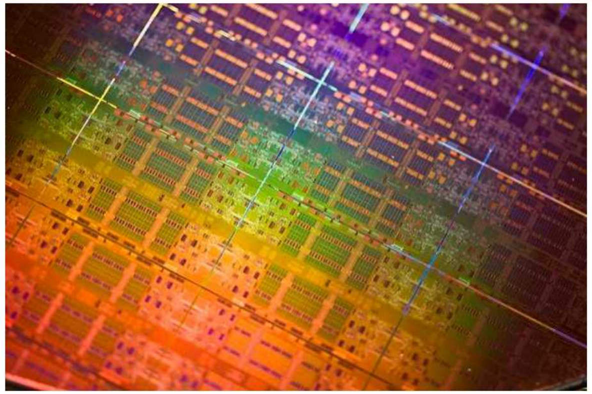

FAIR DEAL GC Thrust 1 : APAM devices

Shashank Misra, Lisa Tracy, Tzu-Ming Lu, Aaron Katzenmeyer

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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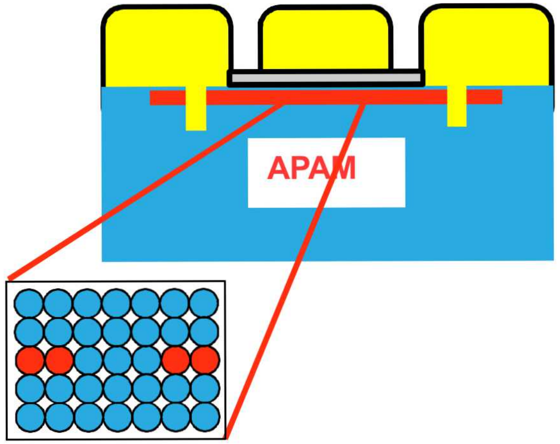
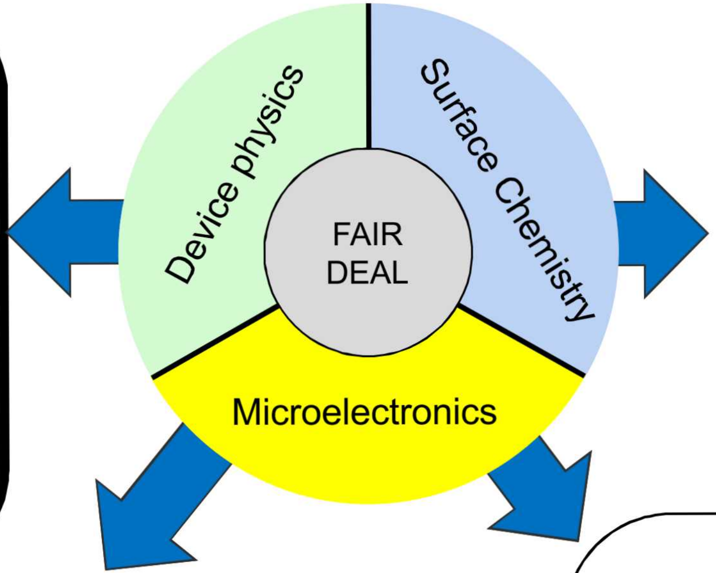
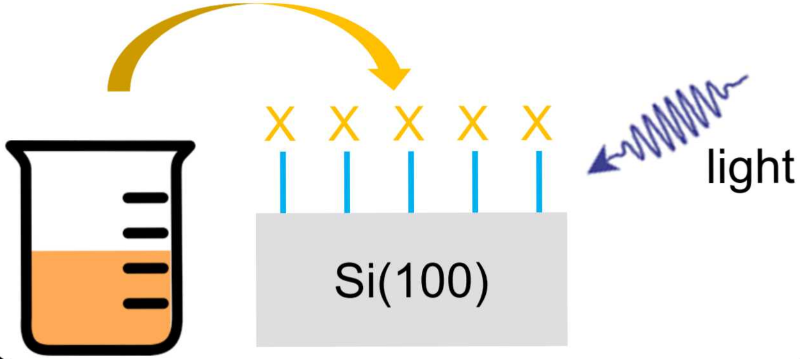
Digital electronics at the atomic limit (DEAL)

Thrust 1: APAM-enabled Devices

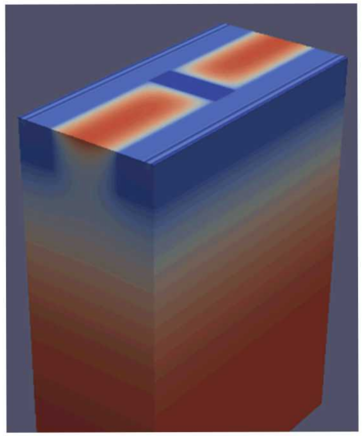




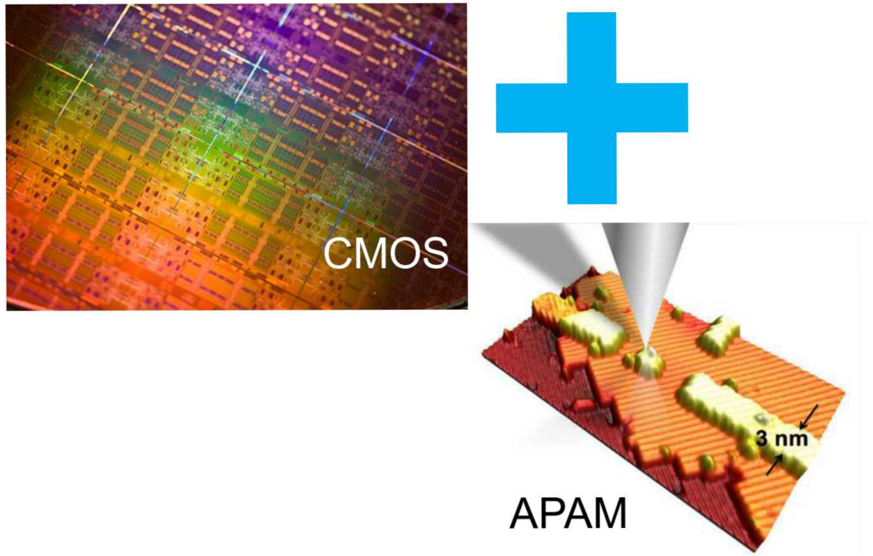
Thrust 4: Application Platform



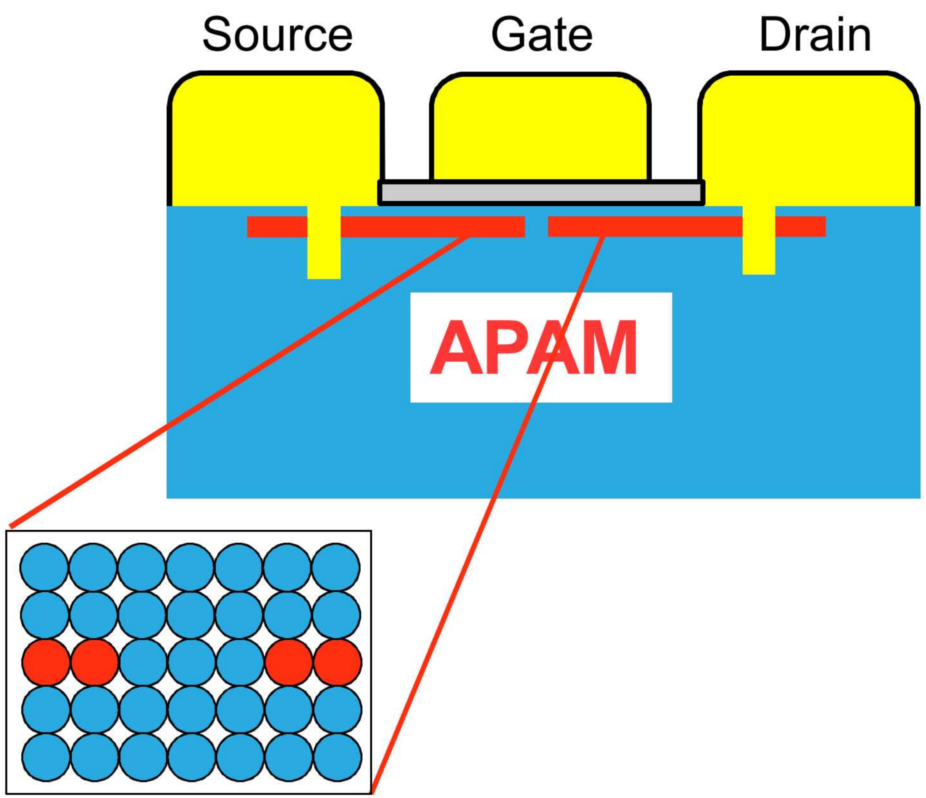
Thrust 2: APAM Modeling



Thrust 3: CMOS Integration

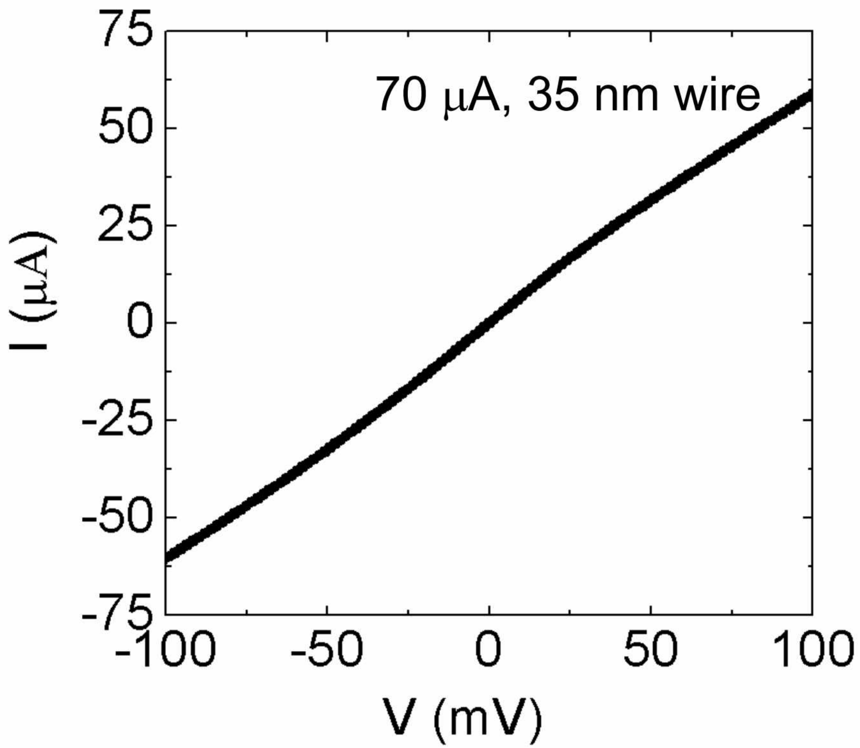


APAM – opportunity for electrical devices



- **Atomic-scale control over device physics**
- **APAM enhances silicon itself**

Ultra-doping = high current densities

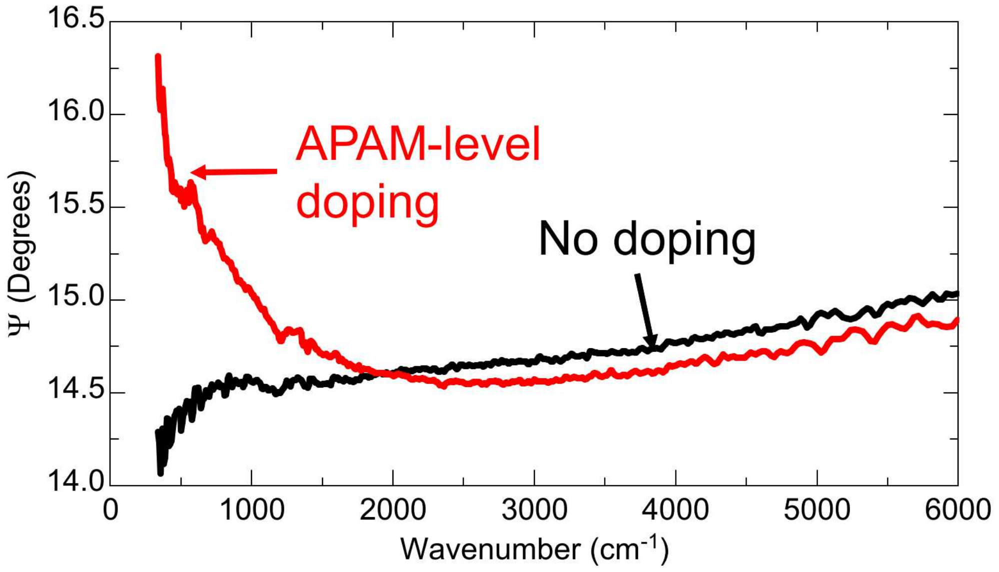


APAM nanowire: ~ 2 mA/ μm (cryogenic)

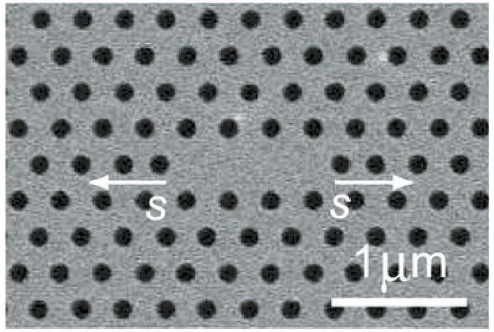
APAM opportunity for optoelectronic devices

First steps to a broad opportunity.

Novel Far-IR to THz response

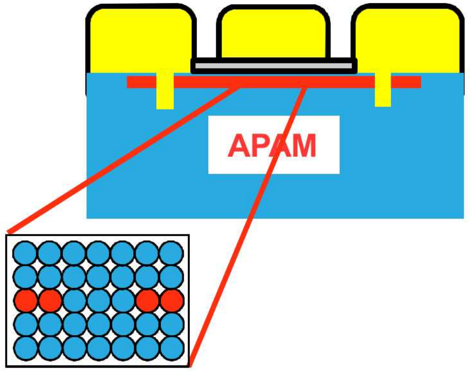


Pattern layer to tune response



Fingerprint

Thrust 1 – link between tasks and exemplars

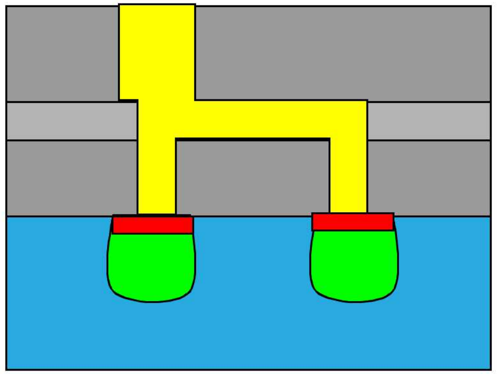


APAM – MOS

Need:
- **Channel engineering**
- Surface gates
- **RT operation**

Interconnects

Need:
- **Channel engineering**
- **RT operation**

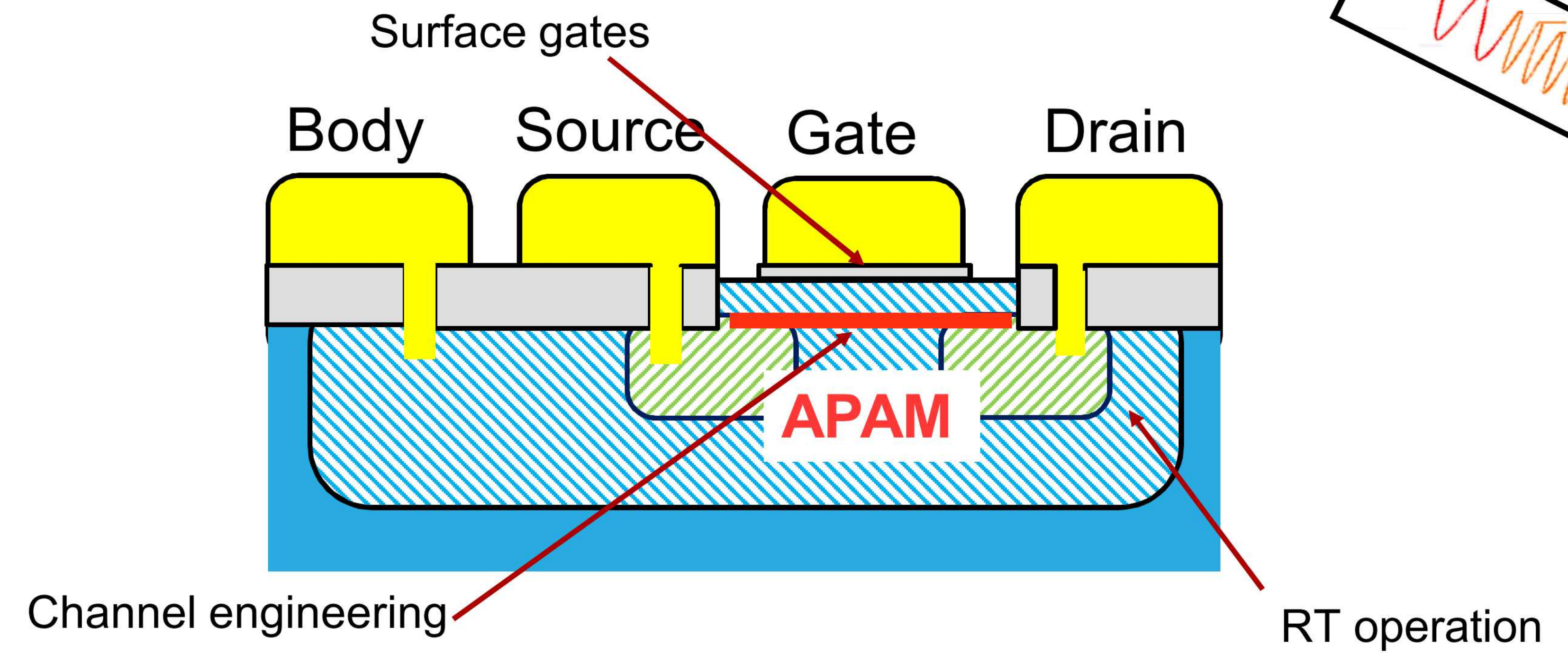


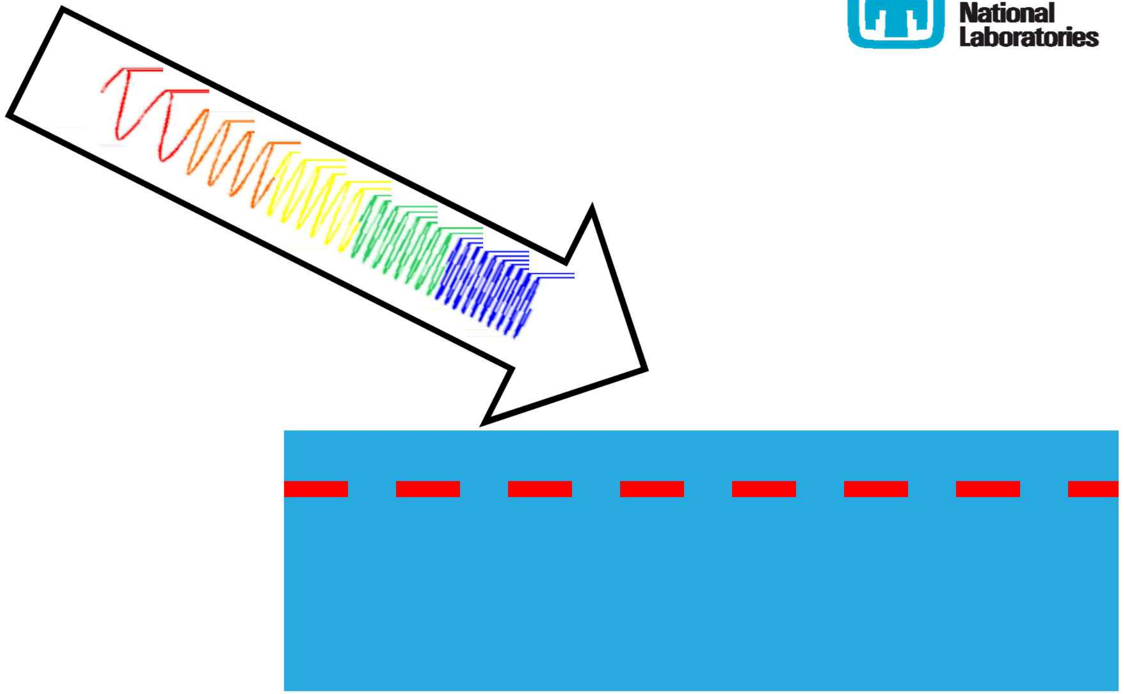
Fingerprint:

Need:
- **Channel engineering**
- Photonics

Bold = critical path

Why is this challenging?





Revised tasks	Difficulty
Surface gates	Dopant diffusion vs. material quality
Room temp. operation	APAM makes control over dopant profiles difficult
Channel engineering	Unclear what critical variables are
Photonic response	Transition from discovery to application

Thrust 1 – organization

Task leads
Surface gating: Tzu-Ming Lu
RT operation: Lisa Tracy
Channel Engineering: Shashank Misra
Photonics: Aaron Katzenmeyer

Make

APAM	Microfab
Shashank Misra	Dan Ward
Ezra Bussmann	DeAnna Campbell
Evan Anderson	Mark Gunter
Scott Schmucker	Philip Gamache
Fabian Pena	Sean Smith
Jeff Ivie	
Joe Lucero	

Measure

Electrical	Characterization
Lisa Tracy	Ping Lu
Tzu-Ming Lu	Aaron Katzenmeyer
Albert Grine	David Scrymgeour

Model

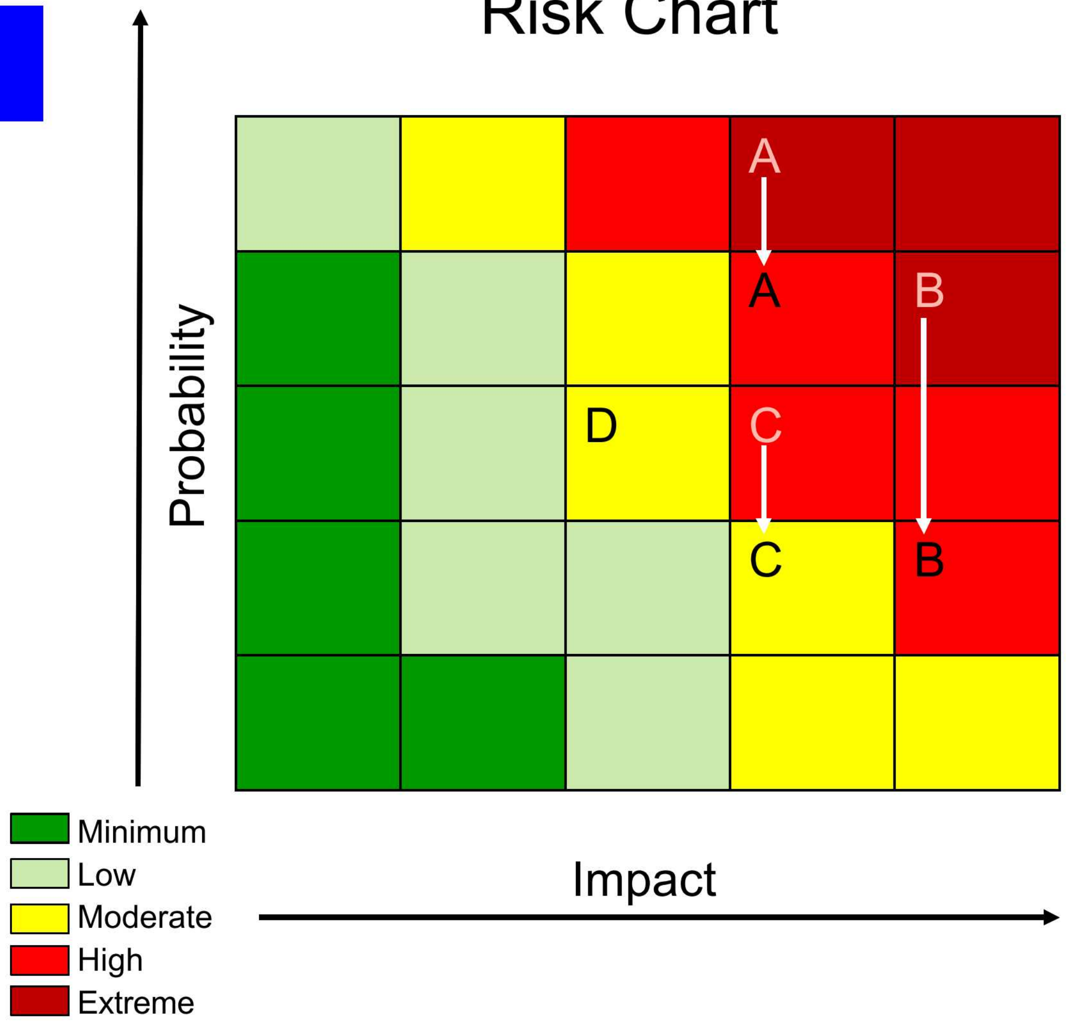
Devices	EM
Suzey Gao	Michael Goldflam
Denis Mamaluy	Steve Young
Juan Granado	Andrew Baczewski

Thrust 1 – Risk reduction in FY 19

#1

APAM Channel	Room T Operation	Surface Gating	Photonic elements
A	B	C	D

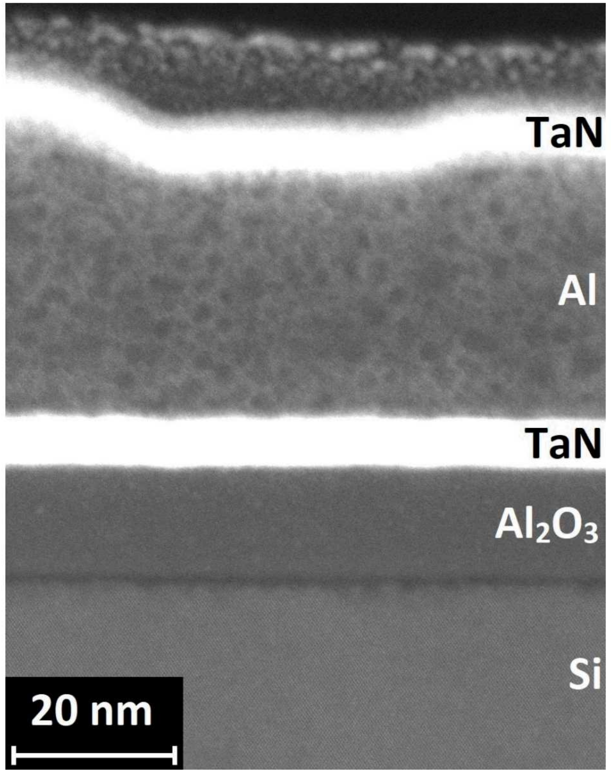
Risk Chart

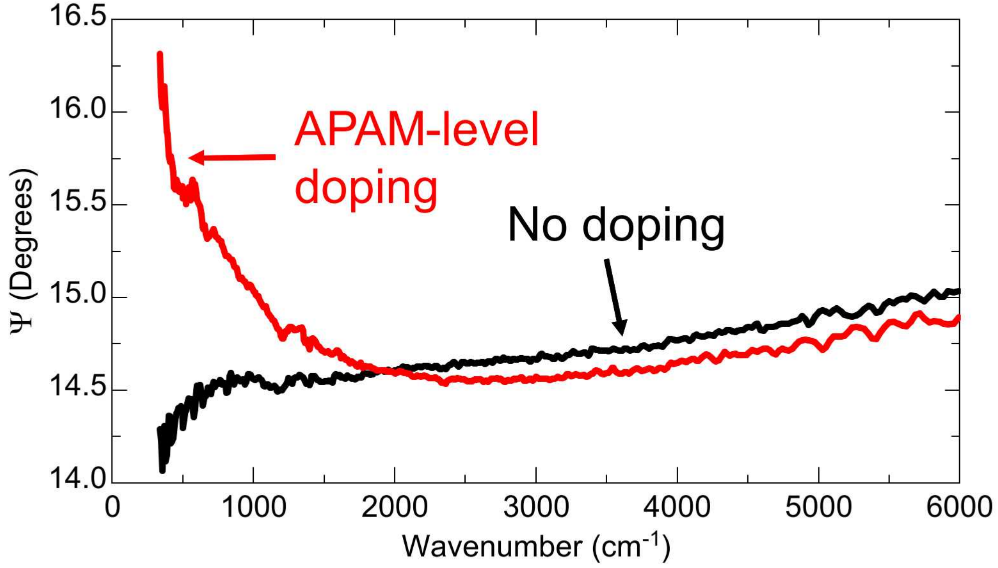


A. APAM channel: Control over defects, but not impurities
B. Room T operation: APAM delta layer works at room temp.
C. Surface gating: Initial success with high-k/metal stack
D. Photonic elements: New task!

Thrust 1 – discoveries

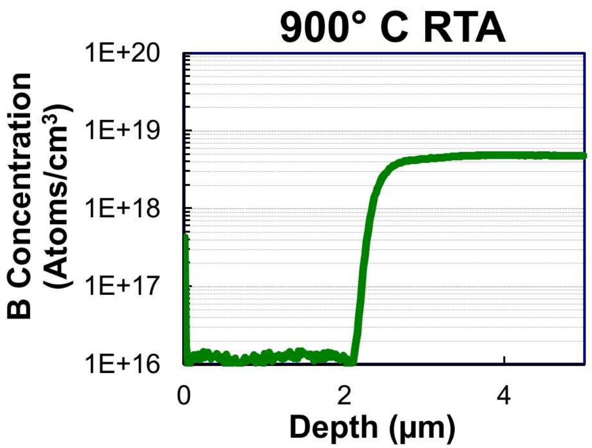
1st fab-compatible gate integrated with APAM

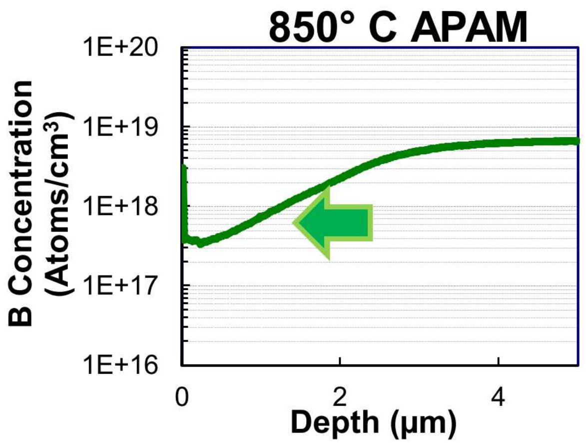




1st measurement of APAM optical response – APAM works at room temperature!

Discovery of acceptor dopant electromigration





Thrust 1 FY 19 output

Written

- 1 publication in submission, 2 in preparation
- Review paper in preparation (Kavli)
- Whitepaper in preparation (NSF)
- 2 Book chapters published
- TA: compressed sensing for scanned probe
- **Parts of two different submissions to DOE RFI on Microelectronics**

Spoken

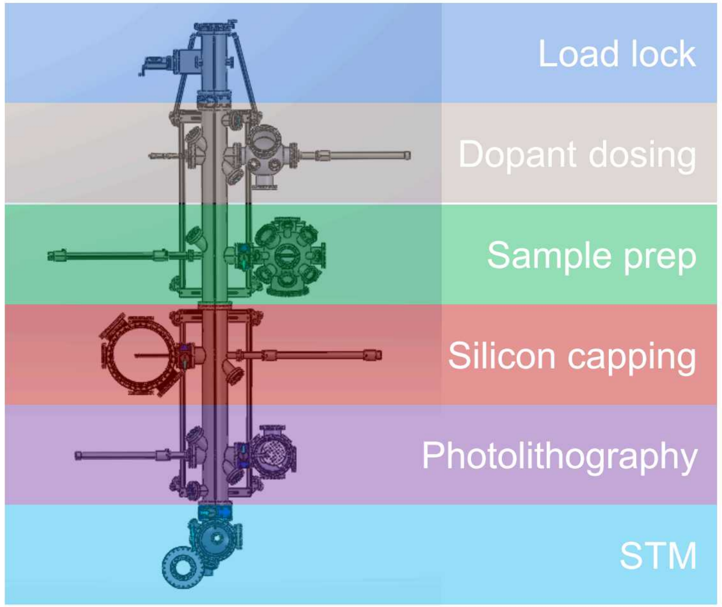
- Workshops: Stanford, Kavli, NSF
- Contributed talks: DRC, ICSI/ISTDM, EIPBN

Collaborations

- Exploring: IBM, UNM

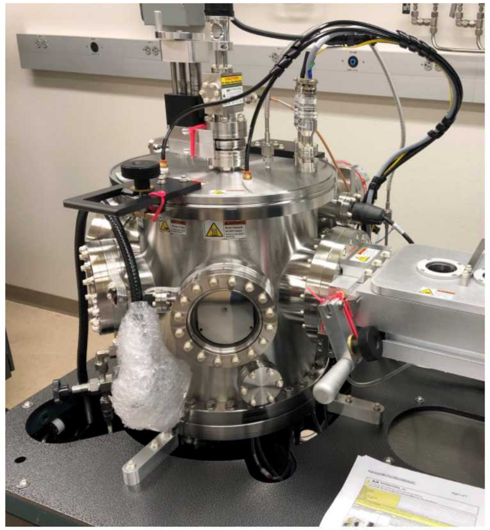
Thrust 1 – increased capability

$600k investment in new APAM system



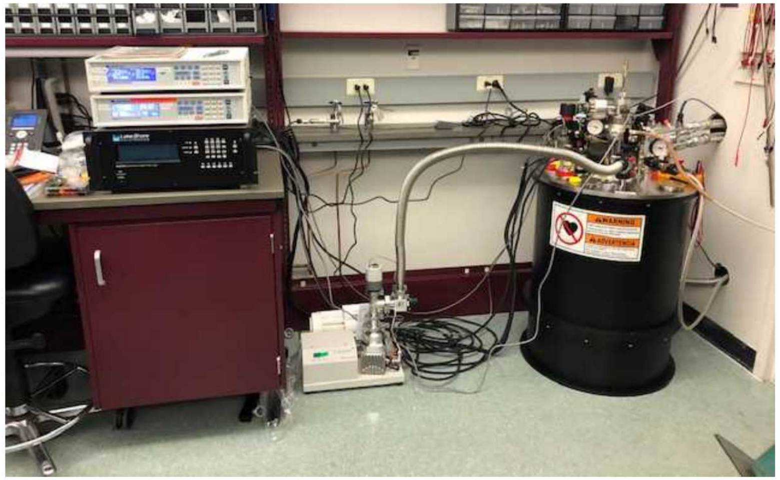
Increase throughput
Separate out parts of the process

$300k investment in high-k/metal gates



10x increase in throughput.
High-k/metal gates for any SNL project.

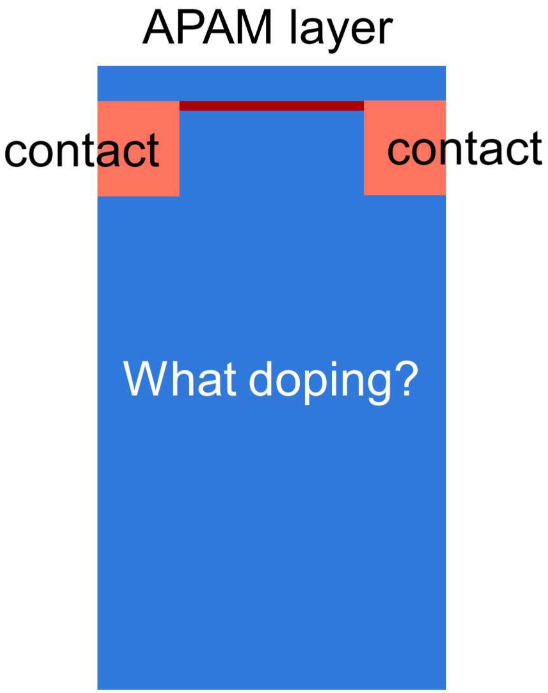
$200k investment in variable temperature measurement system

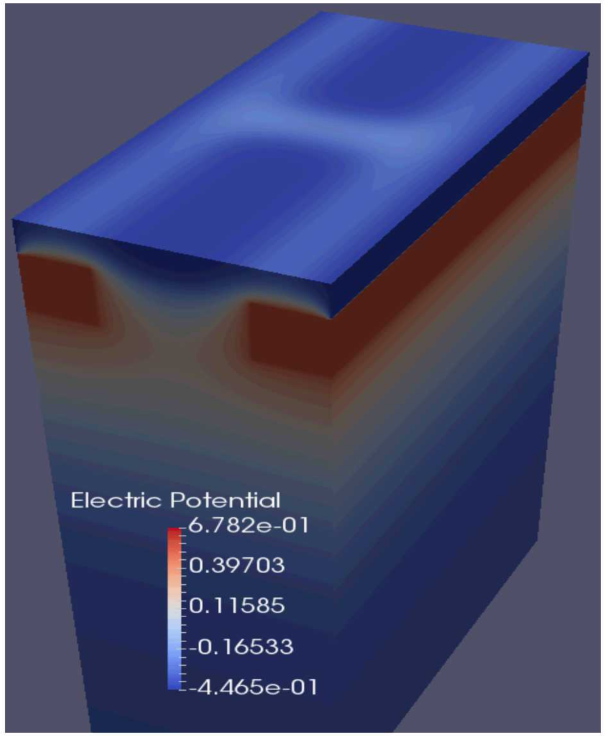


Capability that did not exist at SNL.

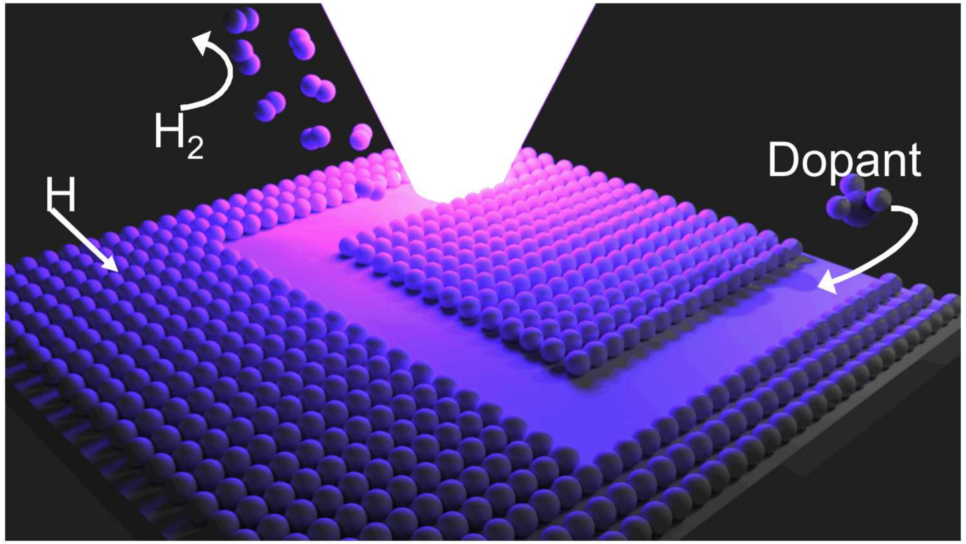
Input from other thrusts

Thrust 2 (Semi-classical modeling) – background doping needed for RT operation





Thrust 4 (Photolithography) – 8x as many devices (process testers) in ½ the time



Plan for FY 20

Thrust #1: APAM devices

Critical path

APAM Channel

Room T Operation

Critical path

Go/no-go

Are gates good enough to make projections?
Can we make them better?

Surface Gating

Photonic elements

Can we design a fingerprint?

Go/no-go

Plan for FY 20

Shashank Misra

Tzu-Ming Lu

Thrust #1: APAM devices

APAM Channel	Room T Operation	Surface Gating	Photonic elements

Lisa Tracy

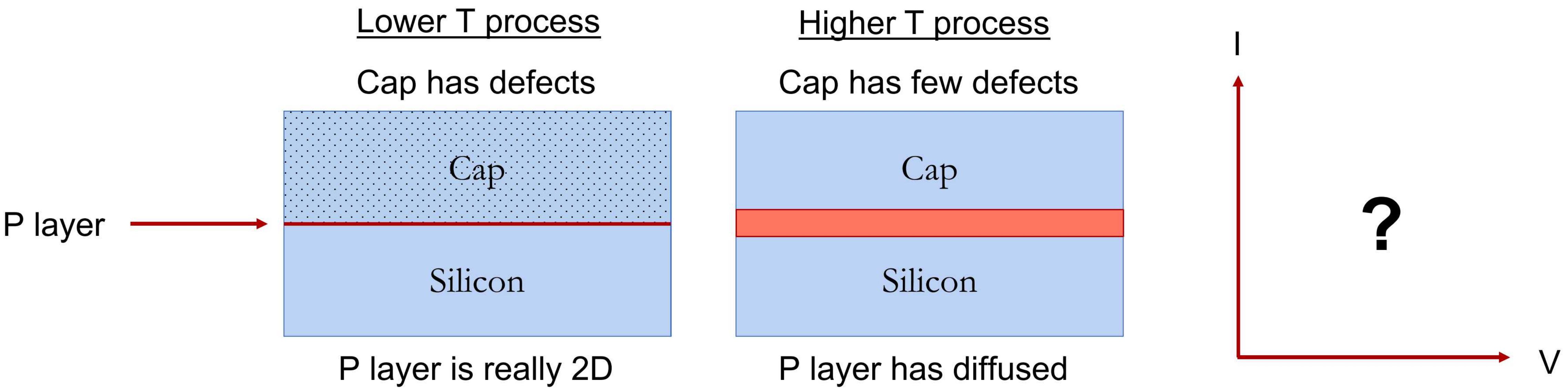
Aaron Katzenmeyer

(2019) Reliability task → (2020) APAM channel

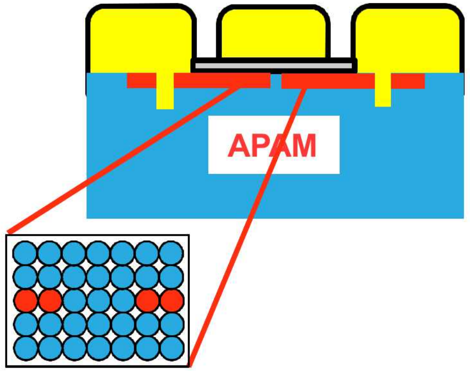
Original motivation...

- Nanowires : geometry determines I-V
- Tunnel junctions : same geometry = different I-Vs

What is the link: APAM process parameters – material characteristics – device performance?



Impact – connection to exemplars

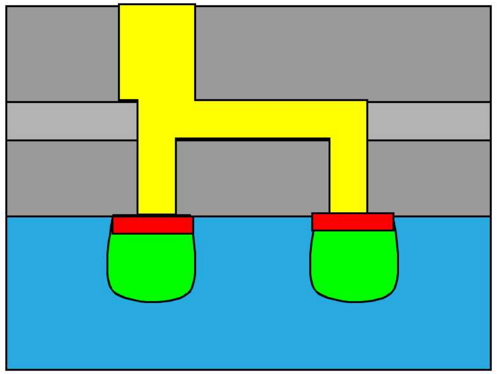


APAM – MOS

Need:
- **Channel engineering**
- Surface gates
- RT operation

Interconnects

Need:
- **Channel engineering**
- RT operation



Fingerprint

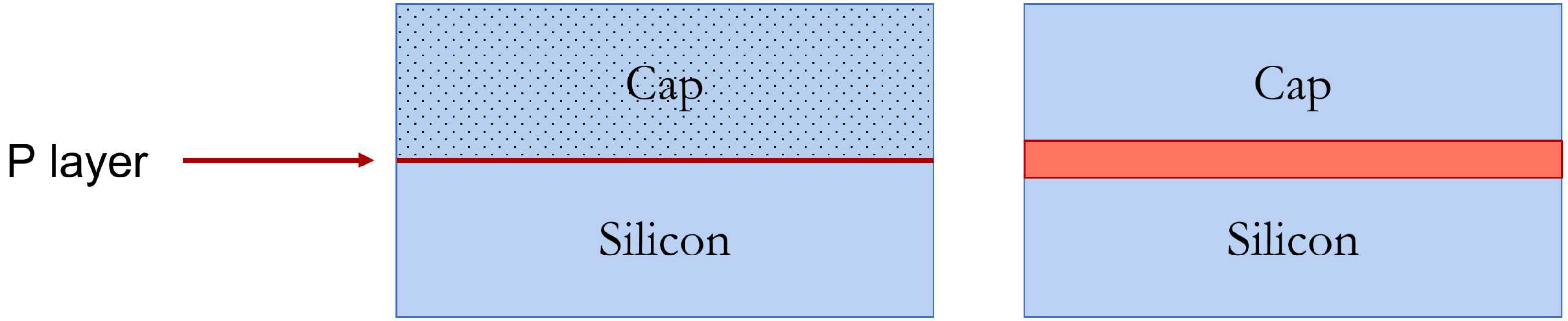
Need:
- **Channel engineering**
- Photonics

Different considerations for different applications – need to understand APAM process space & its implications.

The challenge

Better for drive current?

Better for surface gate?



P layer is really 2D

Cap has defects

P layer has diffused

Cap has few defects

- Material characterization : How do you know when all of the right atoms are in the right place?
- Device performance : What are the key variables and metrics?

This is discovery science – we are trying to develop underlying understanding!

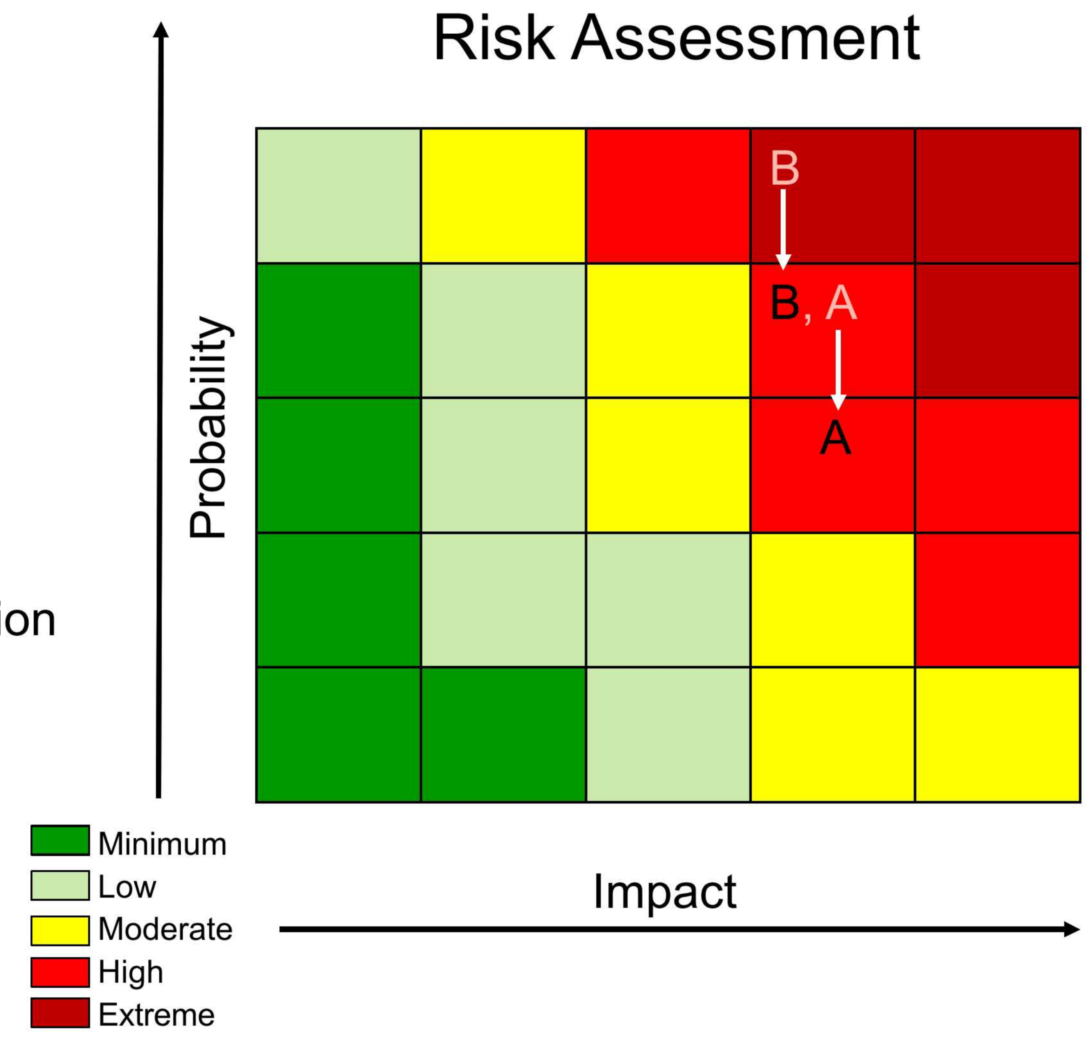
Risk assessment – FY 19 updates

What controls channel properties?

A) Device layer – dopant profile, defects, diffusion
B) Material stack – defects and impurities

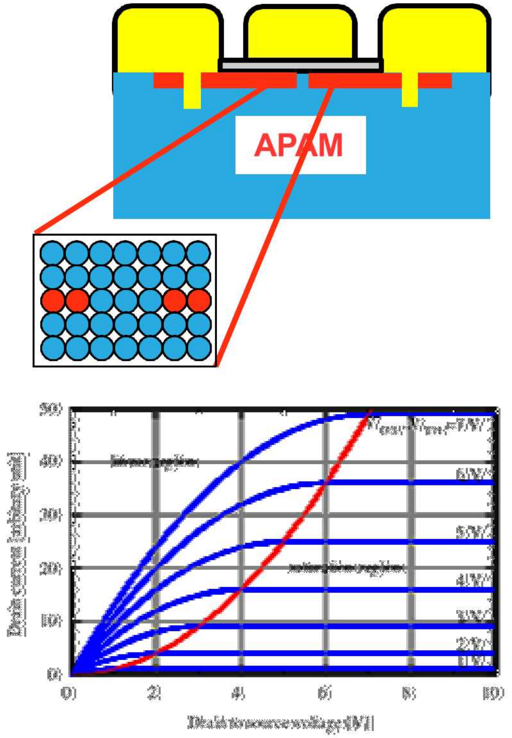
<u>Updates</u>

- Blue factors – have mapped process variables to material characteristics
- Confinement & impurities → open *science* question on relation to electrical and optical response

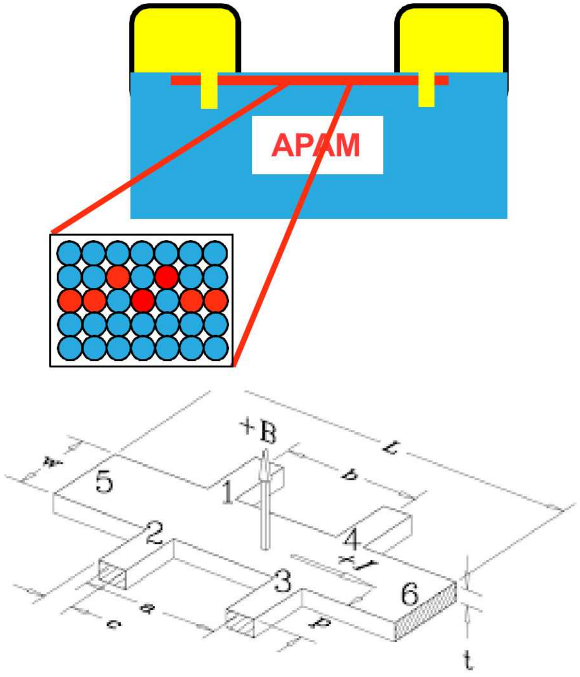


FY19 – Electrical characterization

Transistor



Hall bar



Two-dimensional sheet:

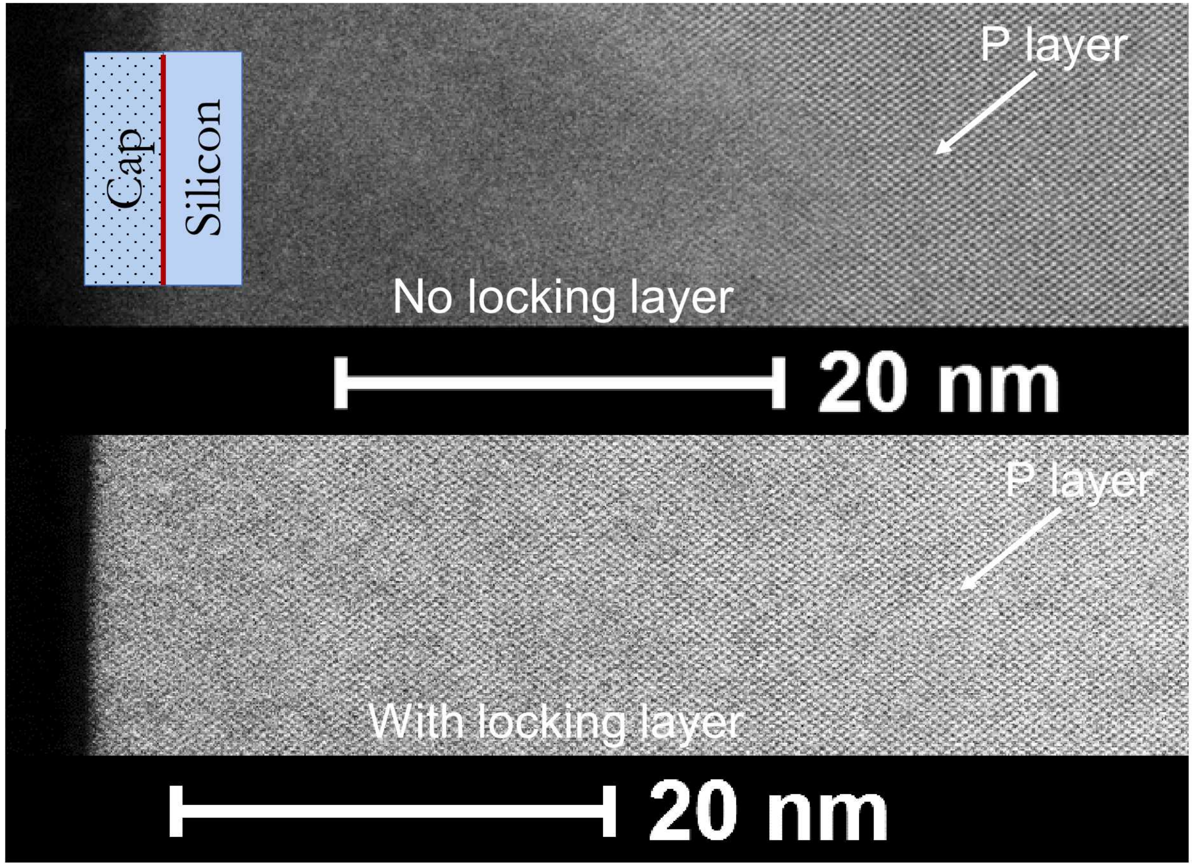
- Resistivity: 500 Ω/sq
- Carrier density: 1.7×10^{14} cm^{-2}
- Carrier mobility: 60 $cm^2/V\text{-}s$

Ultimate answer is application driven.

Hall data - quick way to determine if something has changed. Mapped to different sample/material characteristics.

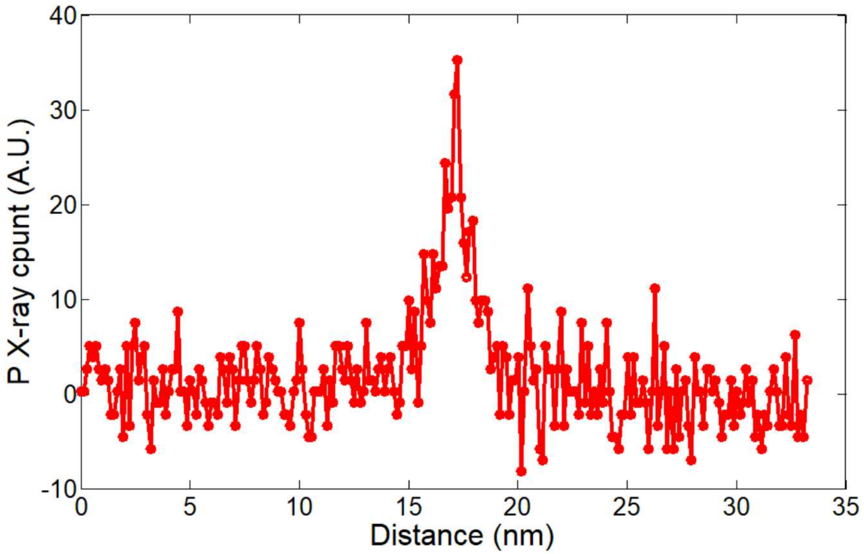
FY19 – Defects in capping layer

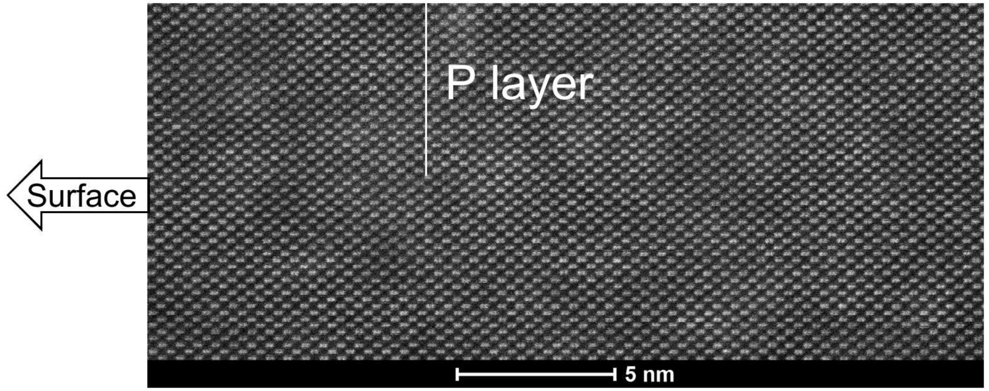
We can control defects. TEM data:



What is effect on confinement of P?

Old P layer plan: TEM sees dopants. Interpretation issues.

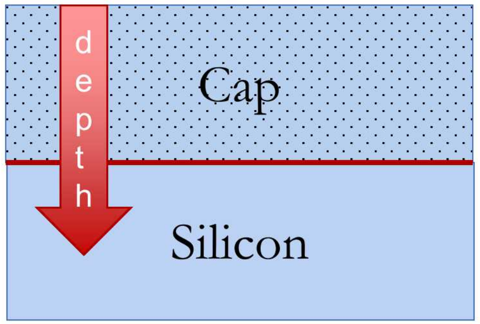


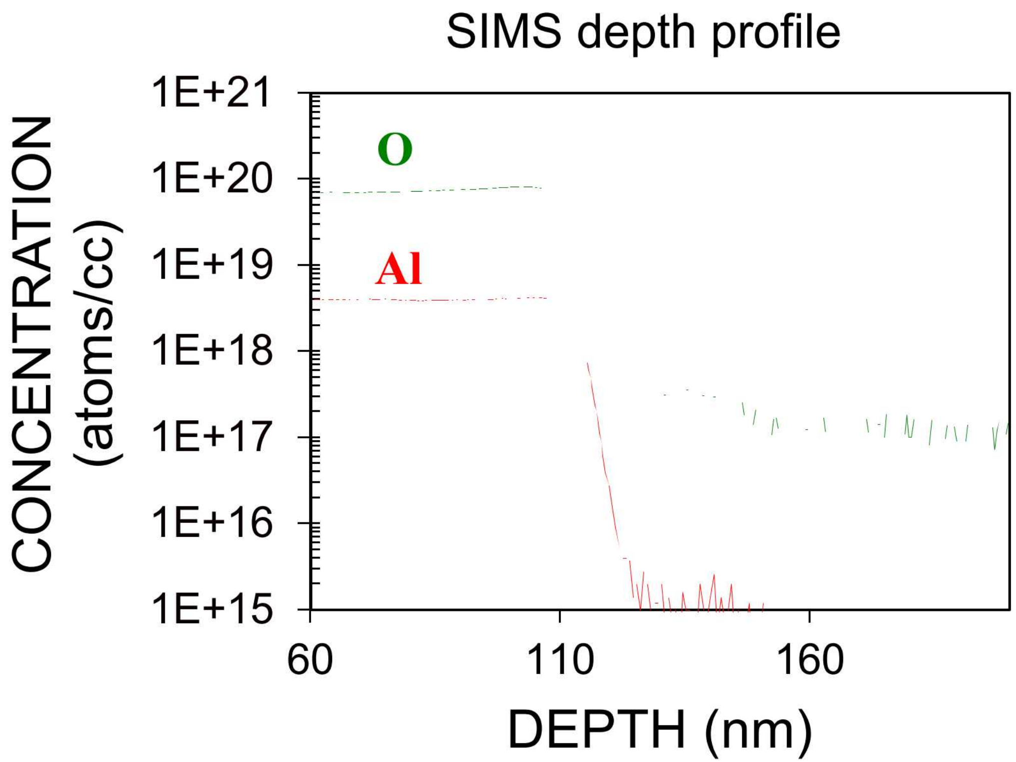


New P layer plan: Optical measurements, weak localization.

FY19 – Impurities in capping layer

What is the composition of the capping layer?

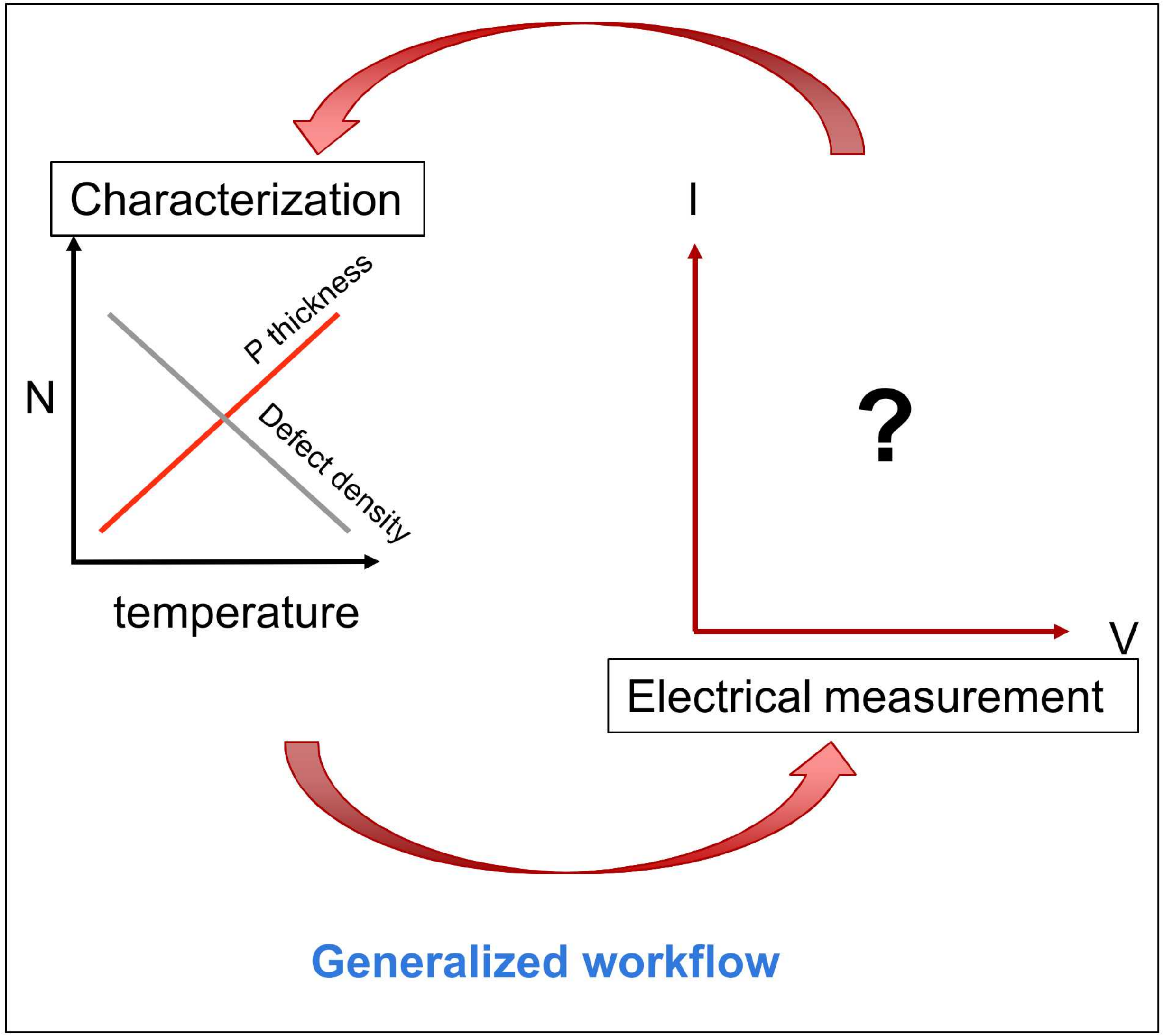


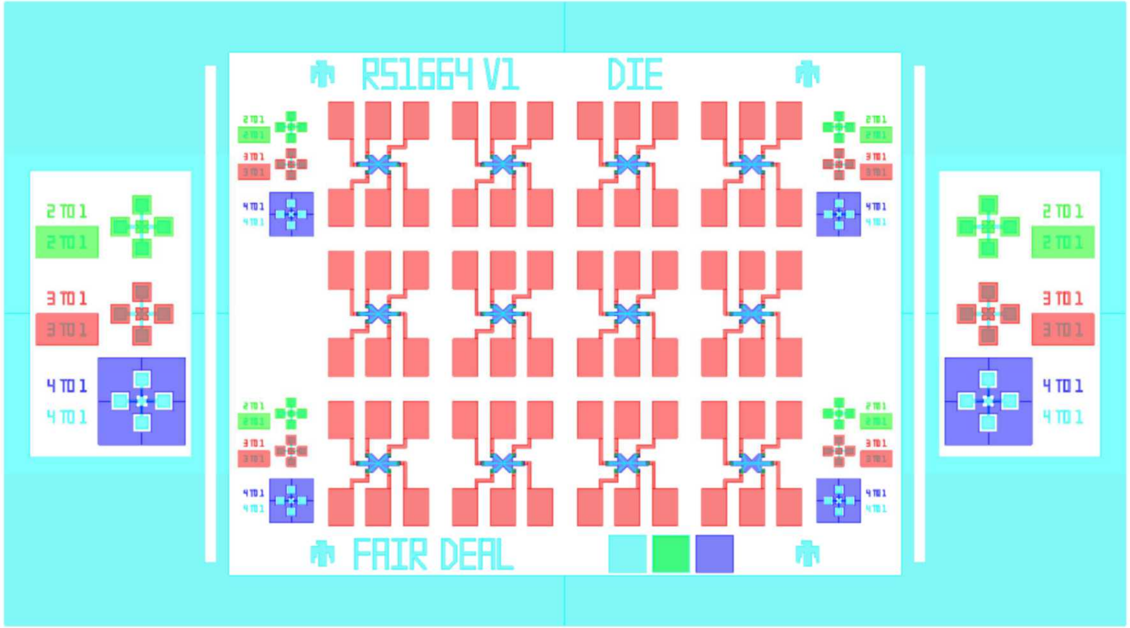


Plan to control impurities

1. Aluminum comes from capping source.
2. Increased pumping decreases oxygen.

FY20 – More advanced electrical characterization

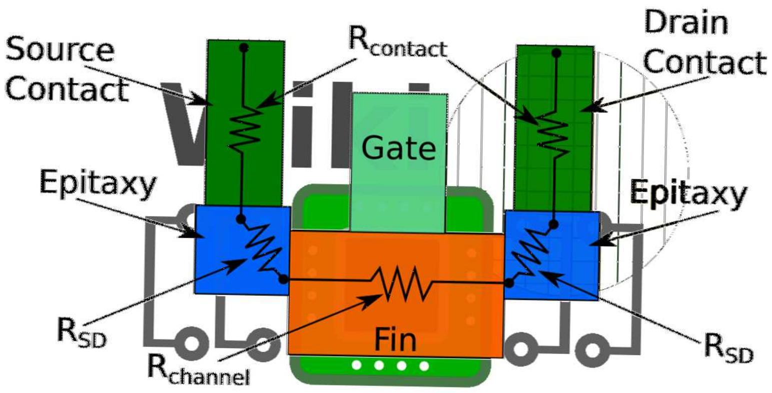


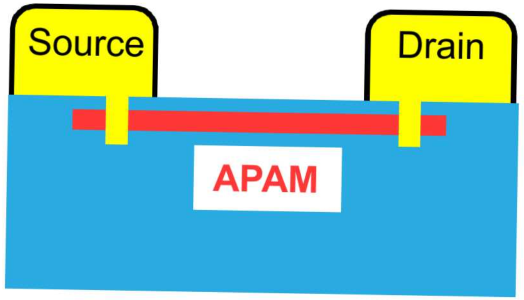


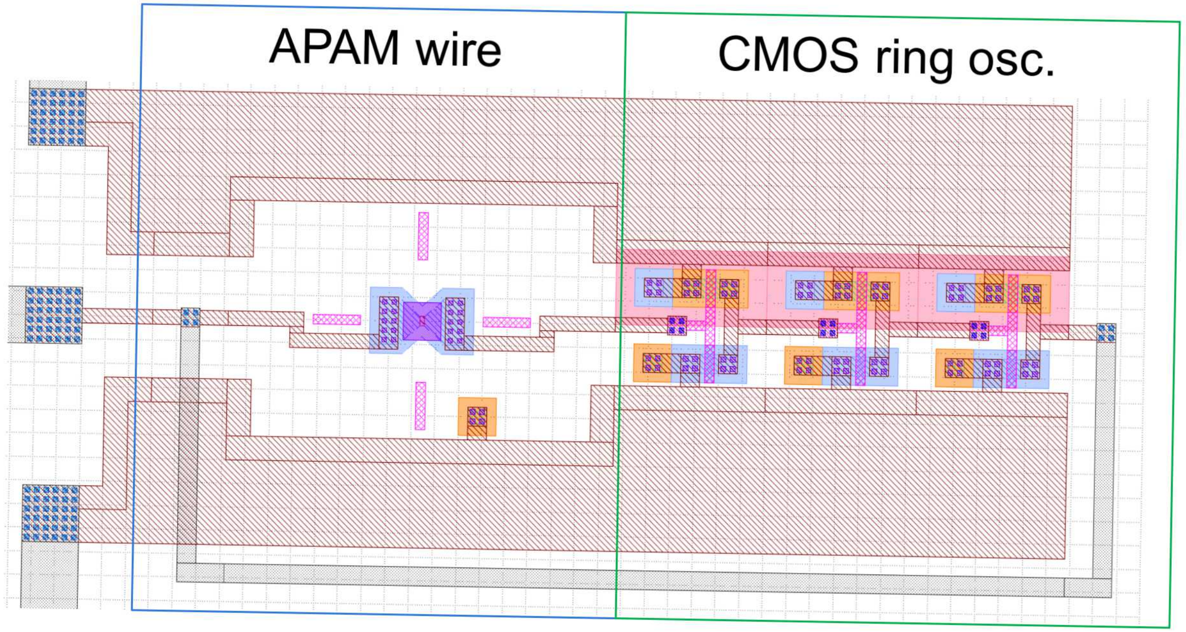
1) APAM-CMOS integration:

"Quick characterization" die – drive current and scaling

FY20 – More advanced electrical characterization







2) Interconnect:

Designing scheme to break apart contact resistances in nanowires.

3) APAM-CMOS integration:

Frequency response of APAM wire at high frequency has never been measured!!

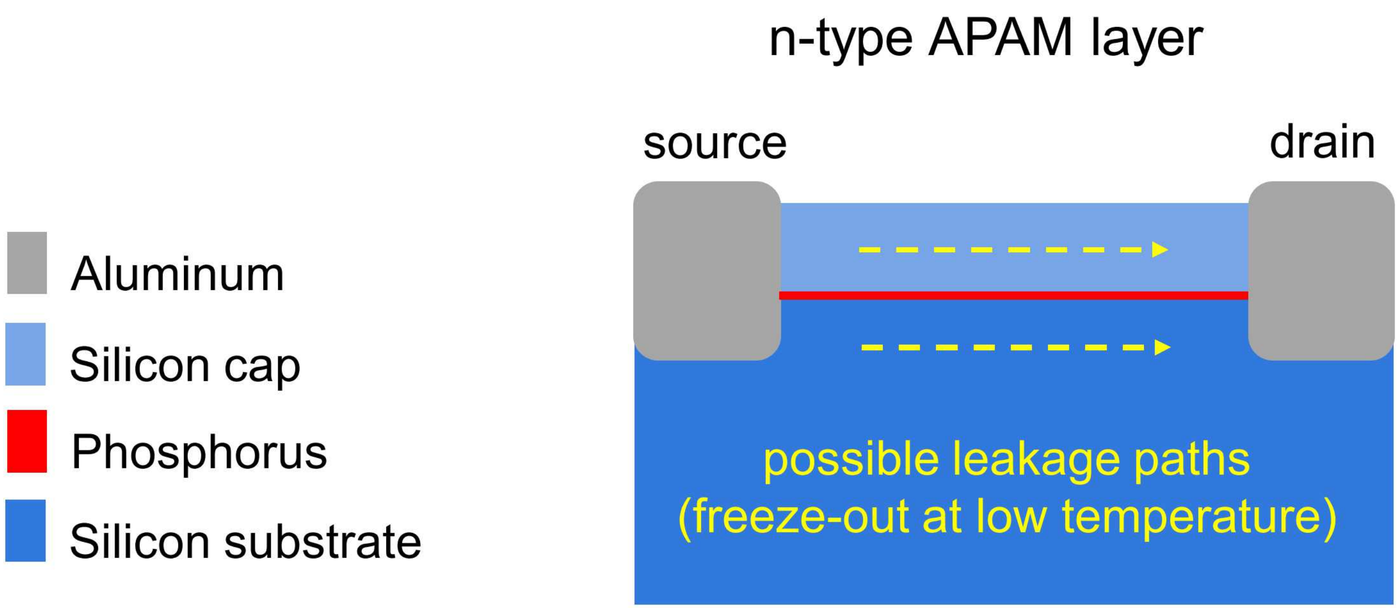
Plan for FY 20

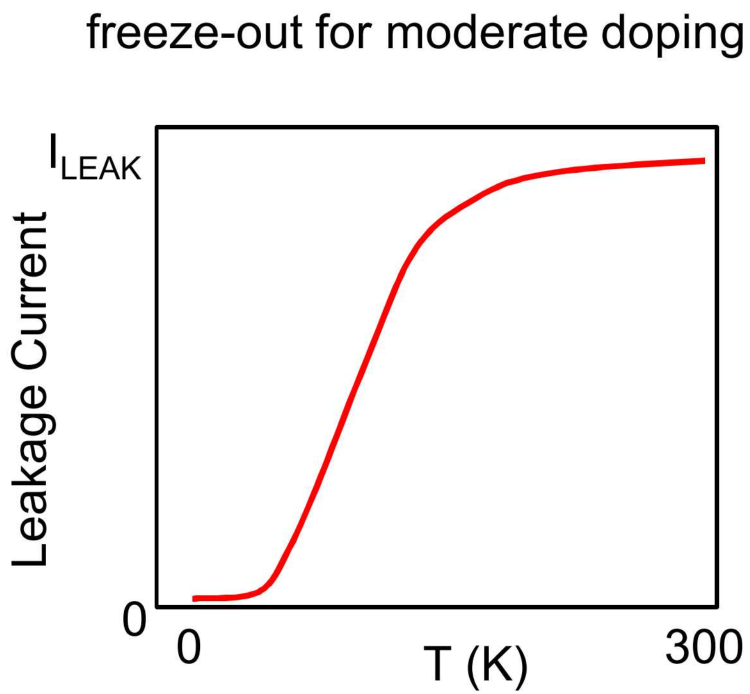
Thrust #1: APAM devices

Shashank Misra	Lisa Tracy	Tzu-Ming Lu	Aaron Katzenmeyer
APAM Channel	Room T Operation	Surface Gating	Photonic elements

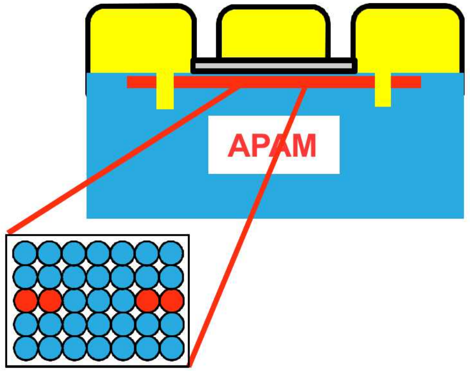
Goal: Room Temperature Device Operation

- Existing devices operate at cryogenic temperatures
- End target: 150°C operation of APAM devices





Impact – connection to exemplars

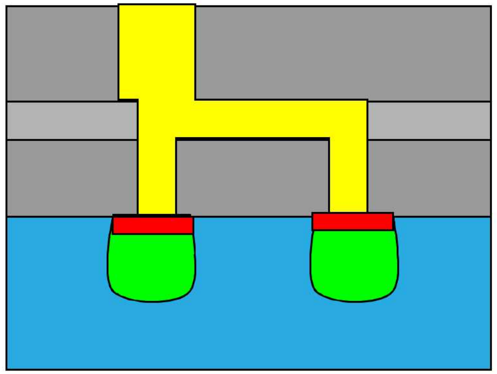


APAM – MOS

Need:
- Channel eng.
- Surface gates
- **RT operation**

Interconnects

Need:
- Channel eng.
- **RT operation**



Fingerprint:

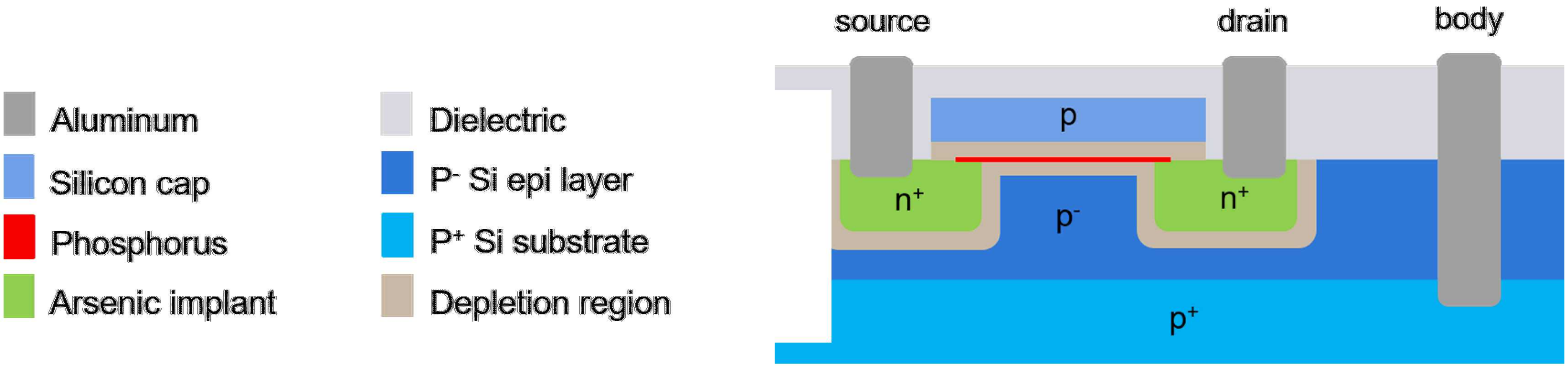
Need:
- Channel eng.
- Photonics
- RT operation

RT operation essential for many applications

Device Isolation at Room Temperature

- New device design and process flow for isolation contacts and additional body contact (reticle set complete, currently in fab)

n-type wire with isolation and body contact



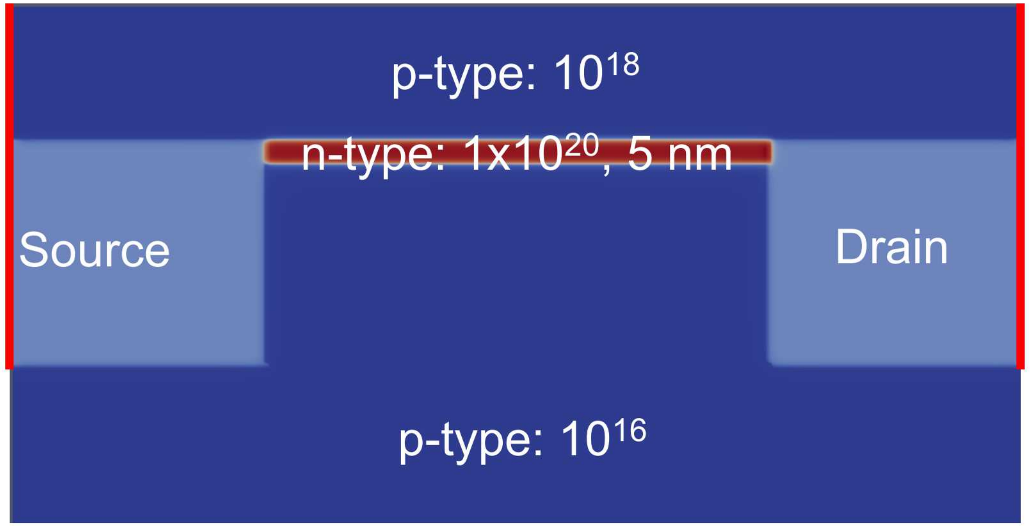
Solution for control over leakage paths

Ward, Campbell

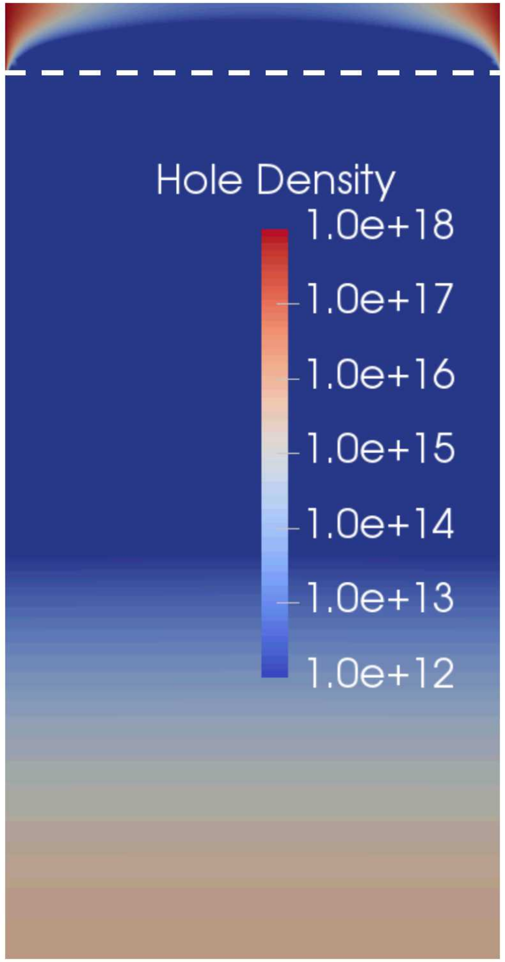
TCAD Simulations

- Semi-classical simulations of APAM test structure to investigate initial device structures

Simulation Structure



Hole Density from TCAD

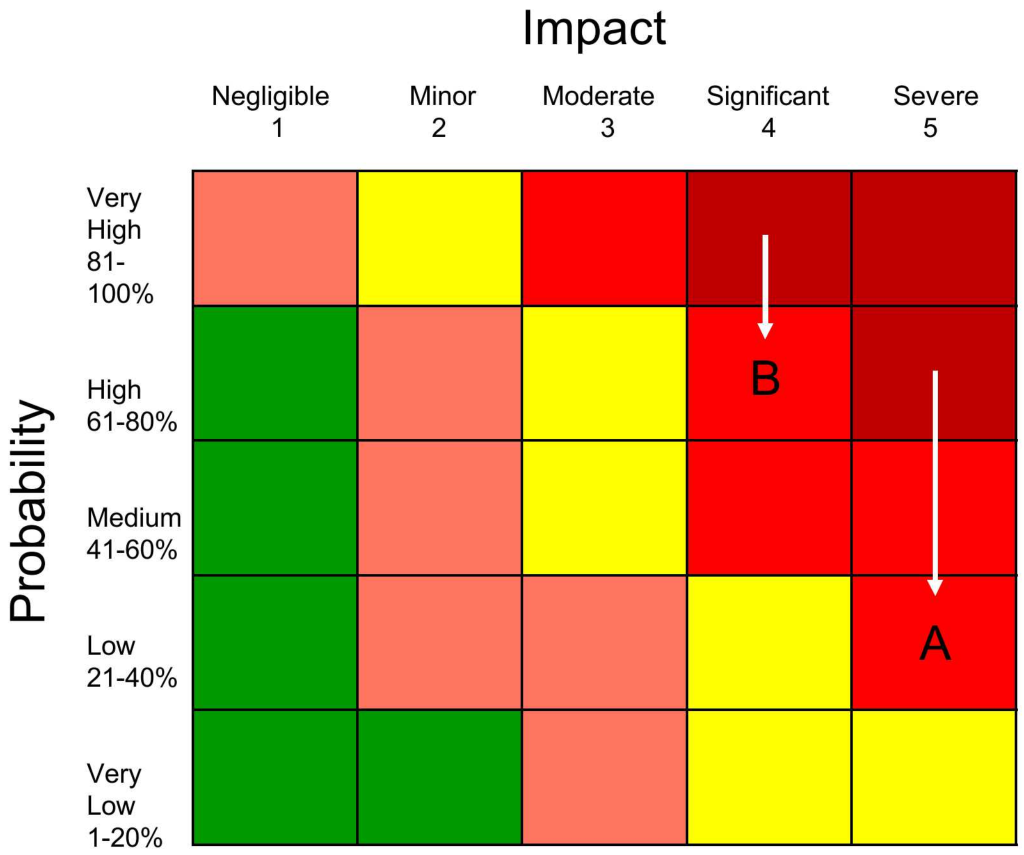


Gao

Updated Room Temperature Operation Challenges

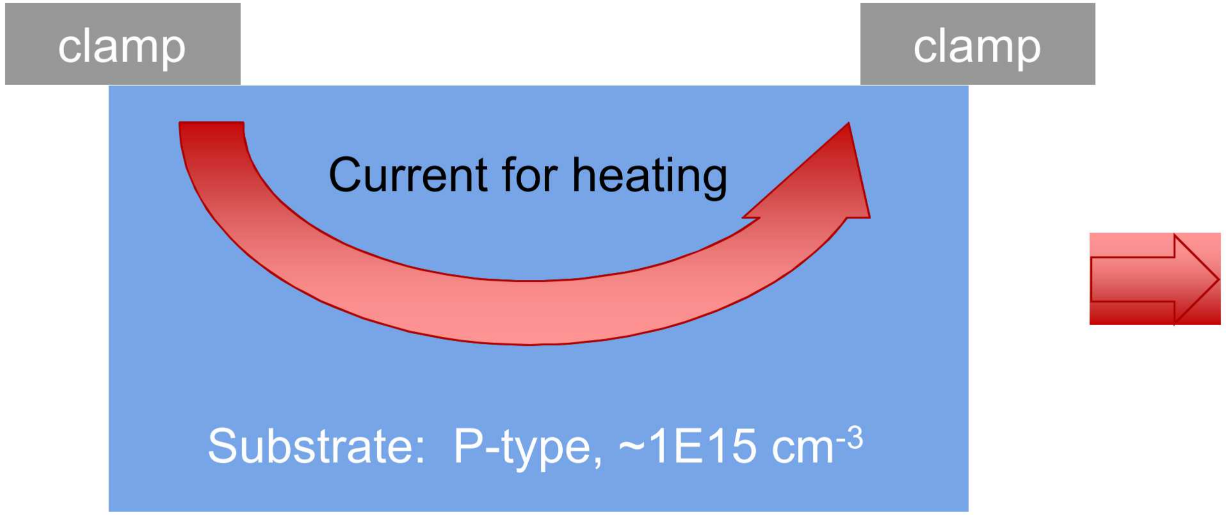
- Non-standard processing required for APAM devices

- Risks:
  A. Isolation of device leads and contacts
  B. Poor control over dopants in surrounding silicon

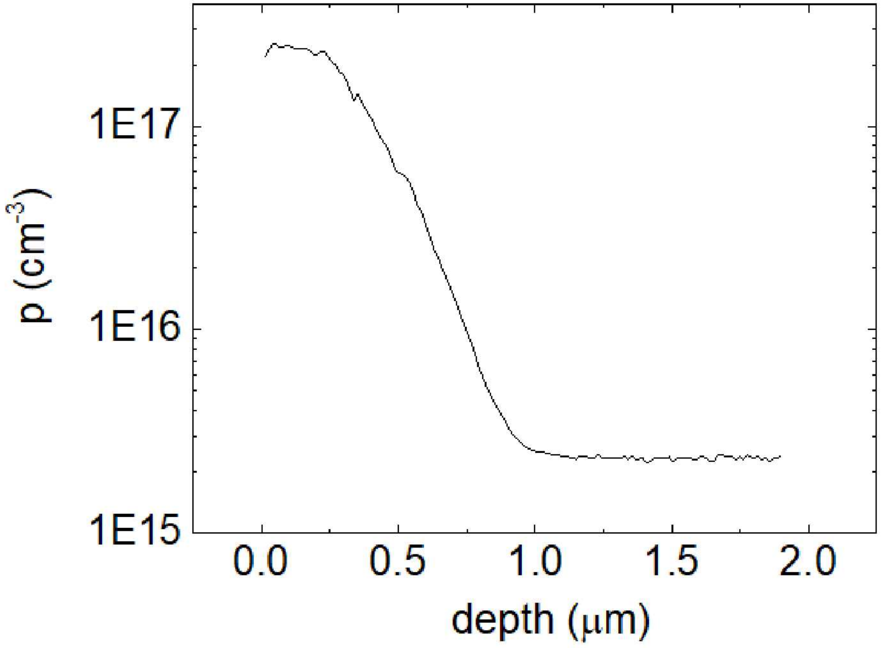


Dopant Profile Control: Substrate Preparation

- Joule heating of substrate used to clean Si surface
- Leads to movement of p-type dopants!
- Alternative substrate prep options in development



Post clean substrate doping



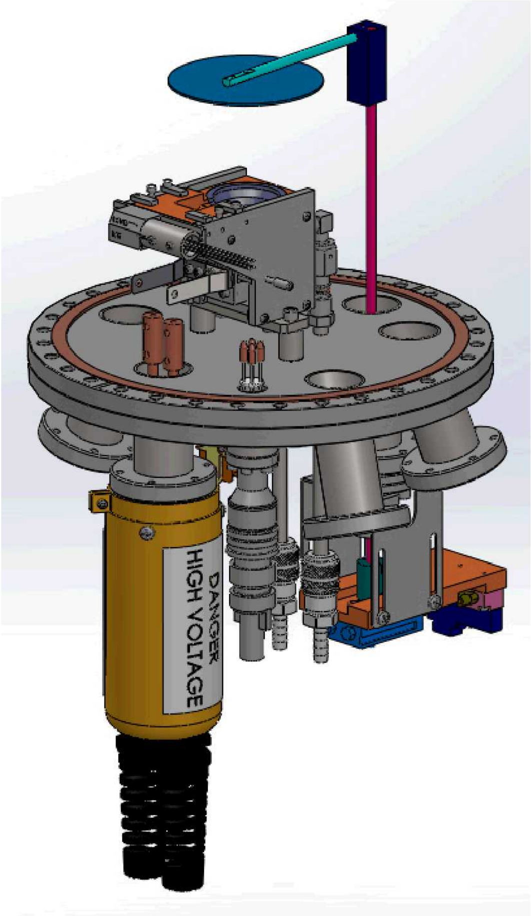
Misra

Dopant Profile Control: Si Cap Epitaxy

- Low temperature Si epitaxy necessary to avoid diffusion of APAM layers
- Non-standard growth temperature leads to impurities (Al, Ni @ ~10^{18} cm^3).
- FY19: New capabilities installed for control over Si cap doping: E-beam source and silane line installed for higher purity Si growth
- FY20: Characterize epi from e-beam source

Silane cabinet

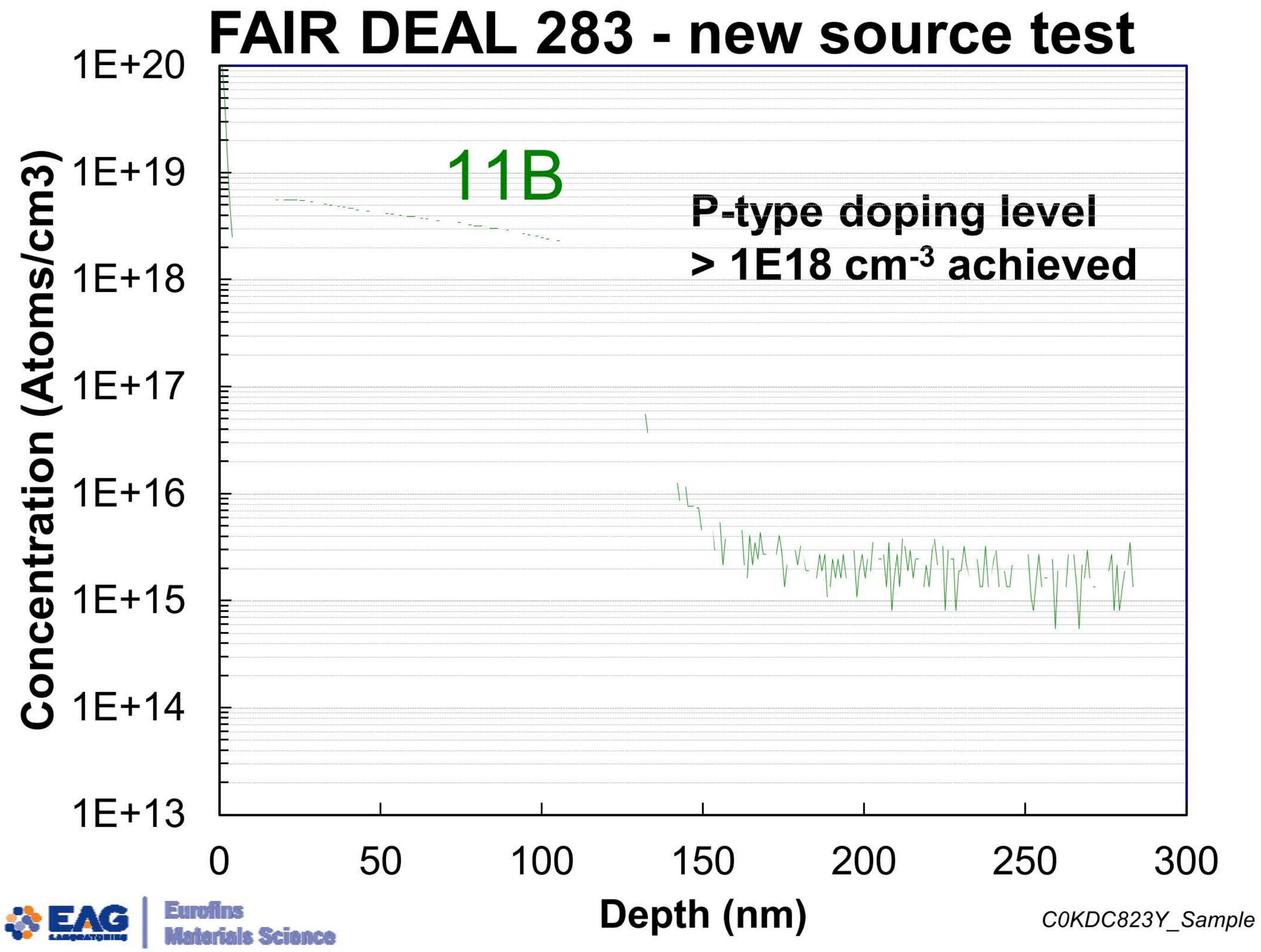
E-beam source



Bussmann

Dopant Profile Control: Adding Dopants

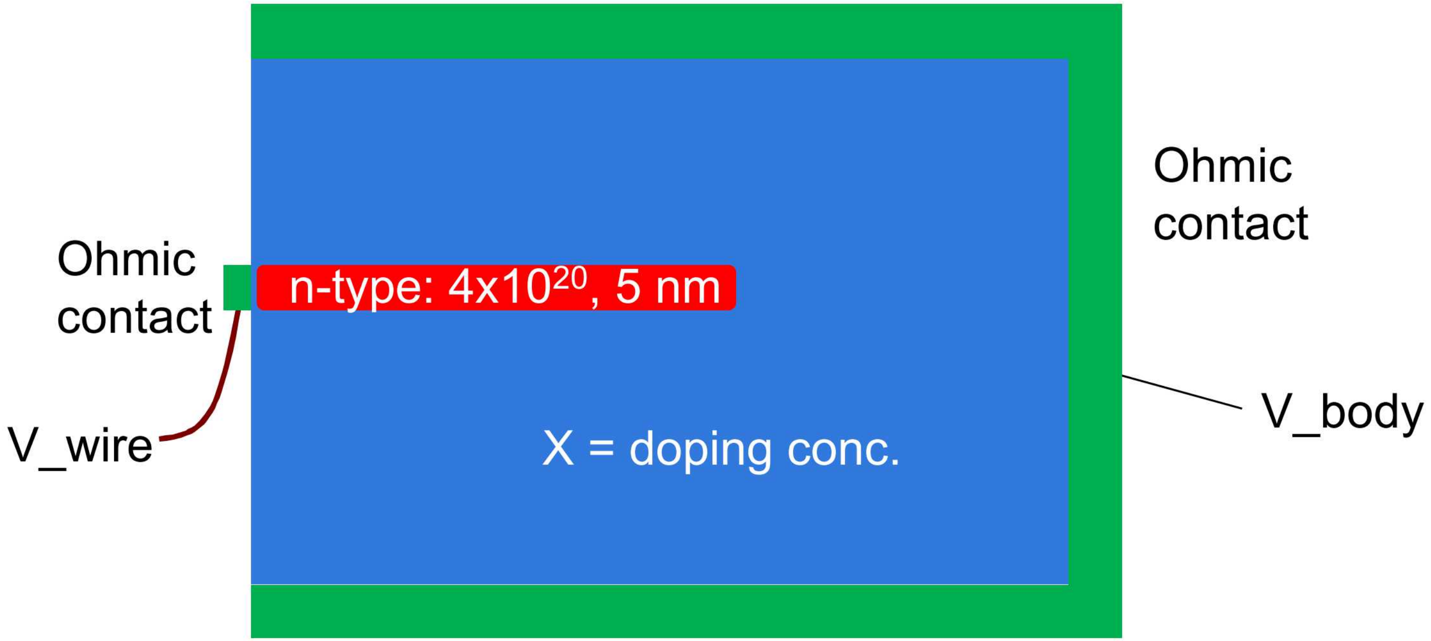
- Co-deposit Si cap from Si sources of varying doping levels
- FY19: Si co-deposition source built
- FY20: Characterize epi (SIMS, electrical transport). Determine doping limits.



Bussmann

TCAD Modeling for Device Isolation

- FY20: What doping levels are acceptable in surrounding Si while avoiding breakdown from delta layer?
- Idealized simulation test structure – lead of tunnel junction device



Leakage current from wire to body?

Plan for FY 20

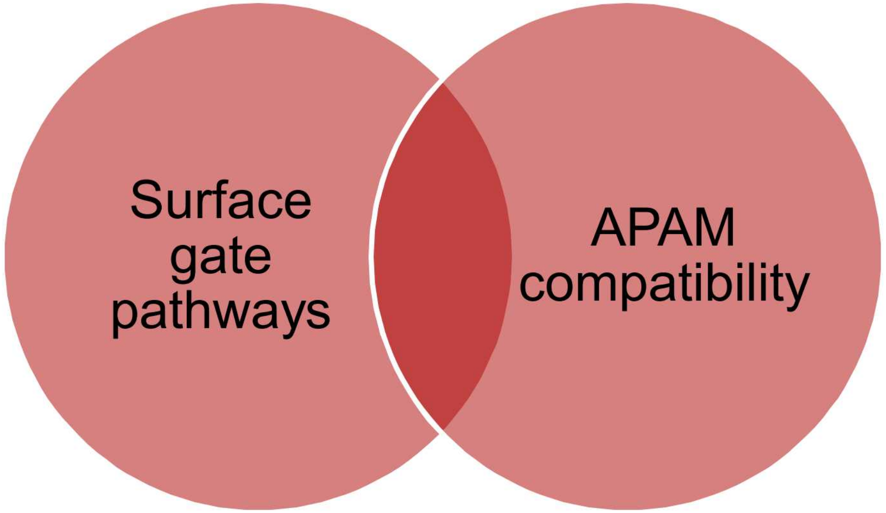
Thrust #1: APAM devices

Shashank Misra	Lisa Tracy	Tzu-Ming Lu	Aaron Katzenmeyer
APAM Channel	Room T Operation	Surface Gating	Photonic elements

Discover Surface Gate stacks for APAM

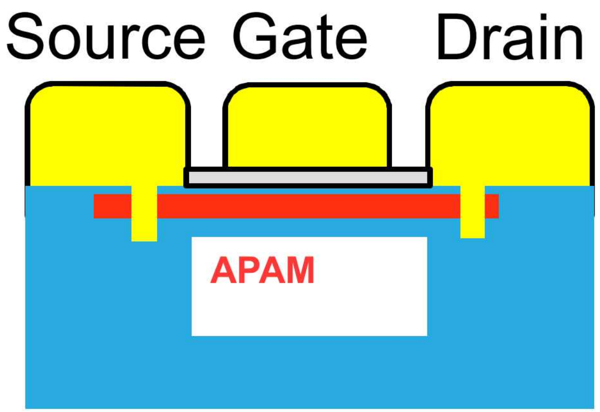
- **Ultimate goal:**

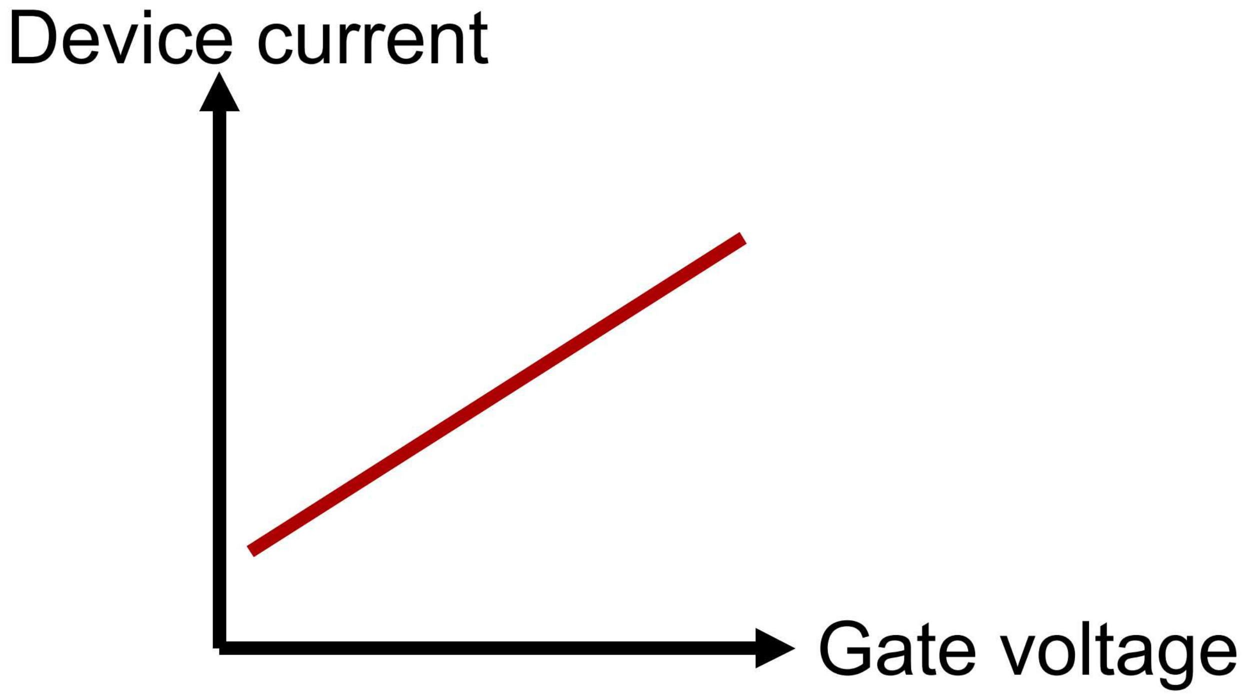
  A surface gate stack that enables proof-of-concept field-effect transistor operations which inform device design and modeling and allow us to project device performance.



Impact – connection to exemplars

APAM – MOS





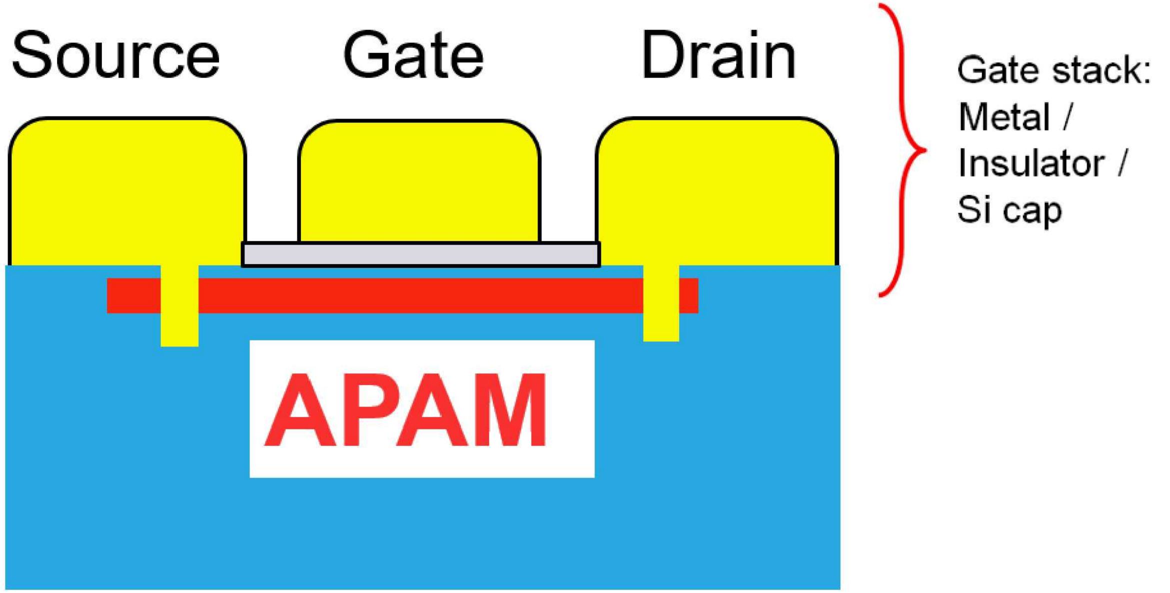
APAM MOS:

Need:
- Channel eng.
- **Surface gates**
- RT operation

Need to identify a gate stack and associated process flow that are compatible with APAM devices.

The challenge

- Thermal oxide can NOT be used because of thermal budget issues.
- There are other options, such as high-k dielectrics, that MAY be compatible with APAM. The standard recipes do necessarily work for APAM devices. R&D is needed.
- Validation and optimization in (a) process and (b) geometry for APAM

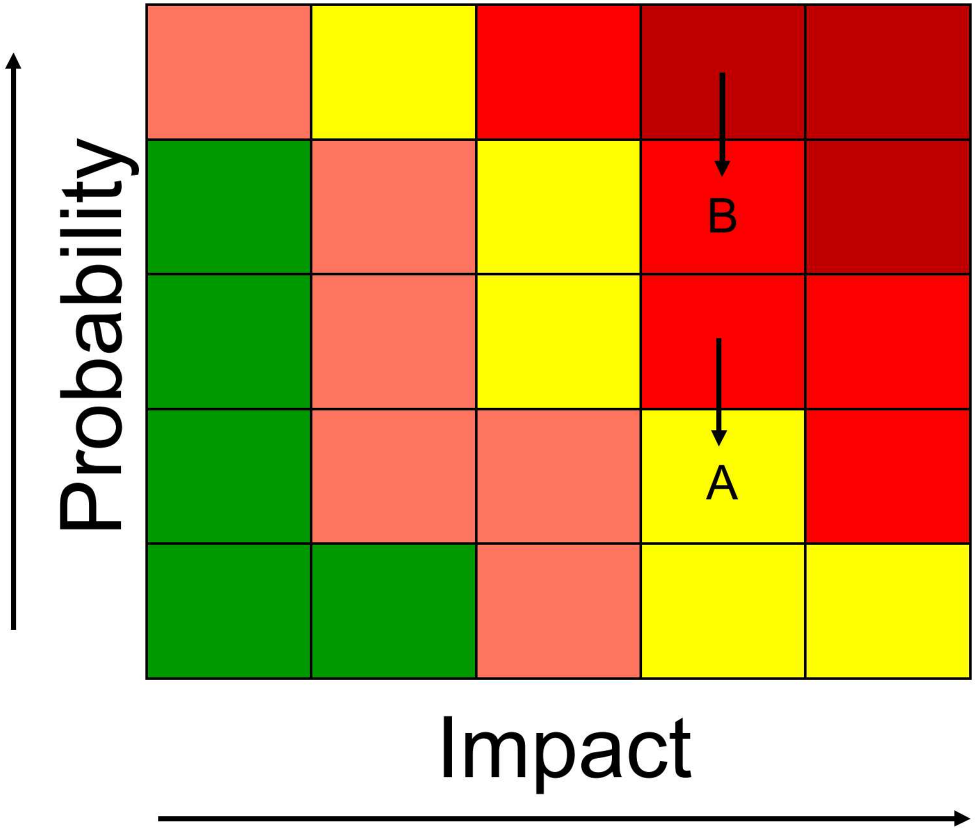


Need a low thermal budget process for surface gates.

Risk Assessment

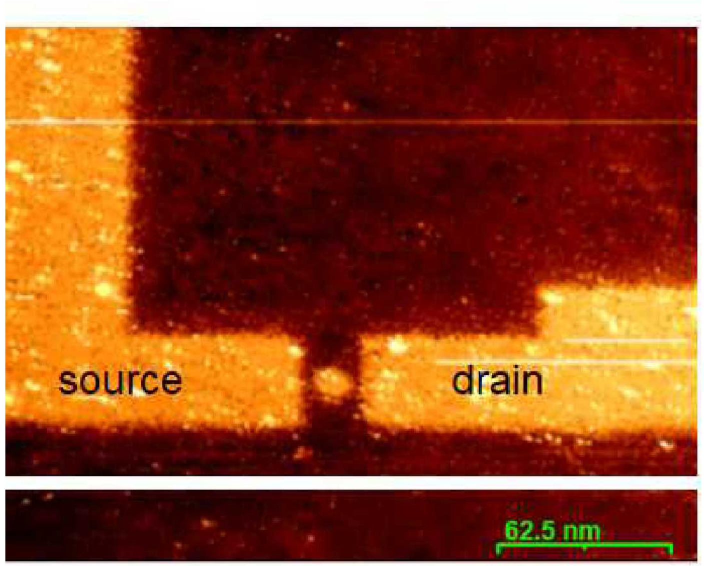
A. research to improve the high-k stack beyond the point of “good enough” may be out of scope.
   - Investment in equipment shortens cycles of learning.

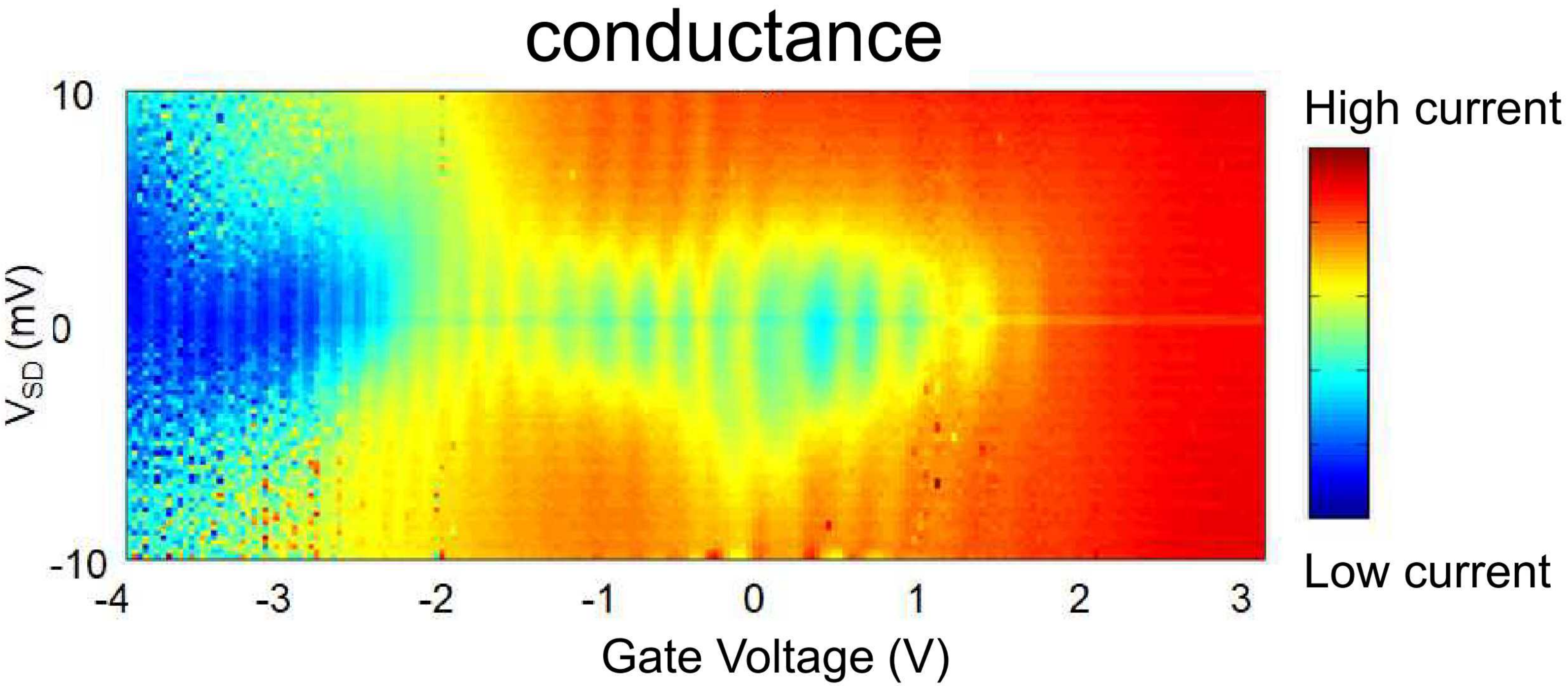
B. Defects and unintentional impurities in the Si cap screen electric fields. (channel task)



Progress: Around last EAB, we had the 1st ever APAM device with a high-k dielectric layer. We've now developed a better process flow for gate stacks.

FY19 – 1st ALD gate oxide on top of APAM device

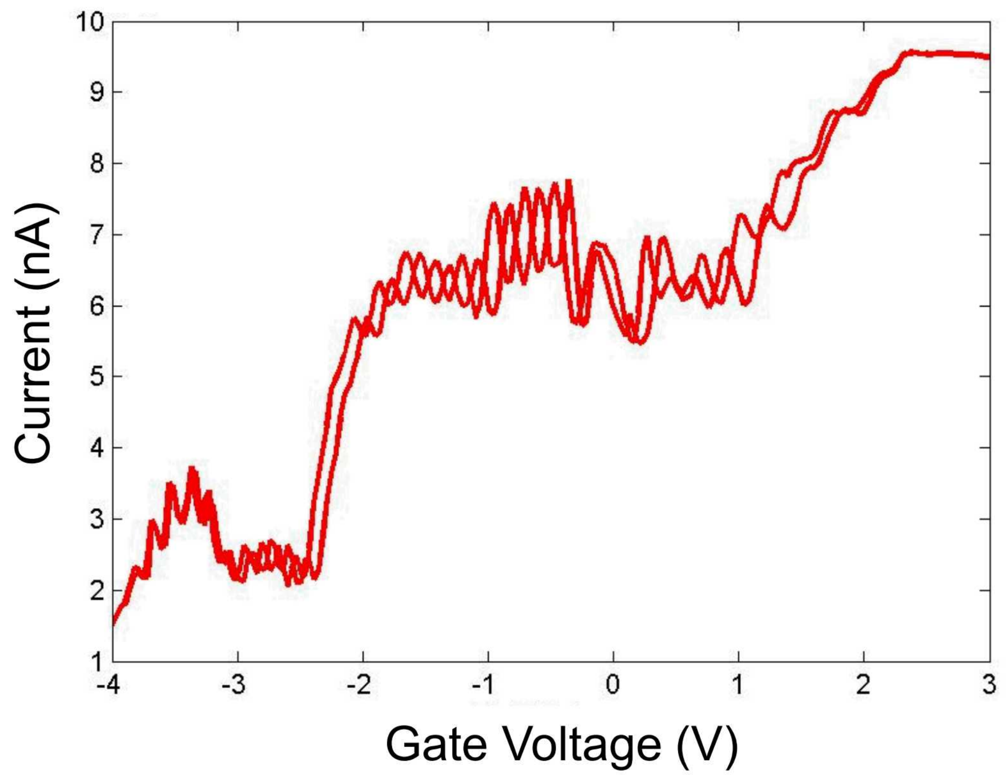


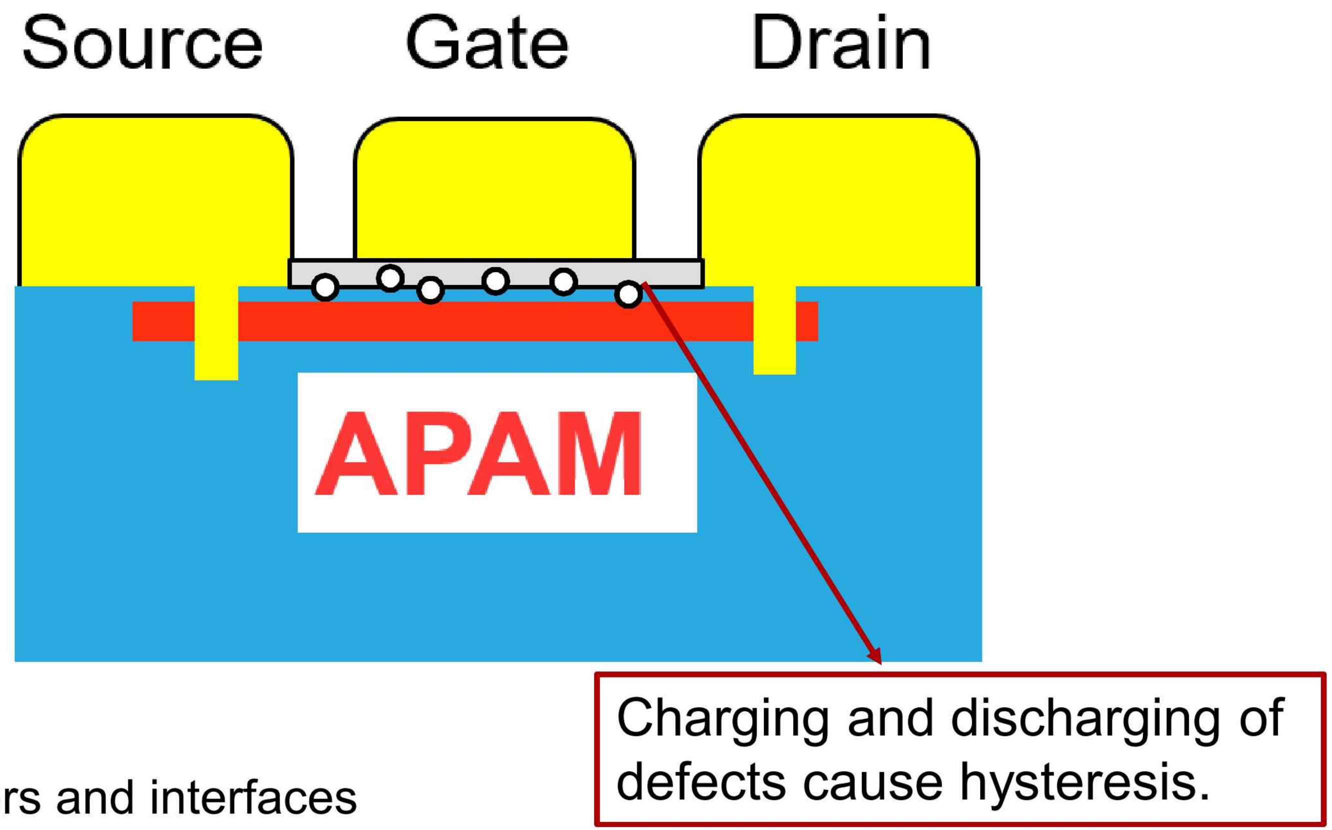


- We use a single-electron transistor so that we can calibrate the energy using voltages.
- The conductance oscillates with gate voltage
  - We can use the gate to change the number of electrons on the island.

The gate works!

The gate stack still needs improvement

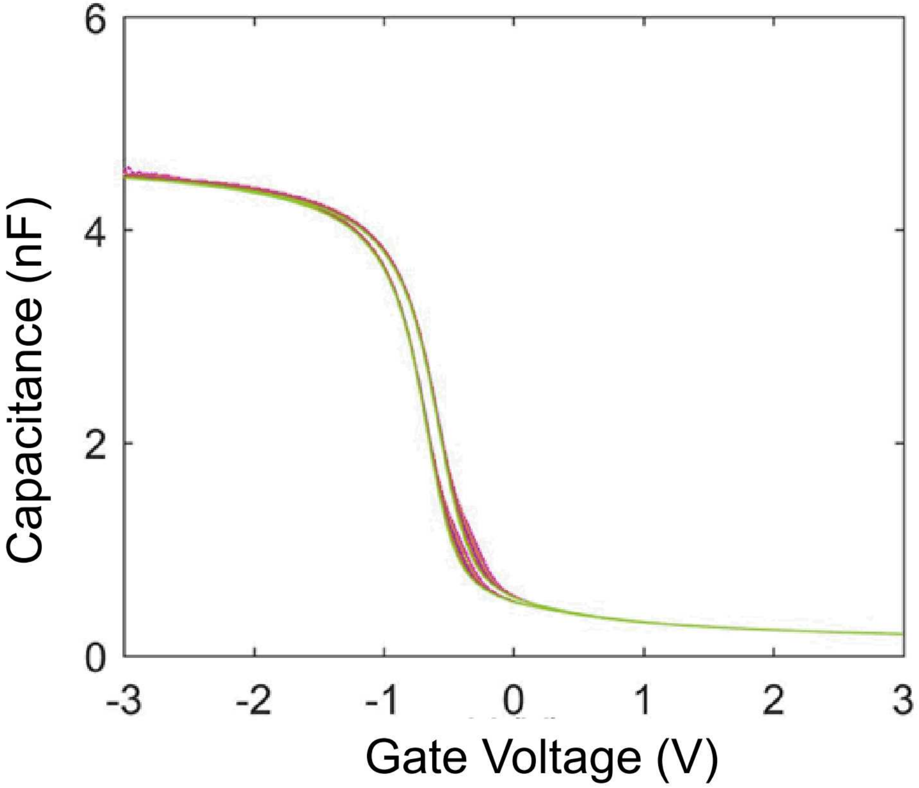




- Hysteresis is observed => non-ideal dielectric layers and interfaces
- The gate does not work at higher temperatures.

We need to address the defect problem to make better surface gates.

Quantifying the quality of gate stack

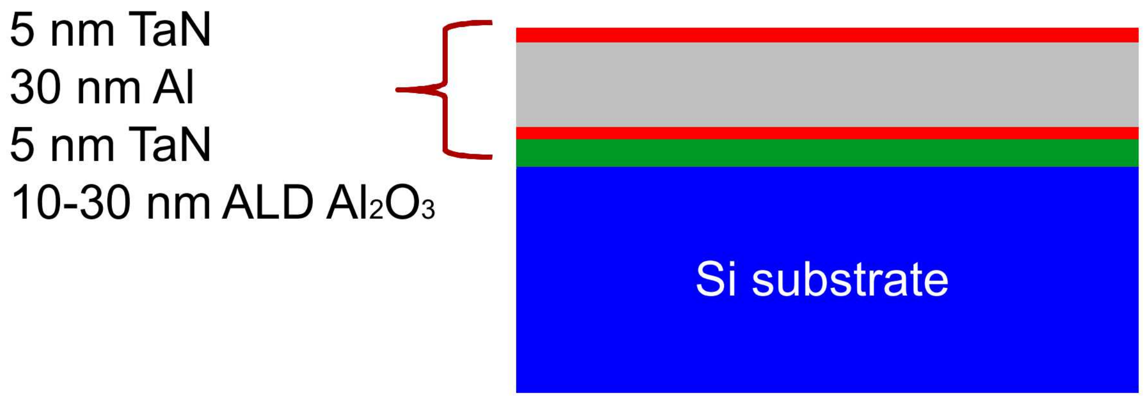


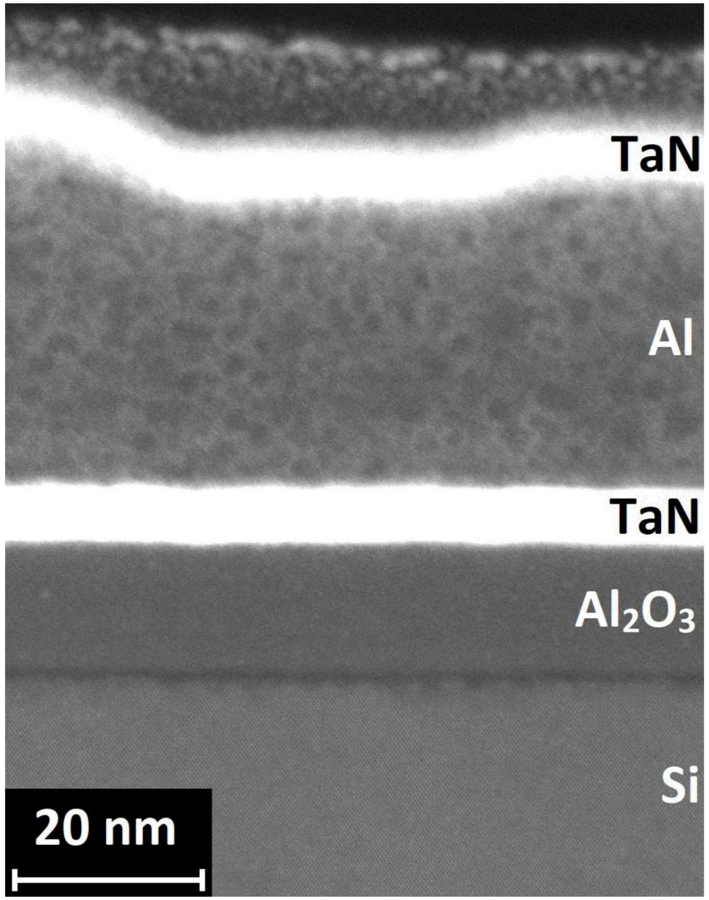
Frequency dispersion and hysteresis in CV measurements on Si MOS control samples yield defect densities ~$10^{11}/cm^2$

This defect density may be sufficiently good for proof-of-principle APAM surface gated devices.

CV measurements allow us to quantify the quality of our gate stack.

FY19 – Developing low-thermal-budget dielectric/gate stacks

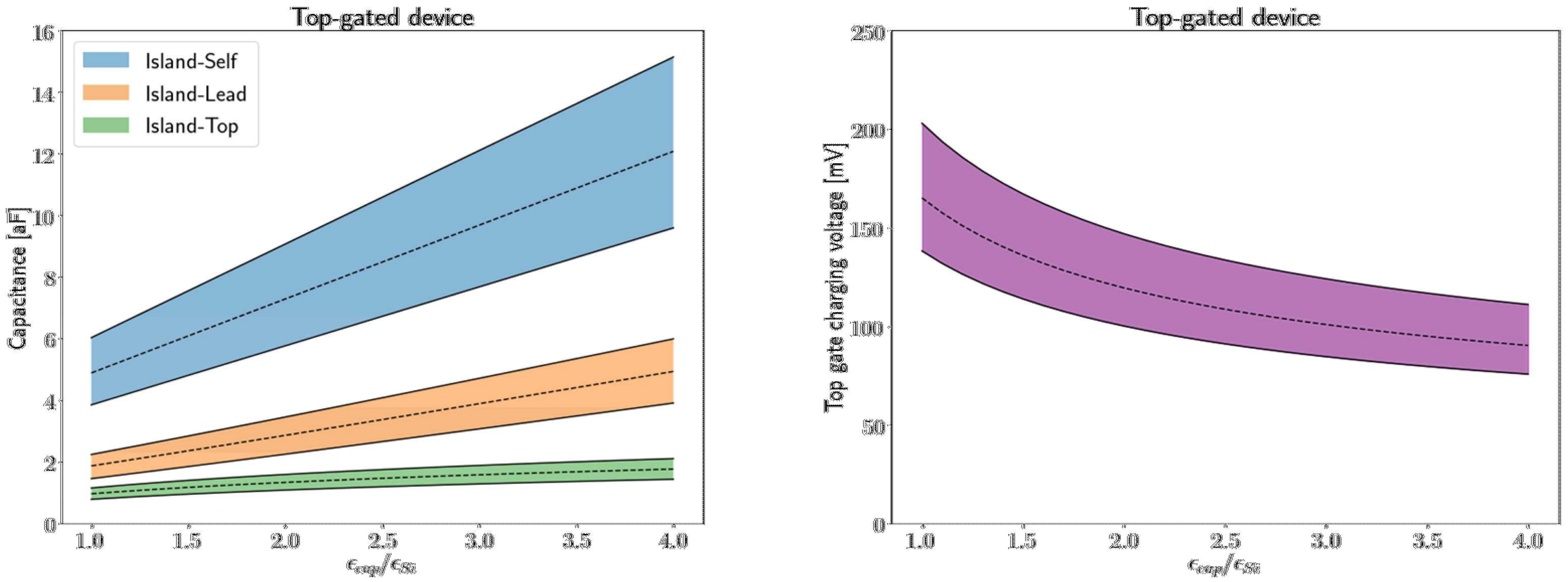




- All processes are performed low temperatures to avoid diffusion of the phosphorus delta layer.
- This is inspired by high-k metal gates for CMOS.
- We tweak the stack for APAM compatibility.

A low-thermal budget baseline process flow has been developed.

FY19, FY20 – Modeling the gate stacks



We are developing models for the gate stack to understand the device CV and IV characteristics.

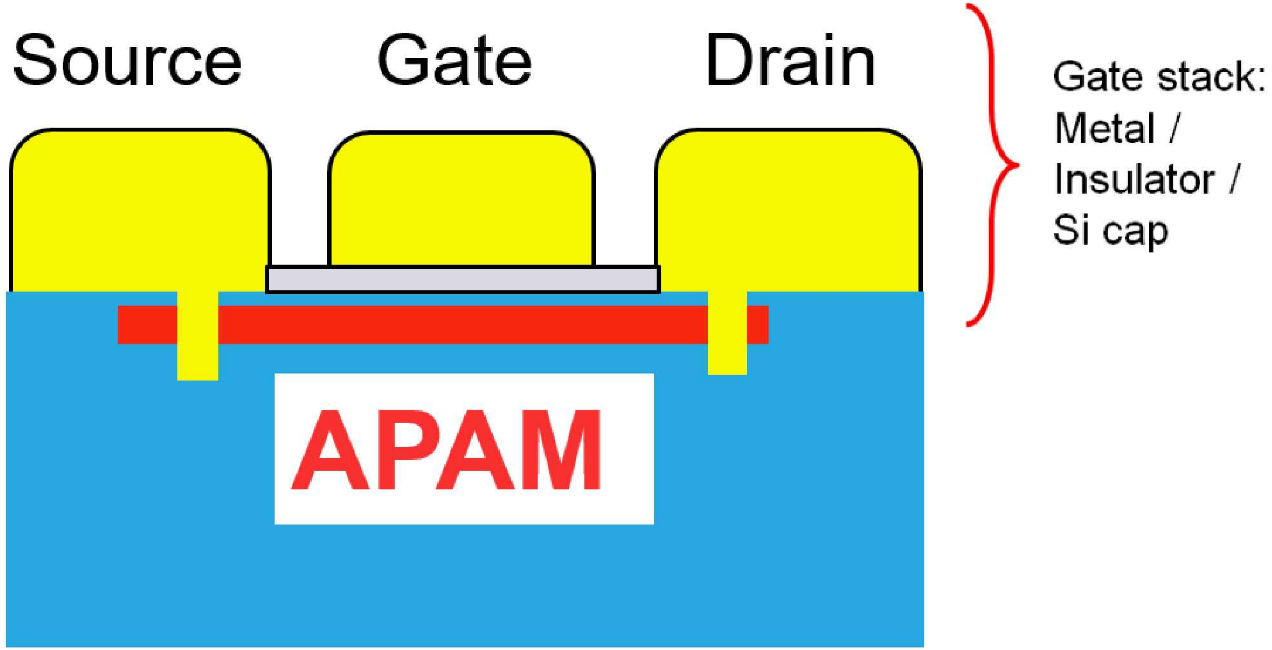
FY20 – surface gated APAM devices

- Many knobs to turn for the gate stack.
  - People usually don't turn these knobs.
  - With new investment, cycles are much shorter.

- Next: gate stack on top of APAM devices

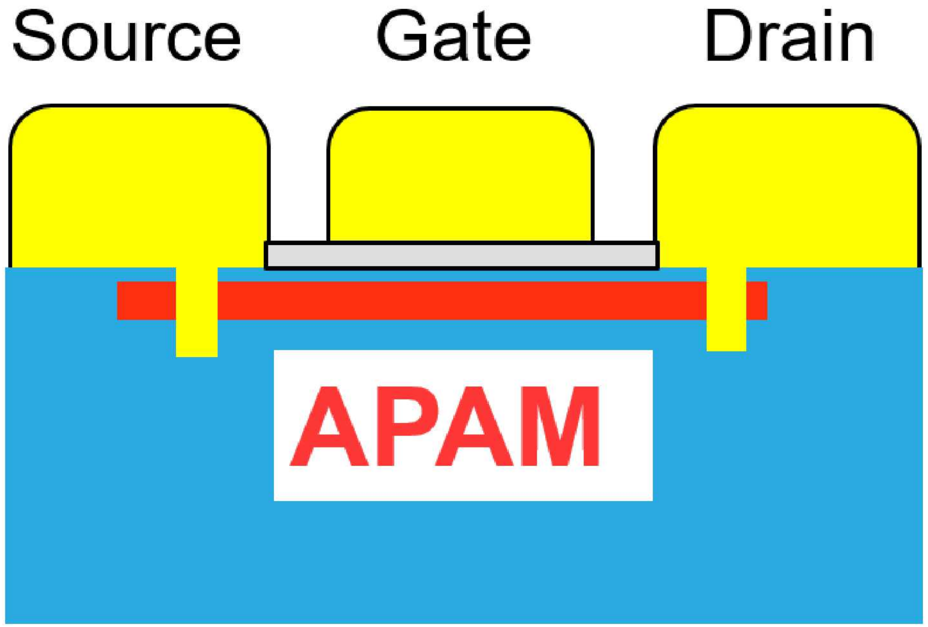
- Modeling and simulation

- The goal: assess whether the chosen process flow for gate stacks is sufficiently good for our proposed device architectures.



Outlook

- Preliminary results are promising (gating phosphorus donors at 4K, CV data at room temperature)
- We are trying extensions of existing solutions already developed for CMOS but not proven for APAM. If this exploratory effort returns a parameter space beyond our scope, we will stop and refocus our resources.



Plan for FY 20

Go/no-go

Are gates good enough to make projections?
Can we make them better?

Critical path

Thrust #1: APAM devices

APAM Channel | Room T Operation | Surface Gating | Photonic elements

Critical path

Can we design a fingerprint?

Go/no-go

APAM Photonics

Sandia National Laboratories

Goal:

Determine if APAM is useful for manipulating light

How we got here:

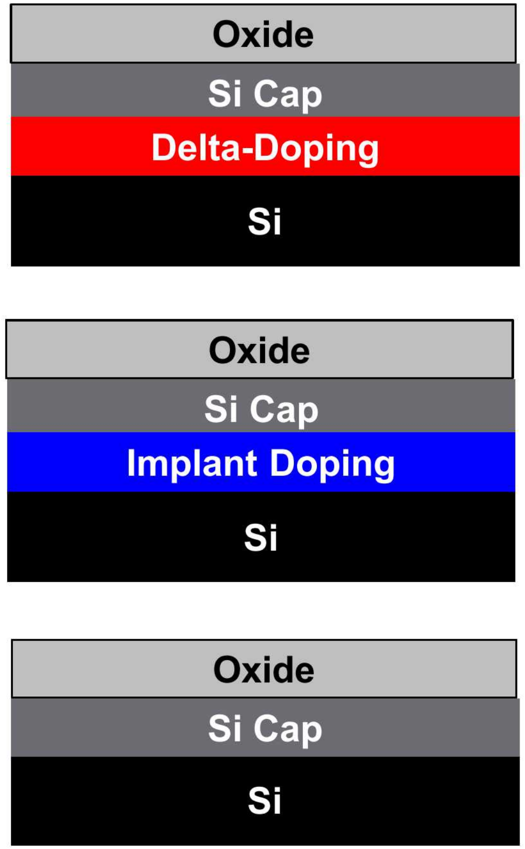
Needed: Faster, easier device characterization → faster cycles of learning

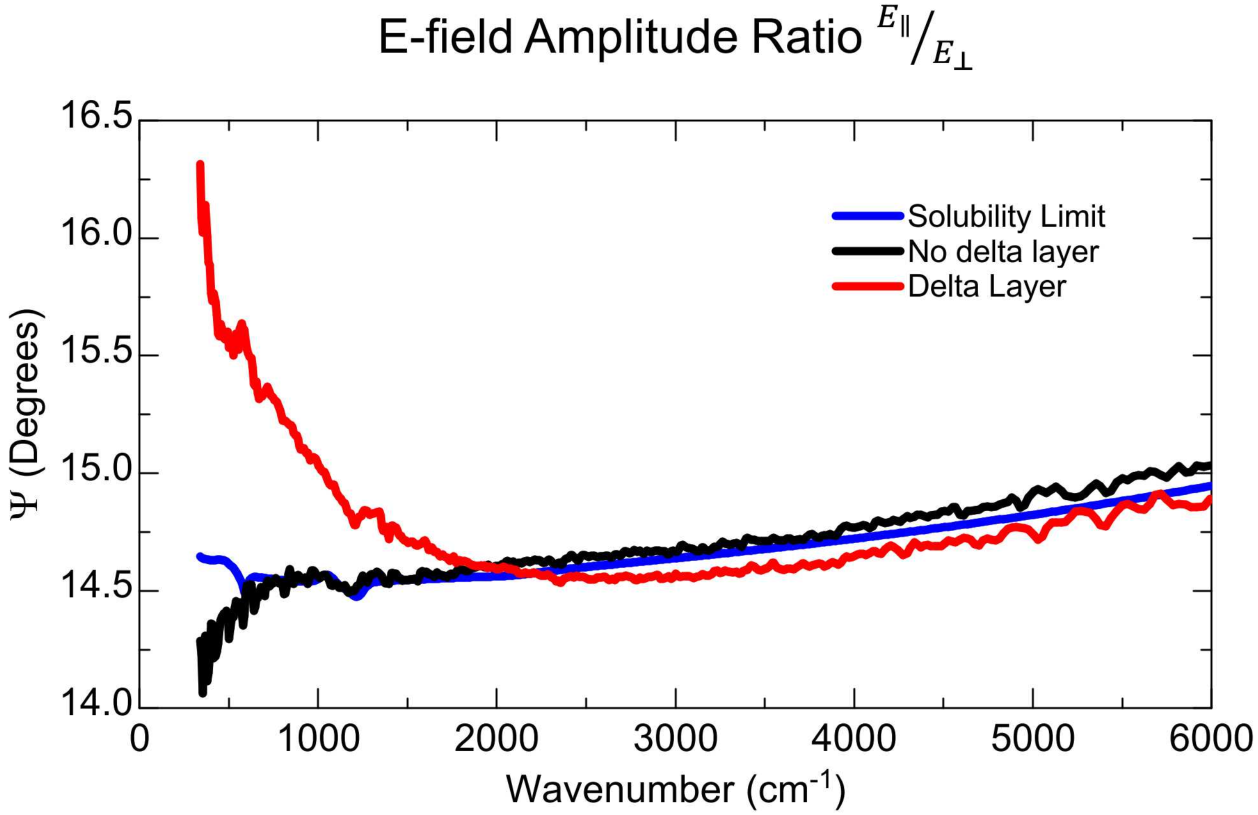
Discovered: IR Ellipsometry – fast, easy, *novel room temperature response**

*Katzenmeyer et al. "Assessing adsorbate-based delta-doping of silicon with mid-IR ellipsometry" (in preparation).

Optical Response – δ-layer vs conventional doping

Amplitude and phase depend on wavelength, angle, polarization
Unique delta layer response – *high* density of electrons!



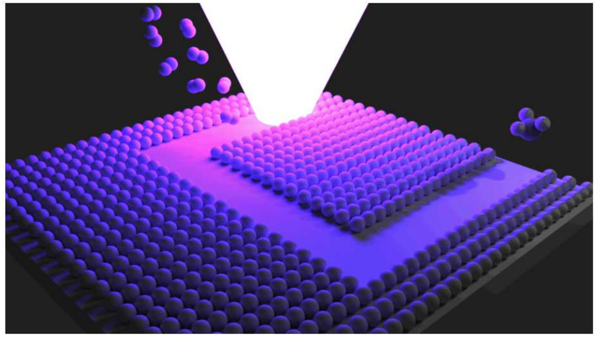


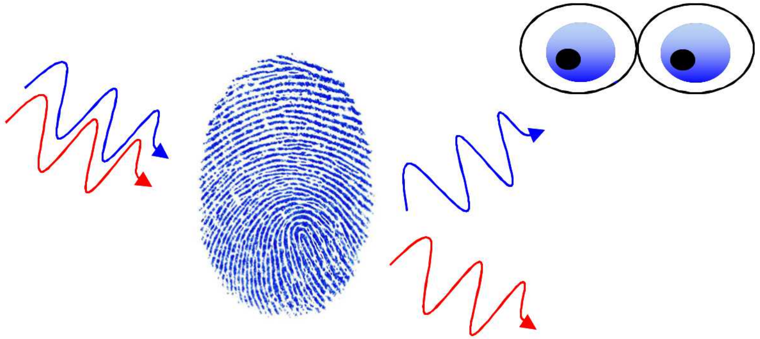
Exemplar: Fingerprint

Engineer a patterned delta-layer (metasurface) for device identification

Need to know what to look for

Wavelength
Polarization
Angle of Incidence
Phase





Design

Simulate

Fabricate

Test

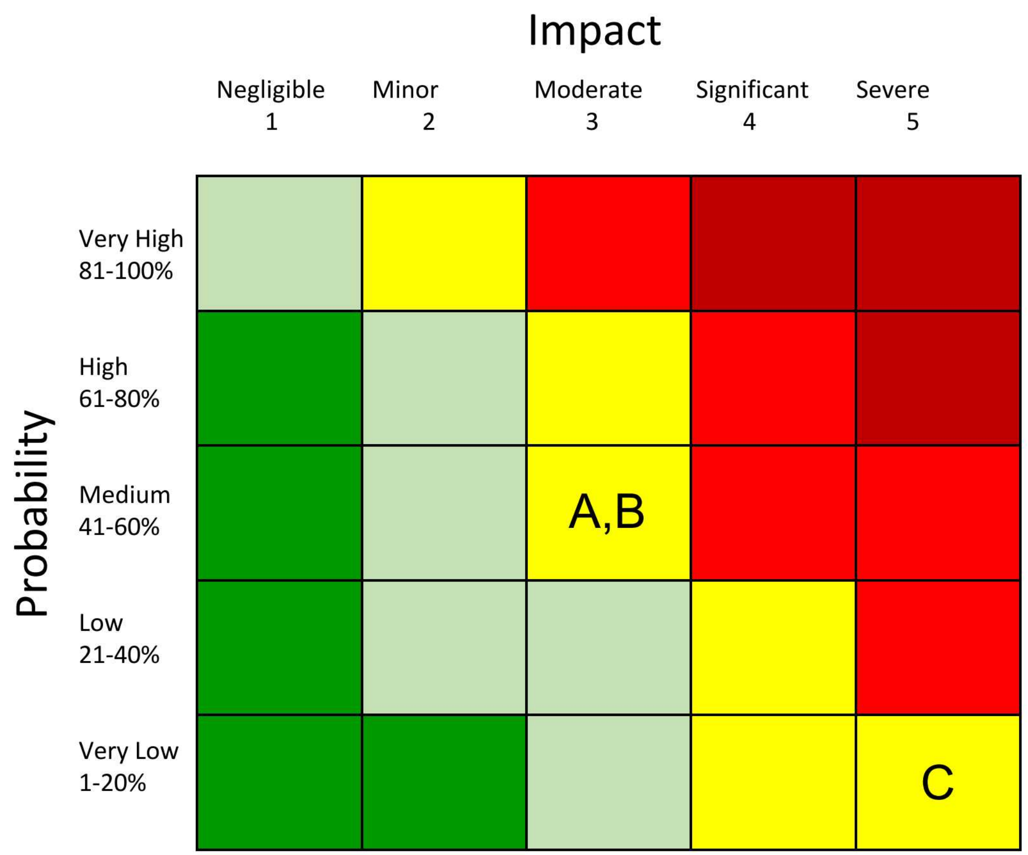
Modify for integration / applications?

Risk assessment

A) Unsure of what to design

B) Patterning method online?

C) Characterization capability exists?



Progress and Outlook

- FY19
  - Determined δ-layer optical constants and RT frequency “window”
- FY20
  - Simplest pattern simulated – looks promising for engineering
  - Design underway
  - Methods identified for initial fabrication and testing
  - After demonstration:
    - Integration needed
    - Identify additional applications

Plan for FY 20

Go/no-go

Are gates good enough to make projections?
Can we make them better?

Critical path

Thrust #1: APAM devices — APAM Channel → Room T Operation → Surface Gating → Photonic elements

Critical path

Can we design a fingerprint?

Go/no-go

Backup slides follow

Thrust 1 FY 20 milestones

Milestones for Channel engineering	Expected Completion
What is thermal budget for P layer diffusion? What variables control 4K wire current density? P density, thickness, defects?	Q1
What variables control 4K tunnel junctions?	Q2
What variables control R(V,f) and C(V,f) for APAM nanowire?	Q3
Design RT channel for APAM NMOS.	Q4

Milestones for Photonics	Expected Completion
Determine dielectric constant of a delta layer.	Q2
Show fab-measure-model control over response from grating	Q3
ID what makes a good fingerprint	Q3
Show control over structure more sophisticated than a grating	Q4
Go/No-go: Design exemplar fingerprint and detector	Q4

Milestones for RT Operation	Expected Completion
Is Si dep prep sufficient	Q1
Determine acceptable cap doping for via modeling. Must allow for <1% leakage through bulk at 1V reverse bias and gating milestone	Q2
Create and test platform for testing delta layers at room temperature where leakage from contacts to substrate is minimal (<1% of sheet current at 1V reverse bias)	Q3
Create and test method of adding dopants to cap during growth. Acceptable doping levels will be determined by modeling and starting carrier concentration in cap before doping	Q4

Milestones for Gating	Expected Completion
Does e beam prep work (SIMS, hall)	Q1
Pick between choices of dielectric based on experimentally measured dielectric layer properties	Q2
Measure the IV characteristics at 4 Kelvin in surface-gated STM-patterned devices with modeling-informed designs.	Q2
Quantitatively correlate dielectric layer properties and IV characteristics through device modeling and simulation.	Q3
Go/No-go: Determine whether the efficiency of surface gating is sufficient for proposed new device architectures. If yes, proceed with new device architectures. If not, identify alternate, viable solutions for gating.	Q4

Thrust 1 FY 19 milestones

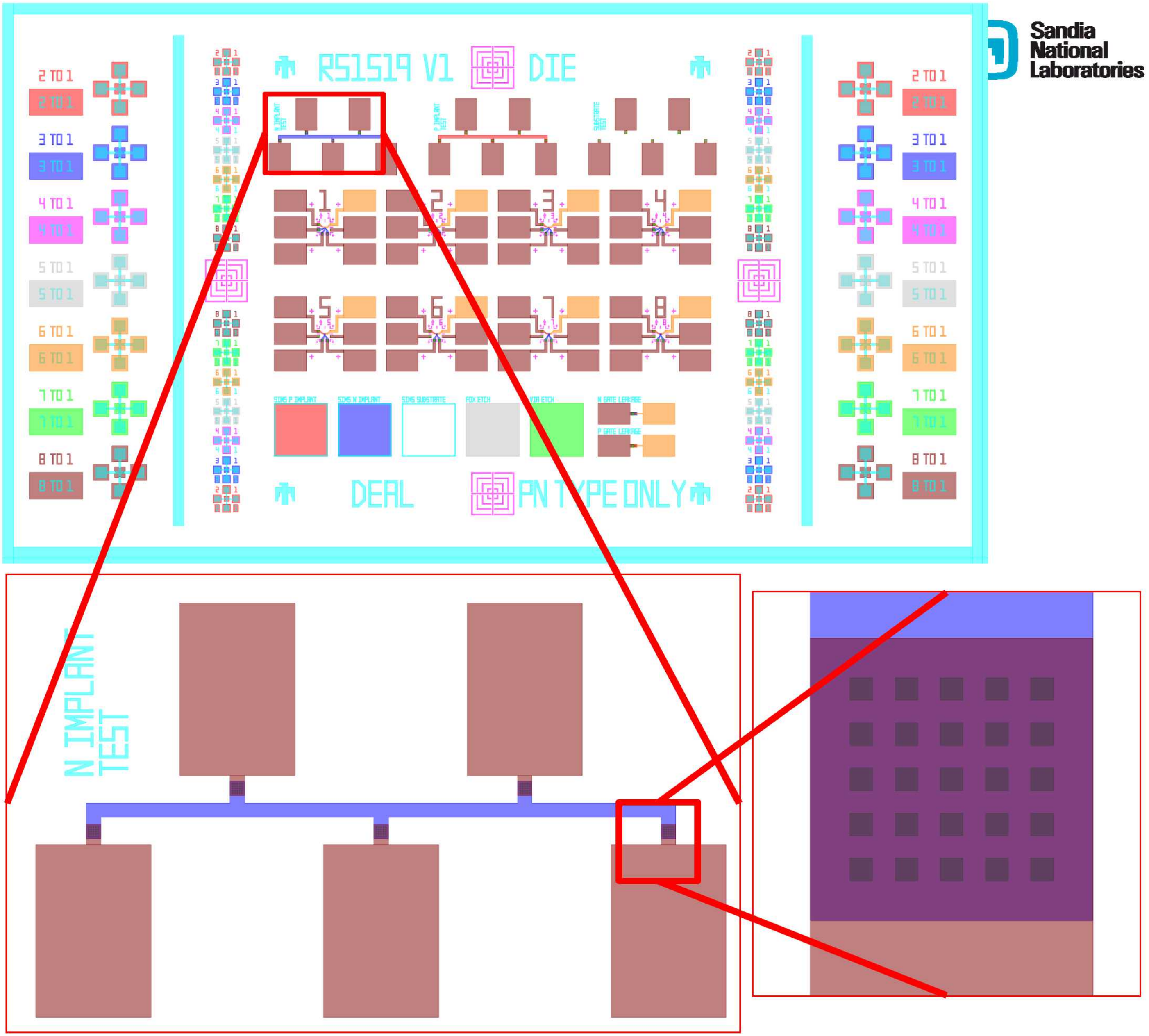
Milestones for Reliability	Expected Completion	% Complete	Comments
ID ways to characterize P layer and defects ID recipes for tight P layer, low defect P layer, low defect cap	Q3	75% 66%	Can't tell thickness of P layer wewith TEM Tight P layer recipes hard to evaluate.
Correlate recipes to performance and repeatability of wire.	Q4	33 %	Delayed to FY 20 – evaluated one of the three recipes.

Milestones for RT Operation	Expected Completion	% Complete	
Order e beam Si source Semiclassical model of depletion identifies scope of problem	Q2	100%	
Design isolation chip Build co-deposition source	Q3	100%	
First data from isolation chip - does this need a redesign? Test e-beam and codeposition sources. Silane facilities in CINT	Q4	33% 25% 100%	Samples STM → microfab 1st set of codeposition samples to SIMS.

Milestones for Gating	Expected Completion	% Complete	
Establish CV data on baseline gate stack	Q3	100 %	Good CV curves. One defect is known to come from AlOx-Si interface. Leakage not understood.
Establish CV data on STM silicon cap	Q4	50%	Samples STM → microfab.
Establish CV data on delta layer	Q4	50%	Samples STM → microfab.

Goals

- Use n-type implant tester on RS1519 to demonstrate substrate isolation from implants
- How does this work?
  - Bond pads must not contact anything other than N^{++} silicon or oxide
  - Vias to N^{++} silicon must not penetrate past region of high doping (must be shallow)



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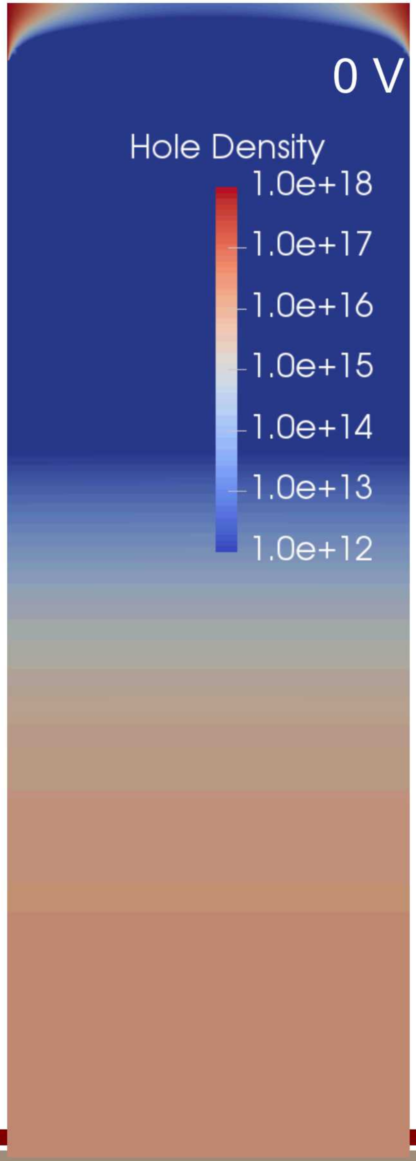
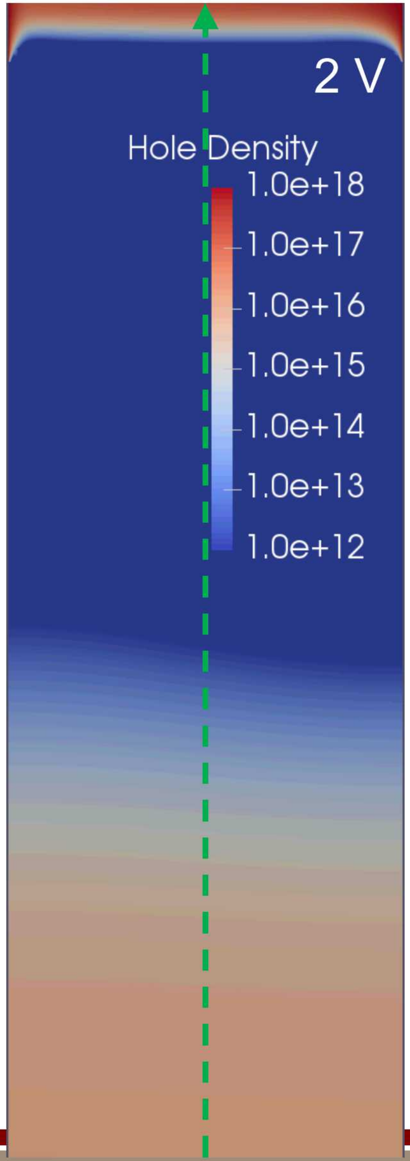
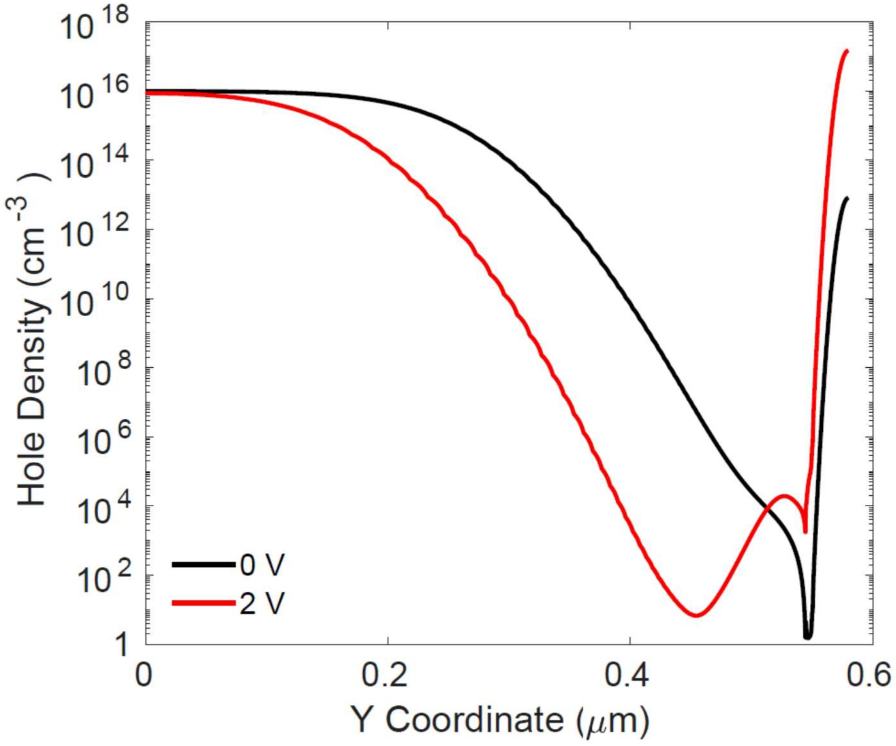
Simulation Results – Hole Density







At 0 V, the hole density in the epi layer is 5 orders lower than the doping.

At 2 V, the hole density in the epi layer is 1 order lower than the doping.

Fin