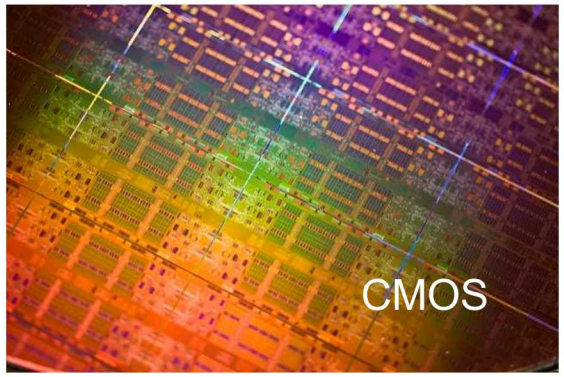
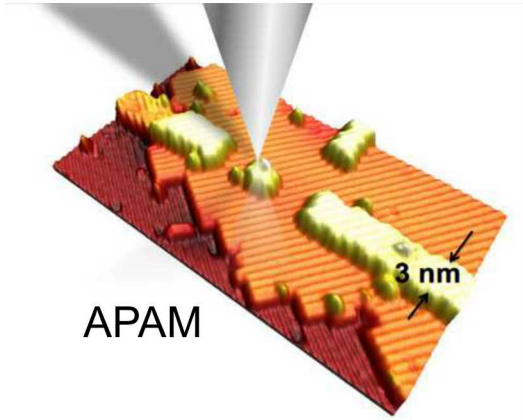
SAND2019-13379PE





FAIR DEAL GC Thrust 3: APAM – CMOS integration

Dan Ward (Lead), Steve Carr, David Scrymgeour

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Digital electronics at the atomic limit (DEAL)

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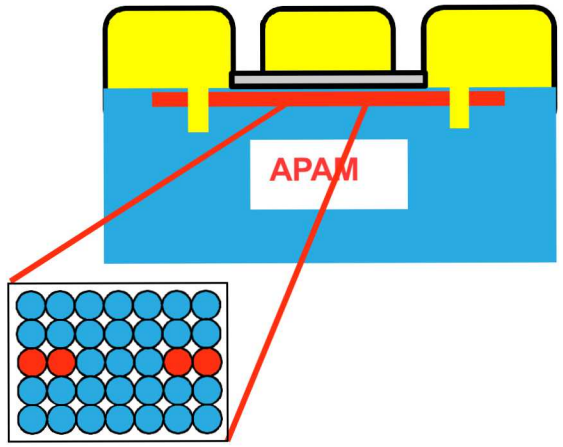
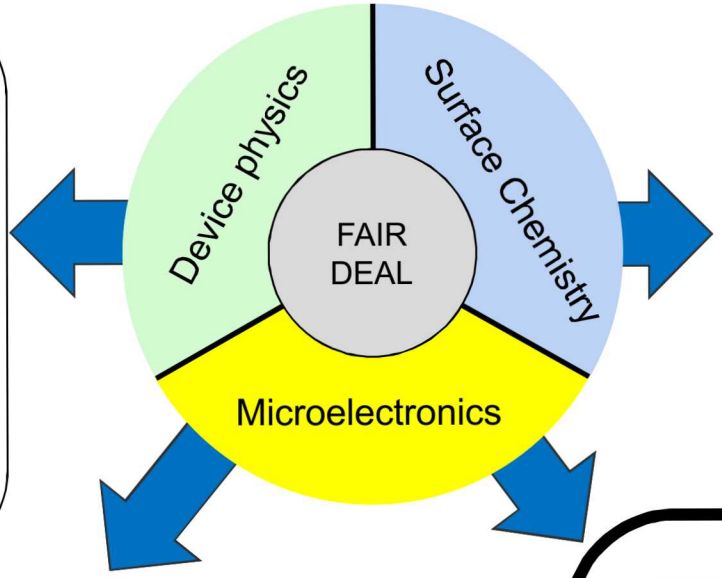
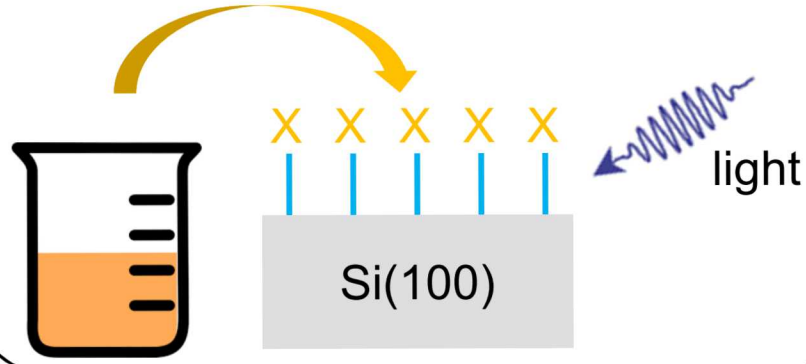
Thrust 1: APAM-enabled Devices

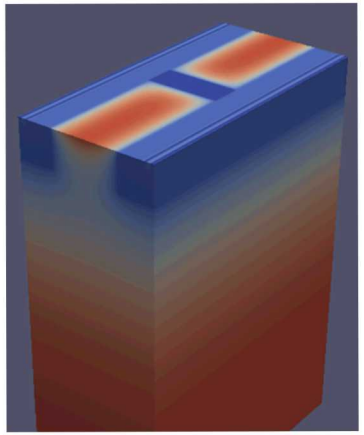




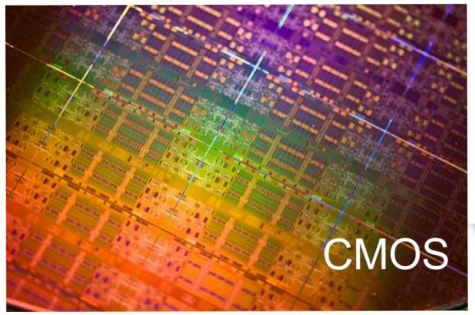
Thrust 4: Application Platform

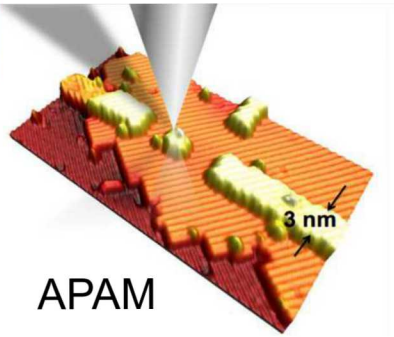


Thrust 2: APAM Modeling



Thrust 3: CMOS Integration





CMOS Integration is critical to furthering APAM

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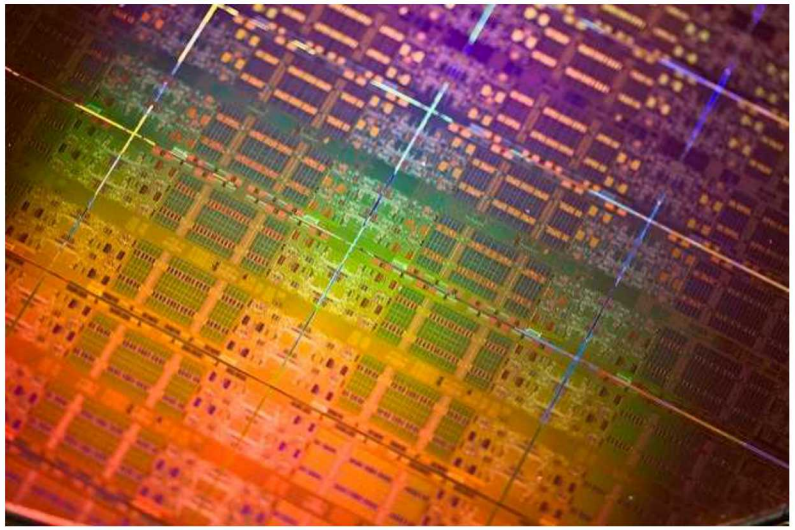
CMOS



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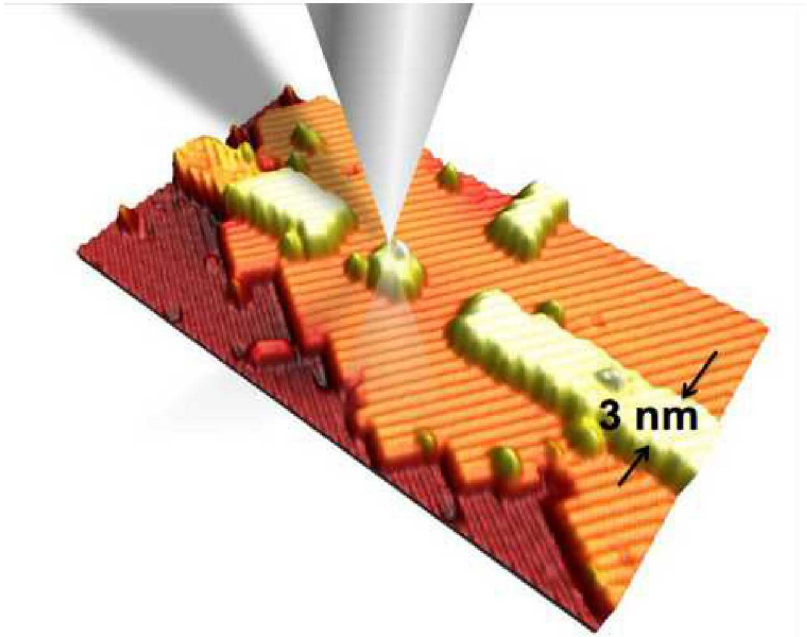
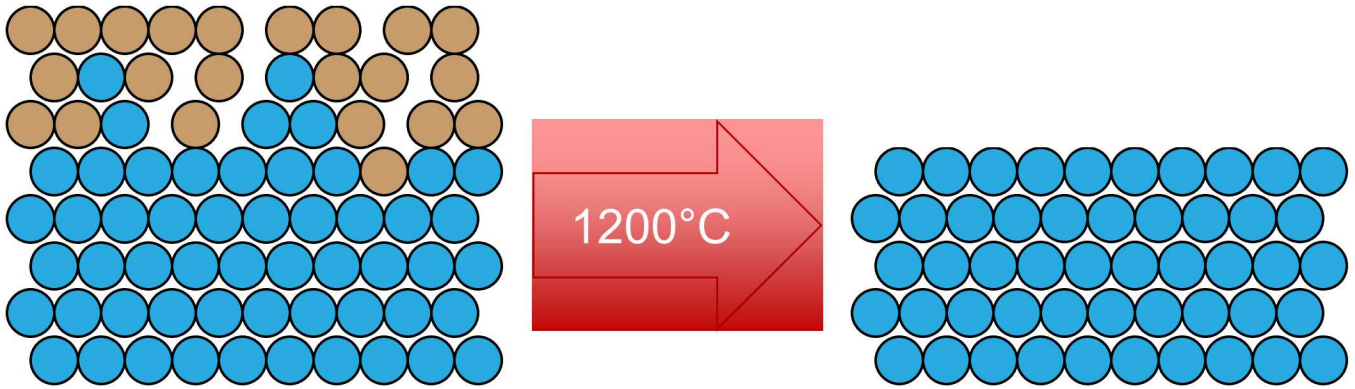
APAM

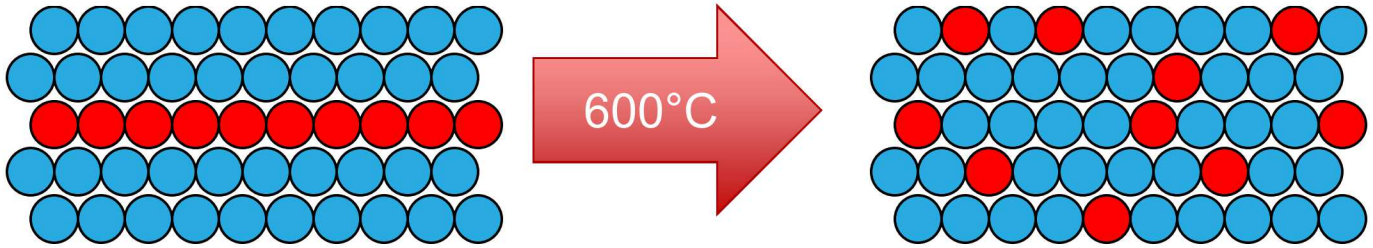


- CMOS is really good at many applications
- APAM will accelerate specific tasks
  - Not seen as a full replacement
  - Determining accelerated tasks now
  - Augment CMOS to provide task specific advantages
- Necessary to combine APAM and CMOS circuits to get maximum benefit

APAM Sample Prep was Incompatible with CMOS



Si
Contaminants
Phosphorus



- Thermal budget of 1200 °C, for a few seconds prevents integration of CMOS elements **before** APAM
  - Dopants diffuse in Si
  - Metals alloy with Si
  - Silicon “flows”
- Thermal budget of 600 °C, for a few minutes prevents integration of CMOS elements **after** APAM
  - Phosphorus atoms diffuse
  - Lose the advantage of APAM
  - Initial CMOS structures need temperatures > 850°C

State of the Art for Integration in 2017

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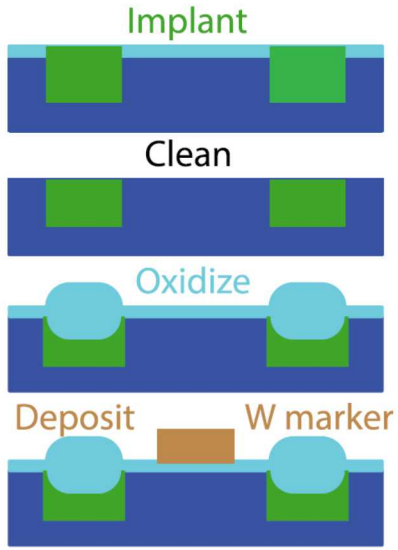
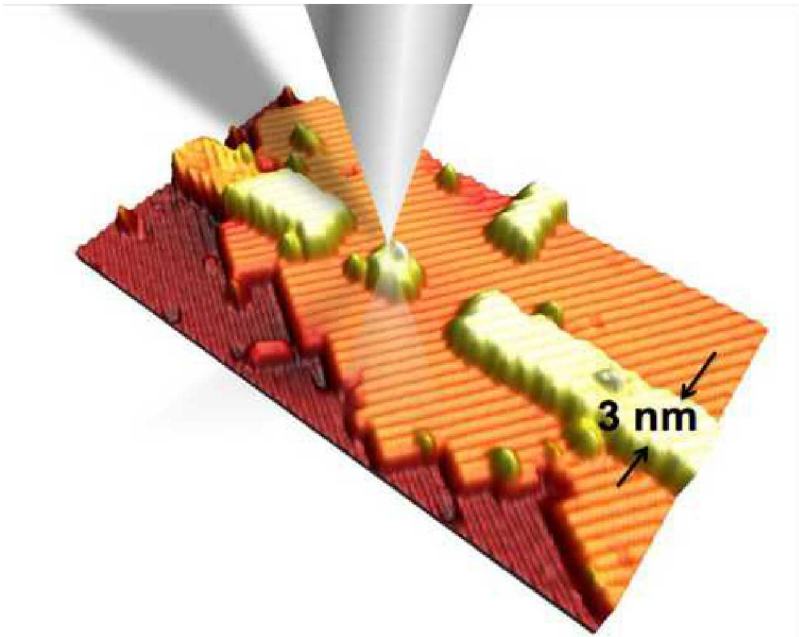
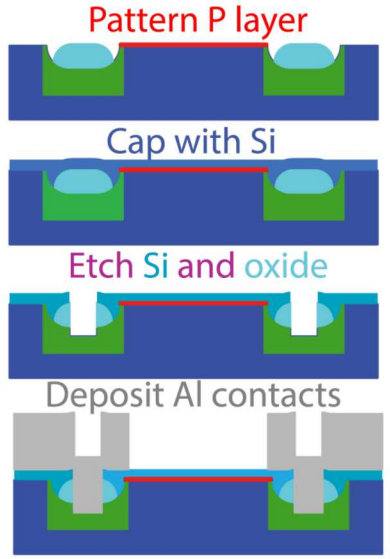
High T Processes (>850°C)

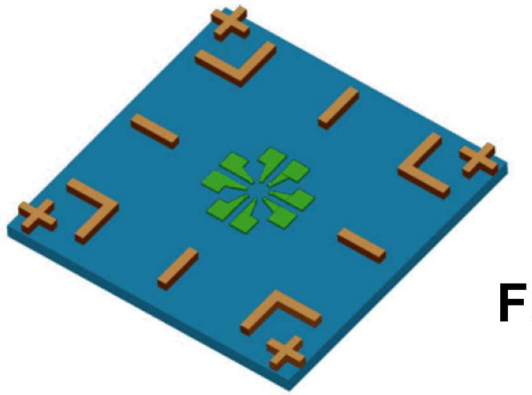


APAM 800°C Process



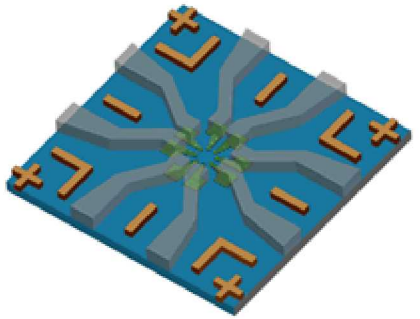
<450°C Processes





Integration proof of principle exists

Full CMOS demonstration opens application space



Ward, **APL** 2017

Can APAM be integrated into CMOS Systems?

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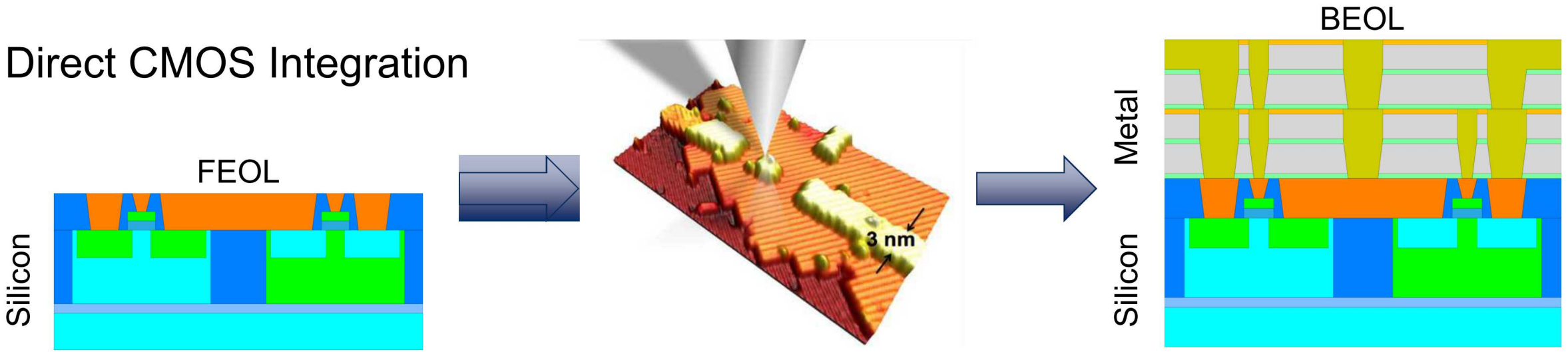
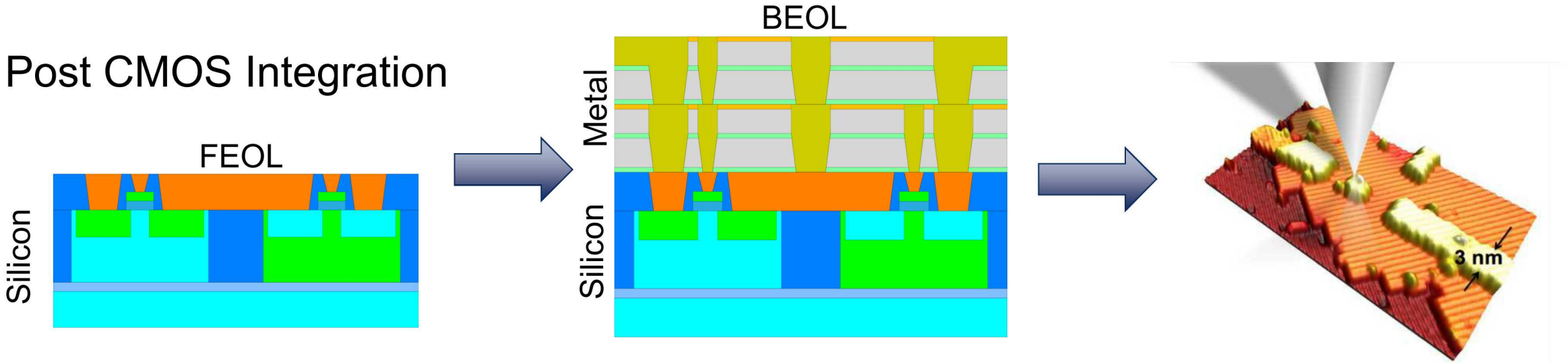
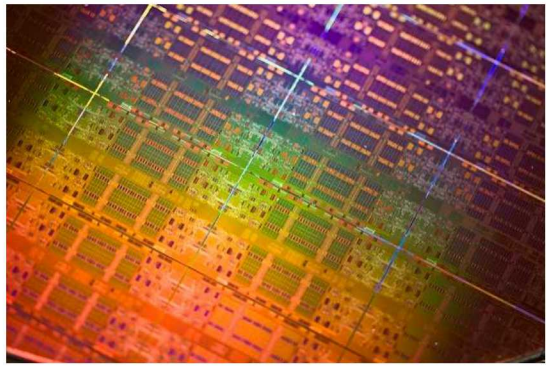
Direct CMOS Integration



Post CMOS Integration



Refinement of integration goals creates new task



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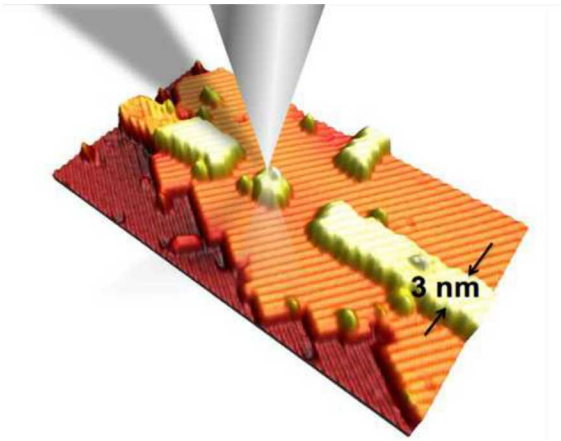
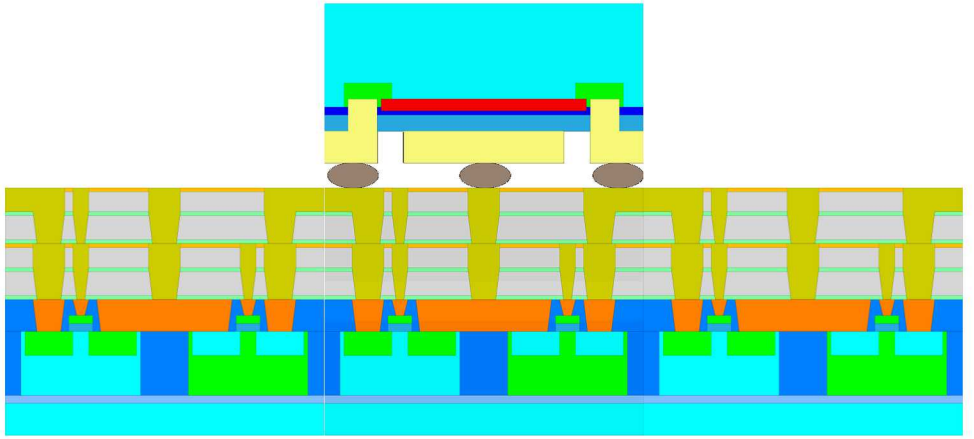


When we succeed: How well does the APAM device hold up compared to CMOS?

New task: Robustness

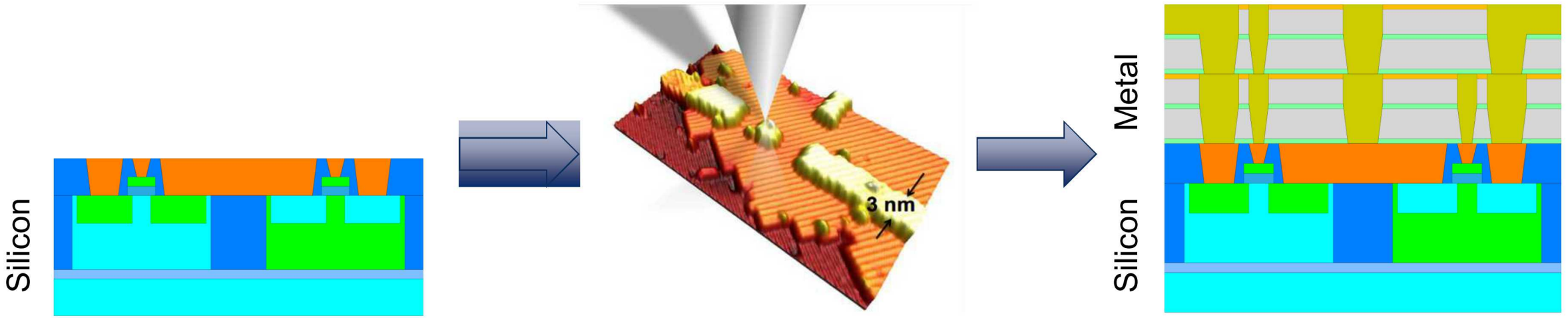


Heterogenous integration task dropped on recommendation of EAB

- IBM already looked into this
- Requires success in the other integration tasks → Redundant

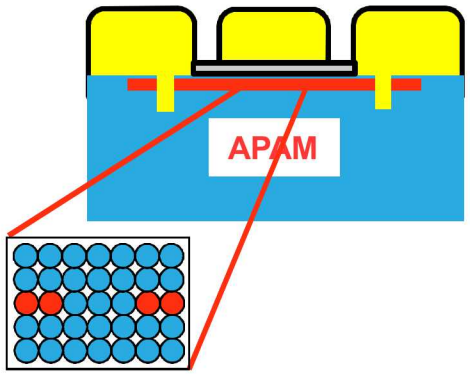
Skeren, et. al., **Nanotechnology 29**, 43 (2018)

Why is this challenging?



Original tasks	Revised tasks	Difficulty
Direct CMOS Integration	Direct CMOS Integration	Process incompatibility between CMOS & APAM. **"No change is a small change"**
Low Temperature Processing	Post-CMOS Integration	Maximum thermal budget of 450C **"No change is a small change"**
Heterogenous Integration	Post-CMOS Integration	Maximum thermal budget of 450C
	Robustness	Completely unexplored research space

Impact of Thrust 3

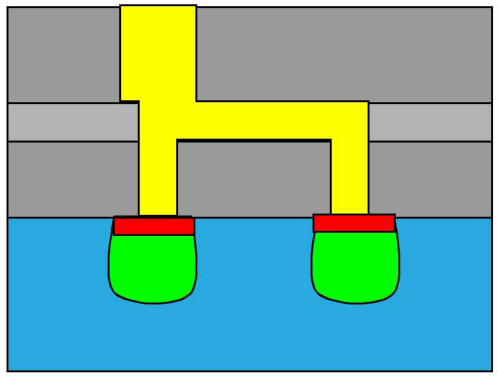


APAM – MOS

Need:
- Direct CMOS Integration
- Robustness

Interconnects

Need:
- Direct CMOS Integration
- Robustness



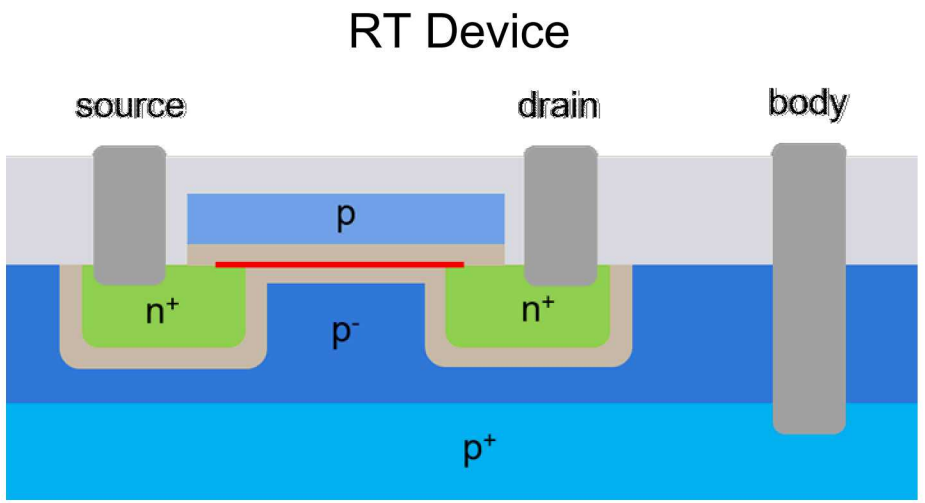
Fingerprint:

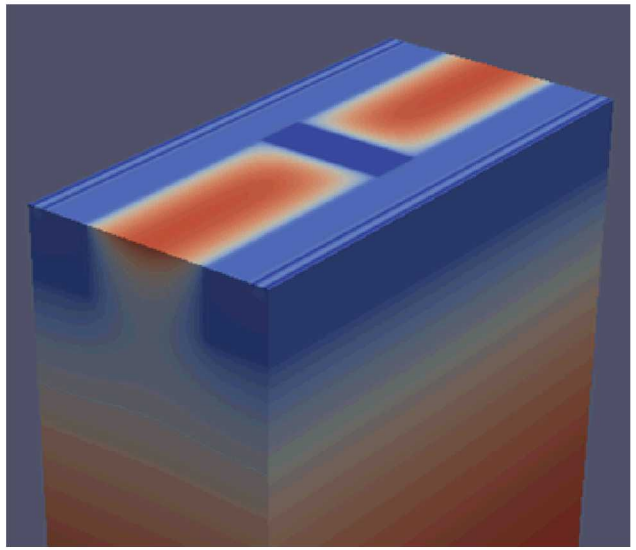
Need:
- Post-CMOS Integration
- Robustness

Want:
- Direct CMOS Integration

Strong ties to APAM Devices and Modeling Thrusts

- Devices operate at room temperature
- APAM/Gate oxide interactions must be understood
- Need to be able to work on various substrates





Tunnel junction model

- Device modeling
- Circuit modeling

Thrust 3 – Metrics

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Collaborations

- Exploring: SkyWater

Talks

- Invited talk at IBM
- 3 contributed talks for application driven engineering audiences

Thrust 3 – Progress is reducing risks

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Direct Integration (A)	Hetero Integration (B)	Low Temp Process (C)	Robustness (D)

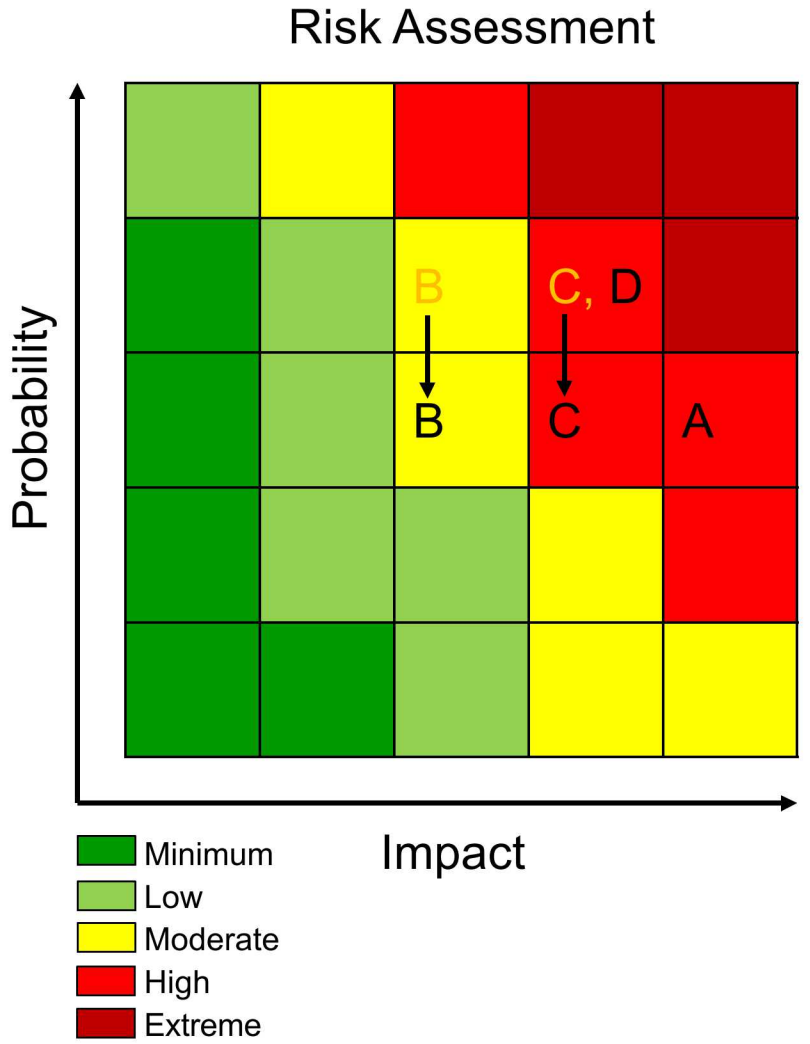
A. Direct Integration: Much more complicated than expected, multiple paths forward

B. Heterogenous Integration: Basic APAM processing is compatible.

C. Low Temp. Process: All processes except clean work. Pushing on surface preparation in FY20

Post-CMOS Integration

D. Robustness: New area of research



Thrust 3 – New capabilities

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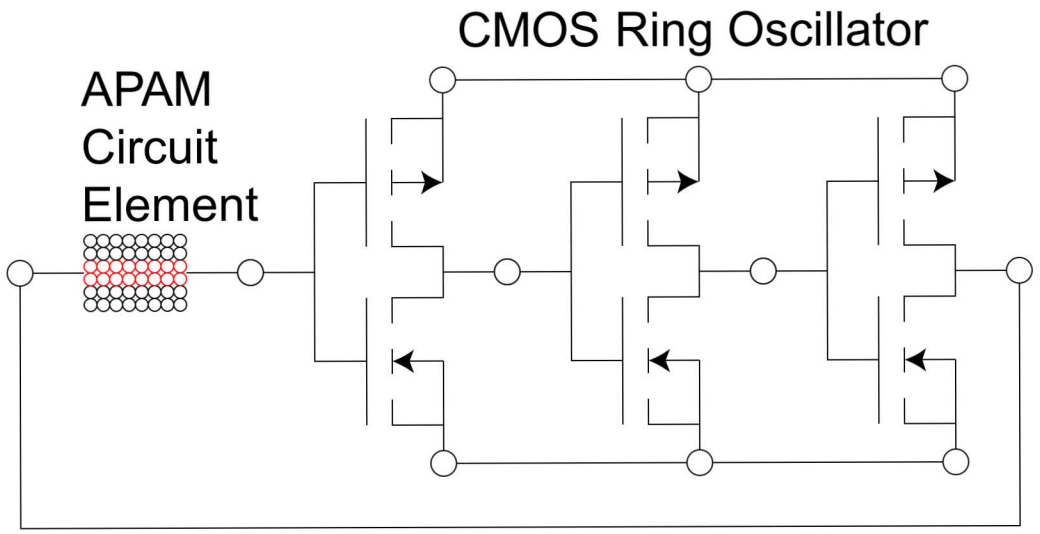
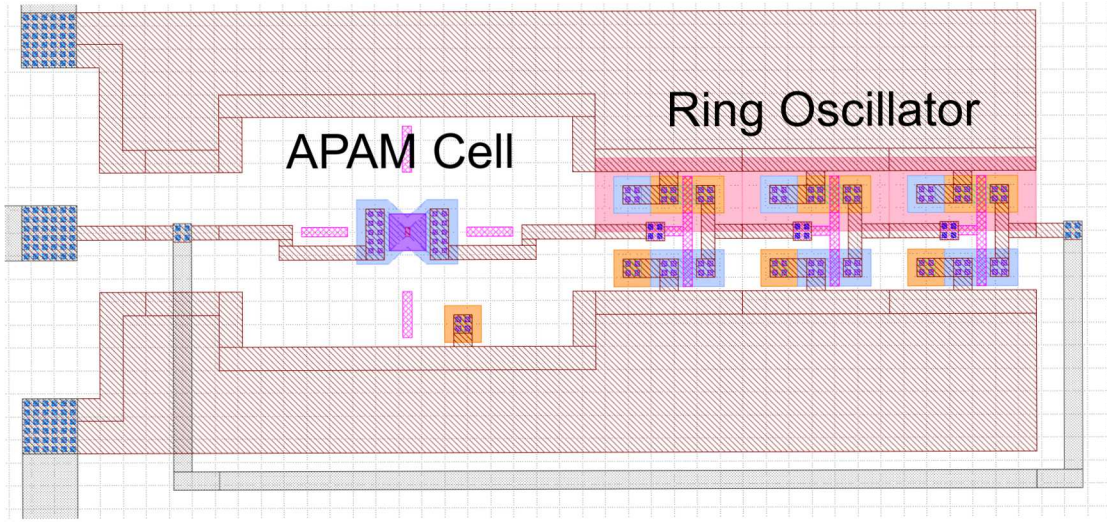
Circuit editor



Physical Layout



Process Design Kit (PDK) Cell for APAM device

Enables building APAM devices directly in Cadence (IC layout software)

Thrust 3 – New capabilities

Robustness
Measurement Setup

Thrust 3 – Discoveries

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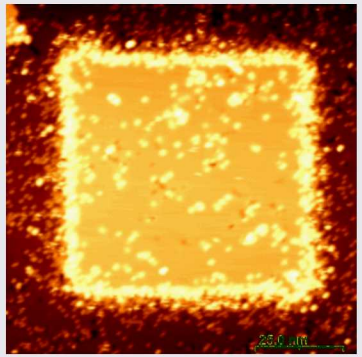
Room temperature processes for everything except prep

1. Clean ?
2. H term & pattern

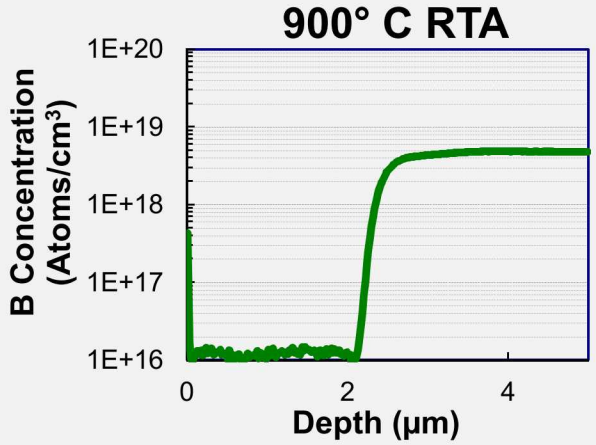


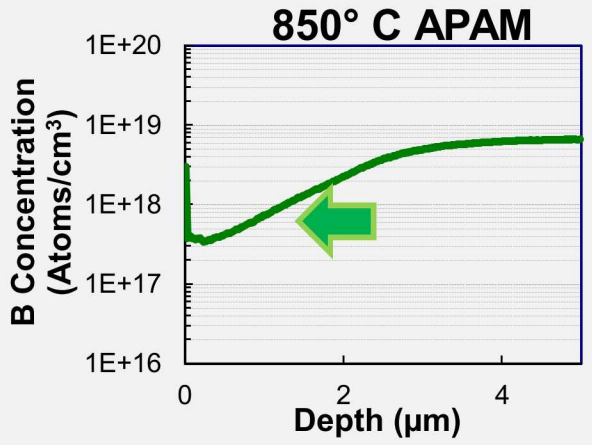
3. PH_3 dose and cap

Normal	σ = **2** mS/sq.
RT process	σ = **0.6** mS/sq.

Polished surfaces can be prepped

Acceptor dopants in wafer electromigrate





Plan for FY 20 – All tasks on Critical Path

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Can APAM be integrated into CMOS Systems?

Critical Path
- How does CMOS affect APAM?
- How does APAM affect CMOS?

Direct Integration

Post-CMOS Integration

Critical Path
- Maximum current densities?
- Maximum operating temperature?

Robustness

Critical Path
- Can APAM process be run at <450°C?
- Is the electrical quality good enough?

Thrust 3 – Organization

Task Leads
Direct CMOS Integration: Dan Ward
Post CMOS Integration: Steve Carr
Robustness: David Scrymgeour

Make

APAM	Microfab	SiFab
Shashank Misra	Dan Ward	Troy England
Evan Anderson	DeAnna Campbell	Andrew Starbuck
Scott Schmucker	Mark Gunter	
Jeff Ivie	Philip Gamache	
	Sean Smith	

Measure

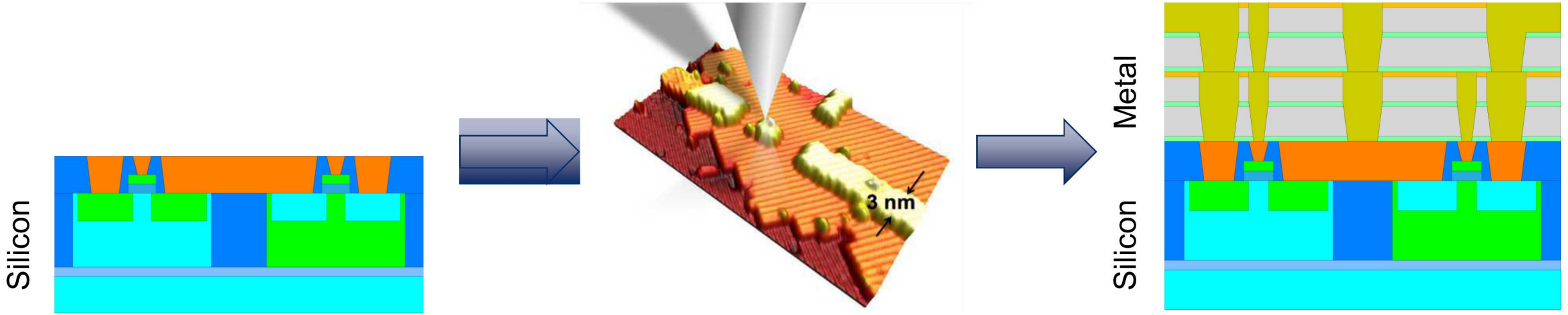
Electrical
Lisa Tracy
Tzu-Ming Lu
Albert Grine
Steve Carr
David Scrymgeour

Model

Devices/circuits
Suzey Gao
Bill Lepkowski
Baozhen Jin

THRUST 3 – DIRECT CMOS INTEGRATION

Direct CMOS Integration



Front-End of Line
(>850 °C)

APAM
(800 °C)

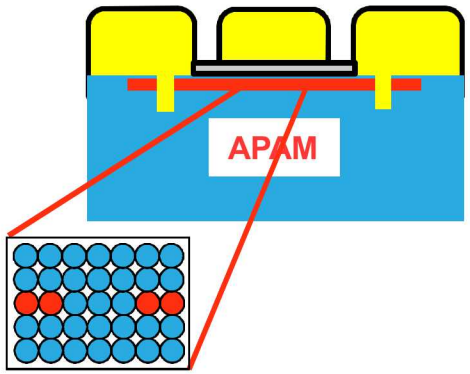
Back-End of Line
(<450 °C)

Scoping problem: What effort level is needed to integrate APAM into a CMOS process flow?

- How does CMOS affect APAM?
- How does APAM affect CMOS?

"No change is a small change"

Connection to Exemplars

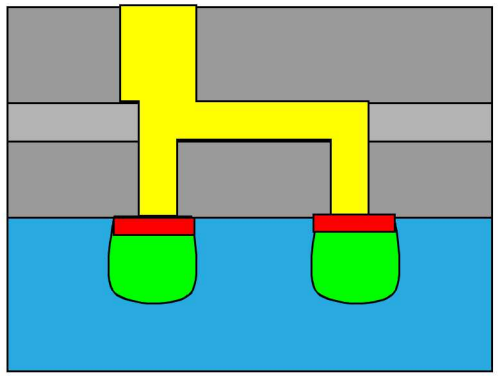


APAM – MOS

Need:
- **Direct CMOS Integration**
- Robustness

Interconnects

Need:
- **Direct CMOS Integration**
- Robustness



Fingerprint:

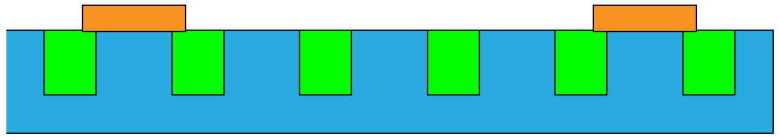
Need:
- Post-CMOS Integration
- Robustness

Want:
- **Direct CMOS Integration**

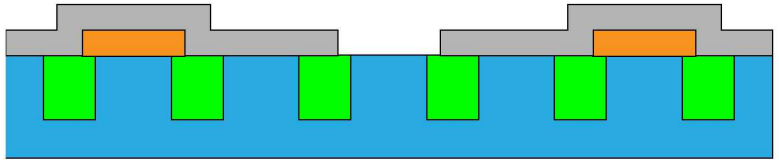
Integration Strategy

1. Run CMOS process through FEOL
2. Put down pre-metal dielectric (PMD)
3. Open windows in PMD
4. APAM Process
    1. Prep
    2. H-terminate
    3. Pattern
    4. Dose
    5. Incorporate
    6. Si Cap
5. Remove excess Si cap
6. Run remaining CMOS BEOL process

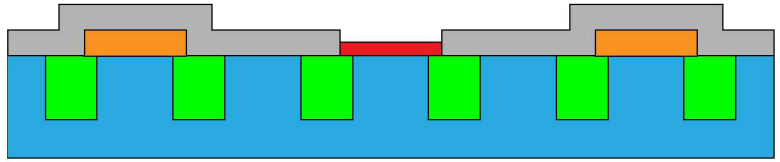
1. CMOS FEOL



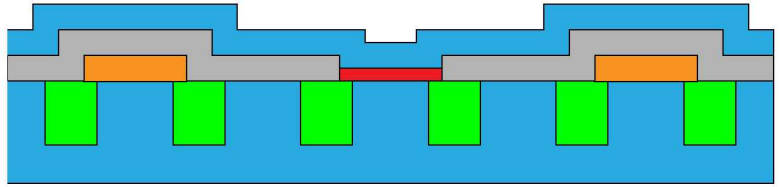
2-3. Open APAM area



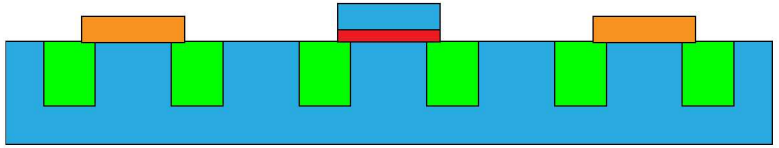
4. APAM Process



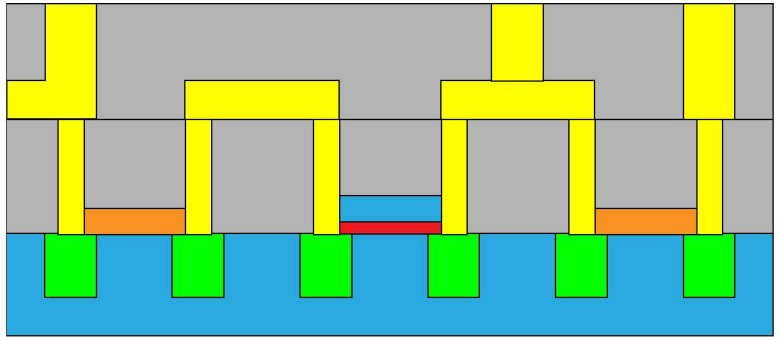
4. APAM Si Cap

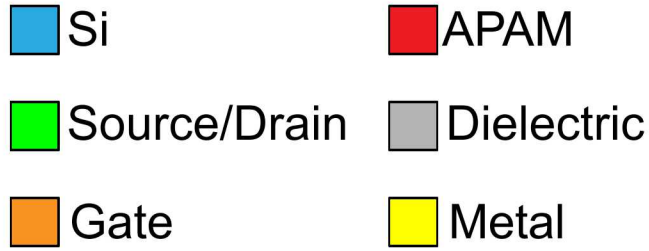


5. Remove excess cap/PMD



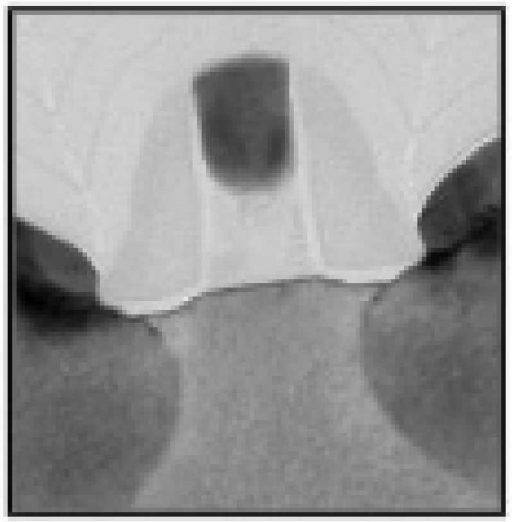
6. CMOS BEOL



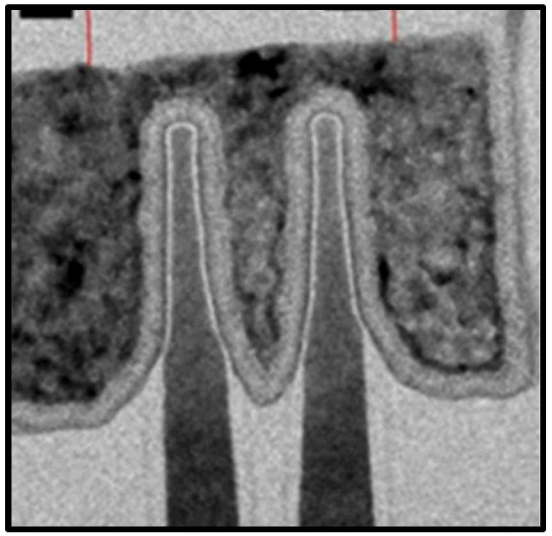


The Challenge

- Many flavors of CMOS
  - µFab
  - SiFab
  - External Foundry
  - 350 nm node ≠ 32 nm node ≠ 10 nm node
- Lots of process compatibility questions
  - Compatibility issues are foundry/node specific
- Limited to die level processing for now
- **Big Question: What can Sandia do to improve confidence in integration possibilities?**



65 nm



10 nm

Different nodes = Different process flow

Direct Integration End Goals

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1. Successfully insert APAM process into three CMOS flows

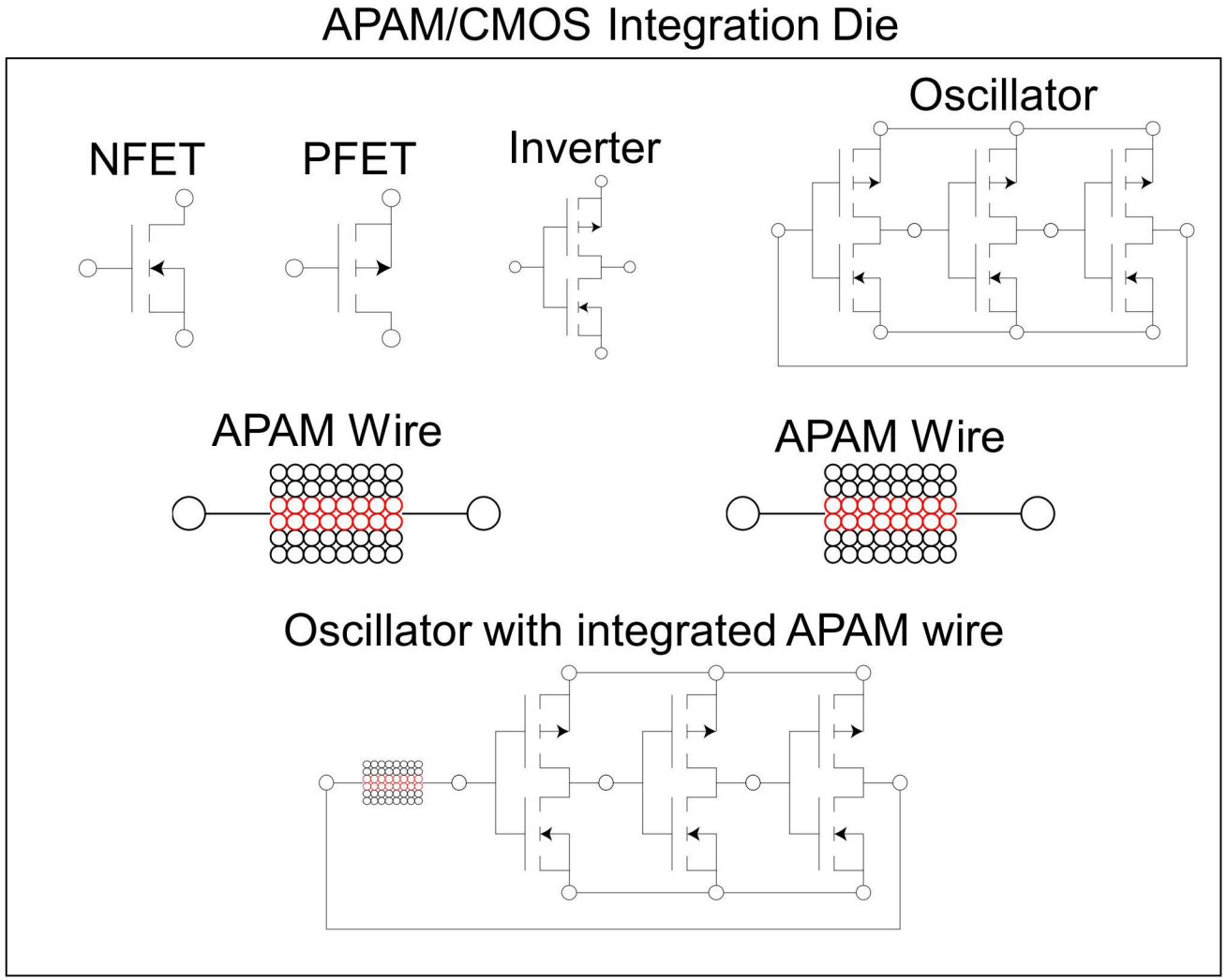
Fab	Feature Size	Benefits
Sandia μFab	2 μm	Fast, 100% control, High flexibility
Sandia SiFab	350 nm	True foundry, On-site → Maximum potential to coordinate/collaborate
External Fab	90 nm	True foundry, Most realistic application space

2. Understand integration process to scope future integration projects
3. Understand impact on APAM performance, what are likely limitations?

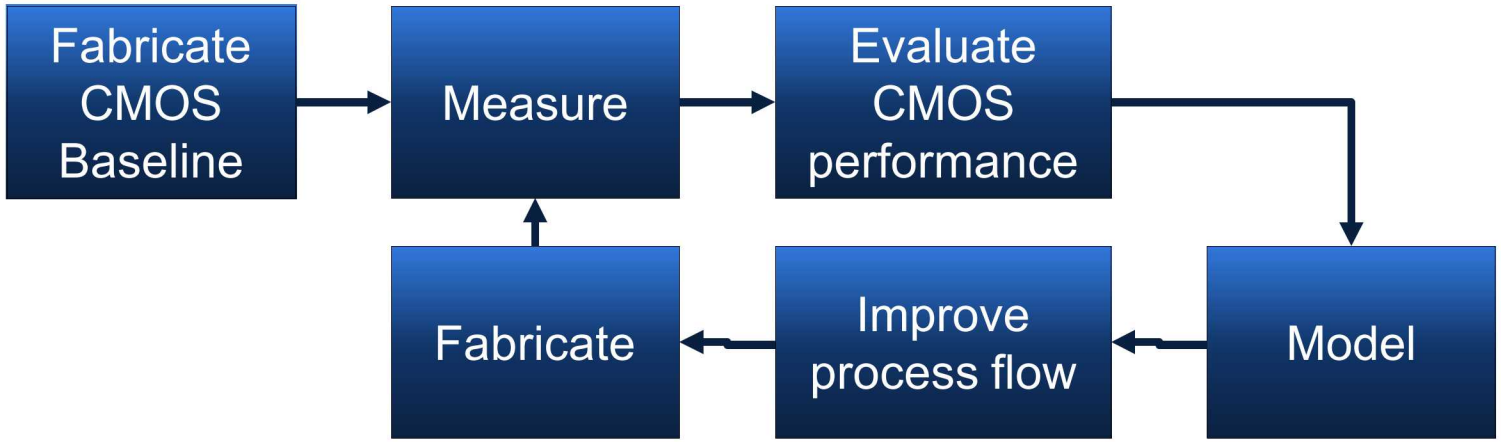
Evaluating APAM/CMOS Integration

Focus on basic structures

- CMOS
  - Transistors
  - Inverters
  - Ring Oscillators
- APAM
  - Wires only
  - Control structures
    - Implanted wires
    - Metal wires
- Integrated structures
  - APAM wire as routing path for CMOS



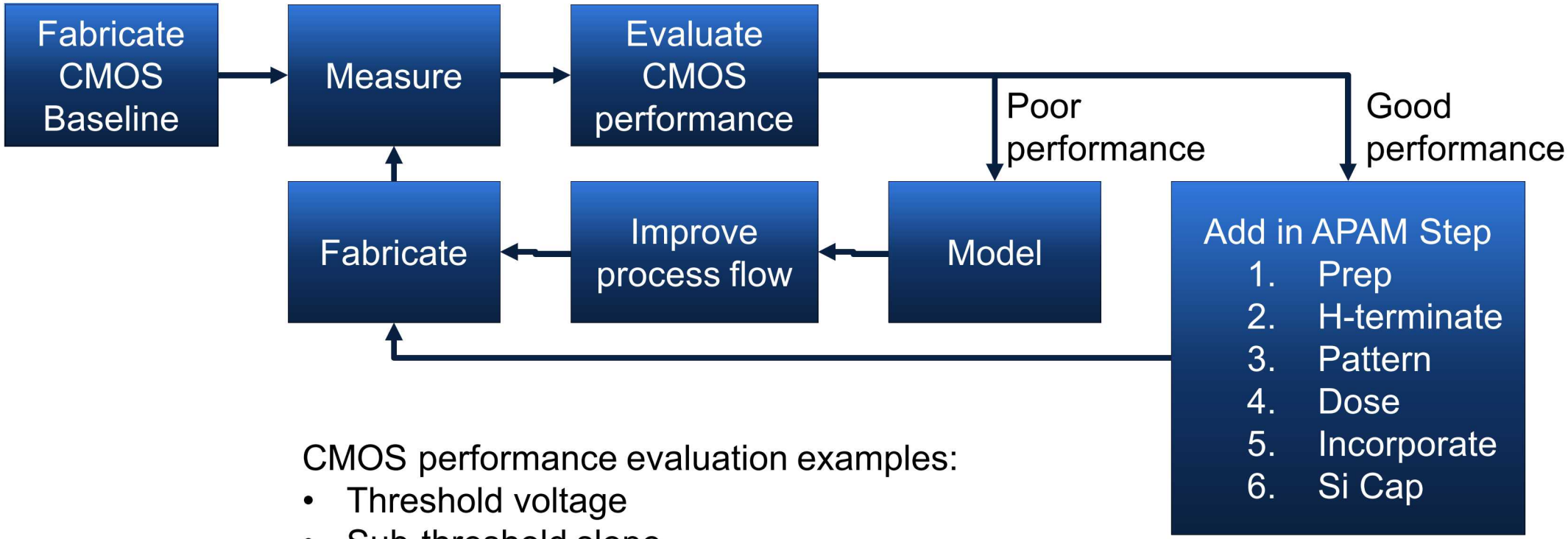
How do we evaluate CMOS/APAM Integration?



CMOS performance evaluation examples:

- Threshold voltage
- Sub-threshold slope
- Transconductance
- Oscillator frequency

How do we evaluate CMOS/APAM Integration?



CMOS performance evaluation examples:

- Threshold voltage
- Sub-threshold slope
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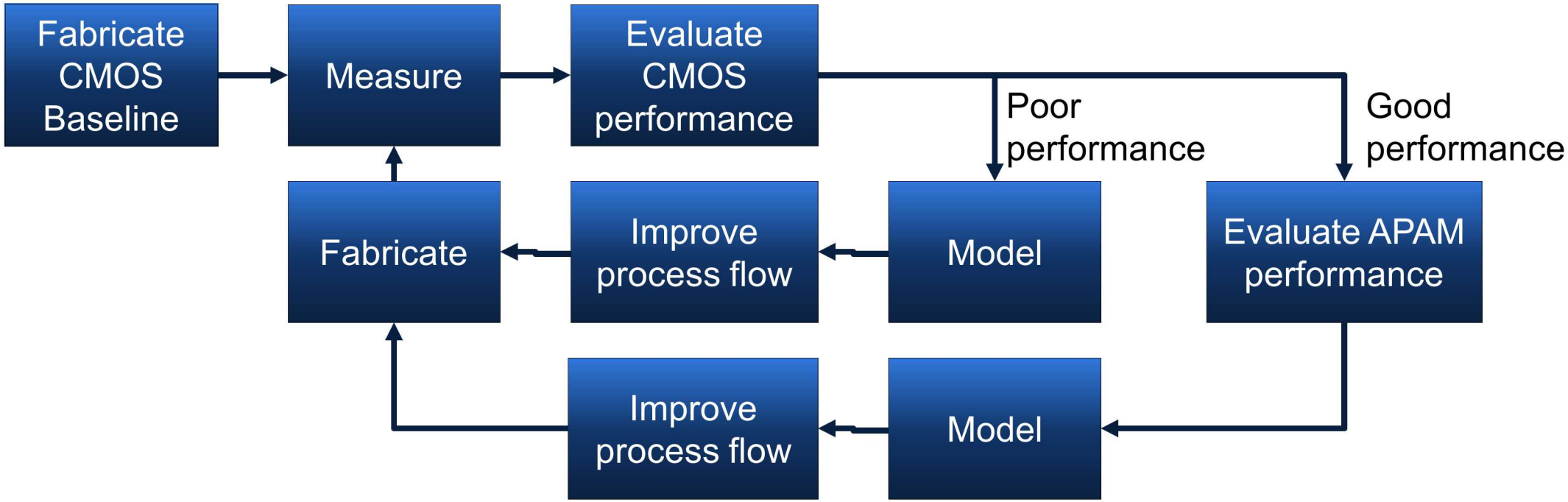
How do we evaluate CMOS/APAM Integration?



APAM performance evaluation examples:

- Resistivity
- Leakage
- Peak current density
- Oscillator frequency

FY19 - Designing for APAM/CMOS Integration

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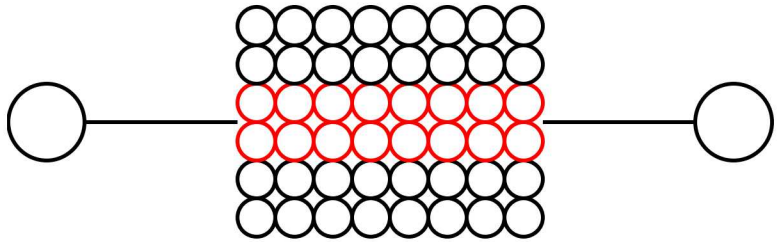
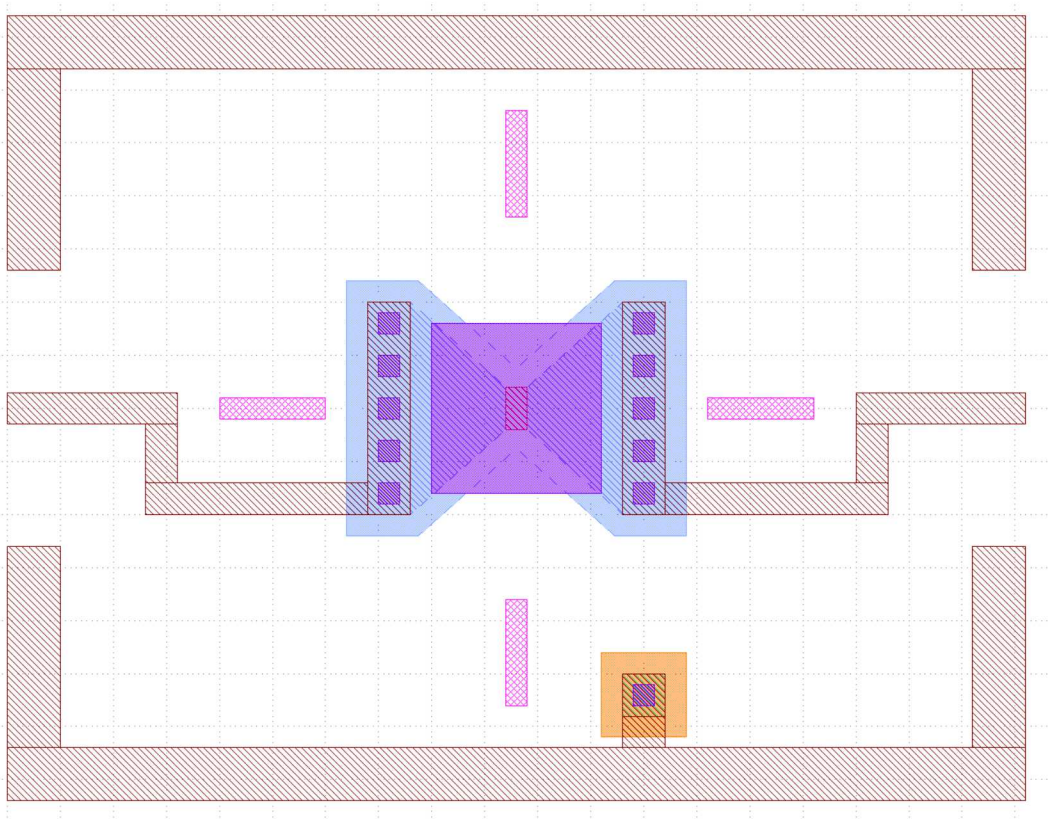
APAM Circuit Element

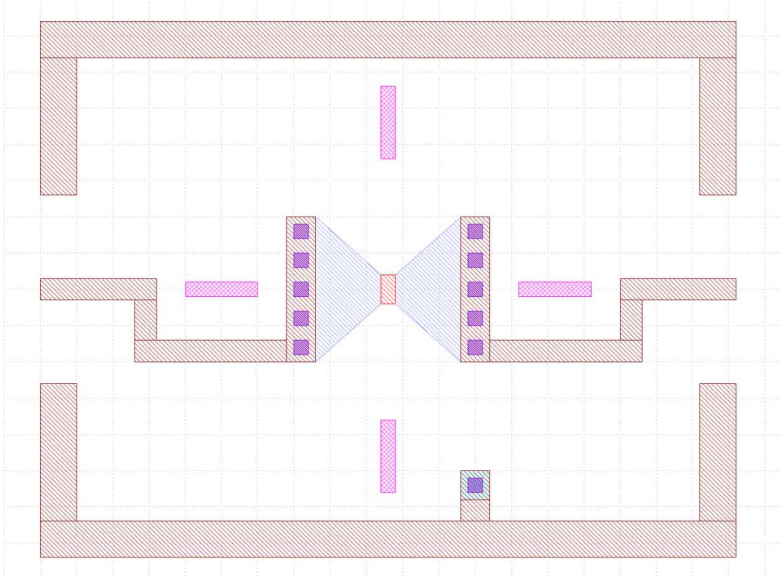


APAM cell for design

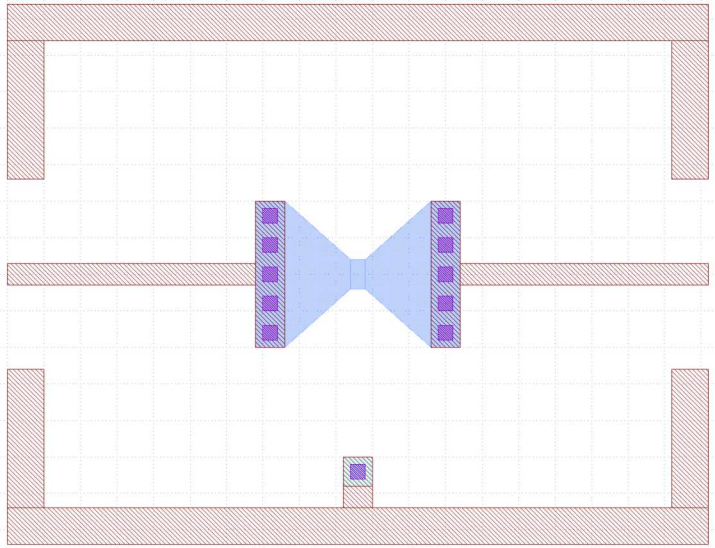


APAM cell for Process Development Kit (PDK) is built
Enables APAM + CMOS circuit design

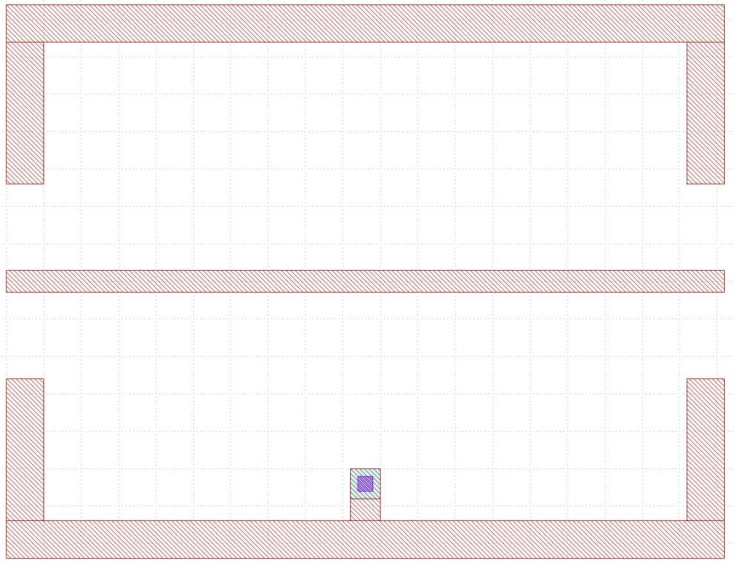
Experimental controls



APAM



Implant Control



Metal Control

Similar footprints/capacitances to help diagnose circuit issues

FY19 - APAM/CMOS integration

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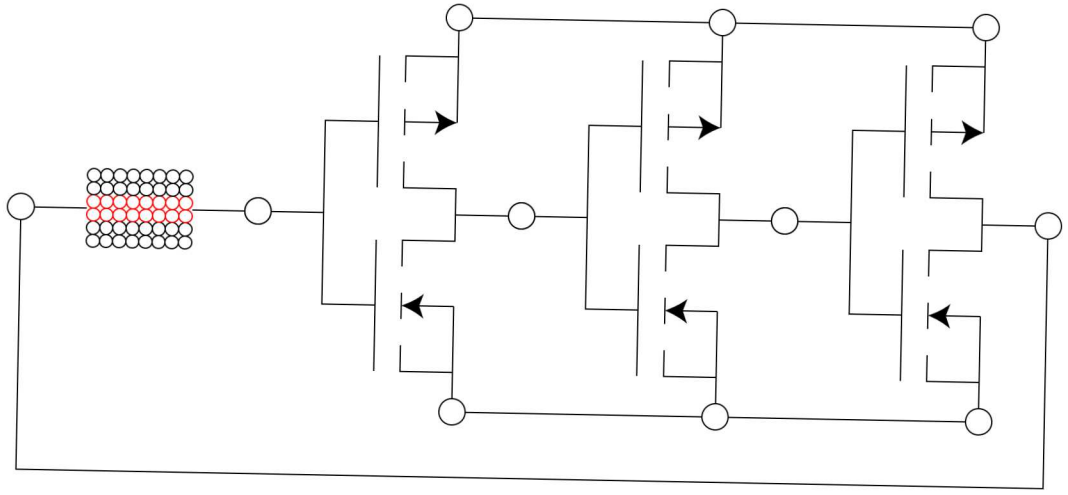
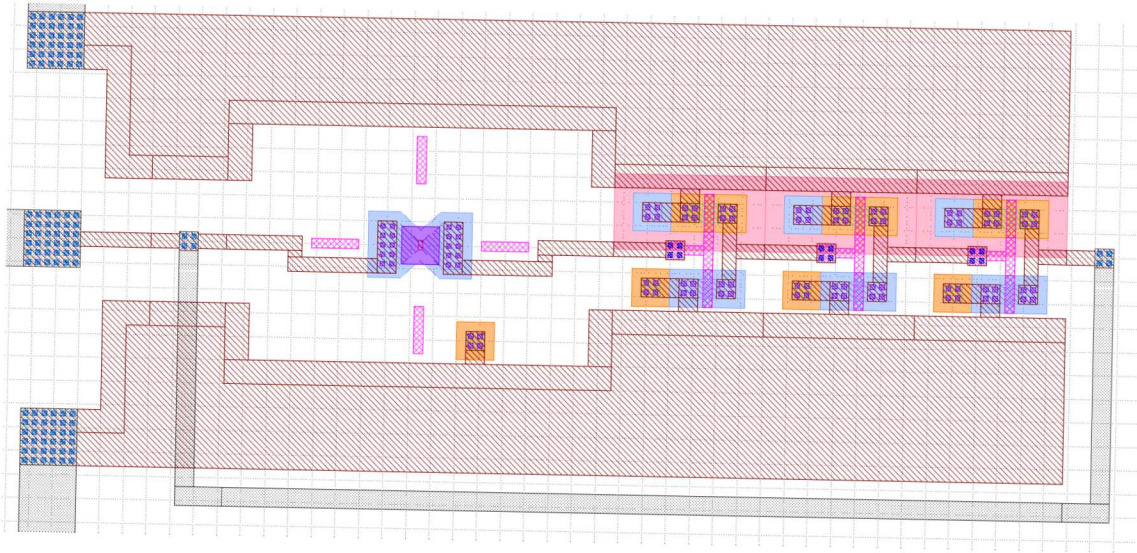
Circuit editor



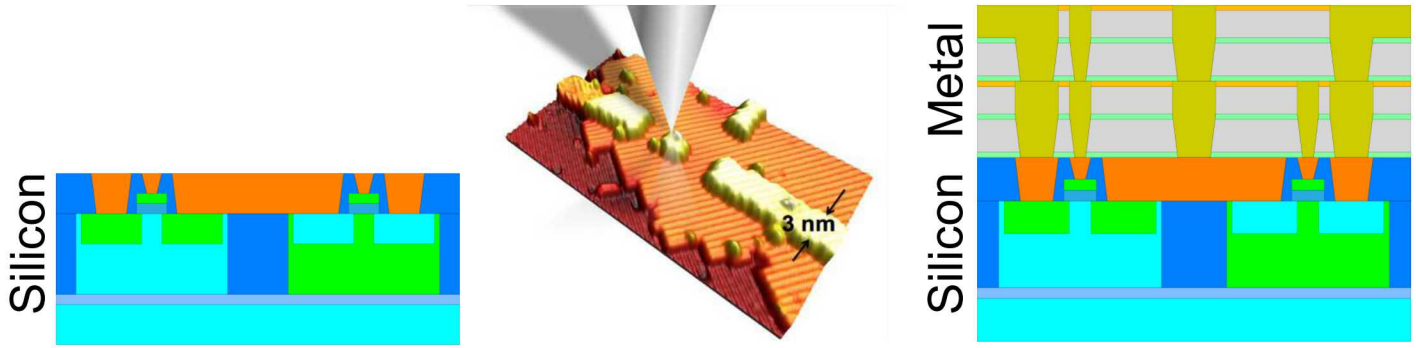
APAM with 3 stage ring oscillator

Physical Layout

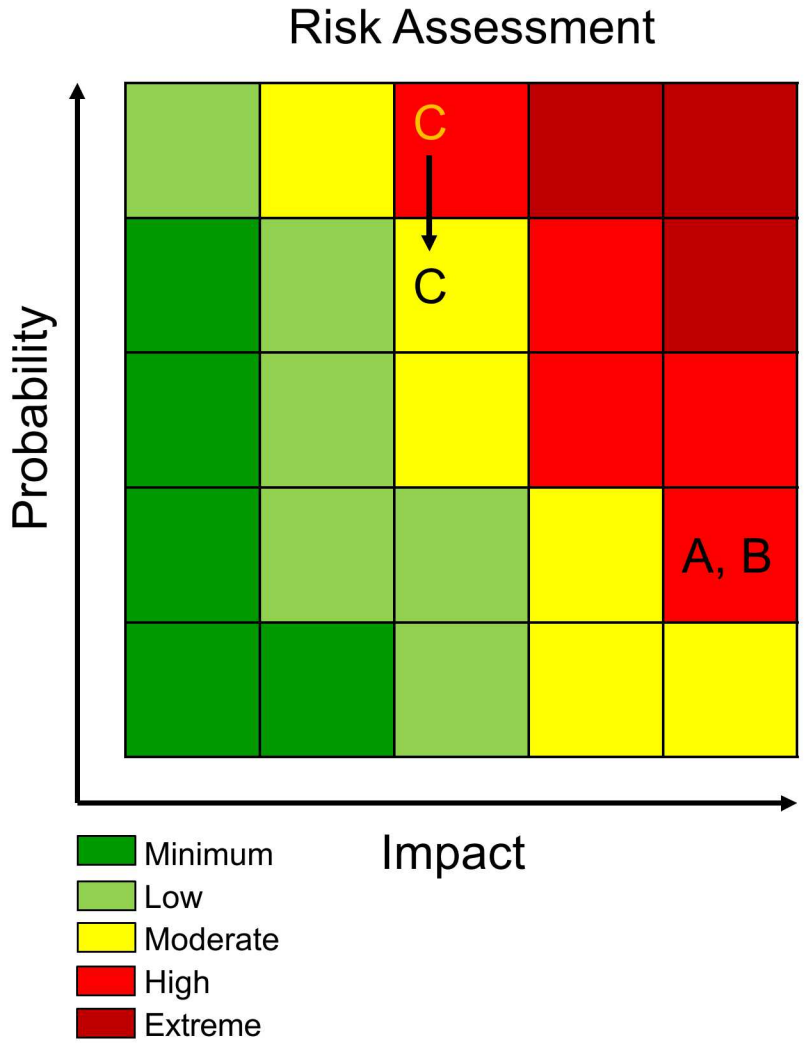


Easily able to design new APAM + CMOS circuits

Risks remain constant going into FY20



- Direct CMOS-APAM Integration
  - A. Incompatible thermal budgets for CMOS and APAM
  - B. Incompatible process flows
  - C. Die level fabrication design challenges

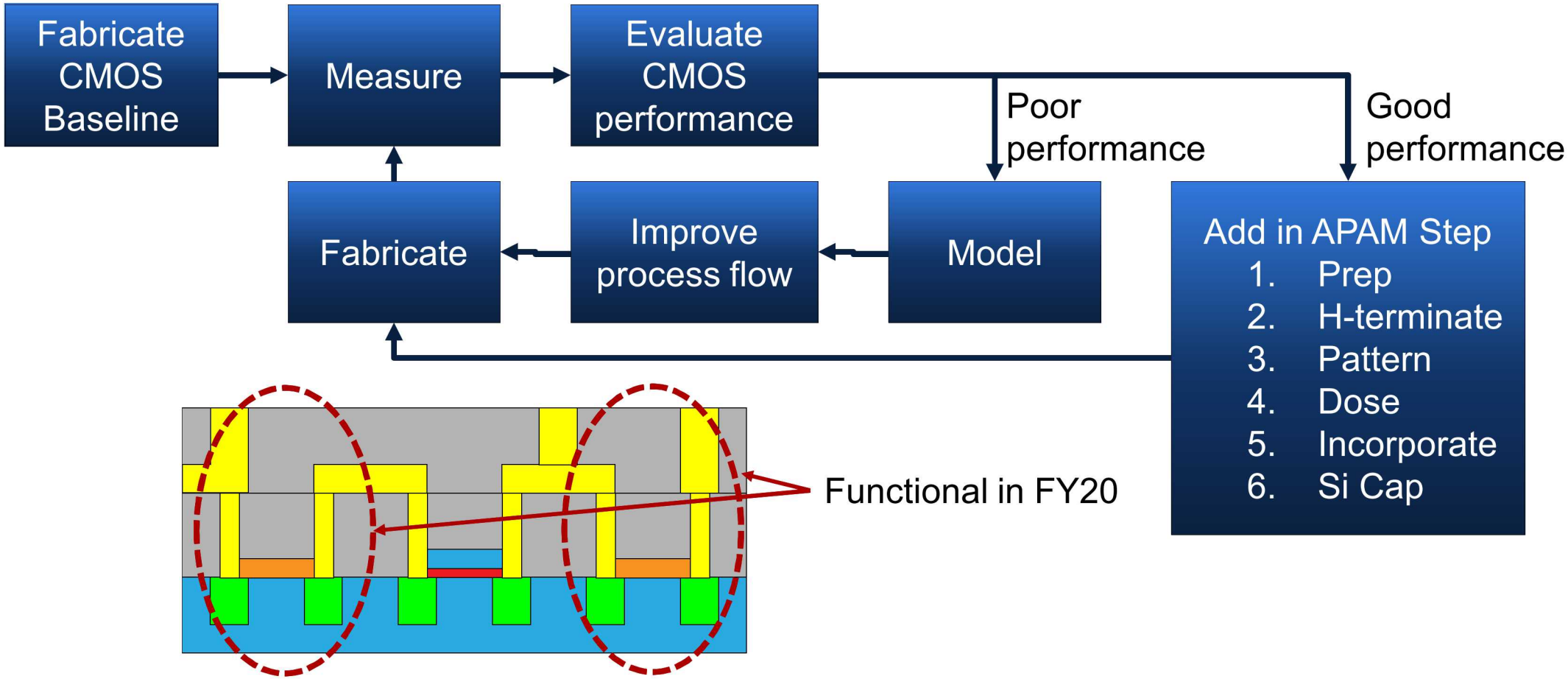


FY20 – Integrating APAM with CMOS

- Understand the “language” of CMOS design – Can talk with other people
  - Developing SOW for SkyWater Technology Foundry to build APAM compatible devices
- Fabrication in progress
  - SiFab lot started
  - µFab lot started

skywater

FY20 – Evaluating APAM/CMOS integration



Goal for FY20: Run full APAM process with functional CMOS

THRUST 3 – POST CMOS INTEGRATION

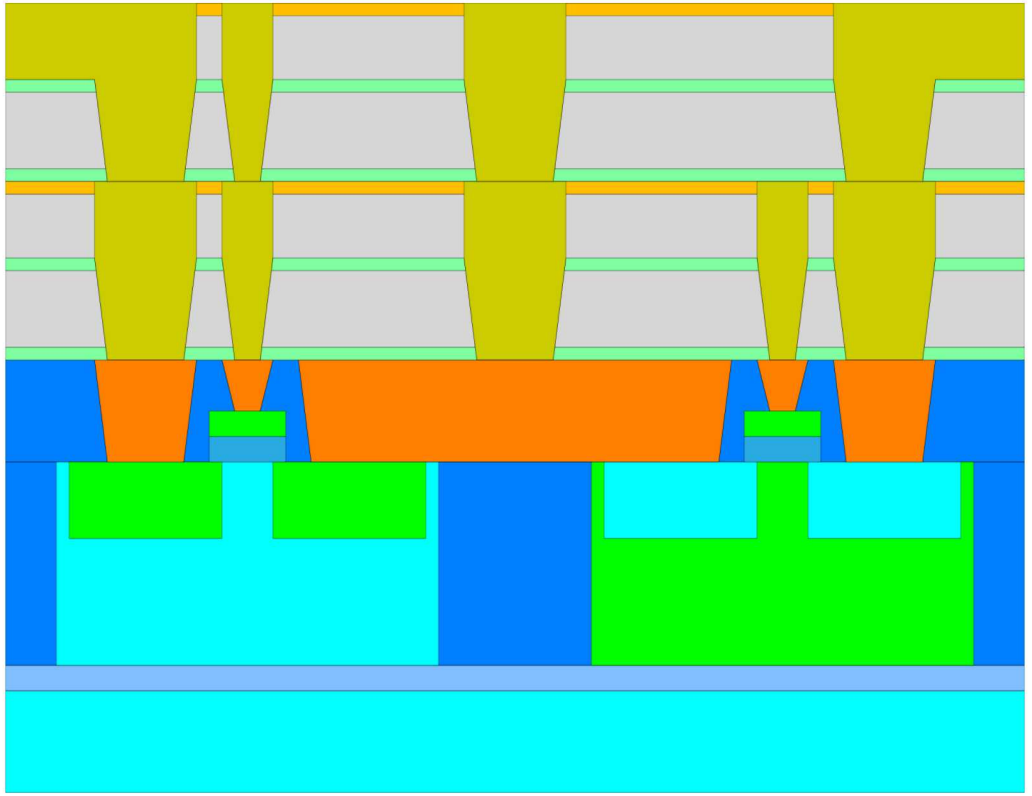
What do we mean by Post-CMOS Integration?

Sandia National Laboratories

Back-End-Of-Line (BEOL)

Front-End-Of-Line (FEOL)

Substrate



Post-CMOS Integration = Processing *after* BEOL completion

The Challenge of Post-CMOS Integration

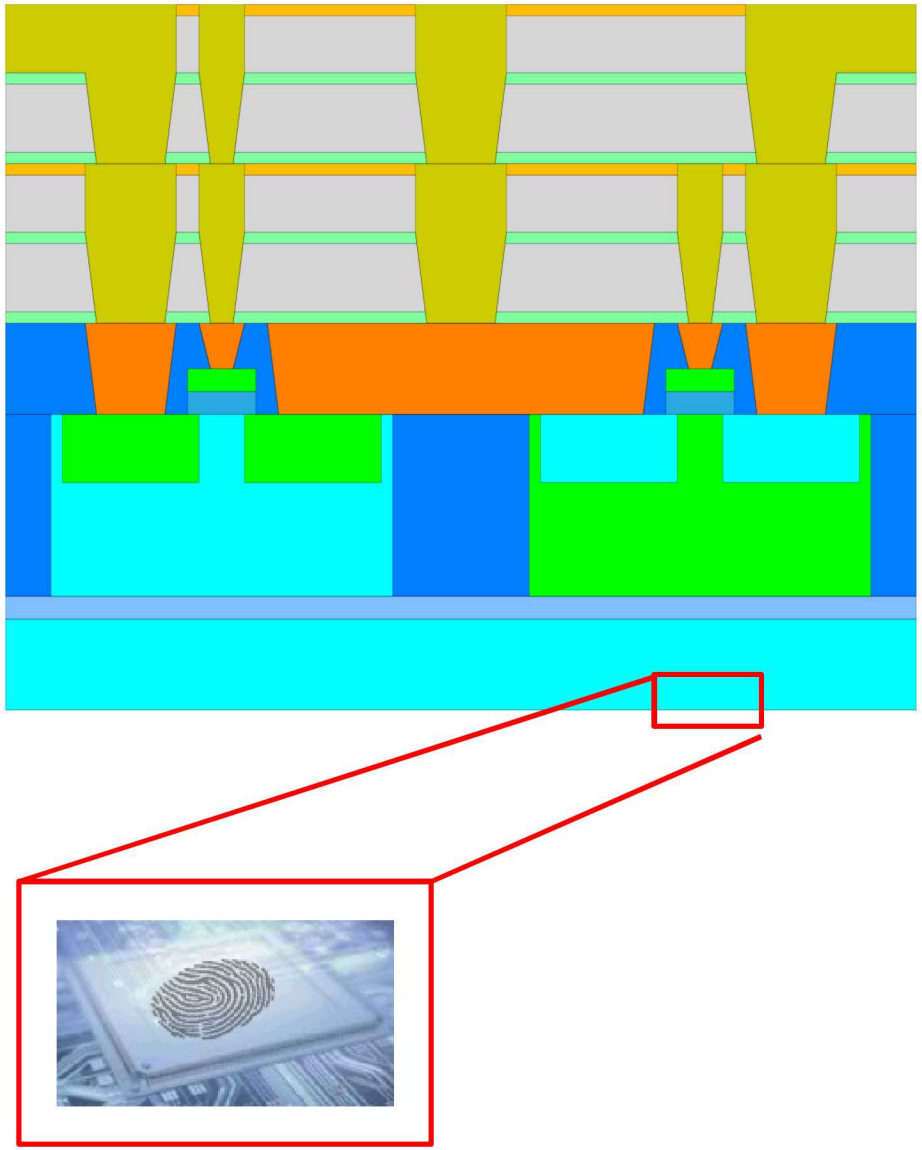
Sandia National Laboratories

Back-End-Of-Line (BEOL)

Front-End-Of-Line (FEOL)

Substrate

Fingerprint

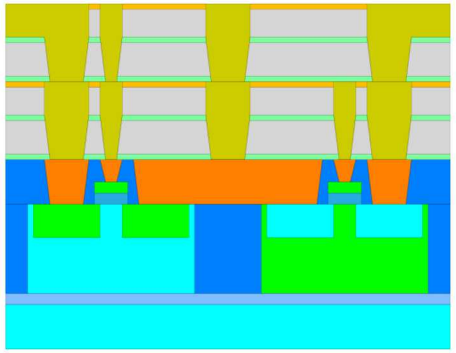


Metal routing, >10 layers

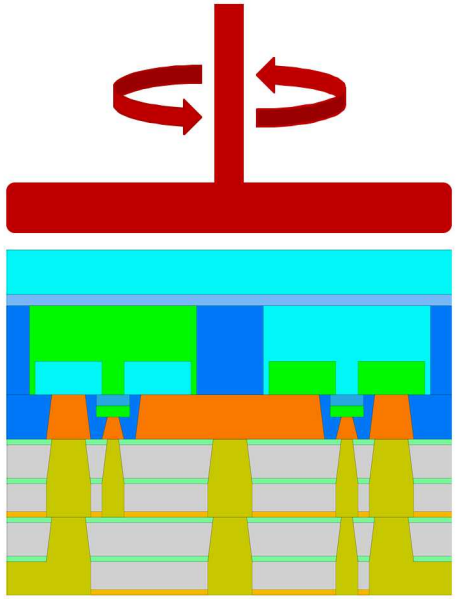
Thermal budget limited to less than 450 °C due to metal routing

Metal routing layers prevent topside access to silicon → Post-CMOS Integration requires backside processing

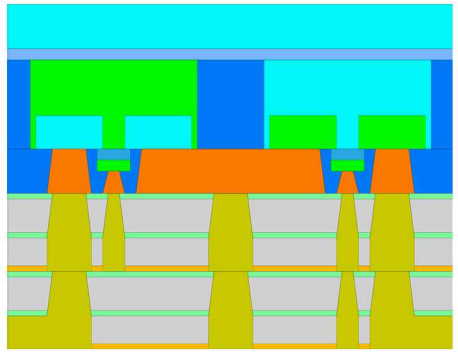
Two Big Questions in Post-CMOS Processing



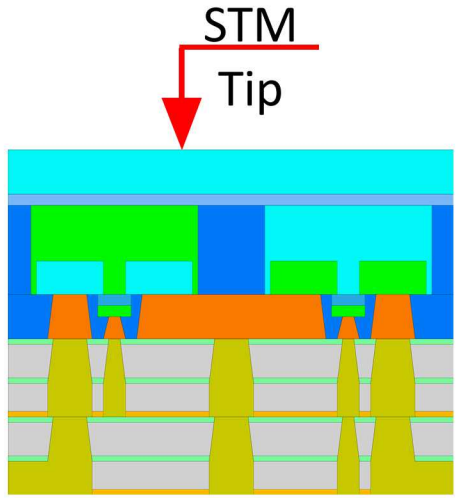
Completed
Silicon Die



Grinding/Polishing
of backside of Die
(optional)



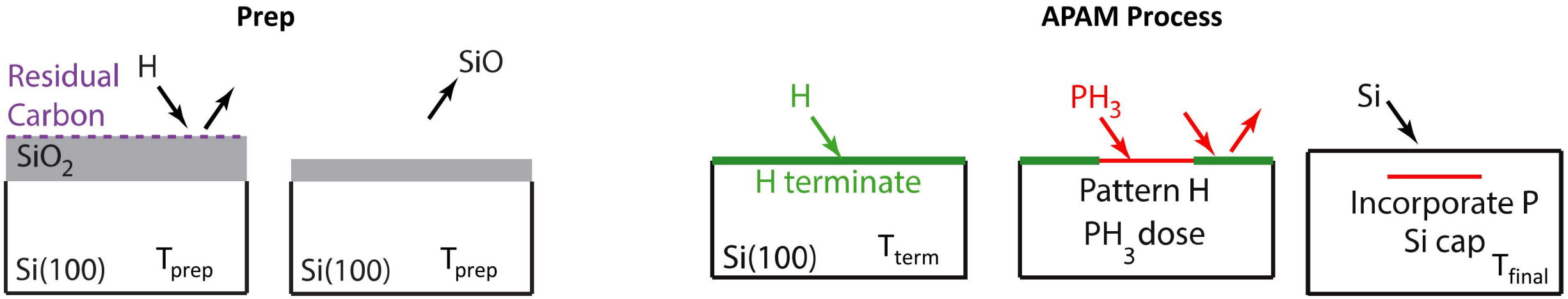
Prep
(Ex-situ and In-Situ)



APAM
Process

1. Can we cleanly remove backside films for APAM processing?
2. How far can we reduce the temperature of the sample prep and of the APAM process?

Post-CMOS process flow: Prep and APAM process

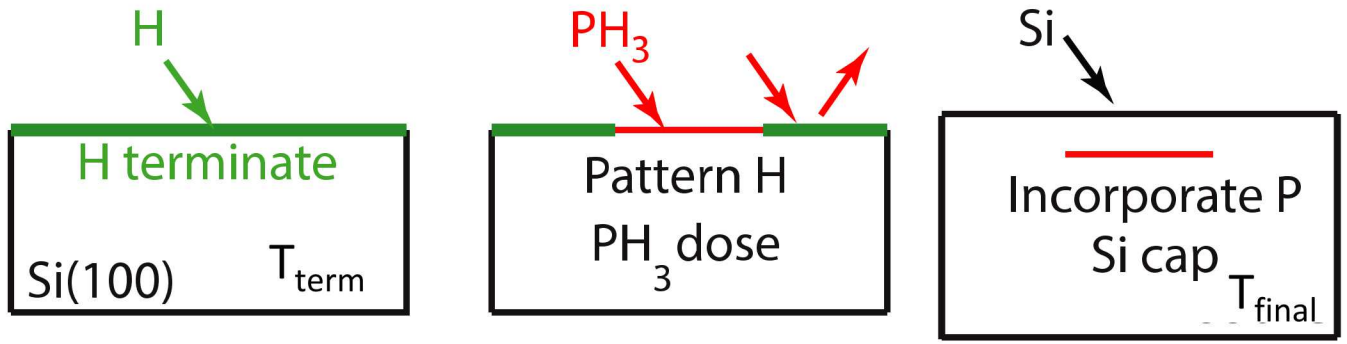


Year	Prep	APAM Process
FY16	T_{prep} = 1200 °C	T_{term}, T_{final} < 450 °C
FY19	T_{prep} = 800 °C	T_{term}, T_{final} = 22 °C
FY20	T_{prep} < 450 °C	Goal achieved in FY19

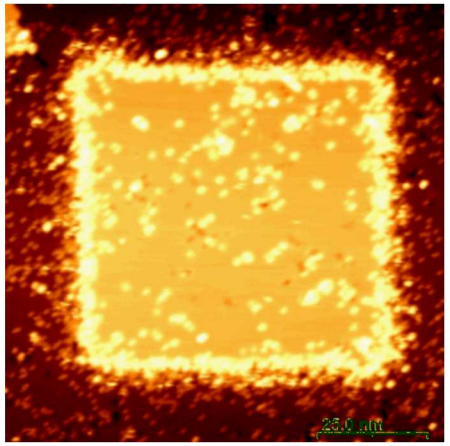
APAM process demonstrated at room temperature in FY19

D.R. Ward et al, *Applied Physics Letters* 111, 193101 (2017).

FY19 – Reduced-temperature APAM Process



T_{term} = 22 °C



First reported STM patterning of RT Hydrogen termination

σ = 2.0 (mS / square) at T_{final} = 350 (°C)

σ = 0.6 (mS / square) at T_{final} = 22 (°C)

First reported transport data on RT APAM process

RT = Room-Temperature = 22 °C

FY19 – Polished surfaces can be atomically clean

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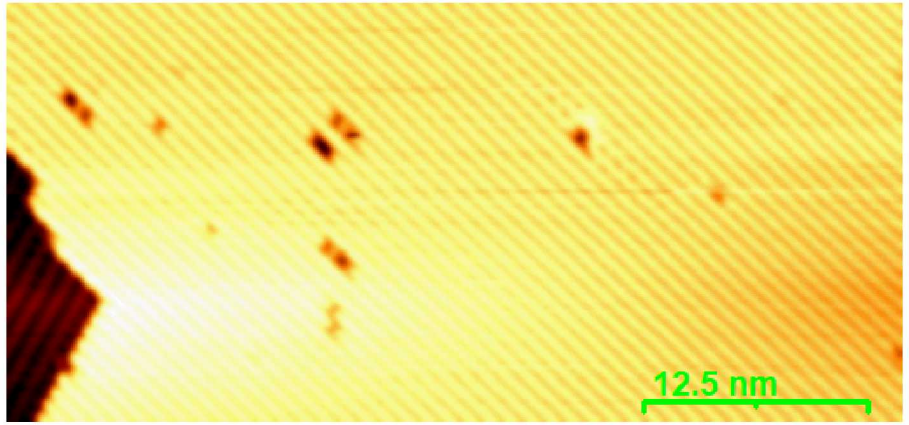
Silicon die

Is this surface clean?

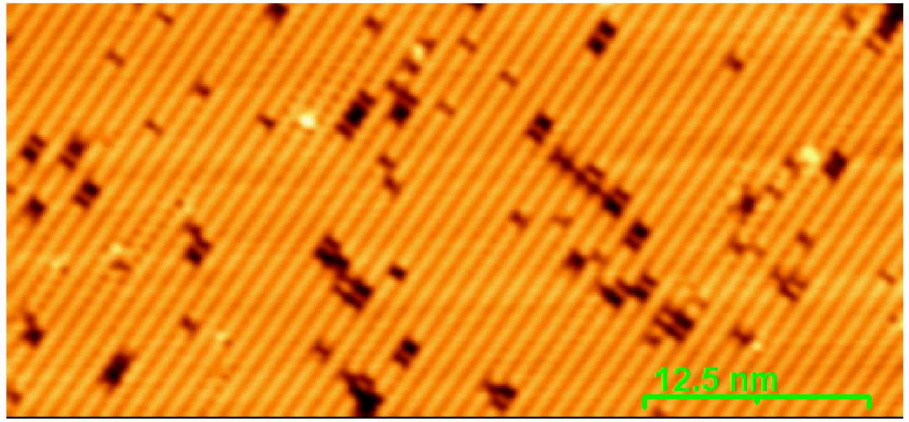
Silicon die



STM image of surface

Is this surface clean?

Silicon die

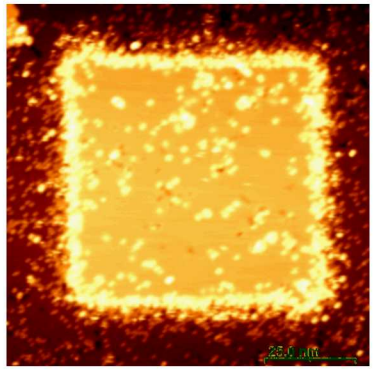


STM image of surface

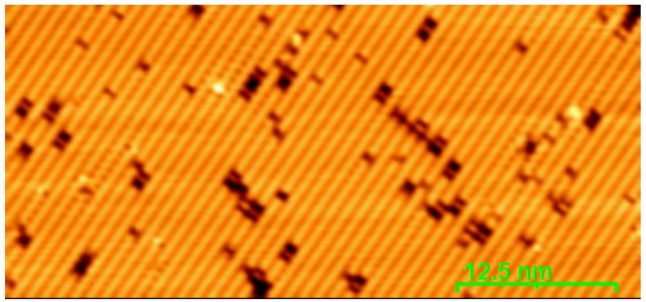
T_{Prep} = 800 °C

⇒ Polished surfaces can be atomically clean.

Risks are going down based on FY19 work



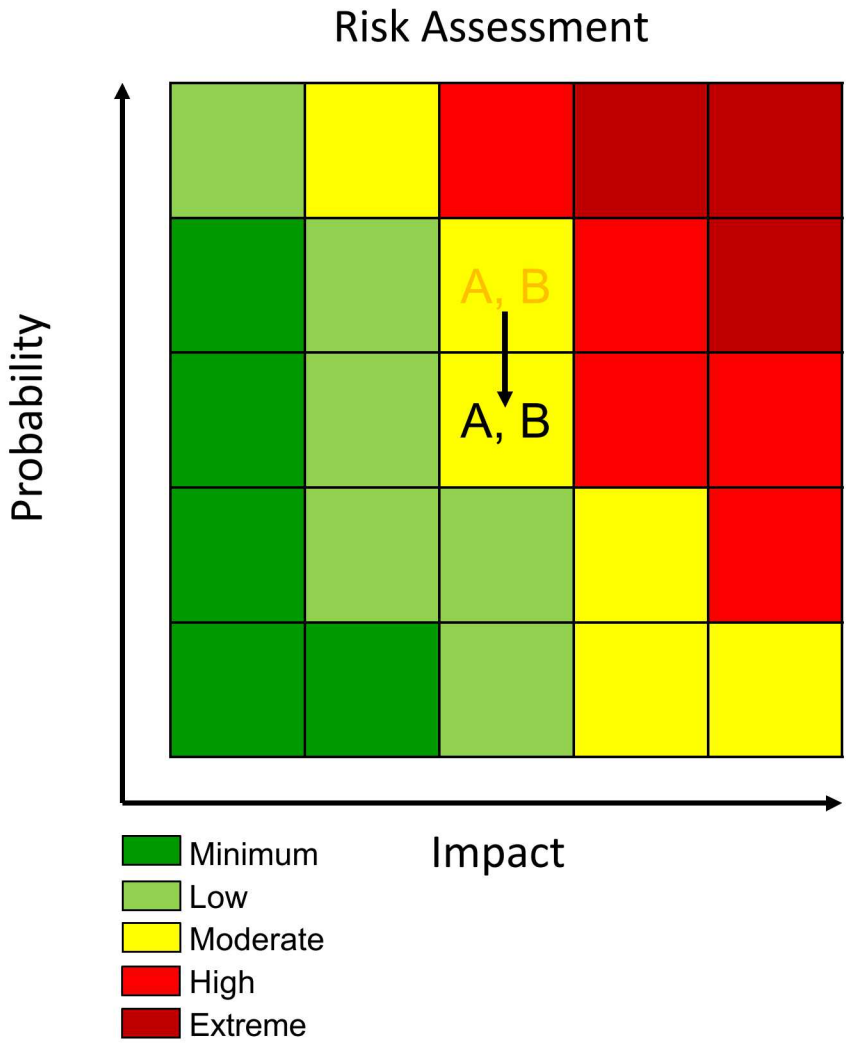
RT termination and patterning



Clean surface post-polishing

- Reduced temperature processing
  - APAM processing can not meet thermal budget requirements of Post-CMOS integration
- Heterogeneous integration
  - Polished surfaces are unable to support functional APAM devices

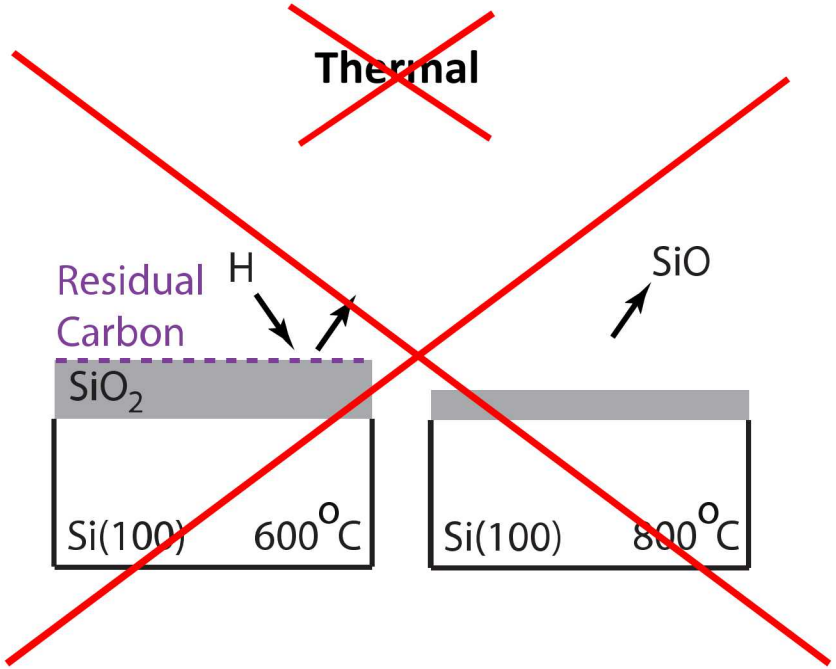
Post-CMOS Integration in FY20



FY20 – Reduced-temperature Prep

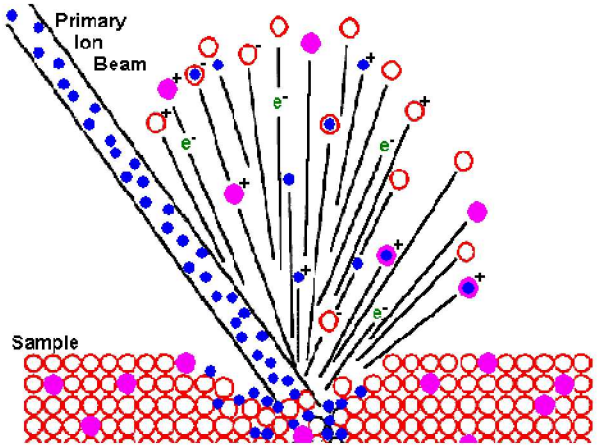
Sandia National Laboratories

Thermal



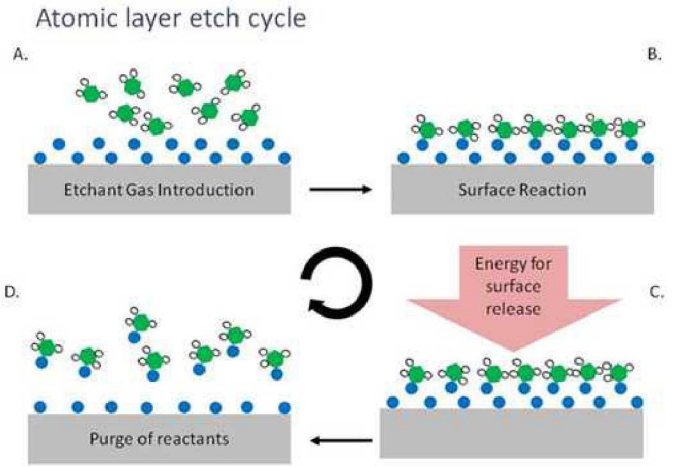
Mechanical

Low Energy Ion Sputtering



Chemical

Reactive Ion Etching



Goal: Discover and evaluate a non-thermal prep <450 °C

- Low energy ion sputtering (mechanical)
- Reactive ion etching (chemical)

- Performance evaluated based on:
  - Electrical conductivity
  - Drive current
  - Infrared response

D.R. Ward et al, *APL* 111, 193101 (2017). http://pprco.tripod.com/SIMS/Theory.htm https://doi.org/10.1007/978-90-481-9751-4_353

THRUST 3 – APAM ROBUSTNESS

APAM Robustness

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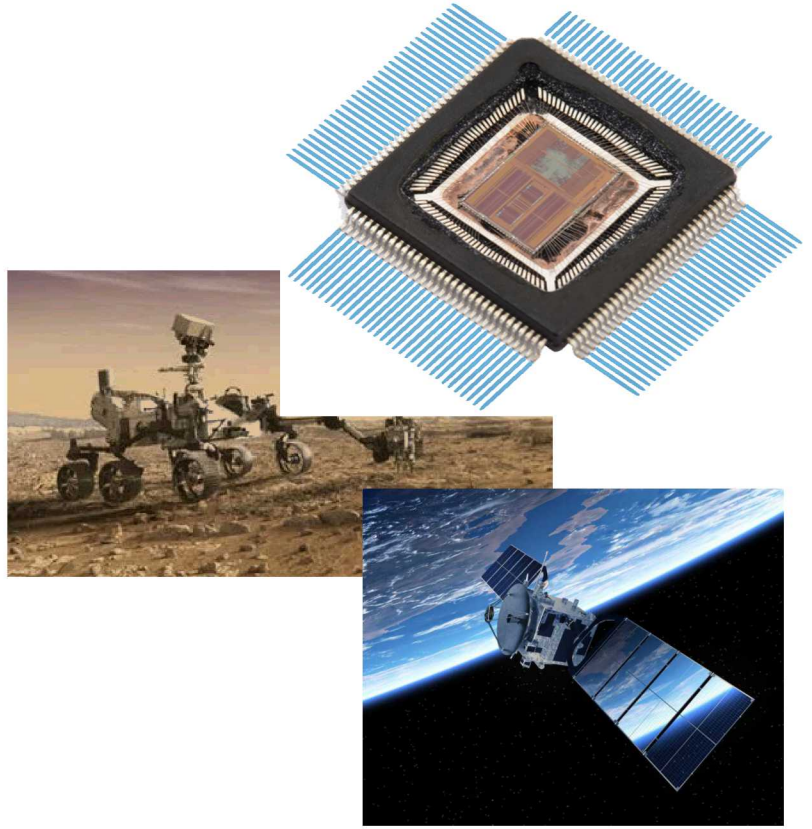
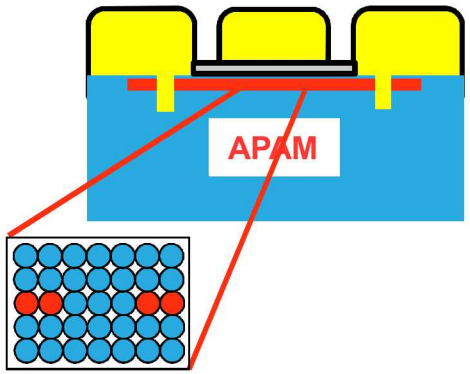
Motivating questions:

- Should Government use APAM?
- Will APAM layer last a week? Month? Year?
- Consequences of extreme environments, SWAP?
- How well does APAM hold up compared to CMOS?



Goal: Understand the properties of APAM structures under bias, current flow, and temperature to establish device lifetimes and compatibility with CMOS.

Connection to Exemplars

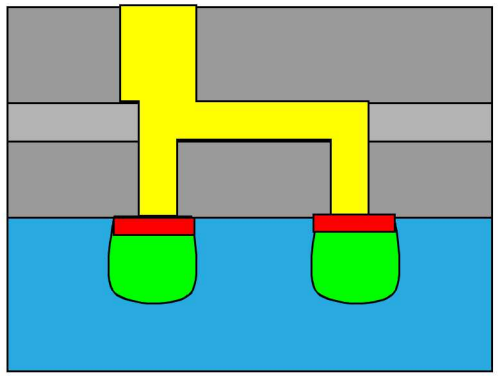


APAM – MOS

Need:
- Direct CMOS Integration
- **Robustness**

Interconnects

Need:
- Direct CMOS Integration
- **Robustness**



Fingerprint:

Need:
- Post-CMOS Integration
- **Robustness**

Want:
- Direct CMOS Integration

What happens at elevated temperatures and high current densities to APAM delta layers?

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No existing research on APAM robustness!

Open science questions:
- Acceptor drift (P) in current?
- Local heating effects?
- Effects of local defects on delta layer survival?
- DC and AC bias effects?

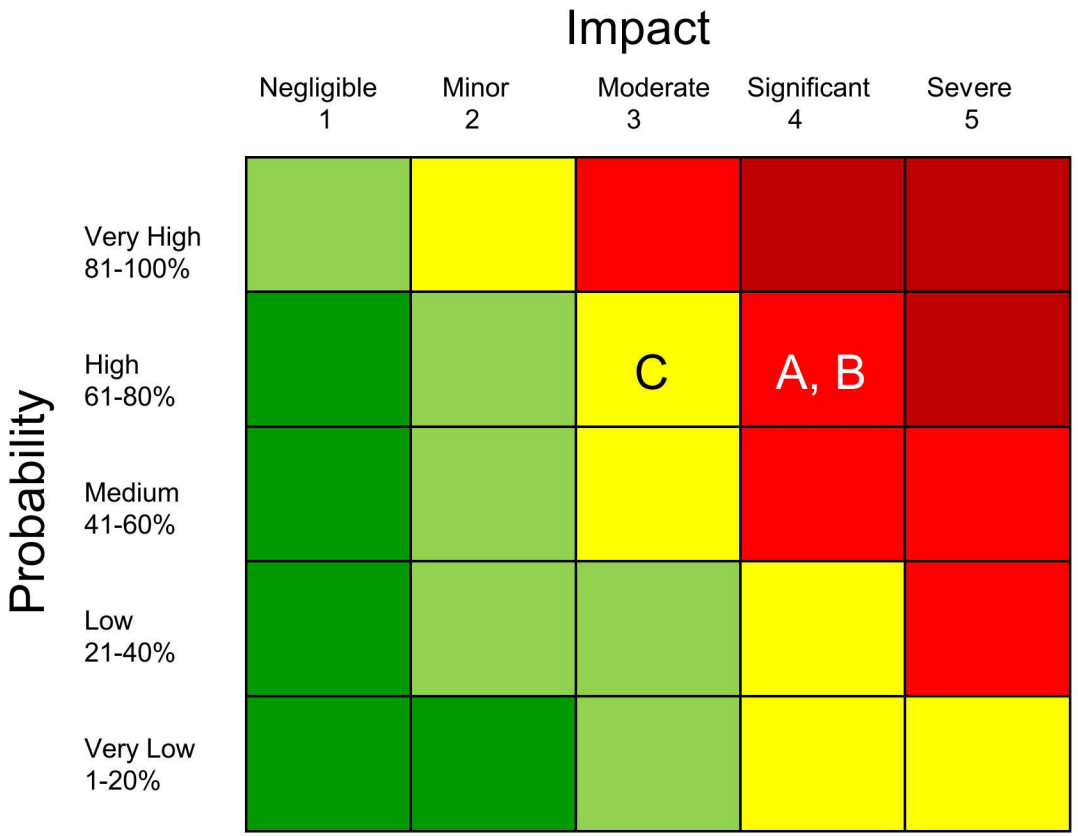
Ties to RT operation in APAM Devices Thrust

Risk Assessment

A: Room temperature operation of delta layers difficult until counter-doping structures perfected

B: Failures do not occur in delta layers, but in any of the many interfaces present in device

C: Defects near delta layer dominate the robustness

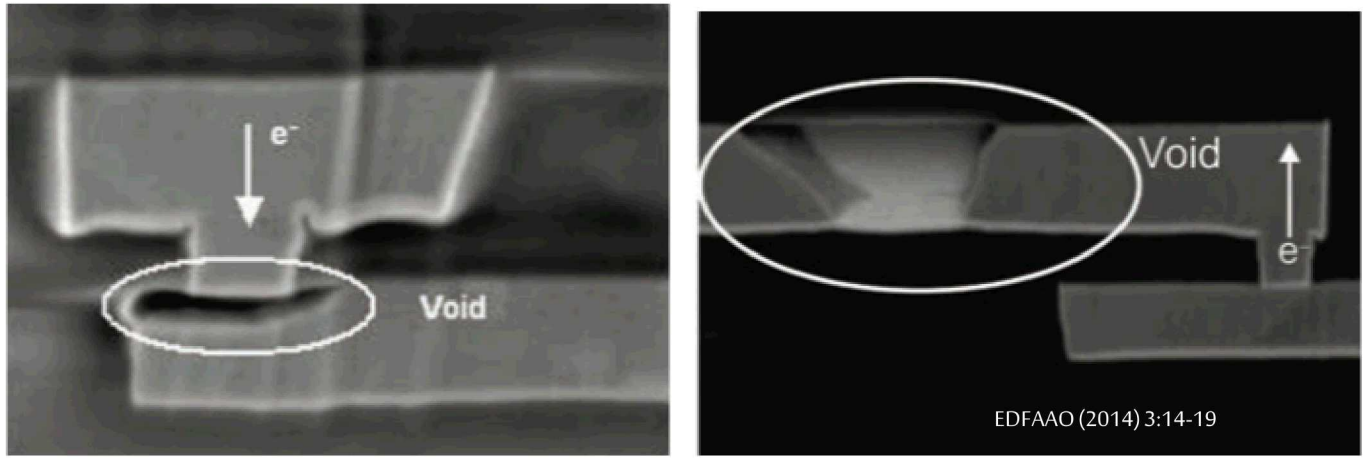


Strategy for answering robustness

- Robustness testing platform – elevated T and variable current density
- Study RT robustness now → SOI device fabrication
- Study defect tolerance of delta layers

Useful analogy:
Electromigration?

Electromigration voids in Cu



Develop APAM Robustness Testing Platform

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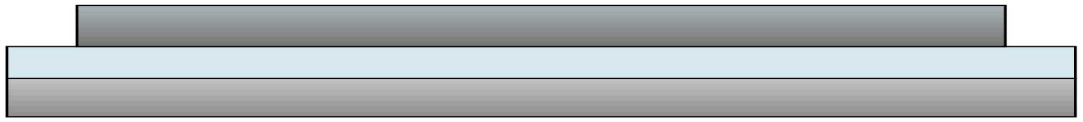
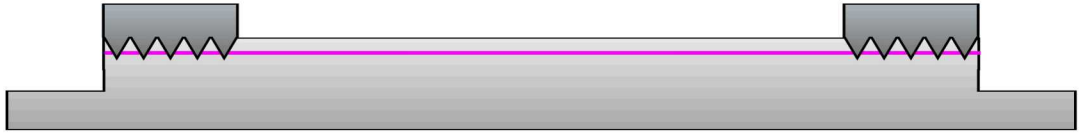
3 types of test devices:

Metal test device



Mock delta layer device

Etched delta layer device

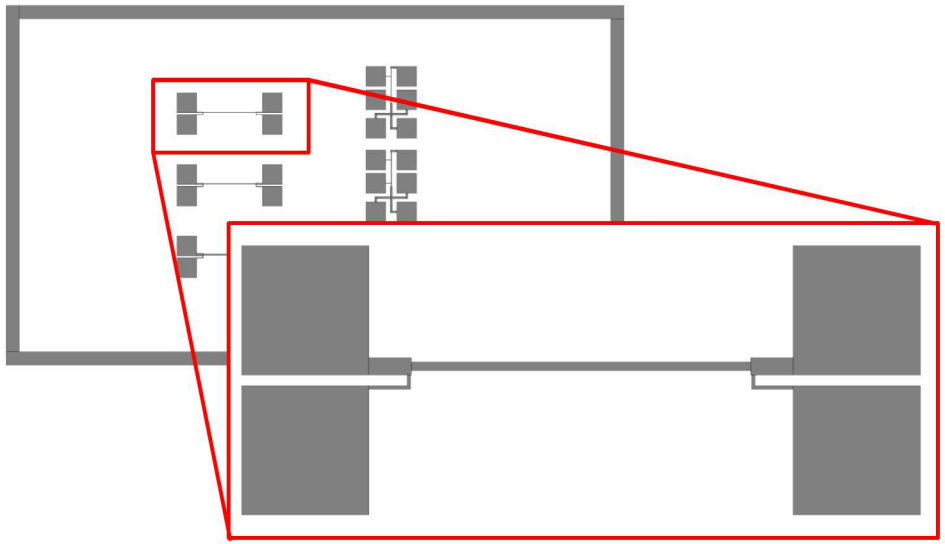


Elevated T & high current density

Precise temperature control and source meters

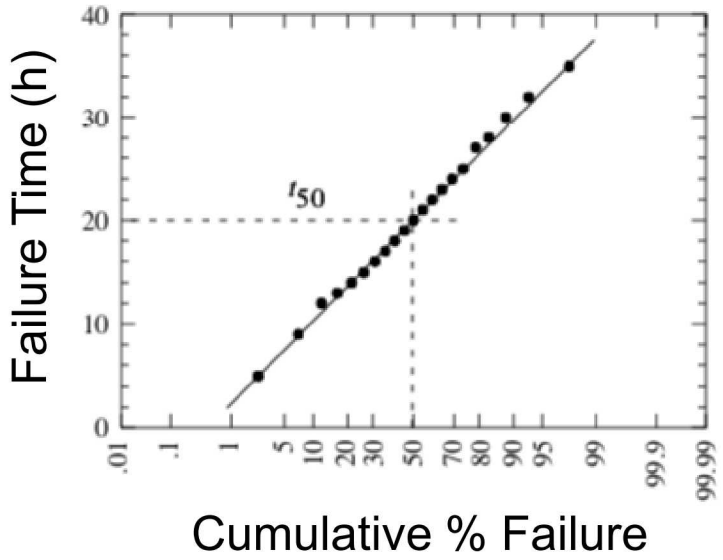
APAM Robustness Testing

Test devices



ASTM 1259M - Electromigration test structure

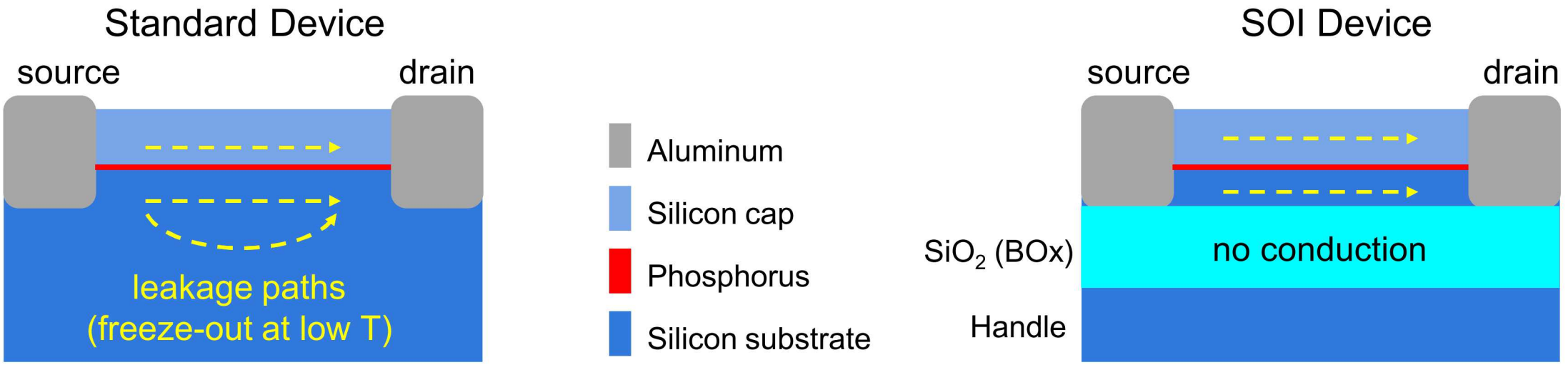
Mean time to failure



What these tests will determine:

- Sanity check for test setup and approach
- Median time to failure of both standard metal lines & delta layers
- Maximum current density as function of temperature

Silicon-on-insulator as path to RT testing now



SOI device to confine conduction to region around delta layer only!

At room temperature:

- In standard device – substrate conduction dominates
- In SOI device – confine conduction to device layer

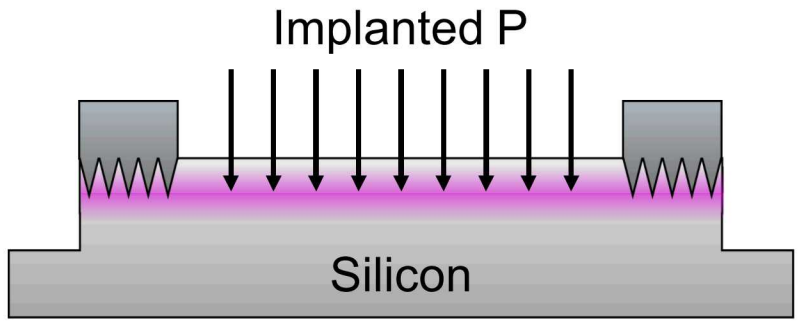
Ties to RT operation in APAM Devices Thrust

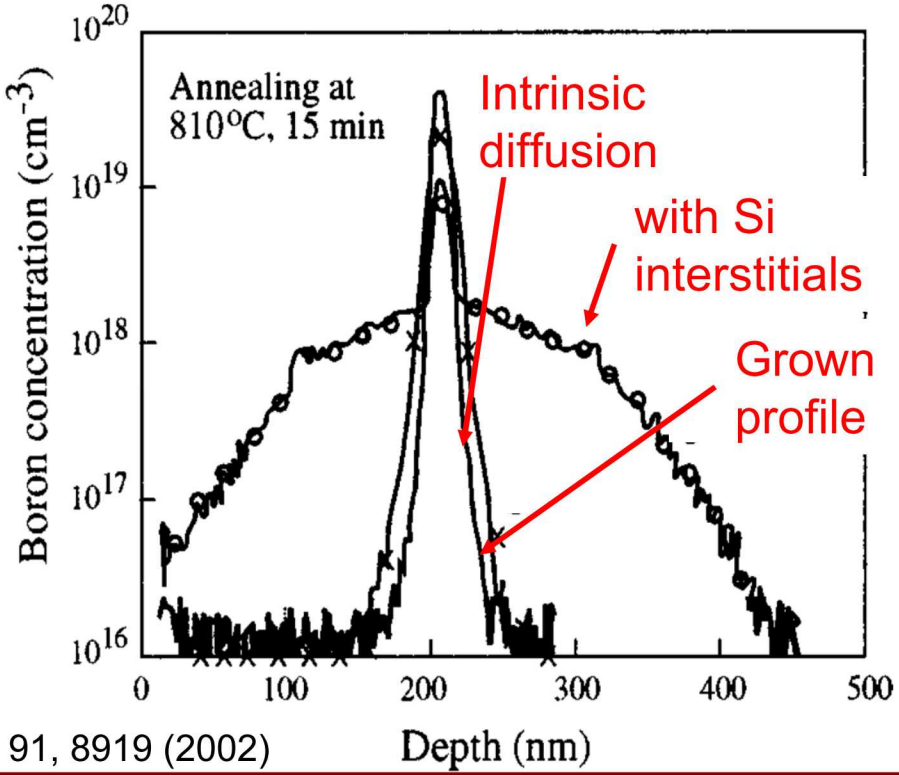
Forecasting the failure mechanism (defects)

Intrinsic diffusion of substitutional impurities (P,B) is small

BUT impurities + silicon interstitials = high diffusion

- Transient enhanced diffusion
- Oxidation enhanced diffusion





JAP 91, 8919 (2002)

Study defect tolerance of conduction:

- Implanted layers contain defects = “Plus one model”
- Establish tolerance of conduction to local defects
- Study robustness of both delta and implanted layers