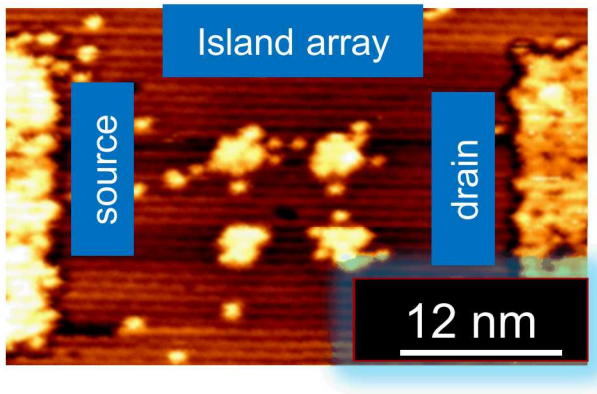
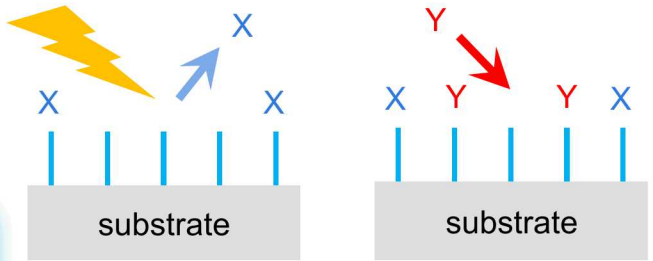
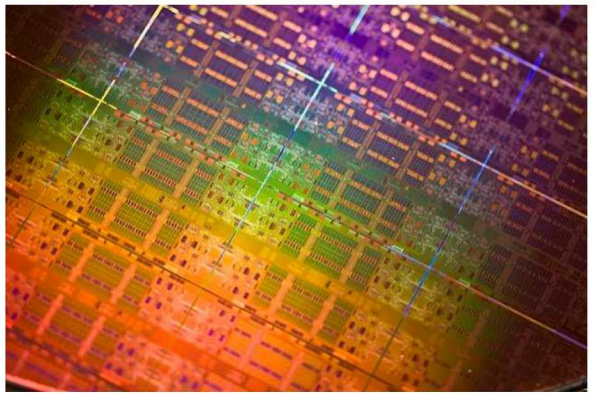
SAND2019-13377PE



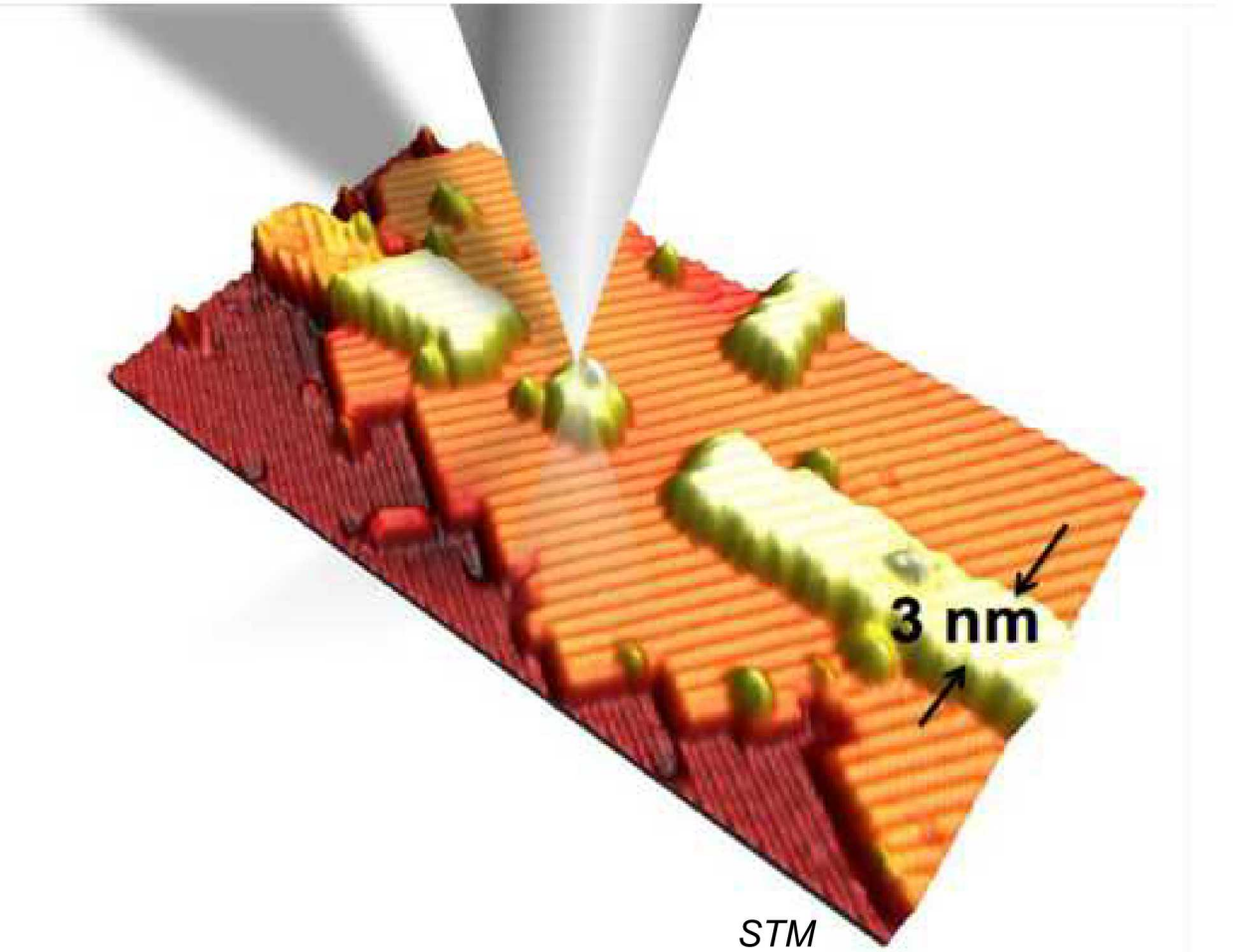



# FAIR DEAL GC Technical Overview – EAB 2

Shashank Misra

# Atomic Precision Advanced Manufacturing (APAM)




*STM*

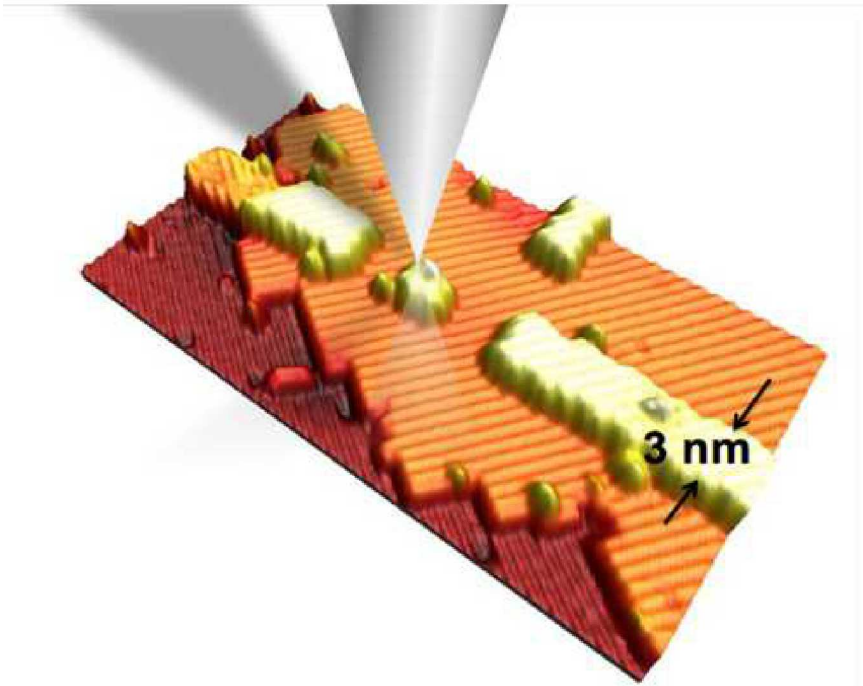
Mission: To assess the opportunities presented by APAM-enabled devices and processing for the digital microelectronics of the future

**F**ar-reaching **A**pplications, **I**mplications, and **R**ealization of **D**igital **E**lectronics at the **A**tomic **L**imit

# Outline

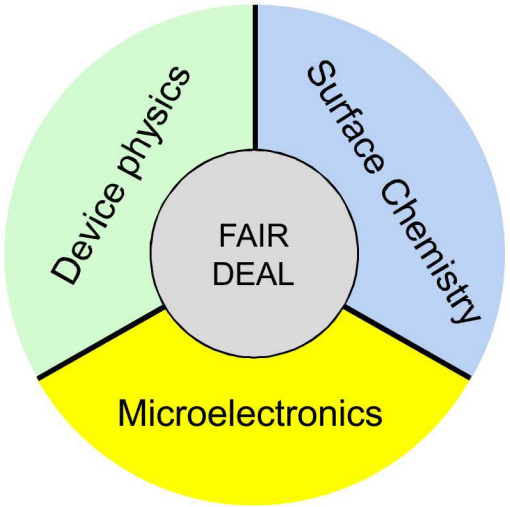
Sandia National Laboratories

## Motivation for FAIR DEAL GC



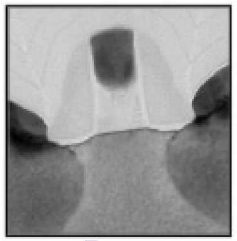

- What is special about APAM?
- Exemplars & Impact

## FY 19 Summary of FAIR DEAL GC

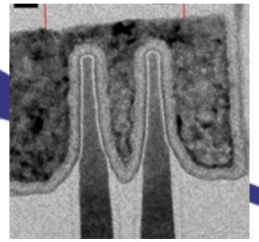


# Where is microelectronics headed?

Historically, shrink transistor → more functionality and declining cost



65 nm

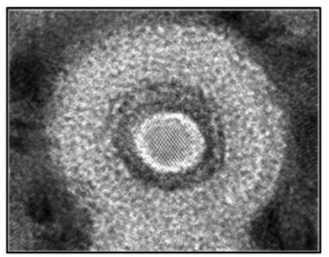


10 nm

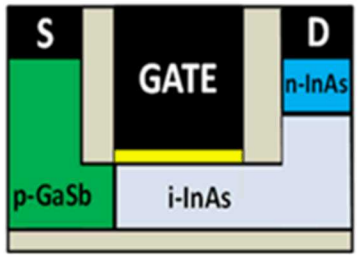
?

5-7 nm

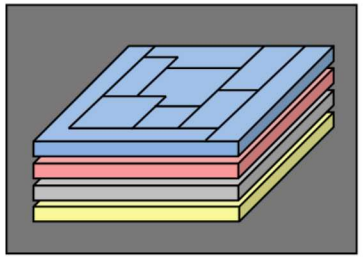
**Unclear technology path.**



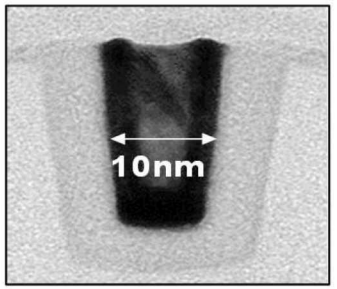
Nanowire Transistors



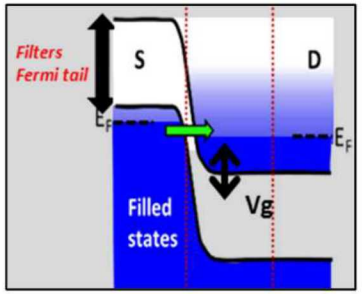

III-V Transistors



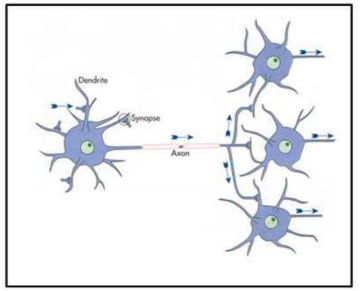
3D Stacking




Dense Interconnects

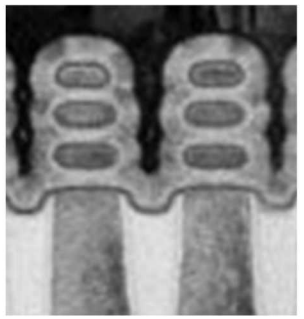



Tunnel FETs



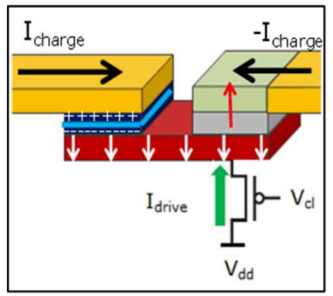
Neuromorphic Computing

*Mark Bohr, Intel 2018*

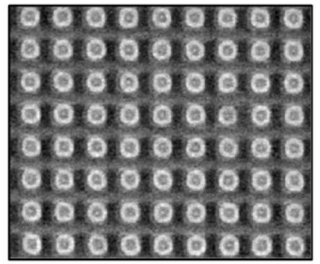


Nanosheets

*Huiming Bu, IBM 2017*




Spintronics

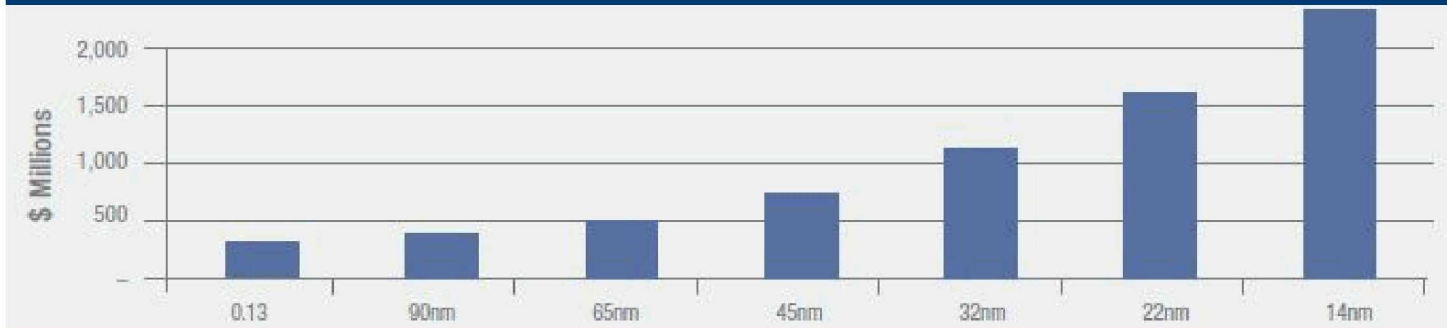


Dense Memory

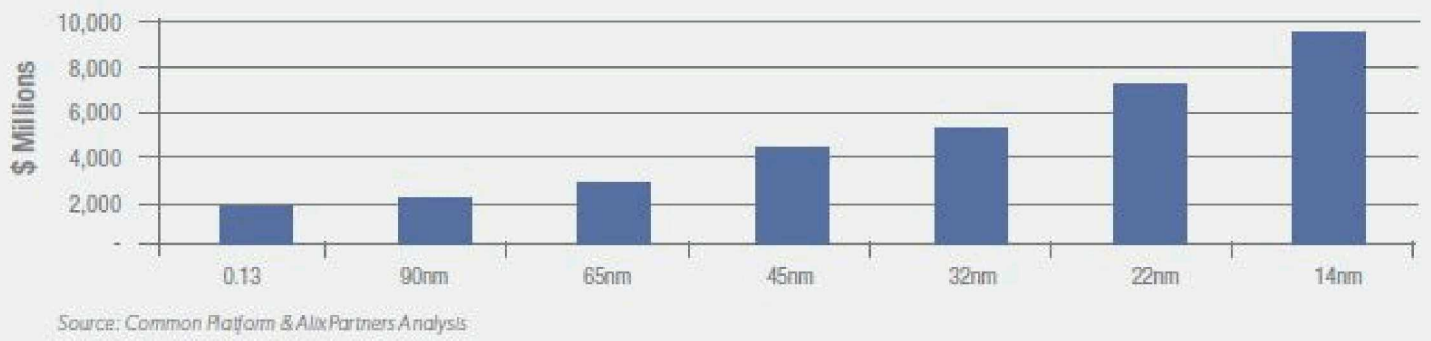
# Emerging risk in manufacturing-driven ecosystem

Sandia National Laboratories

## Process technology development cost by node




## Fab costs by node




- R&D cost rising exponentially
- Tooling/equipment cost rising exponentially

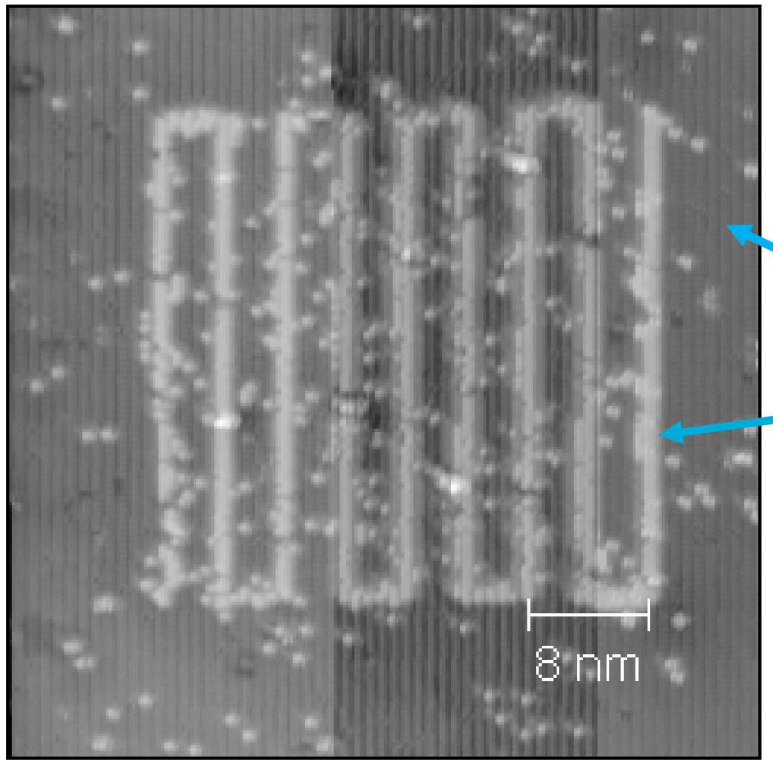
**Opportunity for non-scalable R&D pathfinding**

# How does Atomic Precision Advanced Manufacturing (APAM) work?

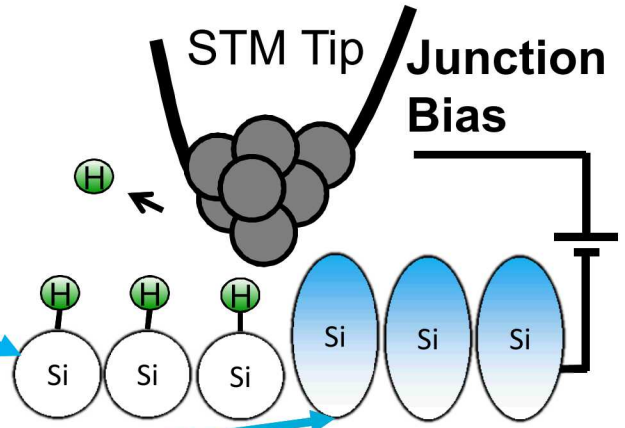
Sandia National Laboratories

"Chemical contrast" at Si surface

- Unterminated Si: 1 reactive bond/ atom
- H-terminated Si: unreactive




*STM*



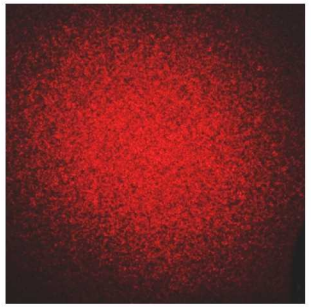

Scanning tunneling microscope (STM) can image and pattern the surface

**Atomic-precision lithography**
**Atom-/molecule- based processing**

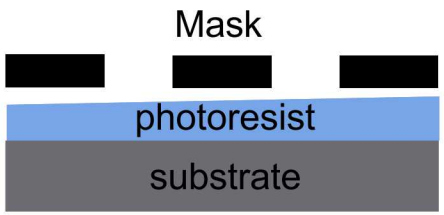
# APAM-style processing

## Traditional (analog) resist

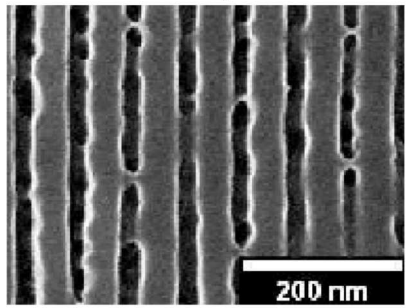
Inhomogeneity of light



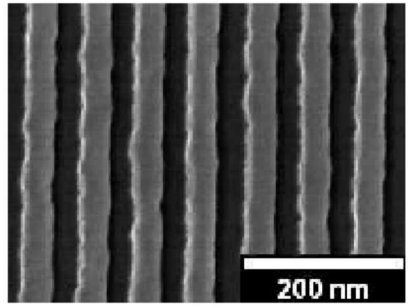
Inhomogeneity of resist



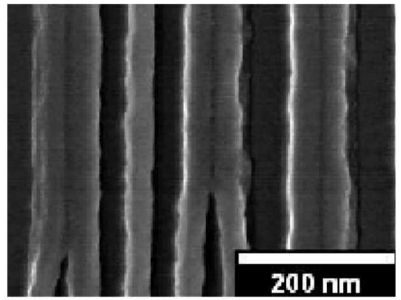

Underexposed




Just right

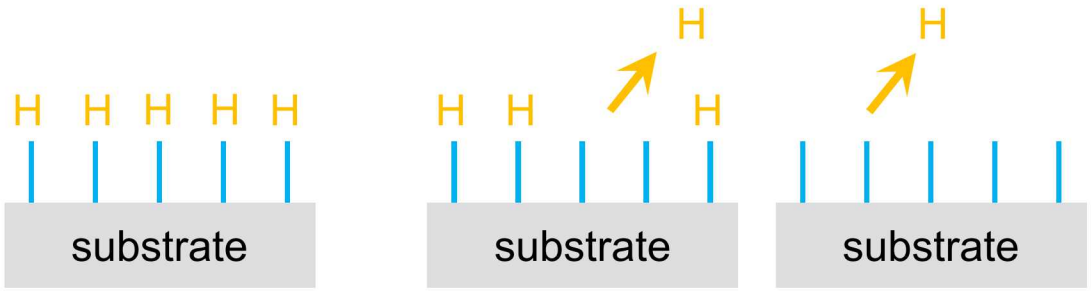



Collapsed




From M. Wang, Lithography

## Atomic-scale (digital) resist




Underexpose = like no exposure

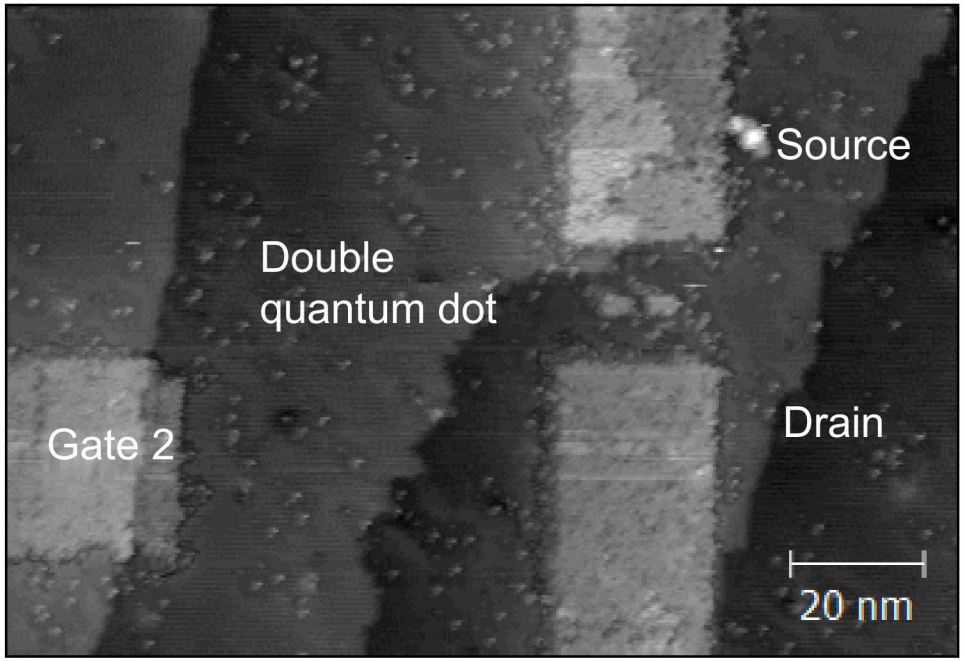
No overexposure on multiple exposure

- Can't be over-exposed or under-exposed
- Remains stable to arbitrary pitch

# Ultra-doping using phosphine surface chemistry

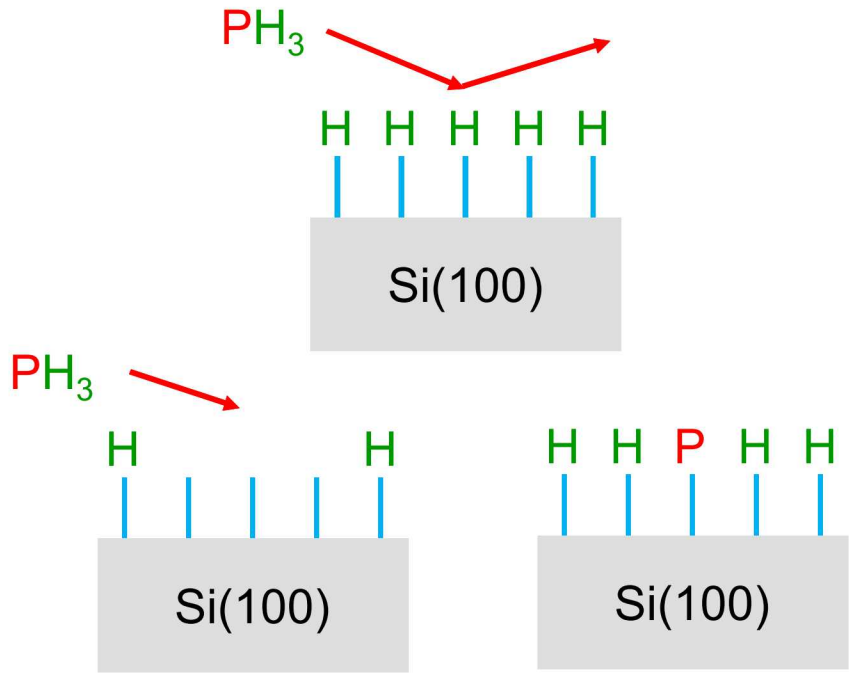
Sandia National Laboratories

Top view




*STM*

Phosphorus ‘donates’ an electron to silicon.

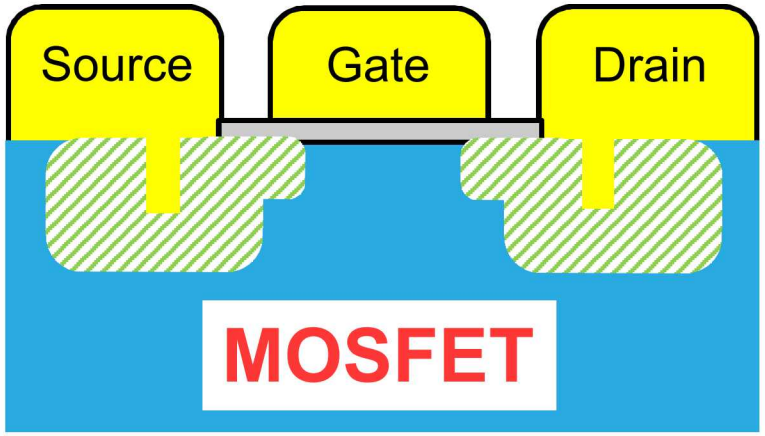


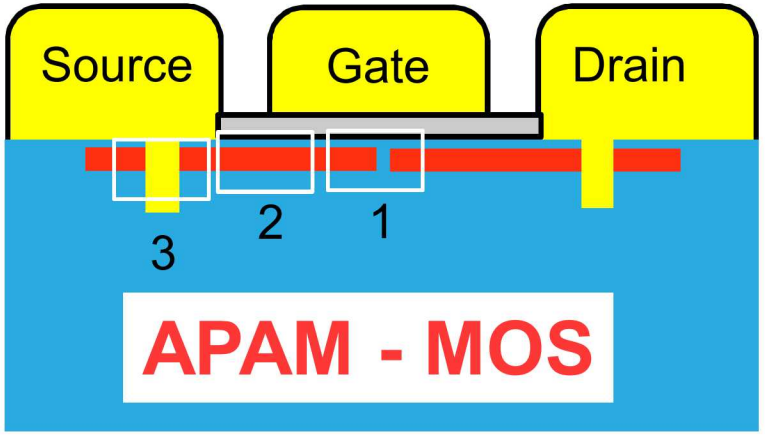

Chemical error correction : need 3 open sites for phosphine

**High dopant density : atomic-scale transformation of silicon material**

# Application #1 : APAM – MOS transistor

EAB: “We recommend a clearer and stronger interdisciplinary engagement between device and architecture communities.”



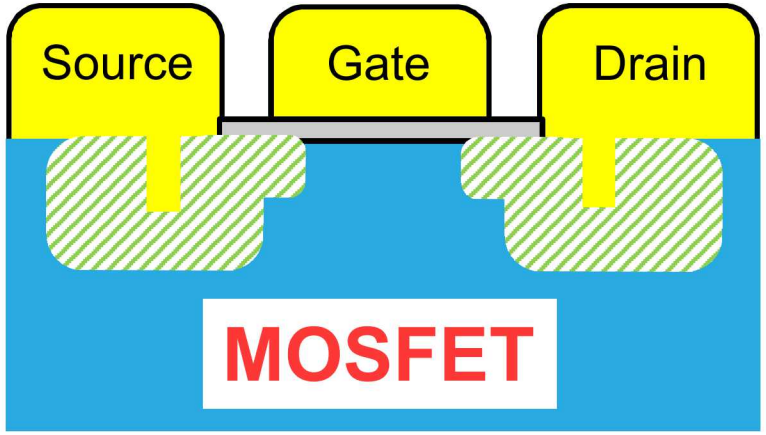



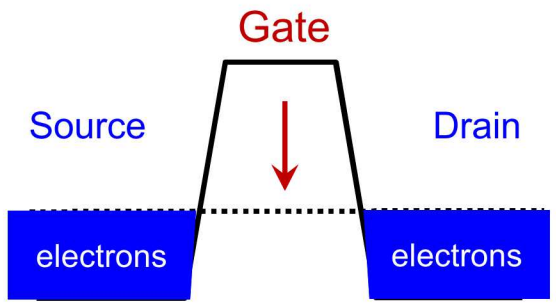

**What is the benefit of looking at a transistor with atomic-scale control?**

1) Channel
2) Lead
3) Contact

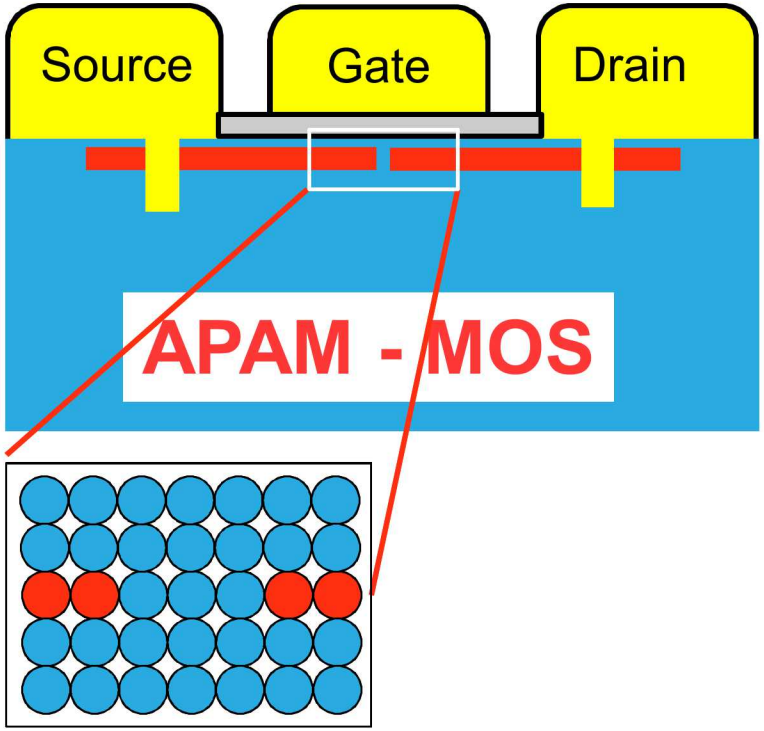
} APAM precision and dopant density

# Application #1 : APAM – MOS transistor




Energy efficiency limited by mechanism and room temperature



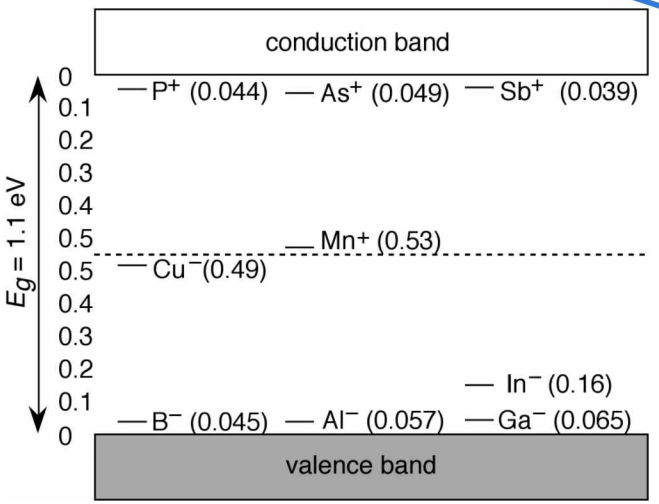

**1. Atomic-scale control over device physics of the channel**

Energy efficiency limit of MOSFET can be overcome?
TFET, barrier engineering, local density of states engineering

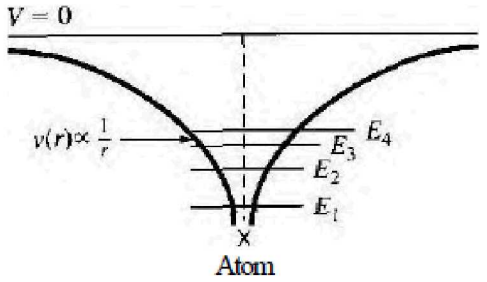
# APAM doping is different than normal doping

Sandia National Laboratories

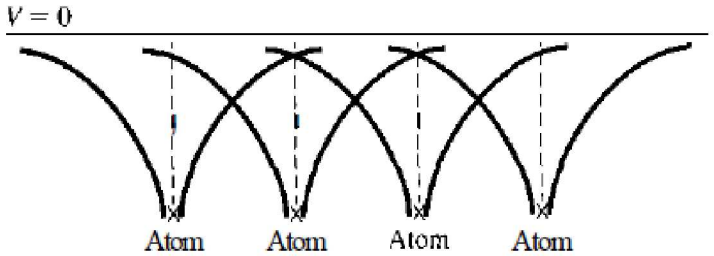
Dopant energy levels



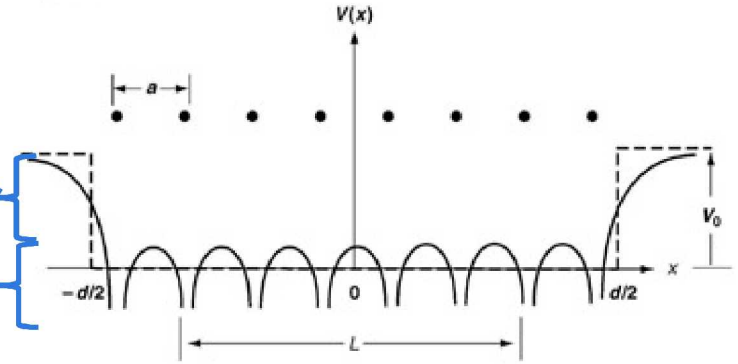

Isolated donor – shallow impurity level relative to Si band




Many donors – impurity potentials overlap…

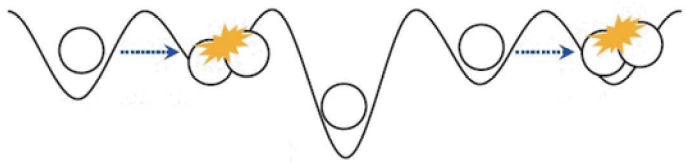



… creating **confinement.**

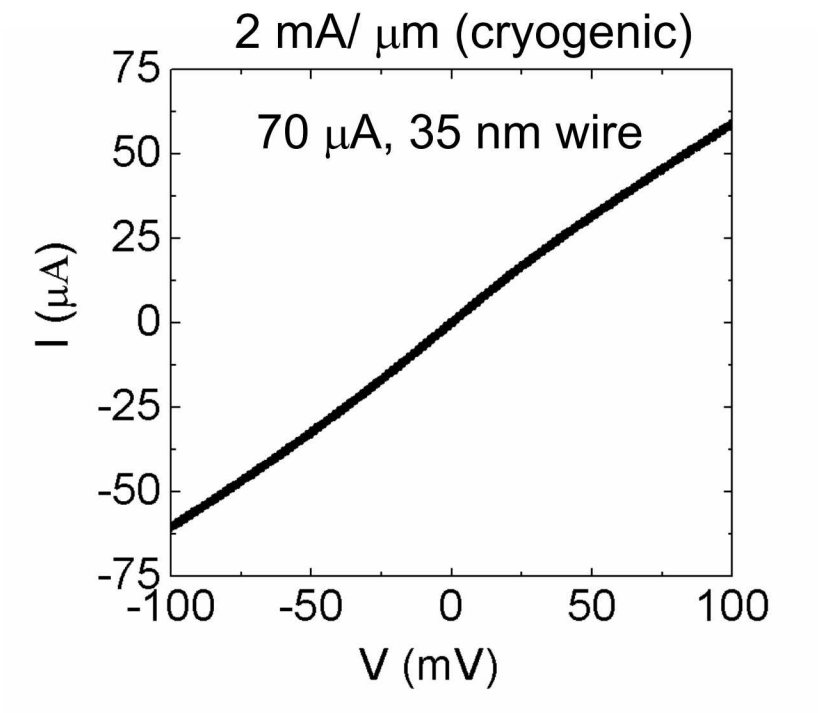



Substantial barrier

Hopping conduction

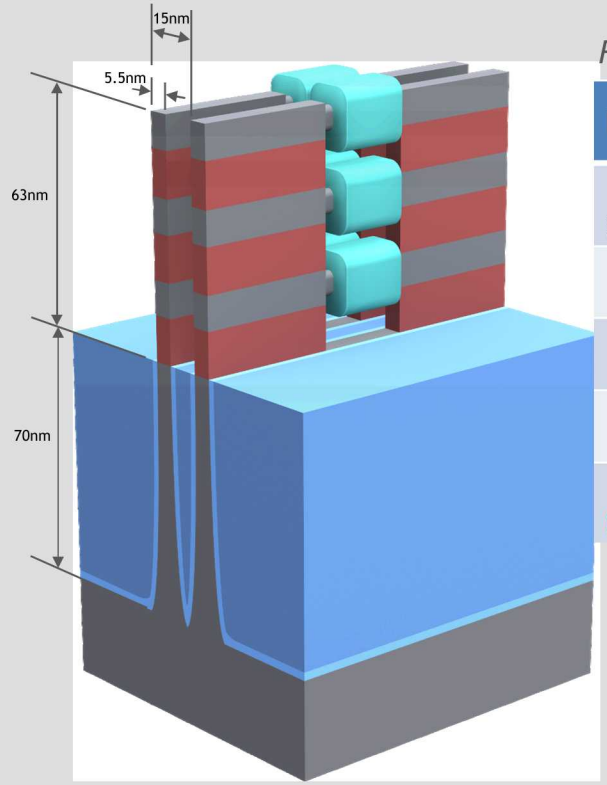


# Consequences of confinement




**APAM wire has extremely high current density**

## Si nanowire FinFET current density

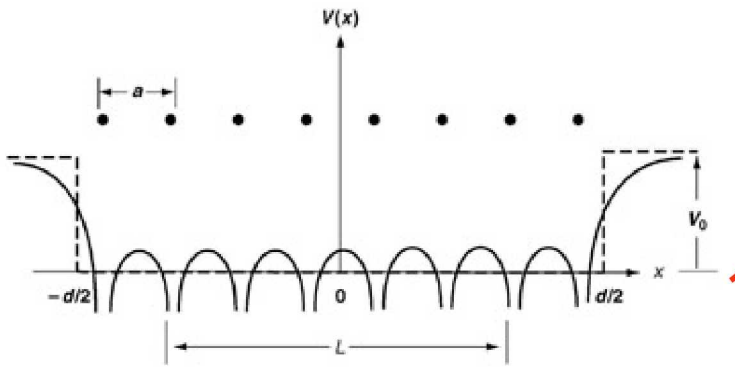


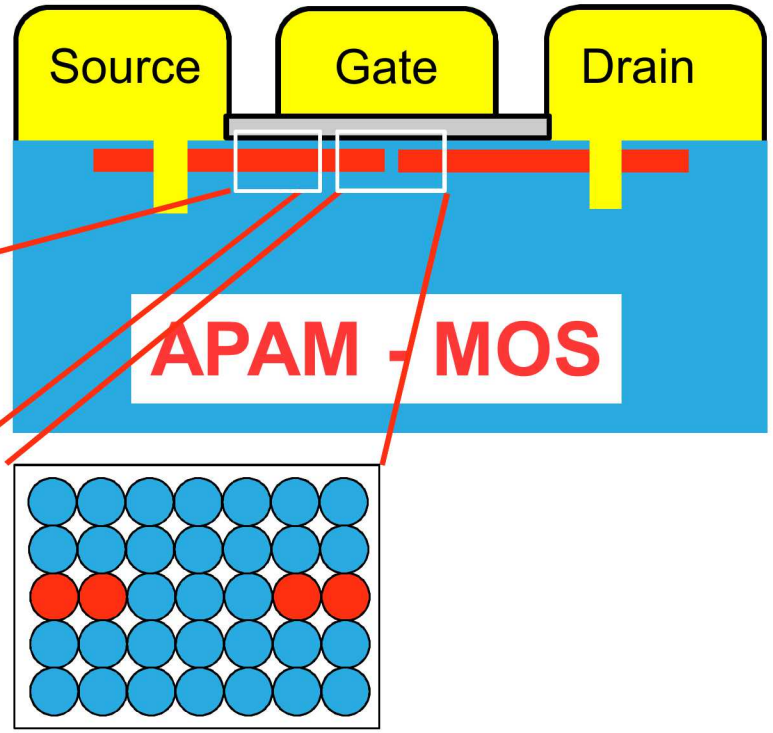

*R. Arghavani estimates*

| Parameters | $I_{ON}$ (mA/μm) @ $V_{GS}=V_{DS}=0.7V$ | $\Delta I_{ON}/I_{ON\_FF}$ |
|---|---|---|
| Si FinFET ($H_{FIN}$=37nm) | 0.630 | 0 |
| 1 NW GAA | 0.286 | -0.55 |
| 2 NW GAA | 0.525 | -0.17 |
| 3 NW GAA | 0.576 | -0.09 |
| Si FinFET ($H_{FIN}$=54nm) | 0.690 | +0.095 |

Current density is a pain-point that can limit transistor speed

# Application #1 : APAM – MOS transistor



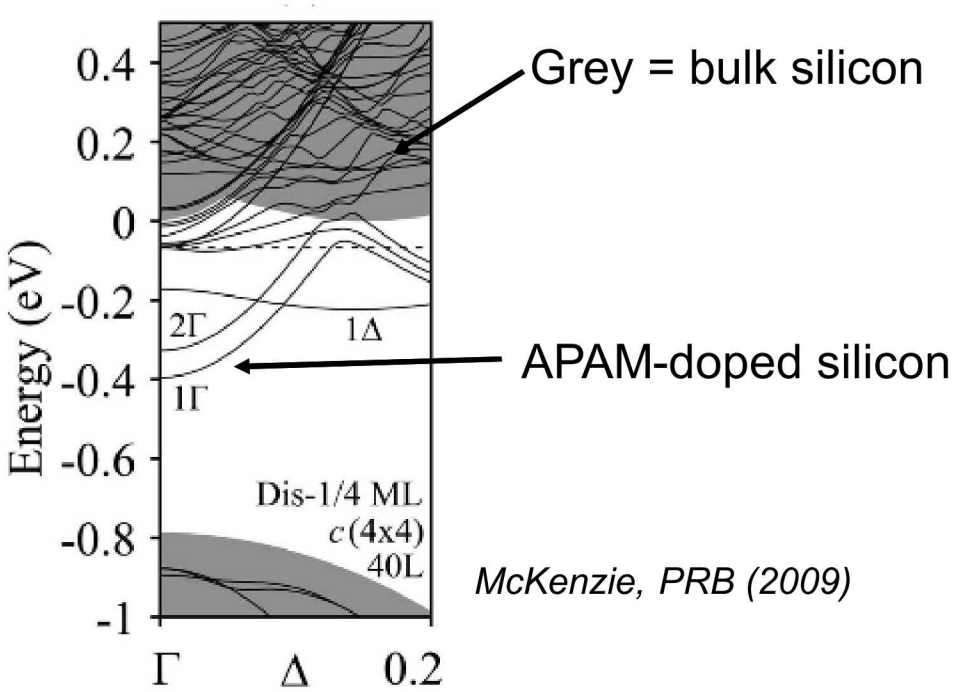

2. **Atomic-scale control over material**

Current density limit to speed of transistor can be overcome?

1. Atomic-scale control over device physics of the channel

Energy efficiency limit of MOSFET can be overcome?

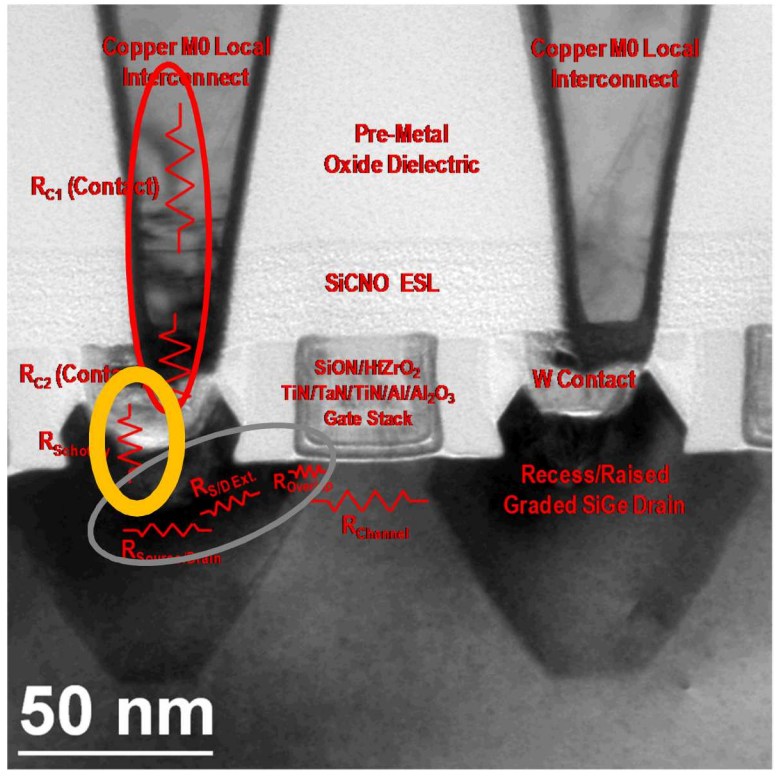
# APAM material is different than normal silicon




*McKenzie, PRB (2009)*

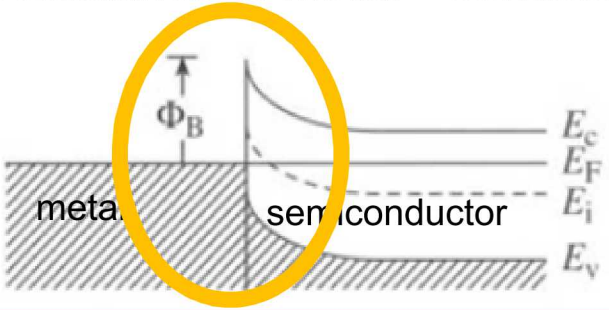
1. Electronic structure of APAM-doped silicon is not like undoped silicon

3. Collapse height and width of metal-semi barrier – **contact resistance is no longer a limitation**

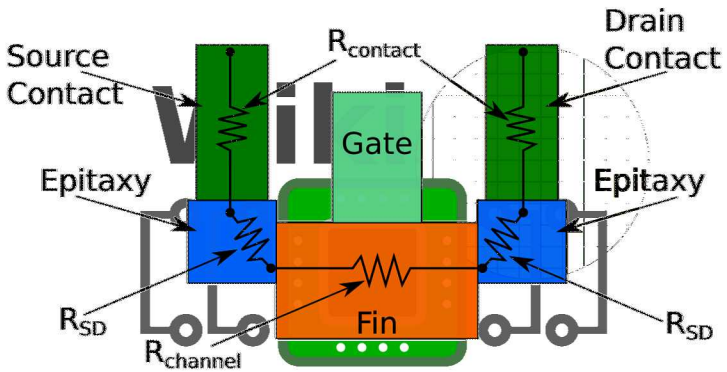



Chipworks, Intel 32 nm CPU (from Core i5 660)

2. Contact size in MOSFET is limited by resistance of metal – semiconductor contact

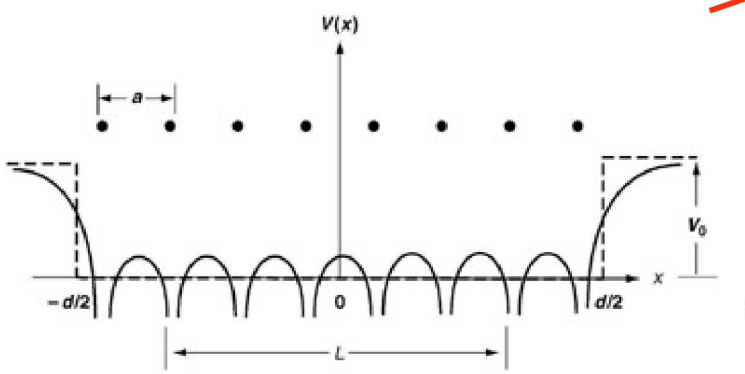


# Application #1 : APAM – MOS transistor



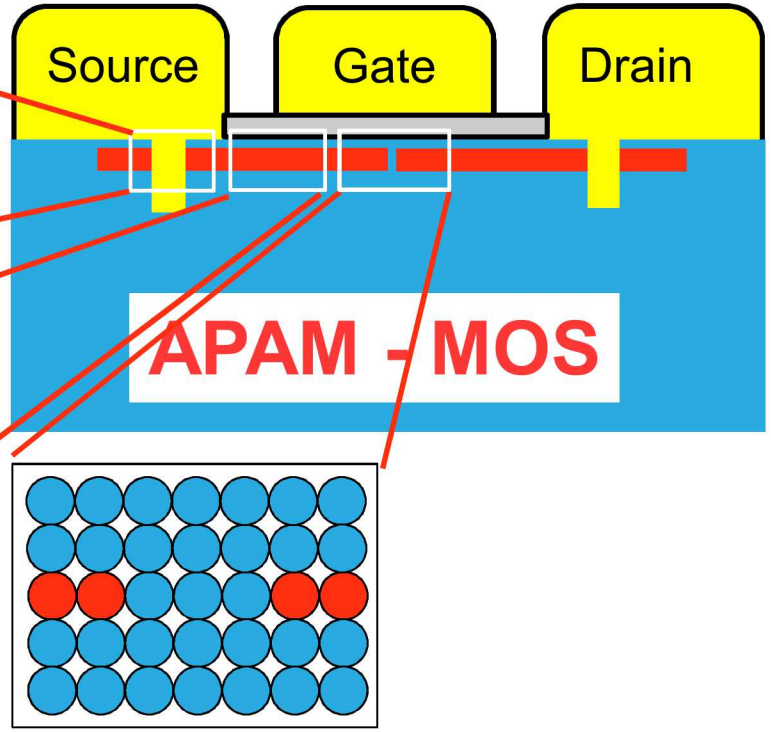

**3. Atomic-scale control over material**

Limitations to contact resistance can be overcome?




2. Atomic-scale control over material

Current density limit to speed of transistor can be overcome?

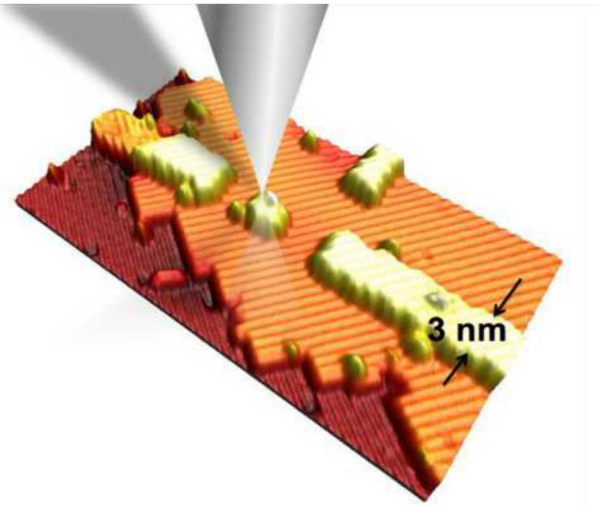



1. Atomic-scale control over device physics of the channel

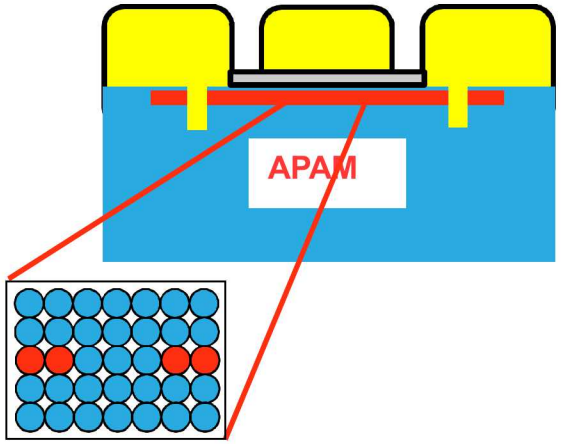
Energy efficiency limit of MOSFET can be overcome?

# APAM Exemplar roadmap

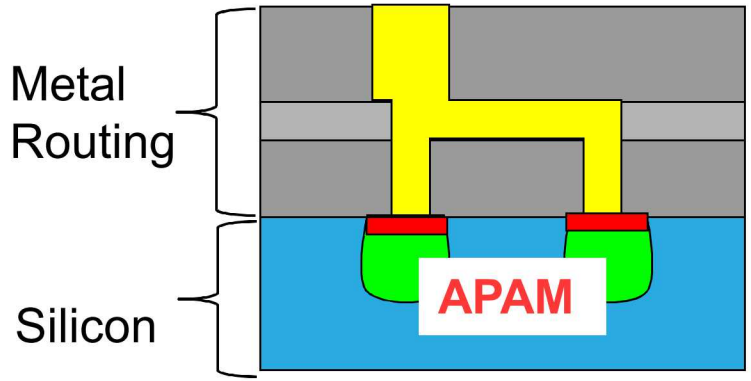
APAM




APAM – MOS transistor




Interconnects




**Dramatic improvement in interconnect resistivity**

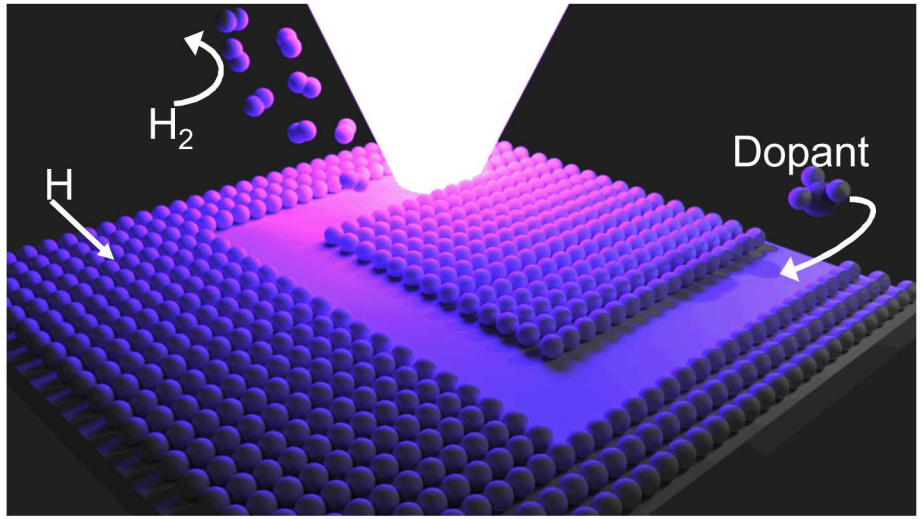
Can be applied to regular MOSFETs?

# APAM-style processing

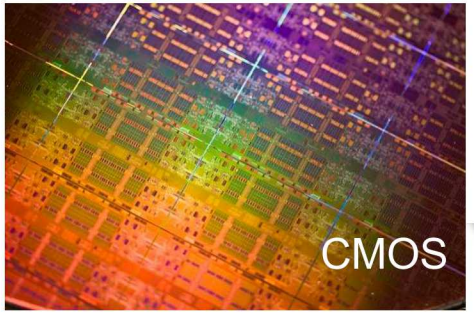
EAB: “Hone… strategic focus on ensuring potential processing pathways that would allowed for assured manufacturing within the US and target operation requirements for National Needs at 150° C or higher”

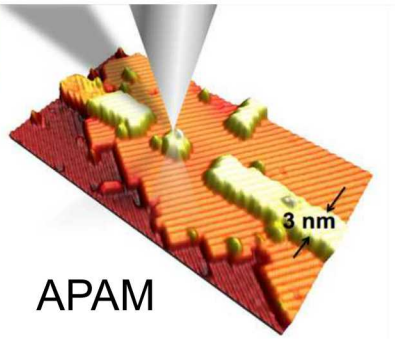
Sandia National Laboratories

## Photolithography



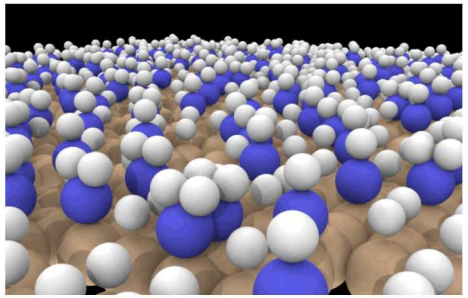

## Integration




APAM

## New resists and dopants



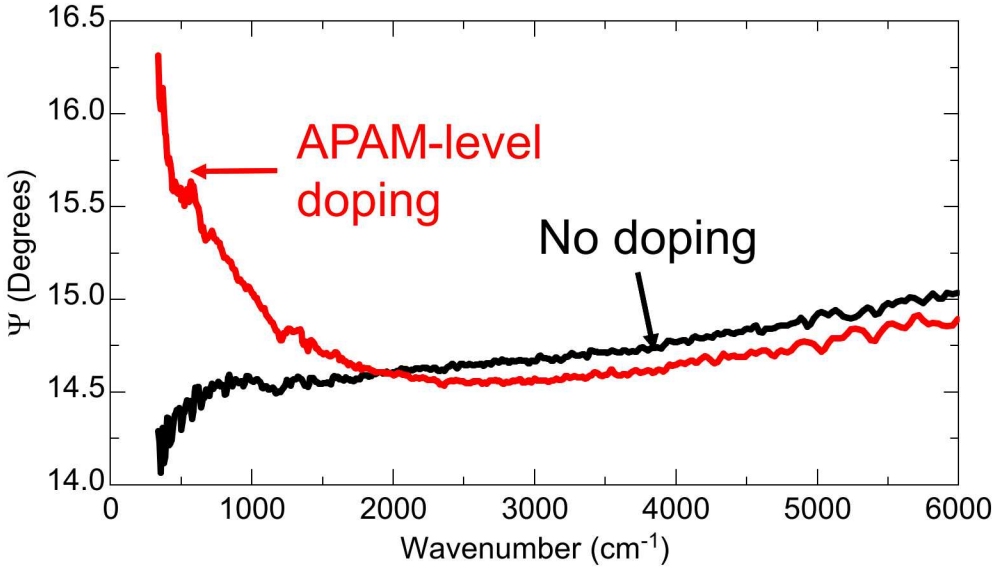
## Robustness

# Same ingredients useful for opto-electronics

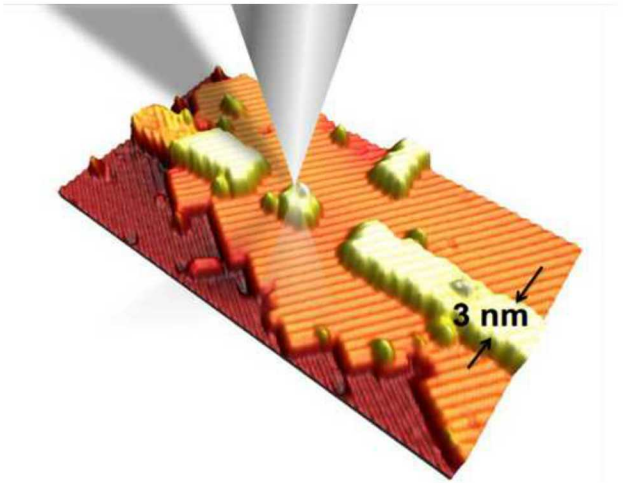
APAM – MOS requires:

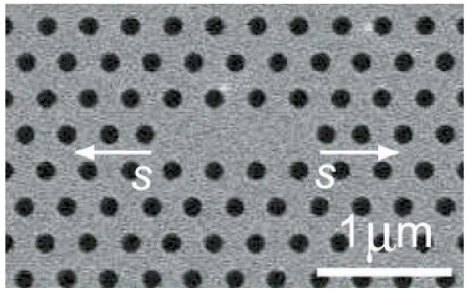
1) Atomic-precision fabrication
2) Confinement (high dopant density)
3) Electronic structure (high dopant density)

Electronic structure & confinement




Lithography




**Novel response in Far-IR to THz…**

**… which may be engineered for optoelectronics**

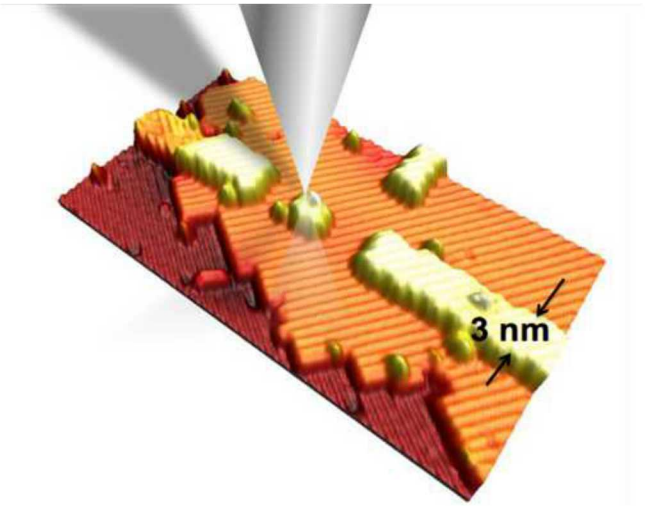
# Application 3: Fingerprint

**Nearer-term… Unique optical barcode**
**Impact : supply chain assurance**

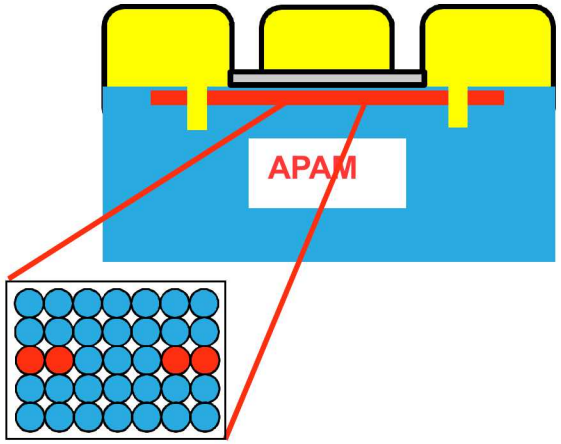
# APAM Exemplar roadmap

Sandia National Laboratories

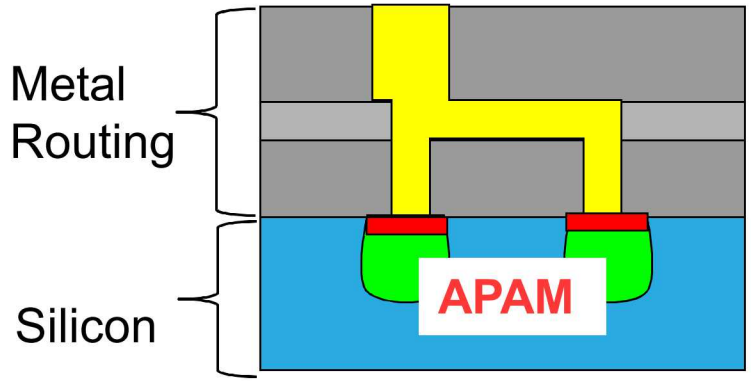
APAM




APAM – MOS transistor




Interconnects

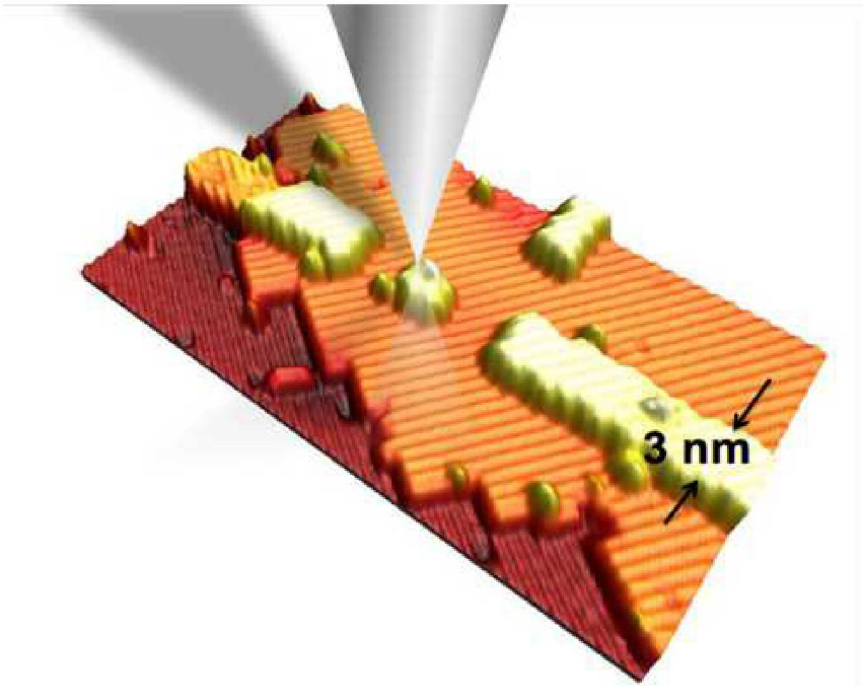



Fingerprint

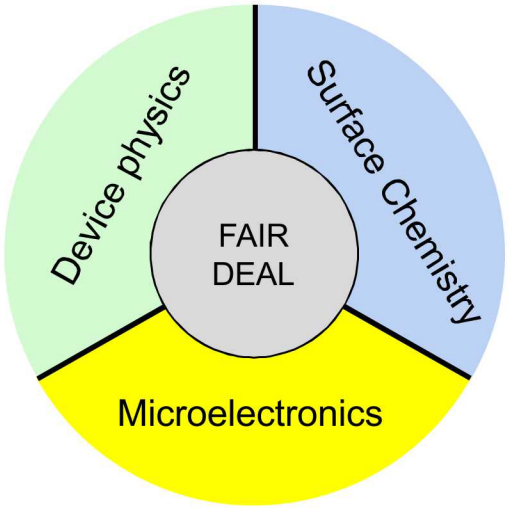
# Outline

Sandia National Laboratories

Motivation for FAIR DEAL GC

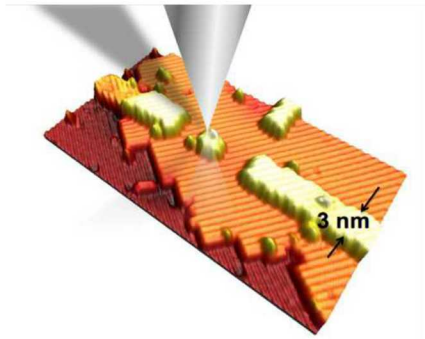



FY 19 Summary of FAIR DEAL GC




- Project outline
- Evolution FY19 – FY20
- Accomplishments – output, milestones, capabilities & partnerships

# Limitations of APAM state of the art




1

Oxide

Silicon

2

Sample clean

× Remove oxide: T > 800°C

3

Hydrogen termination

4

Hydrogen patterning

5

Phosphorus incorporation

× Patterning in UHV, with STM
× Only one proven resist & dopant

6

Silicon capping

7

source

drain

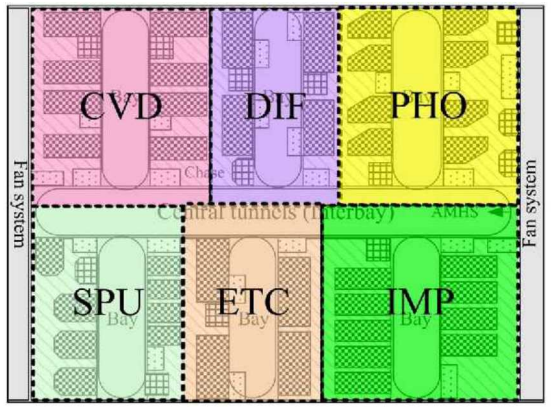
Post-processing

× Limit diffusion: T < 450°C
× Cryogenic operation only

Problems span surface chemistry, device physics, microelectronics

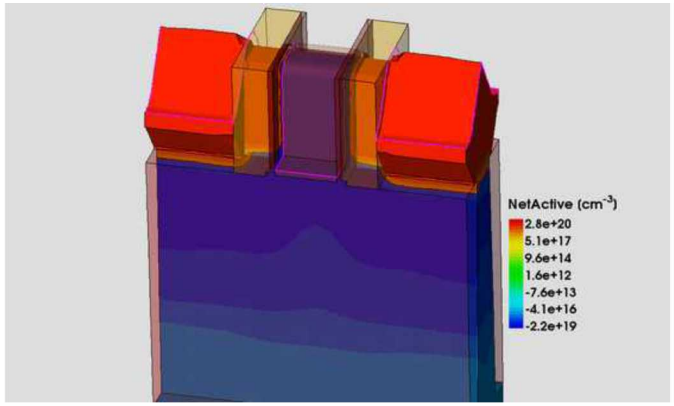
# Bootstrapping process

## Standard fab tools



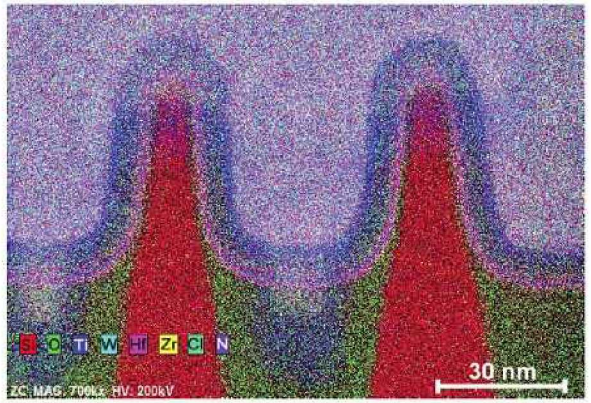

Need to preserve surface

## Process simulation



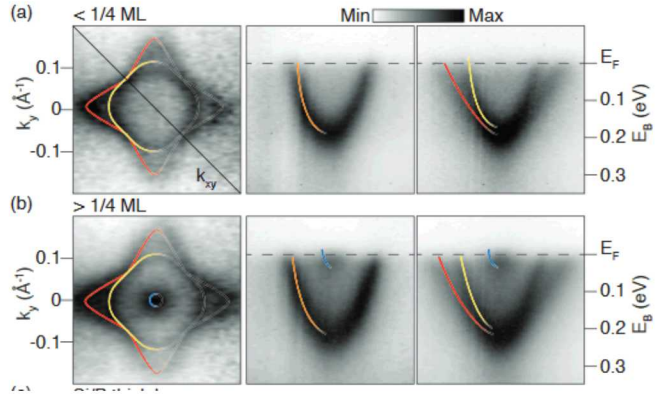

APAM needs nonstandard conditions

## Characterization




Not done thoroughly to date

## Material properties

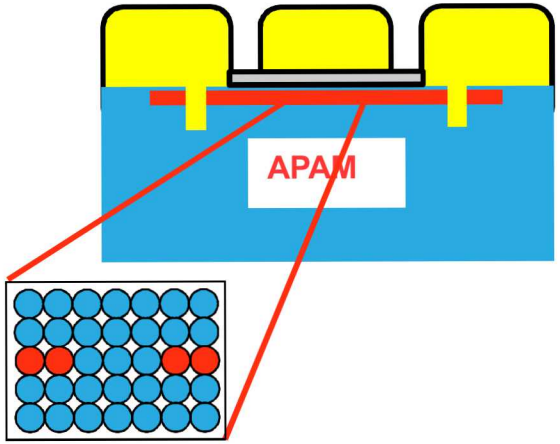


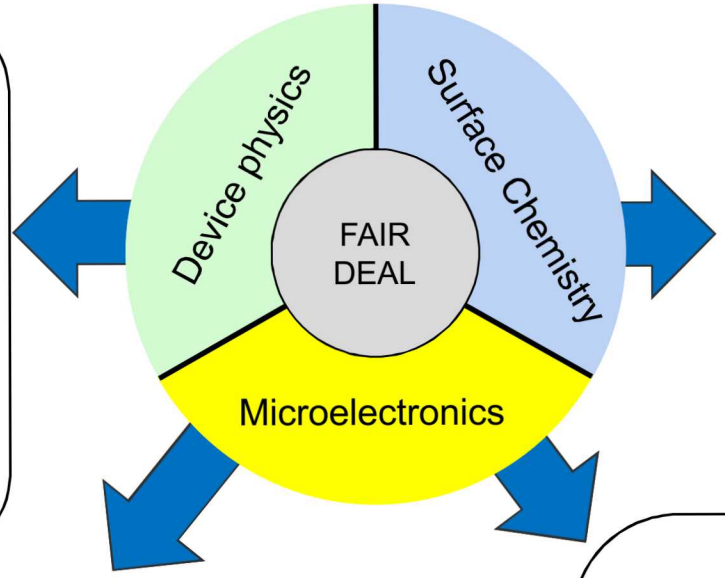

Not well-understood

# Digital electronics at the atomic limit (DEAL)

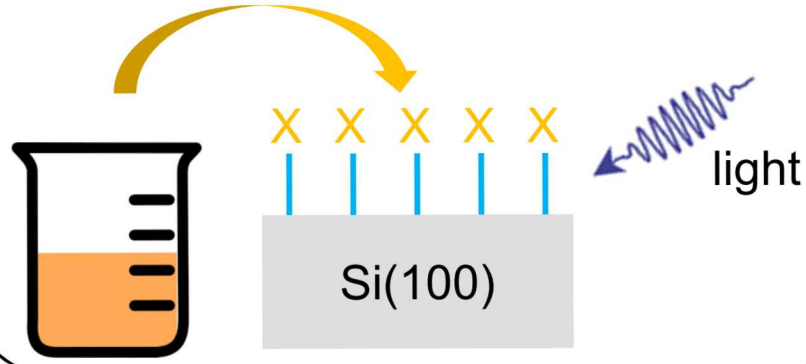
Sandia National Laboratories

## Thrust 1: APAM-enabled Devices

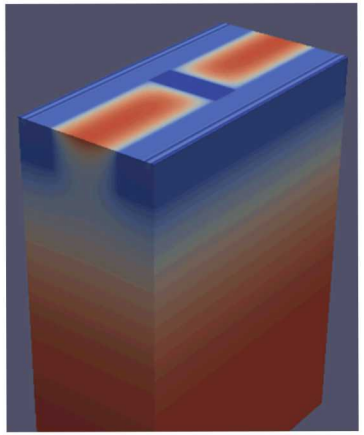


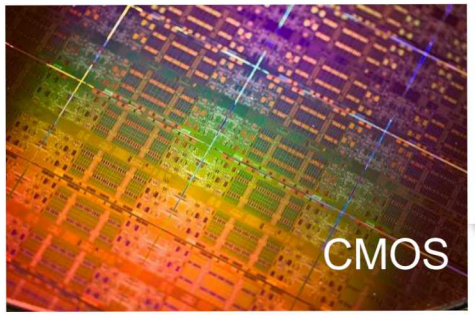

## Thrust 4: Application Platform

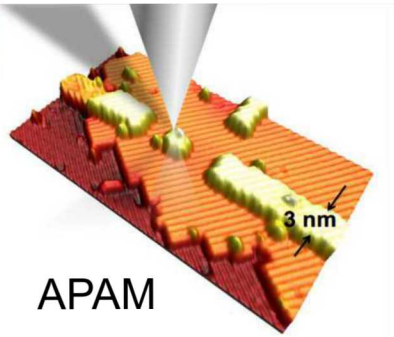



## Thrust 2: APAM Modeling

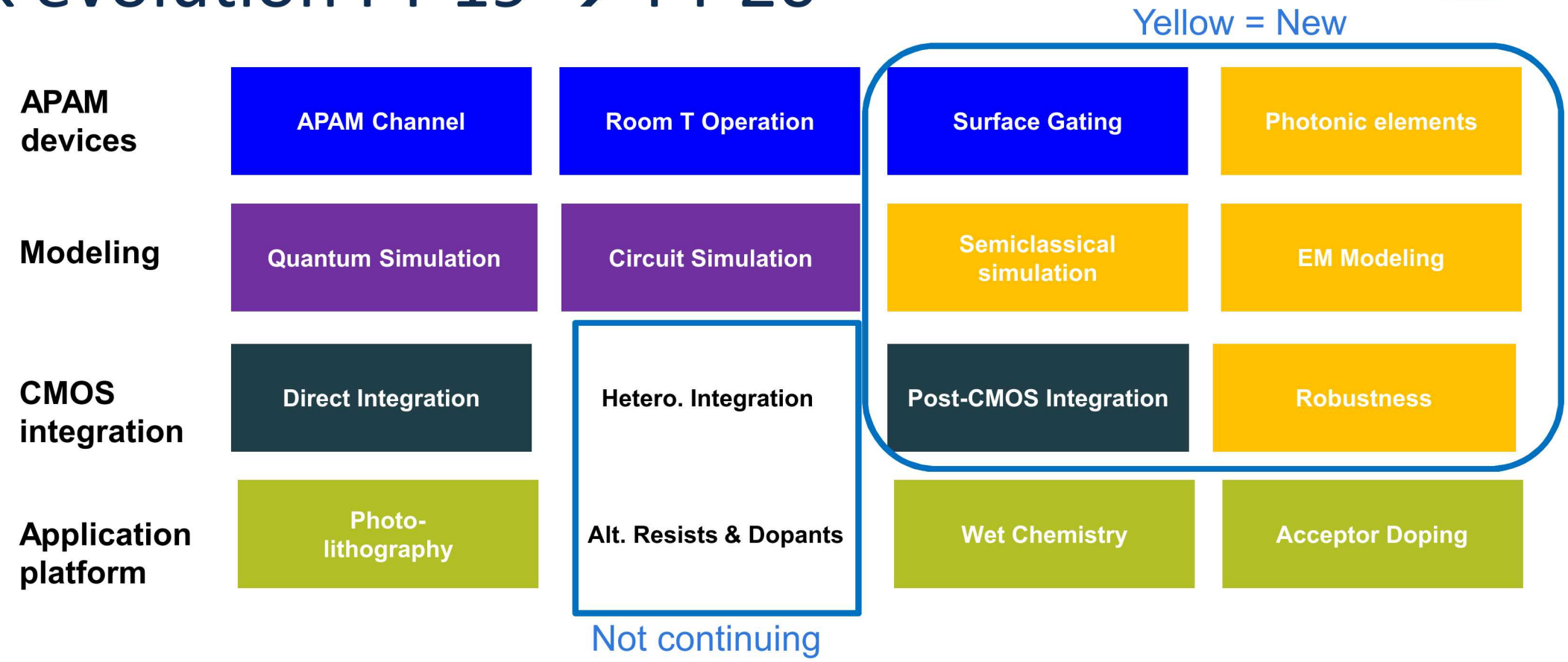


## Thrust 3: CMOS Integration



# Task evolution FY 19 → FY 20



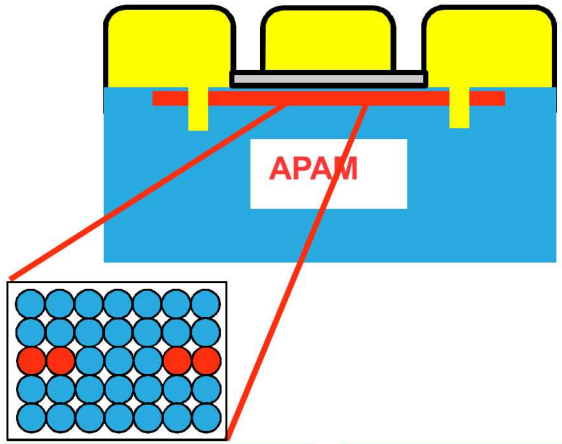

- Hetero integration: dropped due to EAB suggestion
- Alt. Resists and Dopants: answered question
- Moved acceptor doping to thrust 4
- New tasks: Photonics (discovery), semiclassical simulation (need), EM simulation (need), robustness (EAB)

# Critical path

EAB: “complete a critical path analysis to ID the potential single-point failure tasks that place … the project at higher risk of failure”

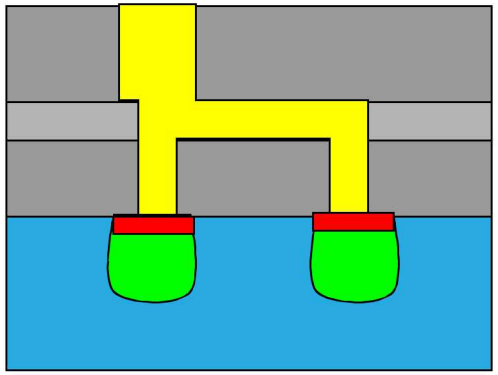
Sandia National Laboratories

## APAM – MOS




| | |
|---|---|
| APAM Channel | Room T Operation |
| Semiclassical simulation | Quantum Simulation |
| Direct Integration | Robustness |
| Acceptor Doping | Surface Gating |

## Interconnect



| | |
|---|---|
| APAM Channel | Room T Operation |
| Semiclassical simulation | Circuit Simulation |
| Direct Integration | Robustness |
| Acceptor Doping | Photo-lithography |

## Fingerprint

| | |
|---|---|
| APAM Channel | Photonic elements |
| EM simulation | |
| Direct Integration | Post-CMOS Integration |
| Photo-lithography | Wet Chem. |

**Blue tasks are key to more than one exemplar – critical path**

# Fully staffed

EAB: "...provide an overall summary on staffing progress and potential needs…"

Sandia National Laboratories

**Bold = new hires / promotions** Underlined = new in role

**Program Leadership**
PI: Shashank Misra
PM: Robert Koudelka
Deputy PM: Paul Sharps

**APAM-enabled devices**
Lead: Shashank Misra

**Integration**
Lead: Dan Ward

**Modeling**
Lead: Suzey Gao

**Application platform**
Lead: George Wang

**Support Team**
Financial: **Jennifer Woodrome**, Laurel Taylor
Logistics: Lori Mann, **Jennifer Woodrome**
Web: **Jennifer Woodrome**
IP: David Wick
Administrative: Nina Martinez

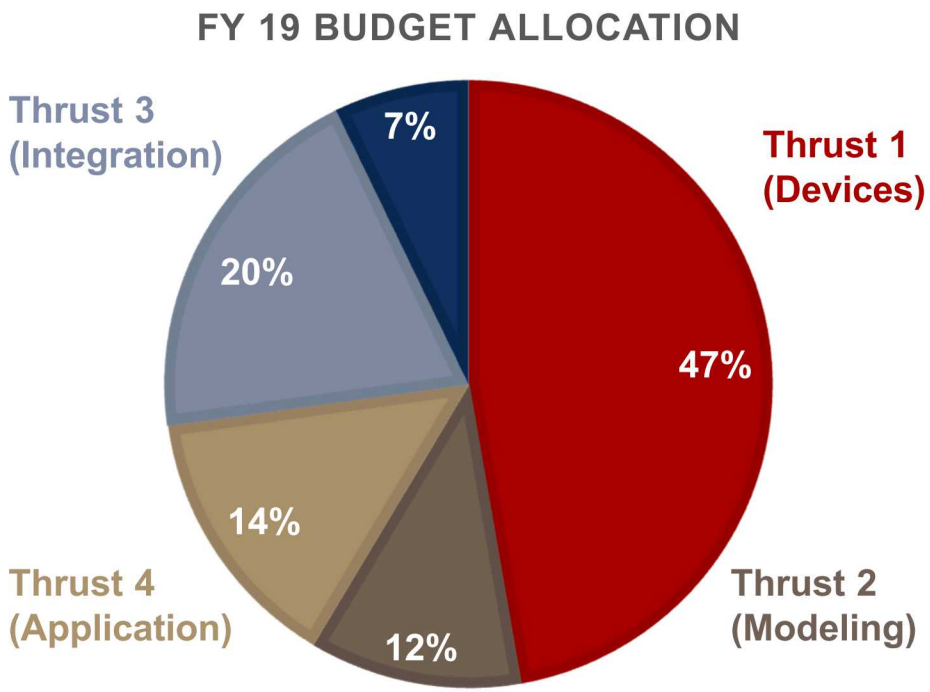
Measurement: Lisa Tracy, Tzu-Ming Lu, Albert Grine, David Scrymgeour, Ping Lu, Aaron Katzenmeyer

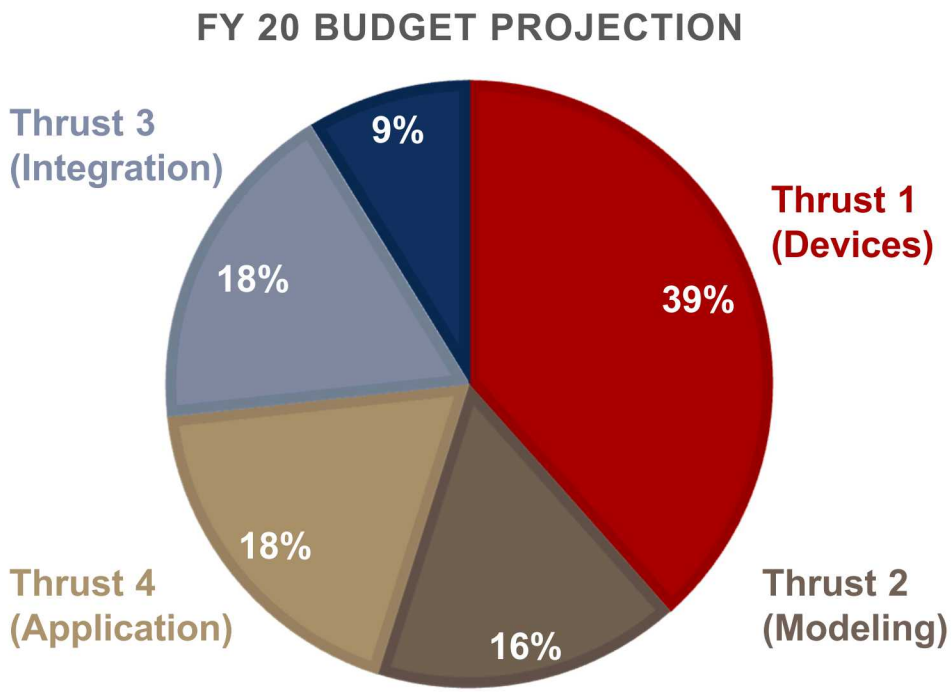
Microfabrication: Dan Ward, **DeAnna Campbell, Mark Gunter, Phillip Gamache,** Sean Smith, Troy England, Andrew Starbuck, Steve Carr, Reza Arghavani

Modeling: Suzey Gao, Denis Mamaluy, **Juan Granado,** William Lepkowski, Michael Goldflam, **Amun Jarzembski,** Thomas Beechem, Andrew Baczewski**, Quinn Campbell, Steve Young,** Peter Schultz

Surface Science: Shashank Misra, **Scott Schmucker, Evan Anderson,** Joe Lucero, **Jeff Ivie,** Ezra Bussmann, **Fabian Pena,** Aaron Katzenmeyer, George Wang, **Esther Frederick, Igor Kolesnichenko,** David Wheeler

# Budget evolution FY19 → FY20



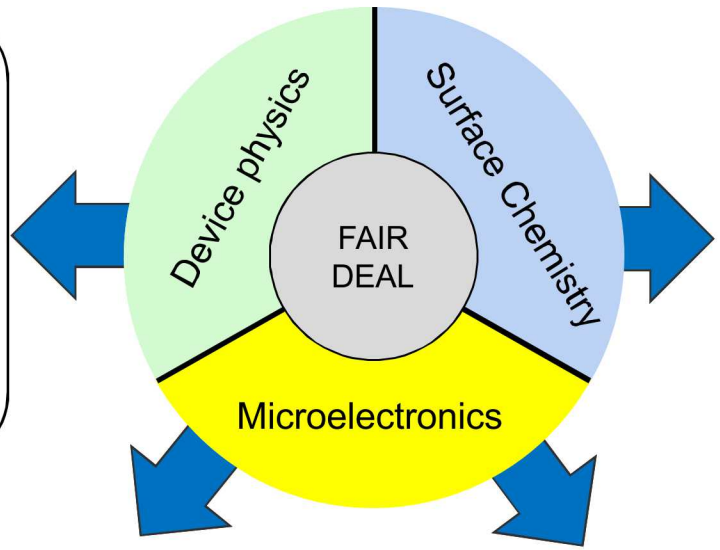

**Shifting from buying capability to using capability**

# FAIR DEAL Output

Sandia National Laboratories

**Thrust 1: APAM-enabled Devices**

2 book chapters
1 invited talk
3 papers in preparation
3 symposiums/workshops
4 contributed talks




**Thrust 4: Application Platform**

1 invited talk
1 postdoc talk award
2 contributed talks

**Thrust 2: APAM Modeling**

1 invited talk
1 conference paper
2 papers in preparation
1 contributed talk

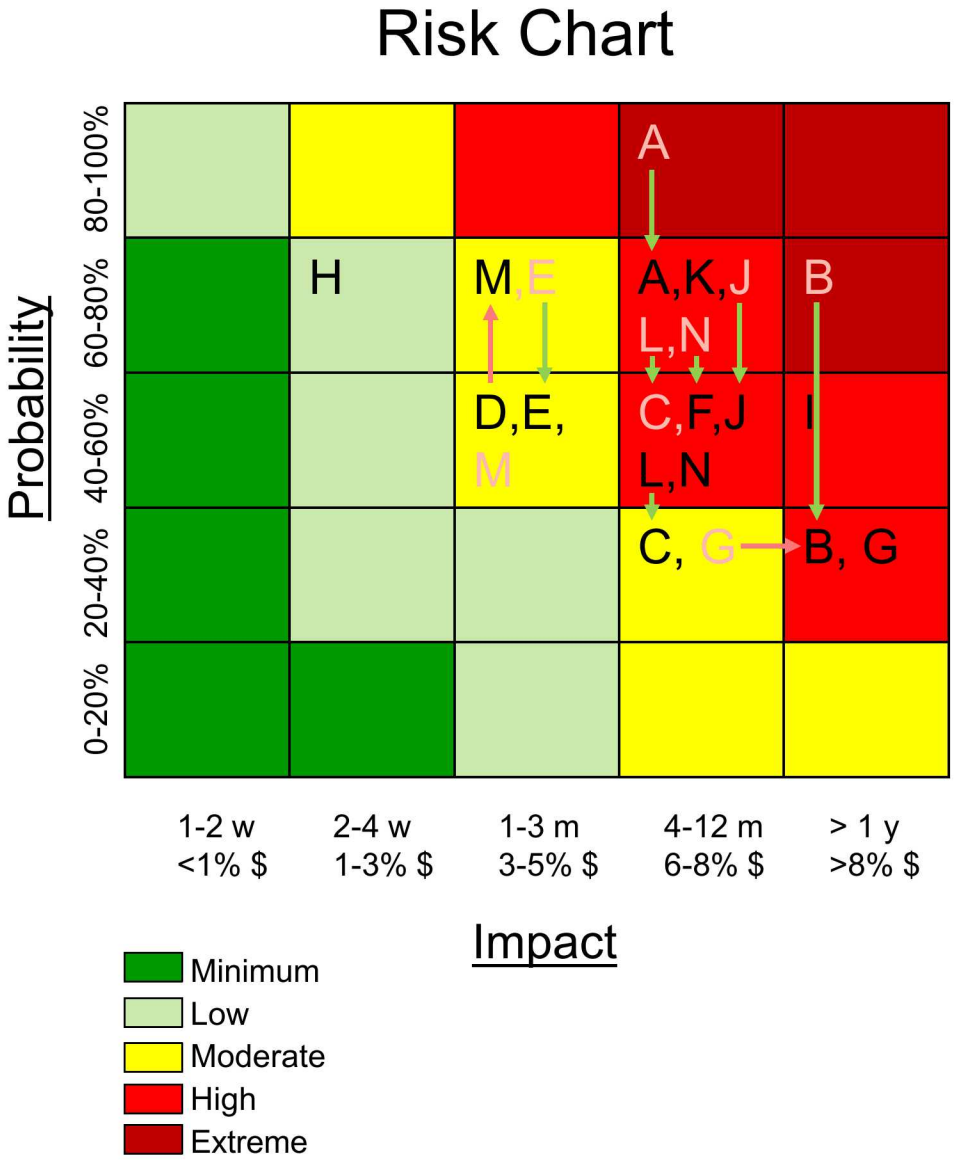
**Thrust 3: CMOS Integration**

1 invited talk
3 contributed talks

**Output is critical : learning, establish position, reduce risk to follow-on projects**

# Risk evolution FY 19 → FY 20

| | | | | |
|---|---|---|---|---|
| #1 | APAM Channel | Room T Operation | Surface Gating | Photonic elements |
| | A | B | C | D |
| #2 | Quantum Simulation | Circuit Simulation | Semiclassical simulation | EM simulation |
| | E | F | G | H |
| #3 | Direct Integration | Post-CMOS | Robustness | |
| | I | J | K | |
| #4 | Photo-lithography | Wet Chem. | Acceptor Doping | |
| | L | M | N | |




**Risk and milestone evolution is different for a science project : learning & strategic shifts reduce risk**

# Thrust 1 FY 19 Milestones – input from Thrust 2

Sandia National Laboratories

On schedule | Delayed | Dropped

| | EAB #1 |
|---|---|
| | Gating |
| Q1 | Evaluate surface gate stack using SET |
| Q2 | Optimize geometry |
| Q3 | Evaluate surface gate stack using MOScap |
| | RT operation |
| Q3 | Implement alternative capping techniques |
| Q4 | Pick technique that gives least doped cap |
| | Channel engineering |
| Q1 | ID recipes based on Hall data |
| Q3 | Characterize dopant location using TEM |
| | Acceptor doping |
| Q3 | Install acceptor precursors (two) |
| Q4 | Test acceptor precursors (two) |

New approach

Wrong question

Wrong question

New approach

| | EAB #2 |
|---|---|
| | Gating |
| Q1 | Evaluate 1st surface gate stack using SET |
| Q4 | Evaluate 2nd surface gate stack using MOScap |
| | RT operation |
| Q2 | Semiclassical modeling – rescope problem |
| Q4 | Bulk leakage: test isolation chip<br>Cap leakage: test capping techniques |
| | Channel engineering |
| Q3 | ID recipes and characterization techniques |
| Q4 | Correlate to electrical charactristics |
| | Acceptor doping |
| Q3 | Collaborator tests M-O precursor |
| Q4 | Install diborane precursor at SNL |

# Thrust 2 FY 19 Milestones – needs from other thrusts

Sandia National Laboratories

On schedule | Delayed | Dropped

| | EAB #1 |
|---|---|
| | Electron quantum simulation |
| Q2 | Adapt and apply quantum simulator to simulate and understand APAM wire electrical response |
| Q4 | Calibrate simulation for APAM wire with data |
| | Bipolar quantum simulation |
| Q2 | Develop plan for bipolar quantum simulation |
| Q4 | Band structure for bipolar APAM devices |
| | Circuit simulation |
| Q2 | Include control gate in circuit simulation |
| Q4 | Demonstrate a reconfigurable switch |

New question

**Modeling need for experiment**

Wrong question

**Modeling need for experiment**

| | EAB #2 |
|---|---|
| | Quantum simulation |
| Q2 | Simulate and analyze electrical response of APAM wire |
| Q4 | Evaluate discrete impurity effects in APAM tunnel junction |
| | Semiclassical simulation |
| Q2 | Quantify epi-layer leakage current in APAM wire for RT operation |
| Q4 | Electron mobility dependence on doping level |
| | Circuit simulation |
| Q2 | Compact model for reconfigurable transistor |
| Q4 | Circuit simulation and design for CMOS ring oscillator |

# Thrust 3 FY 19 Milestones – respond to EAB

On schedule | Delayed | Dropped

| | EAB #1 |
|---|---|
| | Direct Integration |
| Q1 | Design STM compatible CMOS diagnostic chip |
| Q2 | Evaluate thermal budget of CMOS chip ex-situ |
| Q3 | Evaluate thermal budget of CMOS chip in-situ |
| | Heterogeneous Integration |
| Q1 | System-in-package demonstration |
| Q3 | Plan bump bonding scheme |
| | Reduced Temperature Processing |
| Q1 | Evaluate room temperature hydrogen termination |
| Q3 | Develop lower temperature surface cleans |
| Q4 | Demonstrate APAM recipes on thinned silicon |

Rescoped work →

Wrong question

Rescope work →

New Question →

| | EAB #2 |
|---|---|
| | Direct Integration |
| Q3 | Design APAM-CMOS circuit |
| Q4 | Fabricate APAM-CMOS circuit |
| | Post-CMOS Integration |
| Q2 | Demonstrate RT H-termination and pattern |
| Q3 | Demonstrate RT surface prep with oxide removal |
| Q4 | Demonstrate RT surface prep with RIE cleans |
| Q4 | Demonstrate all recipes on polished silicon |
| | Robustness |
| Q3 | Design aging setup |
| Q4 | Build setup, design software |
| Q4 | Demonstrate SOI Hall bar |

# Thrust 4 FY 19 Milestones – leverage community

On schedule | Delayed | Dropped

| | EAB #1 |
|---|---|
| | Photolithography |
| Q3 | Create < 2 um patterned feature with 50% depassivation |
| Q4 | Stage 1 build of stand-alone PL system |
| | Acceptor Doping |
| Q3 | Install acceptor precursors (two) |
| Q4 | Test acceptor precursors (two) |
| | Alternative Resists |
| Q3 | Quantify air & inert stability for H & halogen |
| Q3 | Test P incorporation for H & halogen resists |
| | Wet Chemistry |
| Q4 | MLD chemistry by stamping |
| Q4 | Bring ANT surface analysis capabilities online |

New approach →

New approach →

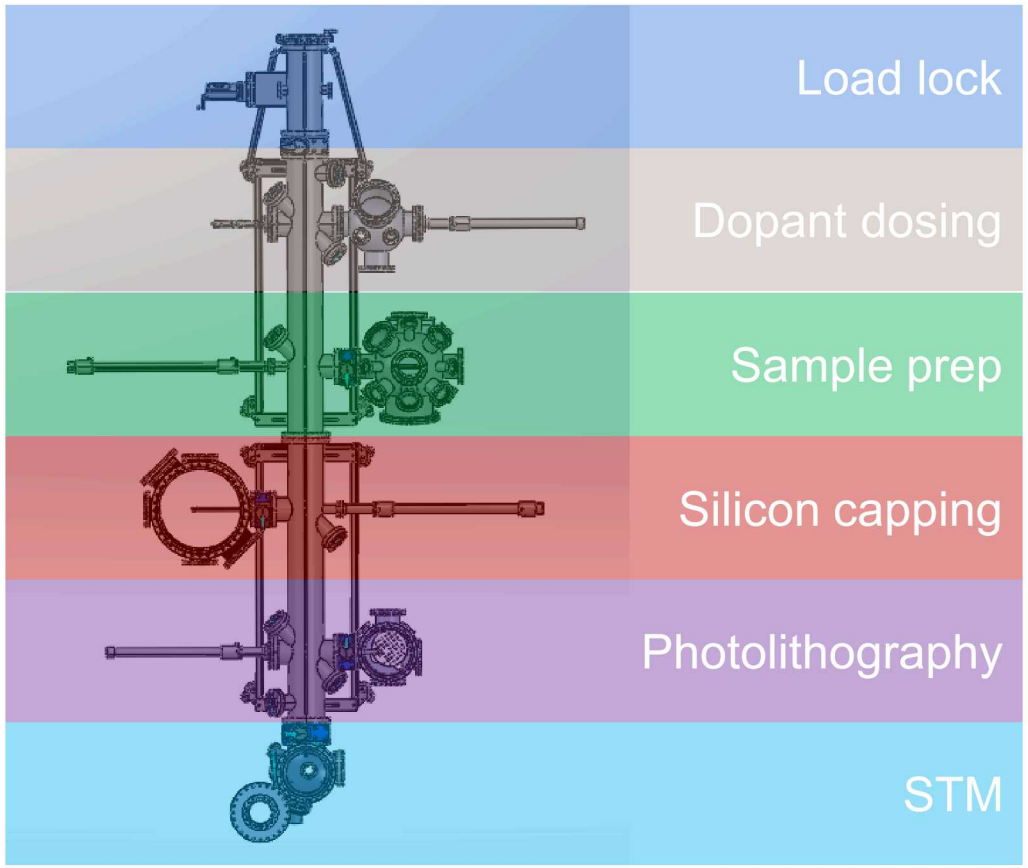
Answered question →

New approach →

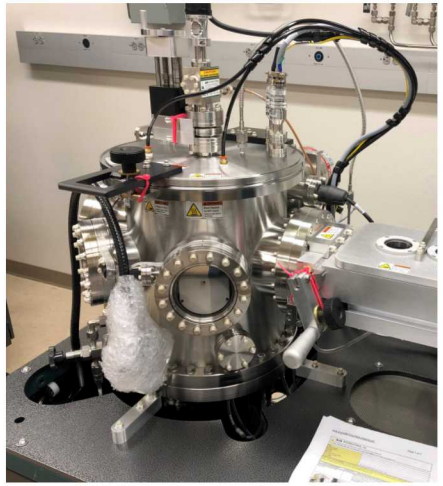
| | EAB #2 |
|---|---|
| | Photolithography |
| Q4 | Determine conductivity for 2 um wide photopatterned wire with new system |
| Q4 | Stage 1 build of stand-along PL system |
| | Acceptor Doping |
| Q3 | Collaborator tests M-O precursor |
| Q4 | Install diborane precursor at SNL |
| | Alternative Resists |
| Q4 | Quantify air & inert stability for halogen |
| | Wet Chemistry |
| Q3 | Collaborators test halide doping chemistry |
| Q4 | Bring ANT surface analysis capabilities online |

# Devices – establish new capabilities

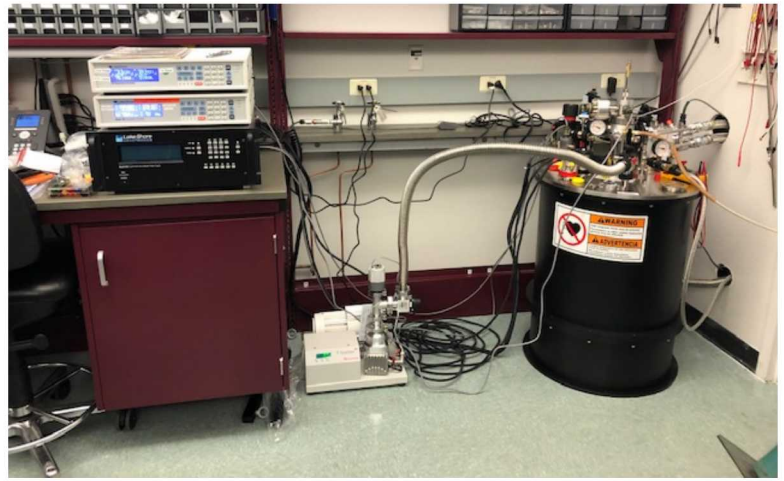
New multichamber APAM system




High-k dielectrics, and metal gates

Variable temperature cryostat



# Modeling – leverage capabilities

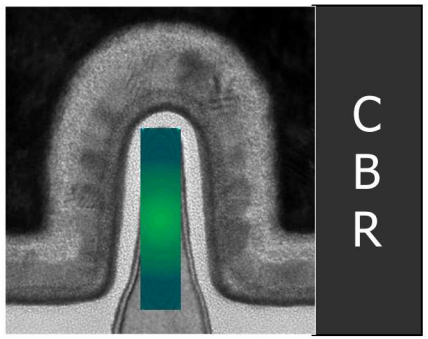
Sandia National Laboratories

Leverage existing codebases

CHARON

Xyce™ PARALLEL ELECTRONIC SIMULATOR

COMSOL

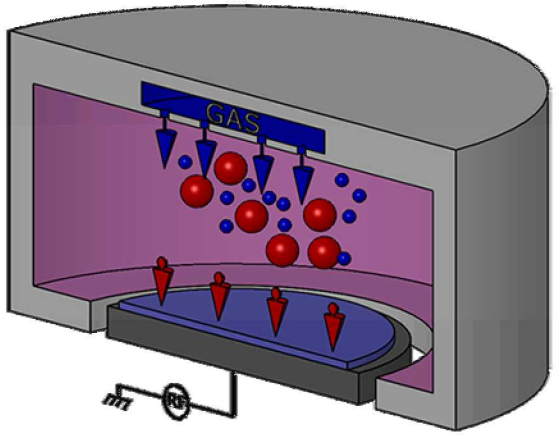



Leverage HPC @ Sandia

# Integration – leverage capability & partnership

Sandia National Laboratories

Hydrogen termination in reactive ion etch
- Use existing tool in new way



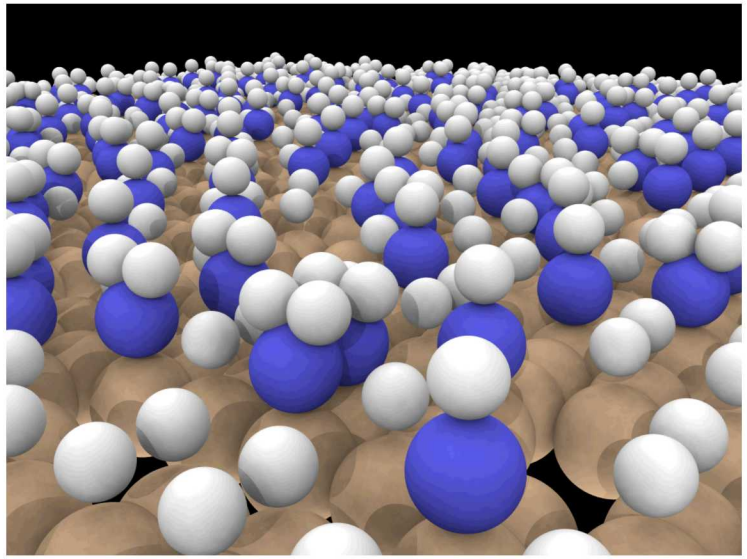

Engage industrial partner: Skywater
- Trusted foundry
- Willing to work with research projects

skywater

# Application platform – capabilities & partnerships

Sandia National Laboratories

Existing codebase - Sandia owns the only APAM-focused DFT + KMC toolchain



Collaborate with others for pathfinding

# Programmatic interaction

Sandia National Laboratories

Path to post-project funding:

1. BES Microelectronics RFI (2)
2. NSF accelerator – analog quantum simulation
3. Face-to-face interactions with customers:
   - Three existing Sandia sponsors
   - Planned: DARPA

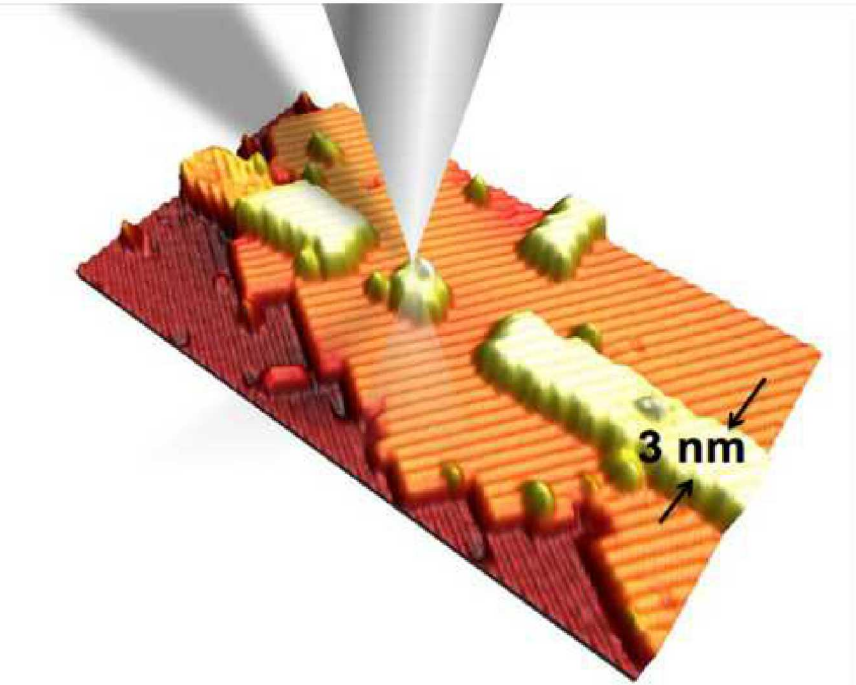
Range of partners for pathfinding → Sandia integrates innovations into devices

Starting conversations about how to partner with industry

# Outline

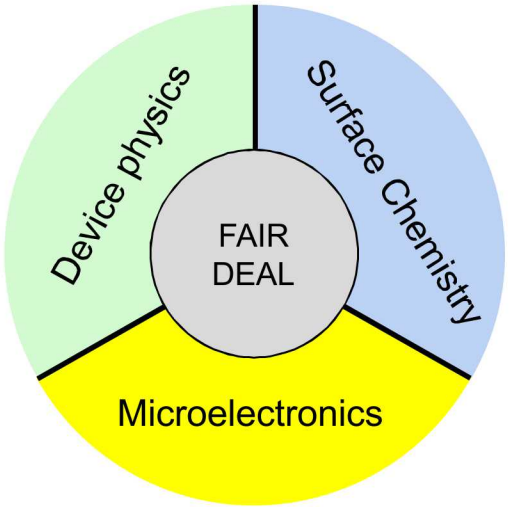
Sandia National Laboratories

## Motivation for FAIR DEAL GC




- What is special about APAM?
- Exemplars & Impact

## FY 19 Summary of FAIR DEAL GC




- Project outline
- Evolution FY19 – FY20
- Accomplishments – output, milestones, capabilities & partnerships

# Project infrastructure

Wiki tracks project – milestones and budget

**1.1 FY20**

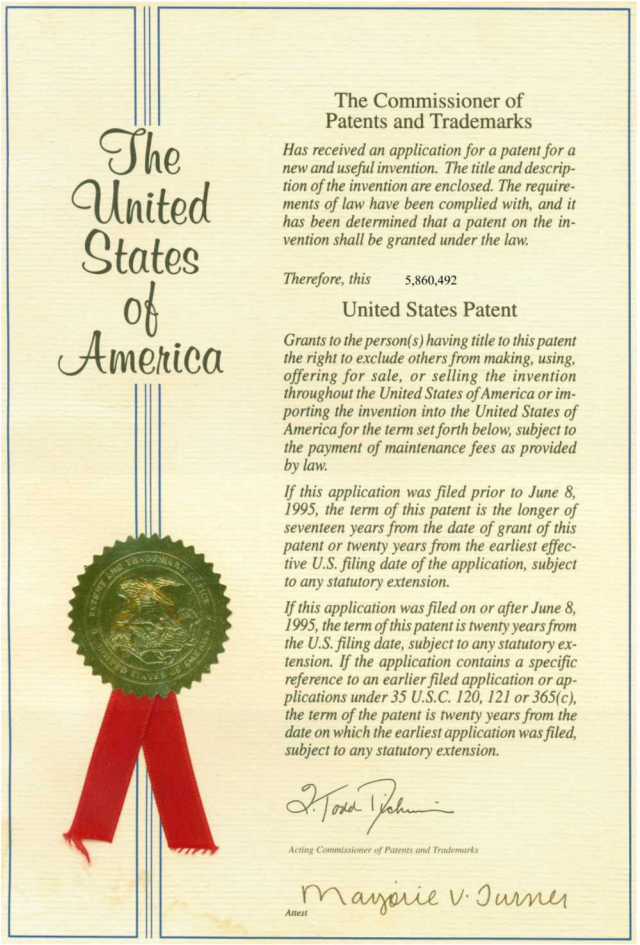
**FY20 MILESTONE PROGRESS**

ON TRACK | DELAYED | HELP | COMPLETED

| Milestones for Photonics | Expected Completion | % Complete |
|---|---|---|
| Determine dielectric constant of a delta layer. | Q2 | |
| Show fab-measure-model control over response from grating | Q3 | |
| ID what makes a good fingerprint | Q3 | |
| Show control over structure more sophisticated than a grating | Q4 | |
| Go/No-go: Design exemplar fingerprint and detector | Q4 | |

Developing security plan with mission partners

Developing IP plan with legal



The United States of America

The Commissioner of Patents and Trademarks

*Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.*

*Therefore, this* 5,860,492

United States Patent

*Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.*

*If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.*

*If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to any statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.*

Acting Commissioner of Patents and Trademarks

Attest