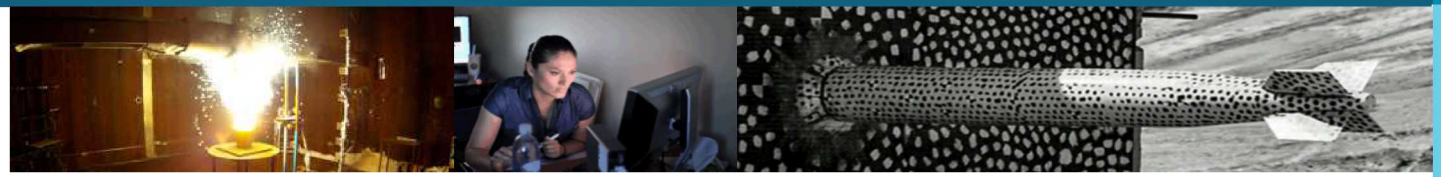
SAND2019-10697PE

Do this!



Signal Integrity and Power Integrity Engineering is really done every day here at SNL on a wide variety of PWA products

The tools and expertise to help you put these into your product are available

Engineer your product, then produce the product you engineered!

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Motivation through real SNL examples

Brent Meyer, 2622

844-1880

btmeyer@sandia.gov

About myself

First PWA design circa 1983
- Light table, two mylar sheets, red and blue tape

Hired into SNL 1985
- PWA designs for flight computers
- Electrical design usually solid, physical design about 50/50

Moved to the MDL in 1990
- ASIC designs for a broad range of products

Back to PWA design in 2007
- Brought rigorous design approach from 17 years in the MDL
- Took this same class the first few months
- Began engineering the entire product
  - Physical design as well as electrical design
- Delivered perhaps 60 PWAs over the years
- Electrical design usually solid, physical design almost 100%
  - Physical implementation still provides opportunities for humility

Signal Integrity Examples

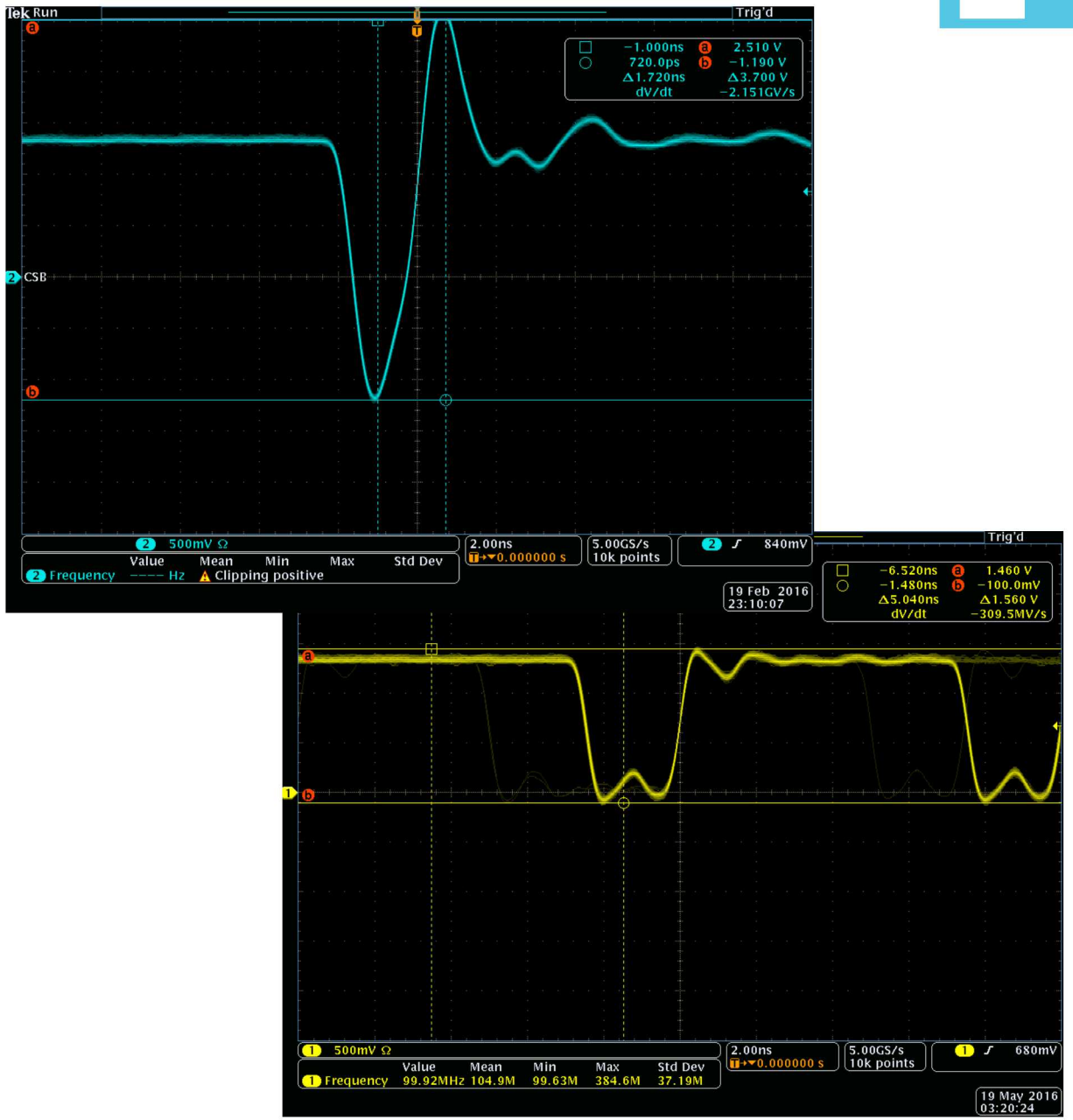
2.5 MHz, 1.8 V, transmit data clock

- Top picture was implemented without paying attention to length or terminations
- Bottom picture was with a source termination
- Both interfaces worked during initial functional evaluation
- But the top design was headed for trouble at some point
- Had to go looking with a scope to find the design oversight!!!

Signal Integrity Examples

DDR3L Chip Select signal

- Both designs were engineered with a 40 ohm source termination on a 40 ohm trace
- The top design was constrained with a 50 ohm trace contrary to specification
- The bottom design was with a 40 ohm trace as specified
- Both interfaces worked during initial functional evaluation
- The top design was headed for trouble…
- Had to go looking with a scope to find the constraint error!!!



Signal Integrity Examples

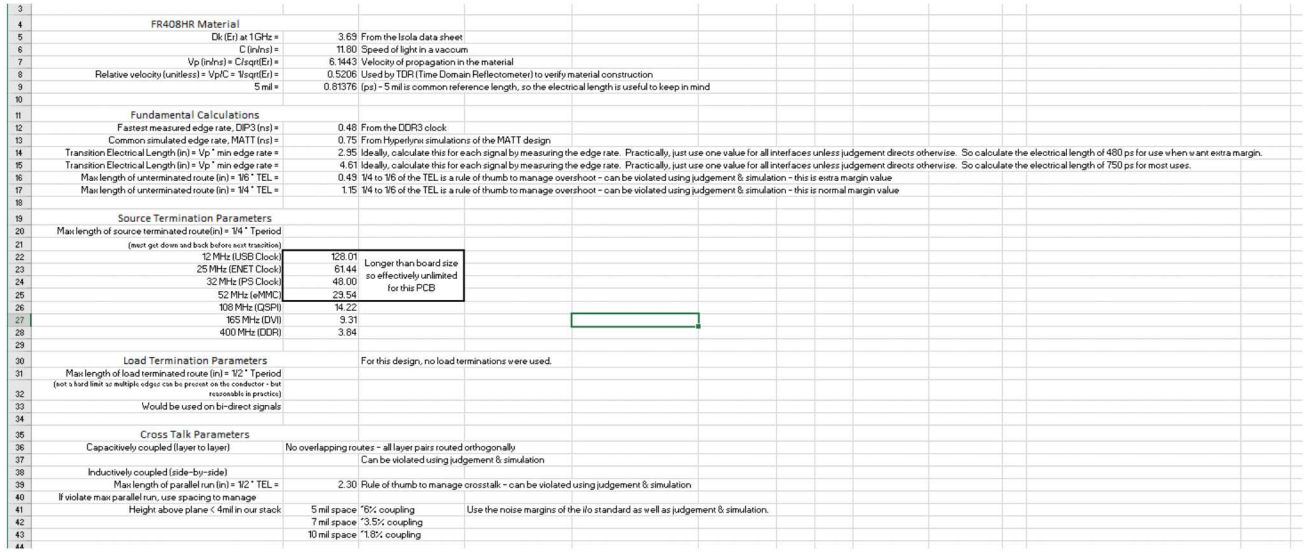
A quick point about doing signal integrity verification with an o-scope

- Both traces are the same 32 MHz, 1.8 V clock signal
- The top trace is with a 1 GHz passive probe
- The bottom trace is with a 2.5 GHz active probe
- Make sure you are using the correct equipment – signal integrity is about the edge rates and you must see the edges!

Signal Integrity Design Tools

Can just use Excel (or even paper & pencil)

- Define basic parameters and guidelines for the product
- Determine edge rates for the various electrical groups
- Calculate the trace lengths at which networks need SI Engineering
- Using these guidelines, create schematic or routing requirements
  - Design terminations for nets that are known to be “long”
  - Define max routing length for unterminated nets

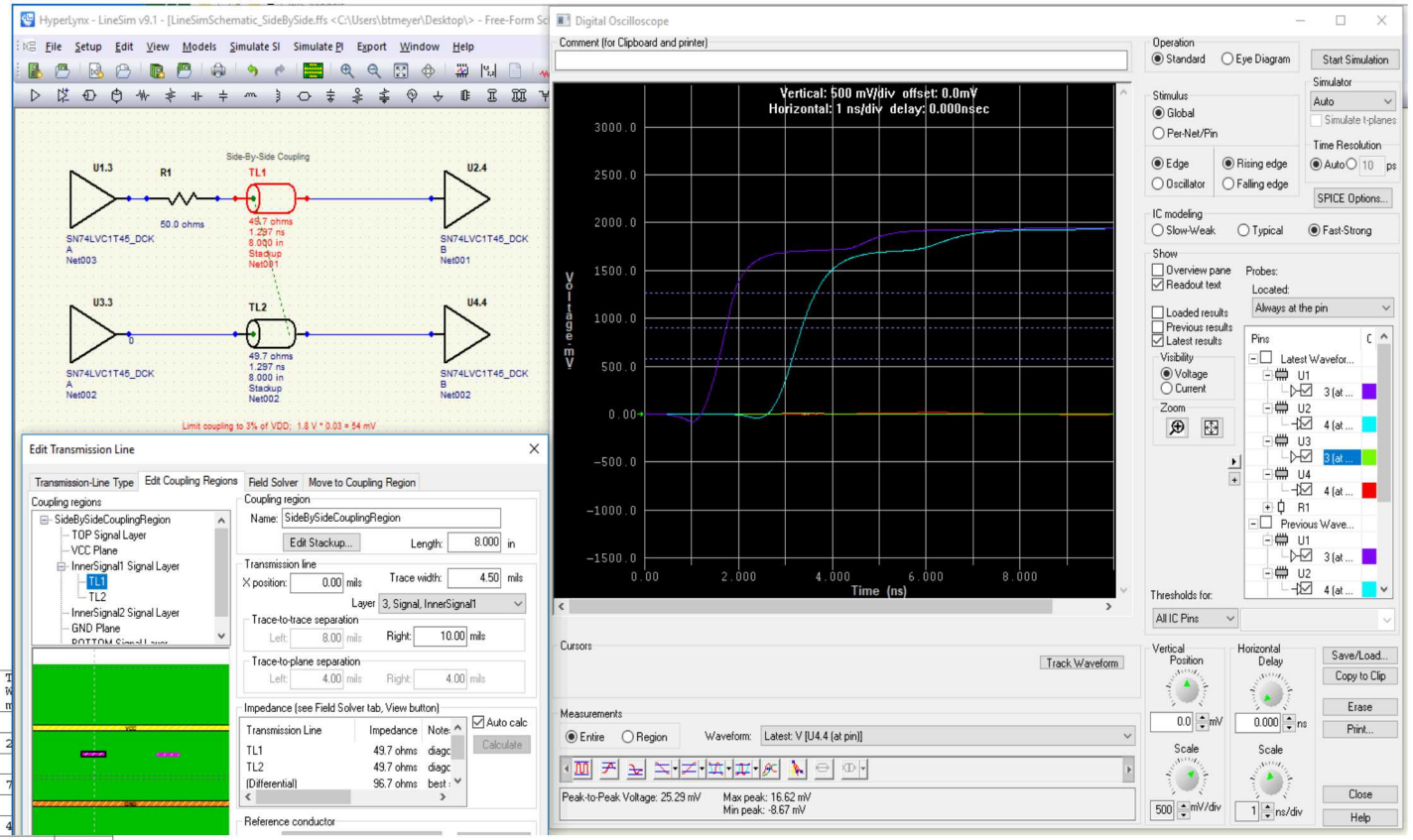


	FR408HR Material			
	Dk (Er) at 1 GHz =	3.69	From the Isola data sheet	
	C (in/ns) =	11.80	Speed of light in a vacuum	
	Vp (in/ns) = C/sqrt(Er) =	6.1443	Velocity of propagation in the material	
	Relative velocity (unitless) = Vp/C = 1/sqrt(Er) =	0.5206	Used by TDR (Time Domain Reflectometer) to verify material construction	
	5 mil =	0.81376	(ps) – 5 mil is common reference length, so the electrical length is useful to keep in mind	
	Fundamental Calculations			
	Fastest measured edge rate, DIP3 (ns) =	0.48	From the DDR3 clock	
	Common simulated edge rate, MATT (ns) =	0.75	From Hyperlynx simulations of the MATT design	
	Transition Electrical Length (in) = Vp * min edge rate =	2.95	Ideally, calculate this for each signal by measuring the edge rate. Practically, just use one value for all interfaces unless judgement directs otherwise. So calculate the electrical length of 480 ps for use when want extra margin.	
	Transition Electrical Length (in) = Vp * min edge rate =	4.61	Ideally, calculate this for each signal by measuring the edge rate. Practically, just use one value for all interfaces unless judgement directs otherwise. So calculate the electrical length of 750 ps for most uses.	
	Max length of unterminated route (in) = 1/6 * TEL =	0.49	1/4 to 1/6 of the TEL is a rule of thumb to manage overshoot – can be violated using judgement & simulation – this is extra margin value	
	Max length of unterminated route (in) = 1/4 * TEL =	1.15	1/4 to 1/6 of the TEL is a rule of thumb to manage overshoot – can be violated using judgement & simulation – this is normal margin value	
	Source Termination Parameters			
	Max length of source terminated route(in) = 1/4 * Tperiod			
	(must get down and back before next transition)			
	12 MHz (USB Clock)	128.01	Longer than board size so effectively unlimited for this PCB	
	25 MHz (ENET Clock)	61.44		
	32 MHz (PS Clock)	48.00		
	52 MHz (eMMC)	29.54		
	108 MHz (QSPI)	14.22		
	165 MHz (DVI)	9.31		
	400 MHz (DDR)	3.84		
	Load Termination Parameters		For this design, no load terminations were used.	
	Max length of load terminated route (in) = 1/2 * Tperiod			
	(not a hard limit as multiple edges can be present on the conductor - but reasonable in practice)			
	Would be used on bi-direct signals			
	Cross Talk Parameters			
	Capacitively coupled (layer to layer)	No overlapping routes – all layer pairs routed orthogonally		
			Can be violated using judgement & simulation	
	Inductively coupled (side-by-side)			
	Max length of parallel run (in) = 1/2 * TEL =	2.30	Rule of thumb to manage crosstalk – can be violated using judgement & simulation	
	If violate max parallel run, use spacing to manage			
	Height above plane < 4mil in our stack	5 mil space	~6% coupling	Use the noise margins of the i/o standard as well as judgement & simulation.
		7 mil space	~3.5% coupling	
		10 mil space	~1.8% coupling	

Signal Integrity Design Tools

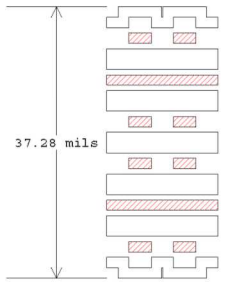
Hyperlynx SI from MGC is available through the ECAD group

- Pre-layout exploration
  - Model drivers, loads, termination options
  - Develop model based requirements



Layer Stackup. Design: Untitled.ffs, Designer: Meyer, Brent T.

Number of layers: 13
Total thickness = 37.28 mils

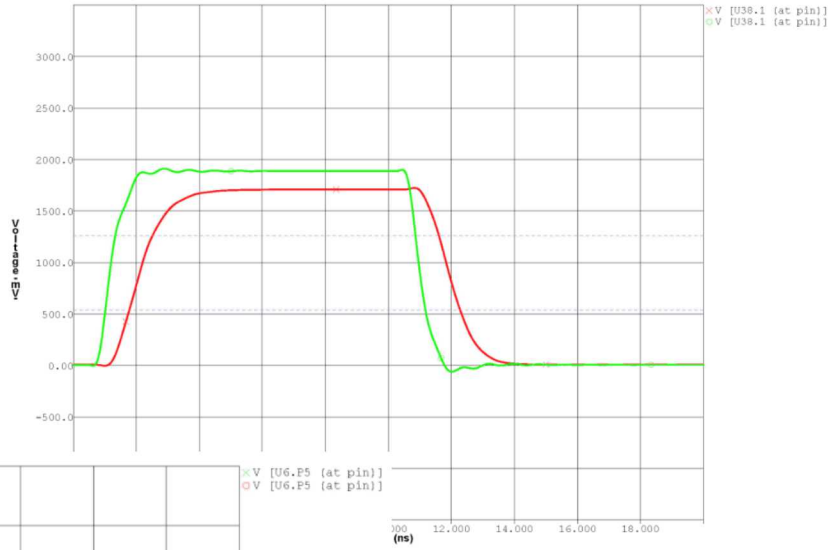


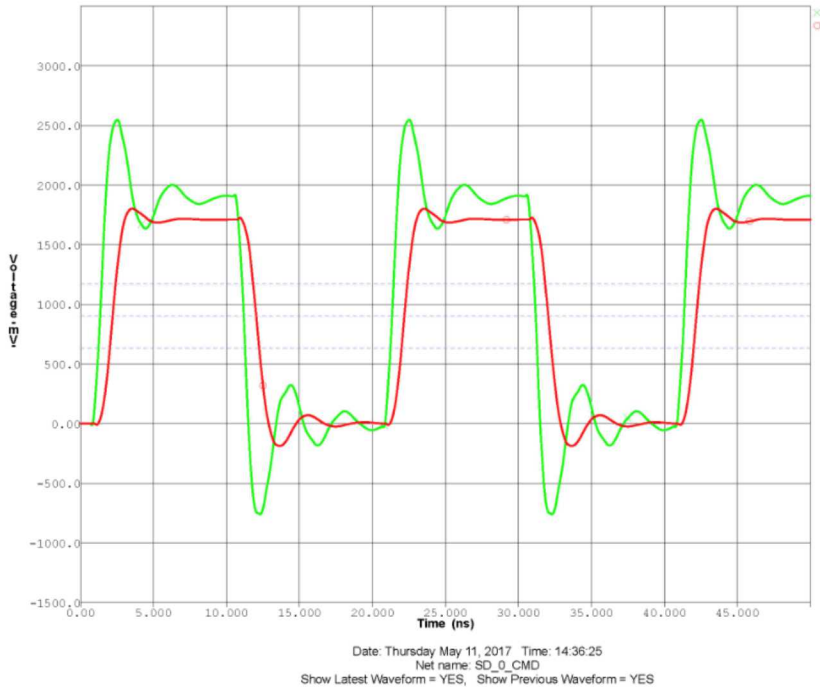
NN	Layer Name	Type	Usage	Thickness mils, oz	Technology	Er	Metal		
1		Dielectric	Solder Mask	0.5		3.3			
2	TOP	Metal	Signal	0.5		<Auto>	Copper		
3		Dielectric	Substrate	10	Prepreg	3.61			
4	VCC	Metal	Plane	1		<Auto>	Copper		
5		Dielectric	Substrate	3.69	Prepreg	3.61			
6	InnerSignal1	Metal	Signal	0.5		<Auto>	Copper		
7		Dielectric	Substrate	3.5	Core	3.77			
8	InnerSignal2	Metal	Signal	0.5		<Auto>	Copper	4.5	49.7
9		Dielectric	Substrate	3.69	Prepreg	3.61			
10	GND	Metal	Plane	1		<Auto>	Copper	7	50.5
11		Dielectric	Substrate	10	Prepreg	3.61			
12	BOTTOM	Metal	Signal	0.5		<Auto>	Copper	20	51.3
13		Dielectric	Solder Mask	0.5		3.3			

Signal Integrity Design Tools

Hyperlynx SI Post-layout Verification

- Export actual layout data from MGC Expedition or other tools
- Import into Hyperlynx
- Setup / verify stack-up information
- Select nets for analysis
- Select conditions for analysis
- Run simulation

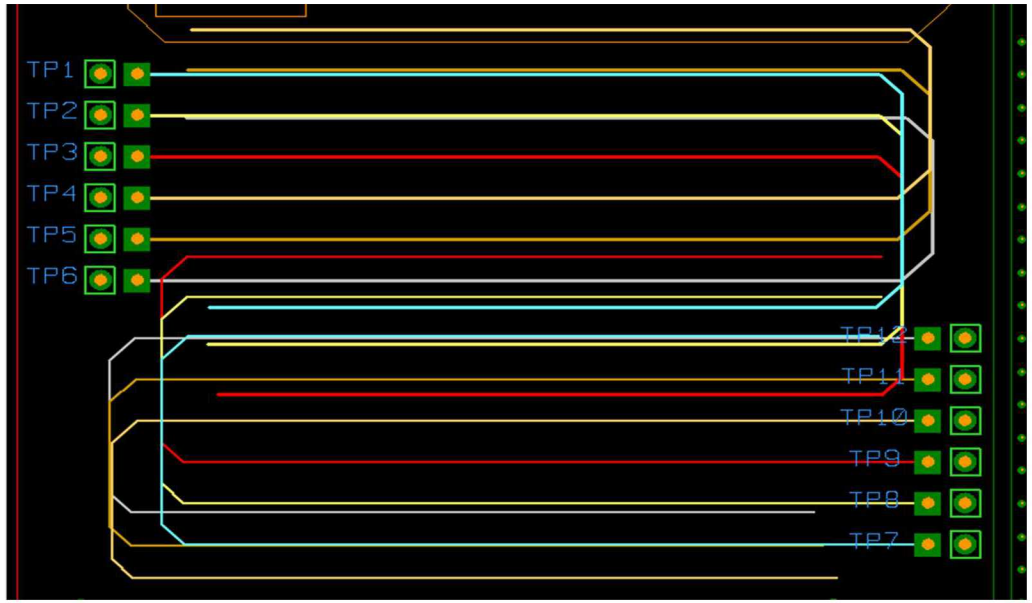


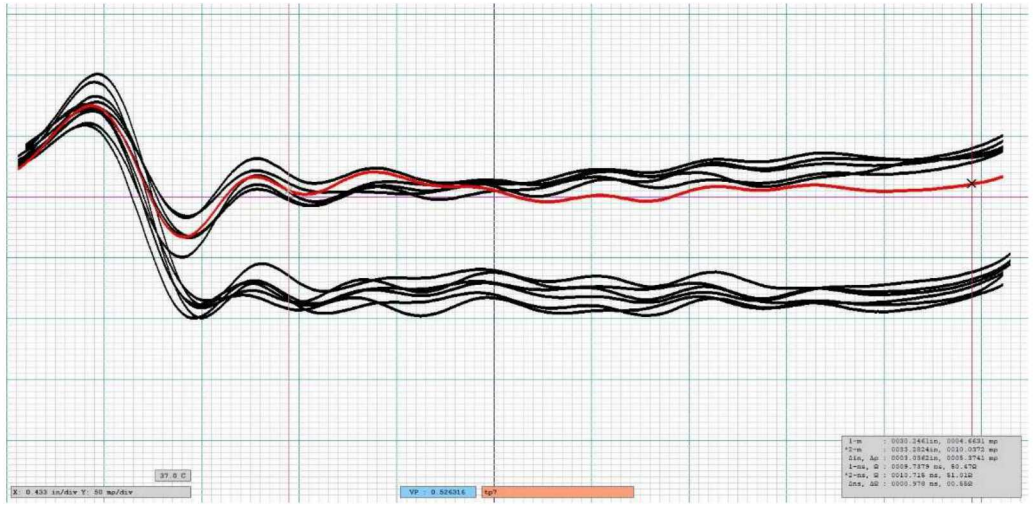


Signal Integrity Implementation Checks

Impedance test traces allow verification prior to committing expensive BOM to assembly

- On-board traces designed into open routing area on product
- Six routing layers with 50 ohm and 40 ohm traces on each
- Use a TDR to check the impedance

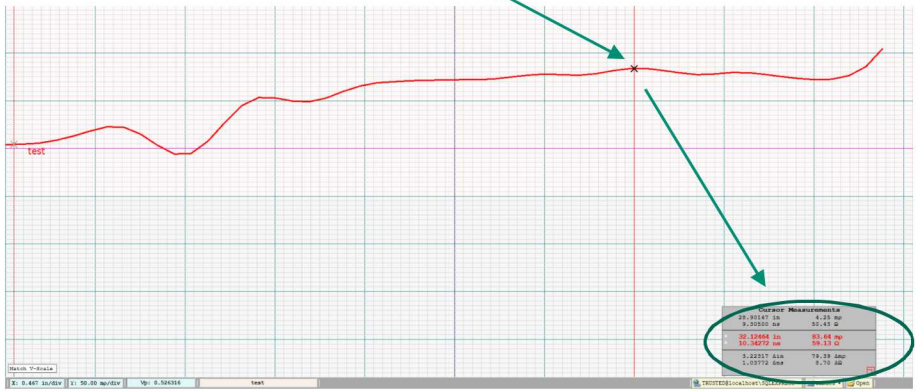




Signal Integrity Implementation Checks

- Vendor designed coupons used to report/certify trace impedance is correct
- TDR report from vendor looks fine
- SNL designed coupons added to the panel just to be sure…
- TDR report from SNL coupon looks bad
  - Notice their coupon is rigid only whereas the SNL coupon is rigid flex…
  - The vendor compensated the entire product based on their rigid data

Layer	Job Number	Serial	Average	Min Z	Max Z	Result	Op..
L4 50	1212517 1.00	03	53.26	51.23	54.16	Pass	FO
L5 50	1212517 1.00	03	51.92	49.89	53.16	Pass	FO
L4 FLEX 50	1212517 1.00	03	53.96	51.64	54.86	Pass	FO
L5 FLEX 50	1212517 1.00	03	52.49	50.17	53.94	Pass	FO
L4 50	1212517 1.00	01	51.37	49.39	52.31	Pass	FO
L5 50	1212517 1.00	01	53.30	50.70	54.64	Pass	FO
L4 FLEX 50	1212517 1.00	01	51.51	49.47	52.40	Pass	FO
L5 FLEX 50	1212517 1.00	01	51.34	45.04	53.33	Pass	FO
L4 50	1212517 1.00	04	51.83	49.80	53.29	Pass	FO
L5 50	1212517 1.00	04	51.47	50.09	52.74	Pass	FO
L4 FLEX 50	1212517 1.00	04	49.33	47.36	50.94	Pass	FO
L5 FLEX 50	1212517 1.00	04	46.11	43.02	48.00	Pass	FO



Power Integrity Examples

Original 10 layer design

- Used plane pairs for both supplies
- But very small board (~2” x 4”)
- High current drivers placed ‘far’ from regulators

Design would upset the FPGA

- Current probe showed where the high current events occurred
- This was able to be correlated with the upsets

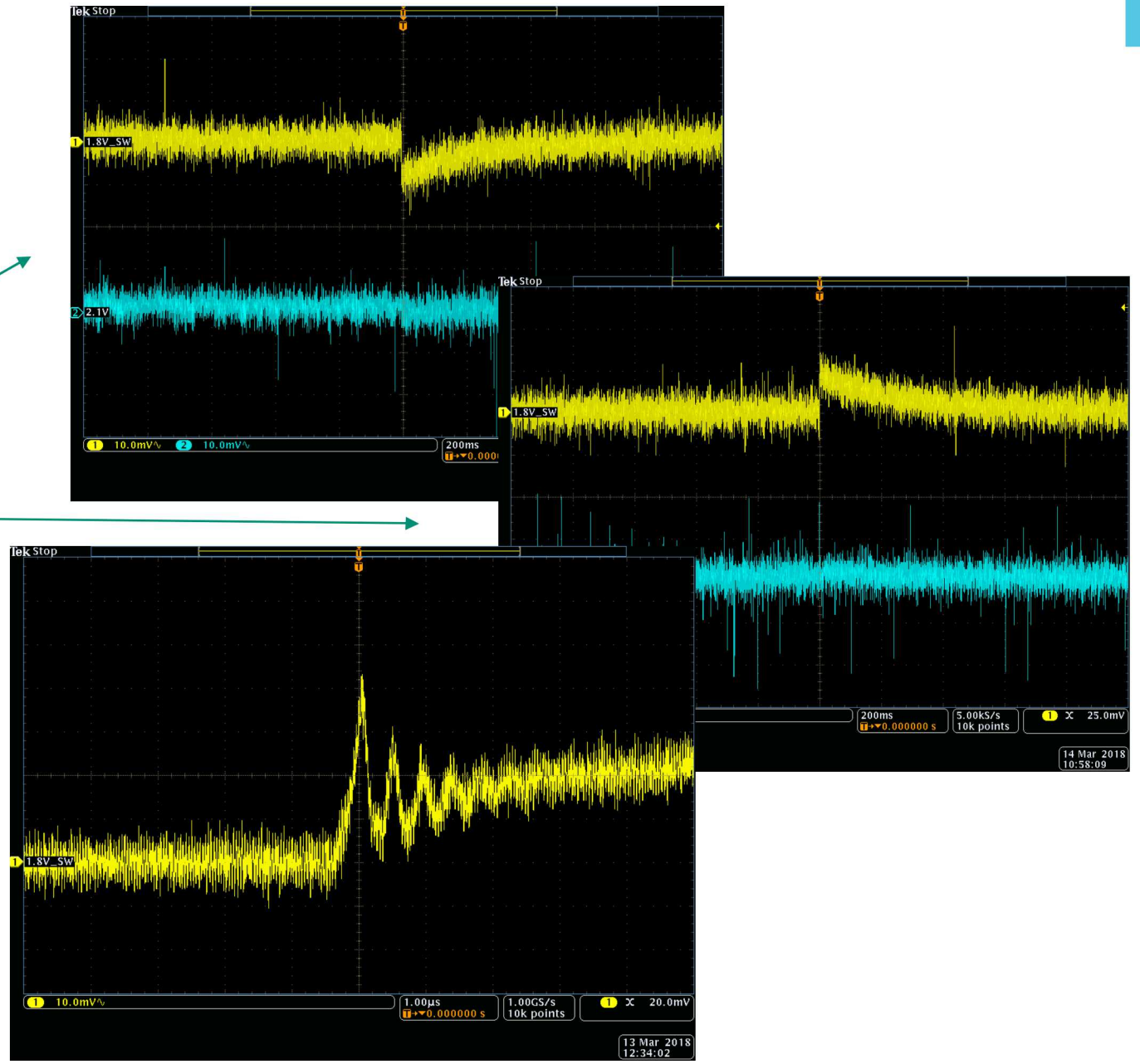
Added additional plane pairs for both supplies

- Now 14 layers
- Also relocated the high current drivers and increased the decoupling
- New design never failed again

Power Integrity Examples

1.8V supply implemented with engineered power integrity

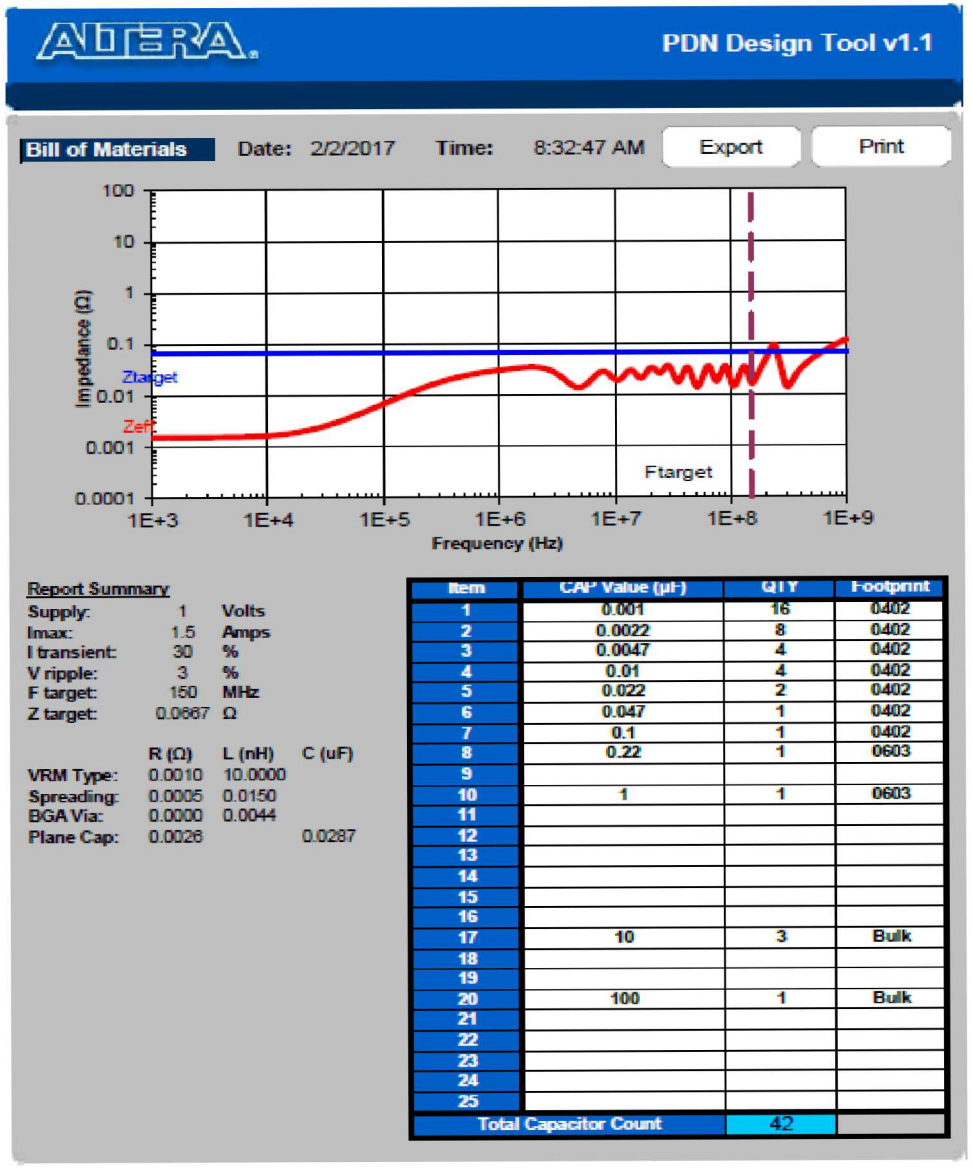
- Switching on a 1 Amp load.
  - Only 10mV on the 1.8V plane
- Switching off a 1 Amp load.
  - Only 10mV on the 1.8V plane
- Zooming in to see the spike:
  - Looks to be ~40mV
  - Could perhaps add some decoupling with response in the 100 – 500 ns range…



Power Integrity Design Tools

Free Excel tool from Altera (now Intel) called PDNtool

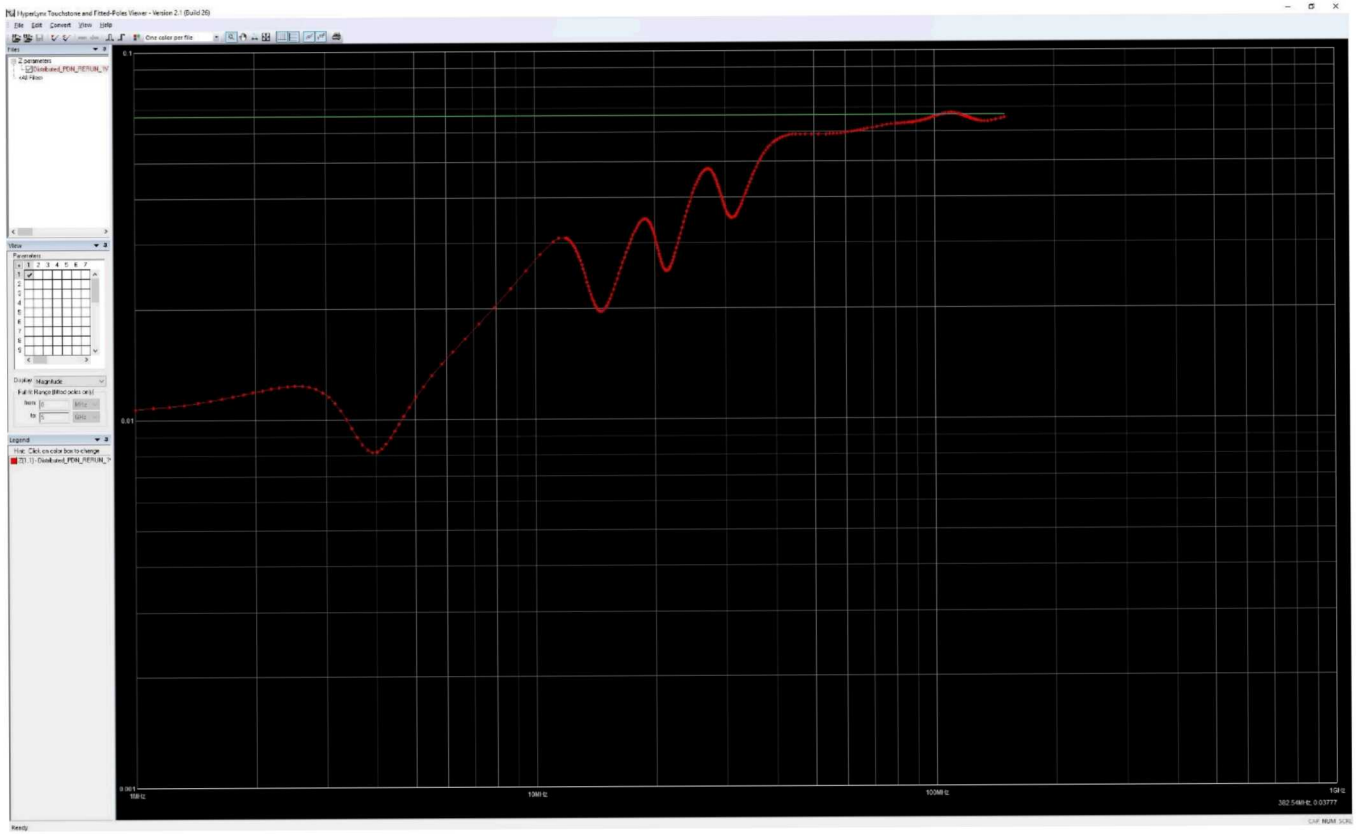
- Pre-layout design tool
- Define the stack-up
- Define the capacitor mounting dimensions
- Define the capacitor parasitic values
- Define the supply characteristics desired
- Select the decoupling capacitor networks required to meet the impedance target



Power Integrity Design Tools

Hyperlynx PI from MGC is available through the ECAD group

- Post-layout design tool
- Model the supply sources
- Model the capacitor parasitic values
- Import the physical design
  - Stack-up
  - Capacitor mounting
- Verify supply impedance

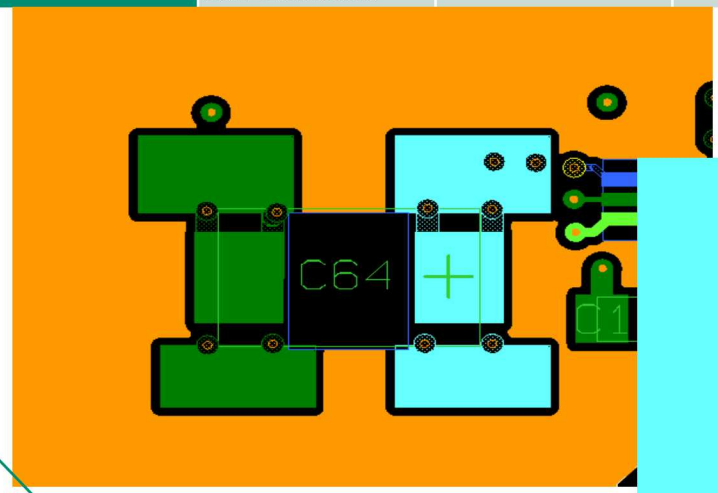


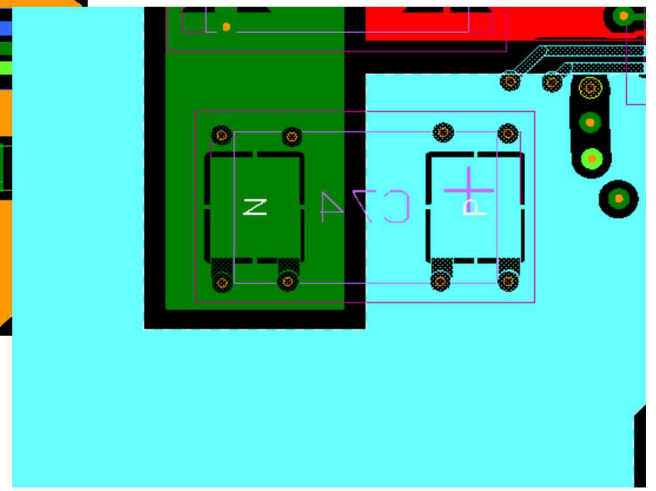
Power Integrity Design Tools

Hyperlynx PI can perform many other post-layout design checks

- Capacitor mounting errors
  - C64 was on the wrong side of the board
  - should have been placed with C74
  - several capacitors shared vias

Capacitor	Model	Value, uF	Mounting Quality	Total Mounting Inductance, nH
C64	C=10uF, ESL=Auto, ESR=25mOhms	10	marginal	2.65
C75	C=10uF, ESL=Auto, ESR=25mOhms	10	marginal	2.29
C91	C=10uF, ESL=Auto, ESR=25mOhms	10	marginal	2.12
C109	C=10uF, ESL=Auto, ESR=25mOhms	10	marginal	2.06
C74	C=10uF, ESL=Auto, ESR=25mOhms	10	good	1.71



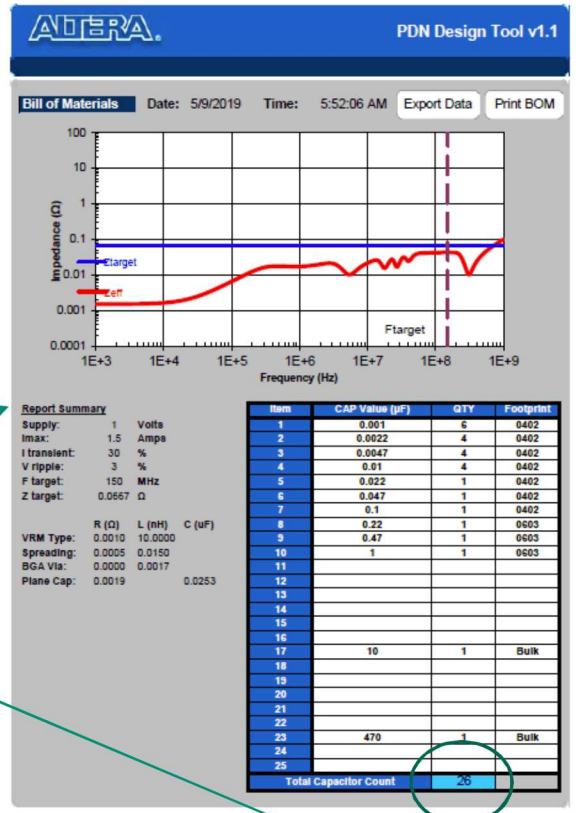


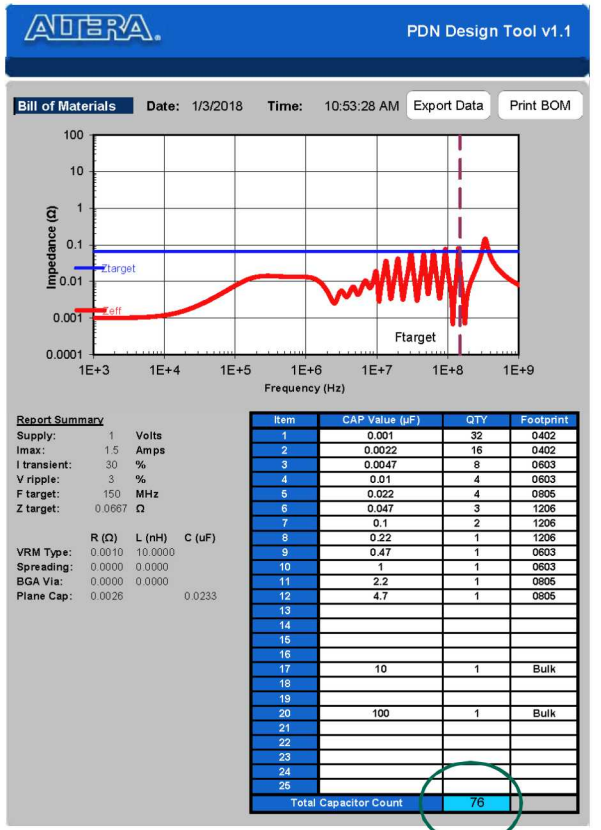
Capacitor	Model	Value, uF	Mounting Quality	Total Mounting Inductance, nH	Estimated ESL, nH	Actual Resonance Frequency, MHz	Resonant Frequency for User-Specified ESL (w/o Mounting), MHz	Comments
C2	C=0.0022uF,	0.0022	good	0.55	0.16	144.75	N/A	Mounting shared with other capacitors
C3	C=0.0022uF,	0.0022	good	0.42	0.16	165.44	N/A	Mounting shared with other capacitors
C45	C=0.001uF,	0.001	good	0.34	0.16	271.01	N/A	Mounting shared with other capacitors

A few notes about capacitors

Understand the effect of different dielectric materials

- Using X7R – standard decoupling design
  - Significant supply chain issues
- Tried using COG
  - No supply chain issues
  - But sharp response required 3x the number of caps
  - It worked well in reality – and procurement was a breeze - but the cost was very high



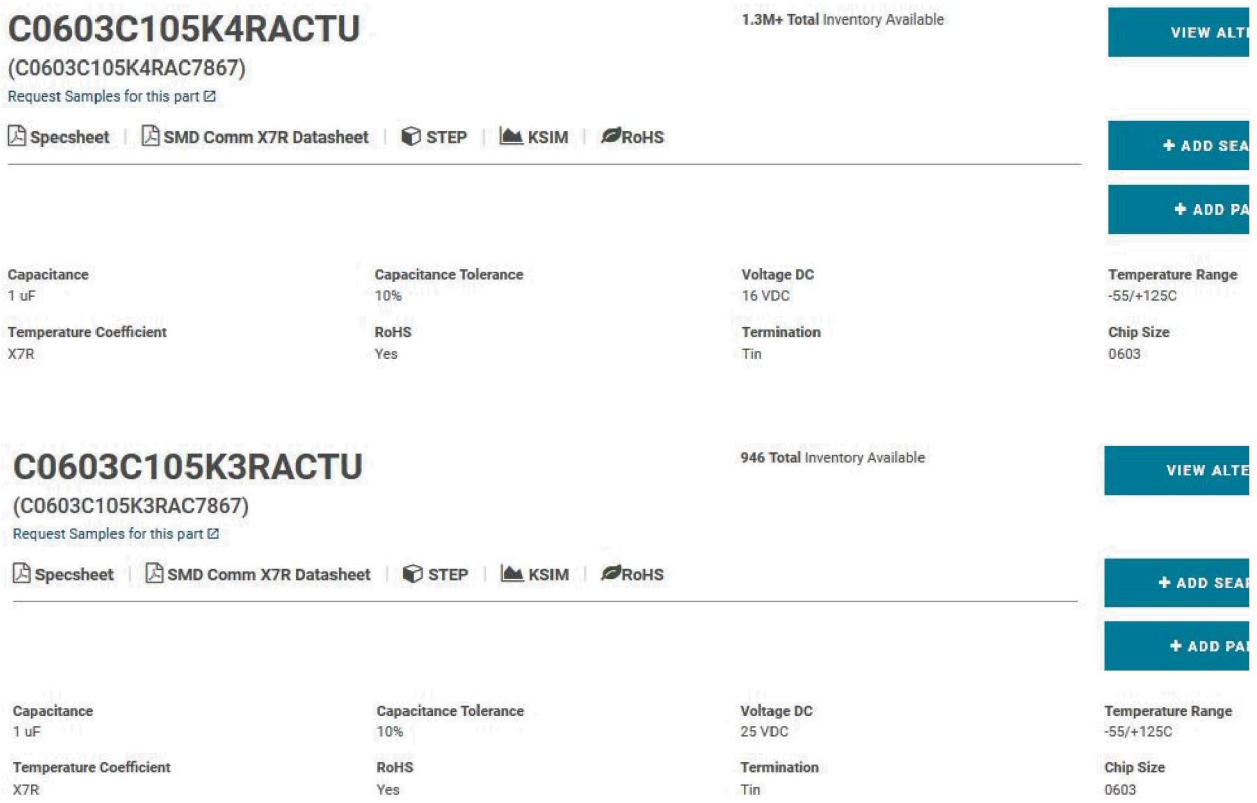


A few notes about capacitors

Understand the effect of Vbias derating for all Class II MLCC

- The top capacitor is on the BOM, but is not available
- The bottom capacitor is in stock at the distributor

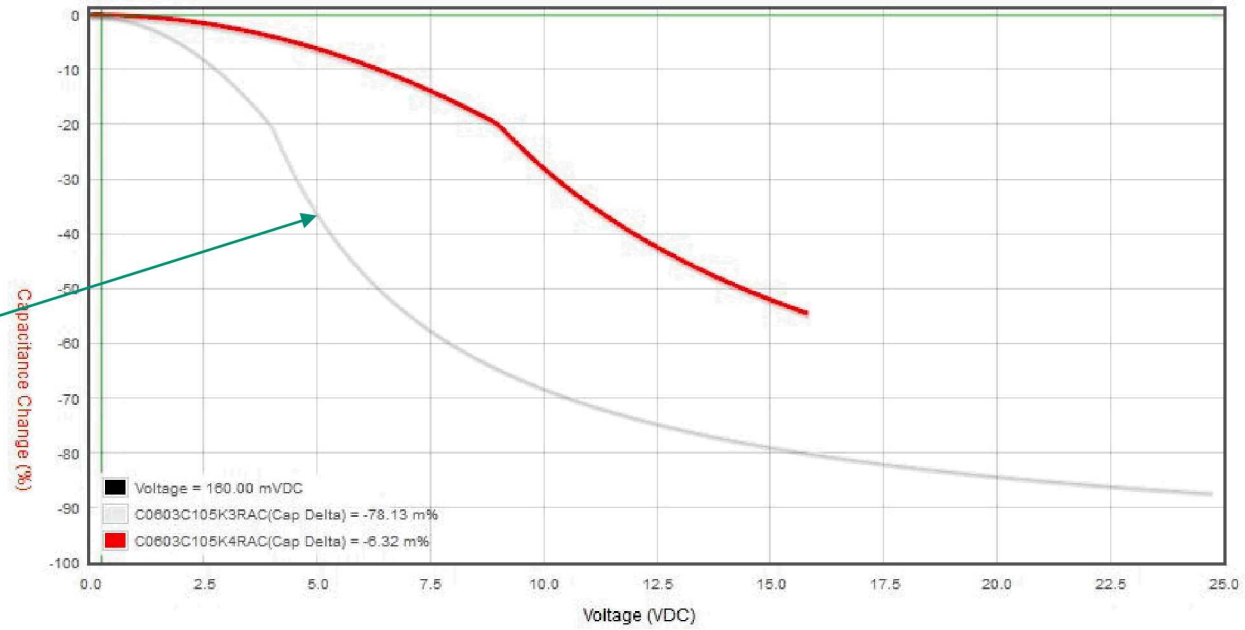
- Can we make this substitution?



A few notes about capacitors

Vbias derating is not included in the part definition

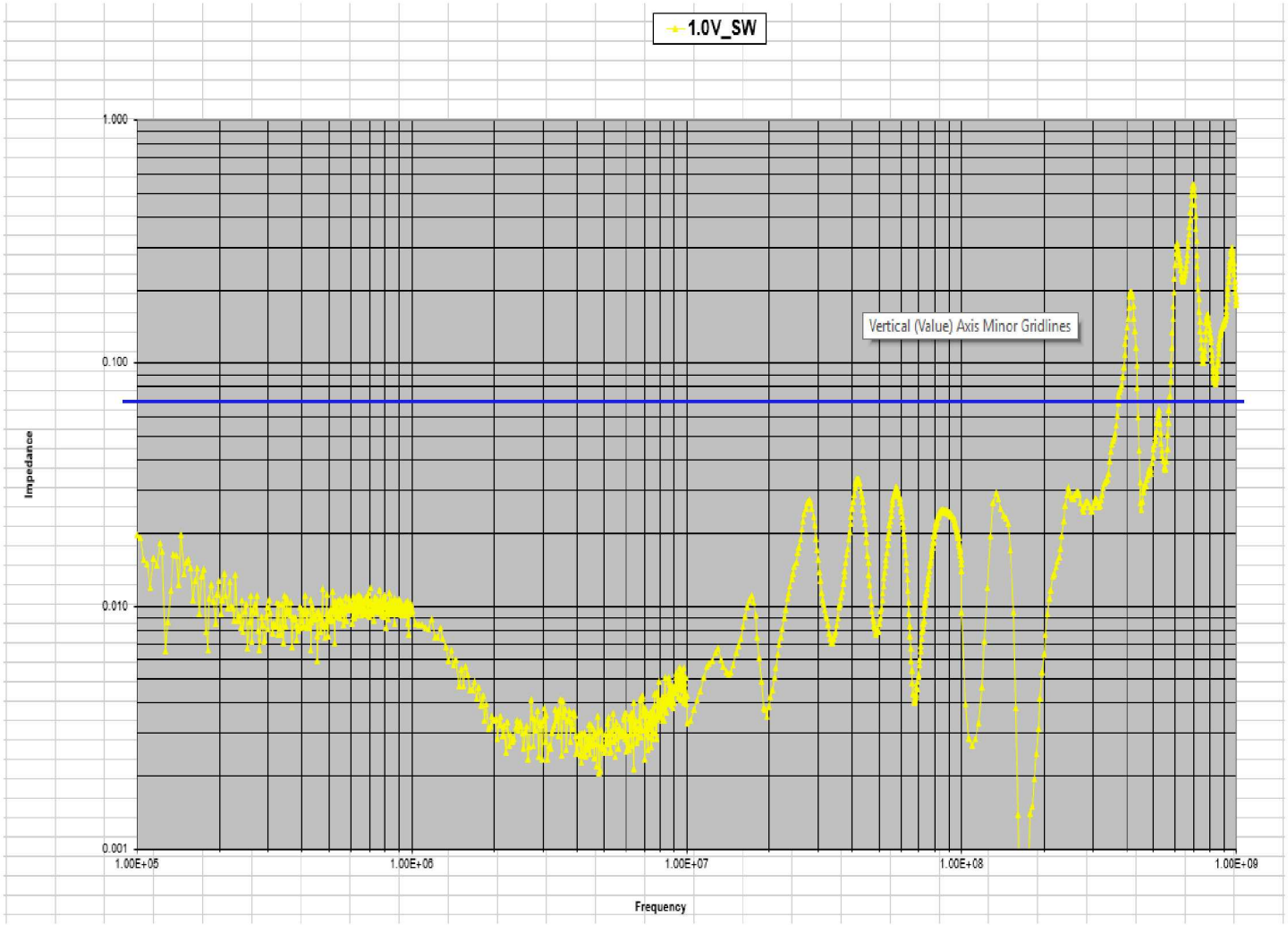
- Only available from the vendor data sheets or web-tools
- Top (red) trace is the 16 V part
- Bottom (grey) trace is the 25 V part
  - At 5 V, the capacitance is -36%!
  - Clearly not a good substitute



Power Integrity Implementation Checks

Use a Spectrum Analyzer to verify the supply impedance after fabrication and assembly

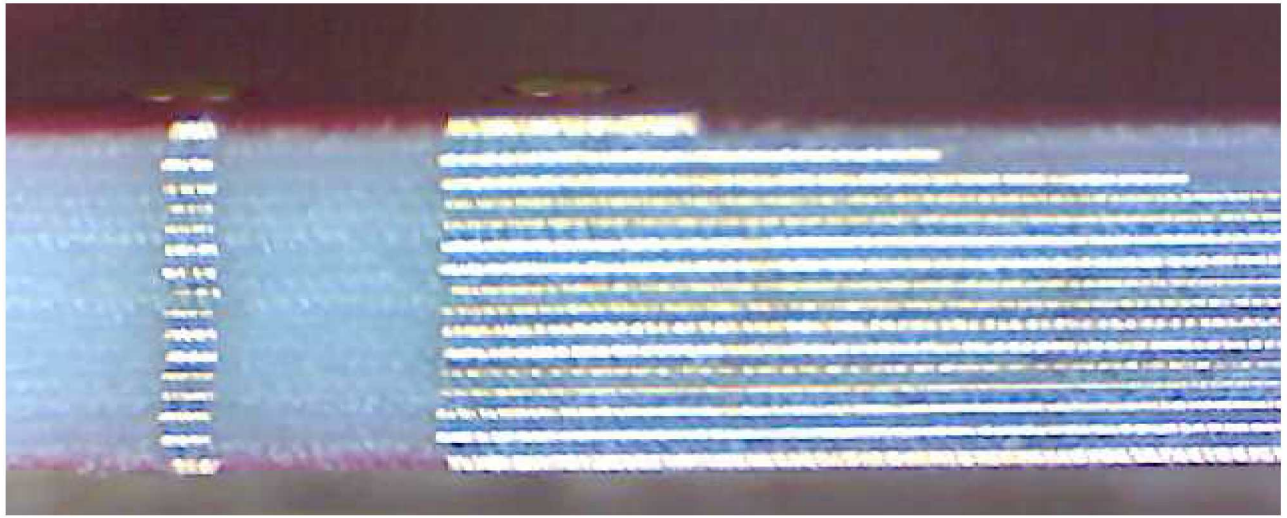
- Can find gross implementation errors (incorrect caps) before you spend days debugging a flakey board

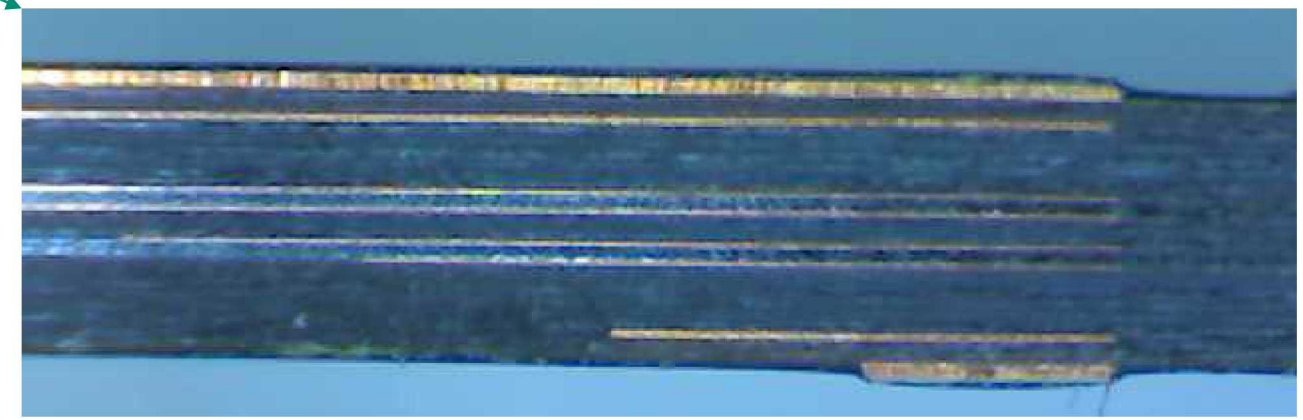


Power Integrity Implementation Checks

Include stacking stripes

- On product itself
- On SNL designed coupon
- Verifies panels are in the correct order
- Gives qualitative verification of copper weight
  - Could even be measured if necessary





Power Integrity Implementation Checks

Actual manufacturing errors have been found

- IPC analysis report confirmed correct construction
- But stacking stripes uncovered an error!
  - One of the cores used by a power plane pair was ½ oz instead of 1 oz
  - Of the PWBs delivered, some were incorrect, some were correct
  - The construction analysis was performed on a good panel…
- Root cause analysis was that an off shift operator was filling in for the kitting operator who was out sick

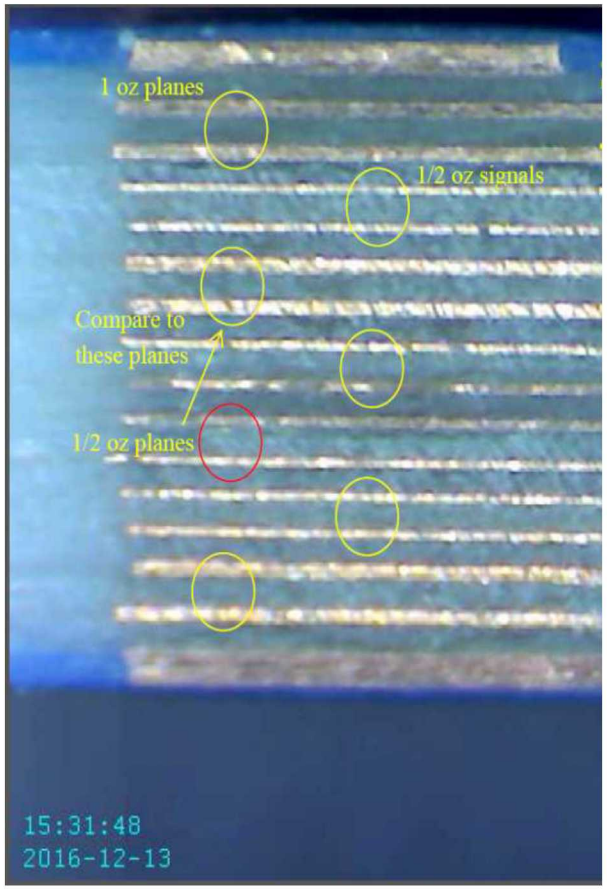
IPC 6012 Report

Dielectric/Conductor Thickness

LAYER	REQUIRED CU FOIL	ACTUAL FOIL + PLT	REQ'D DIELECTRIC	ACTUAL DIELECTRIC
1	0.0004	0.0029		
			0.0038	0.0037
2	0.0012	0.0012		
			0.0035	0.0037
3	0.0012	0.0012		
			0.0034	0.0030
4	0.0006	0.0006		
			0.0035	0.0037
5	0.0006	0.0006		
			0.0035	0.0030
6	0.0012	0.0012		
			0.0035	0.0039
7	0.0012	0.0012		
			0.0034	0.0030
8	0.0006	0.0006		
			0.0035	0.0035
9	0.0006	0.0006		
			0.0034	0.0030
10	0.0012	0.0012		
			0.0035	0.0039
11	0.0012	0.0012		
			0.0035	0.0030
12	0.0006	0.0006		
			0.0035	0.0036
13	0.0006	0.0006		
			0.0034	0.0030
14	0.0012	0.0012		
			0.0035	0.0034
15	0.0012	0.0012		
			0.0038	0.0036
16	0.0004	0.0026		
17				
18				
19				
20				
21				
22				

OVERALL THICKNESS: 0.0697
SPECIFIED THICKNESS: .0720+/-.0070

Date: 10/29/16



Do this!

The engineering rigor Mr. Ritchey is teaching really does matter

SNL has what you need to implement this rigor on every product

Engineer your product, then produce the product you engineered!