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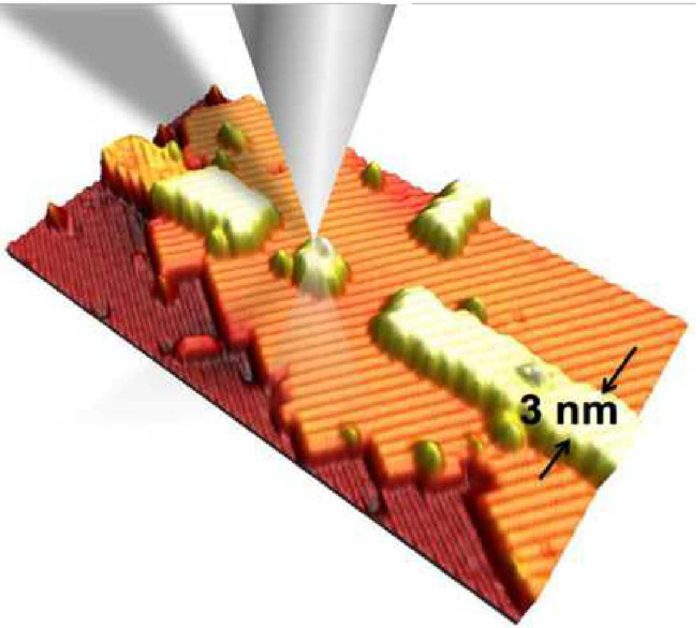

Atomic precision advanced manufacturing for digital electronics

Shashank Misra

U.S. DEPARTMENT OF ENERGY
NNSA National Nuclear Security Administration

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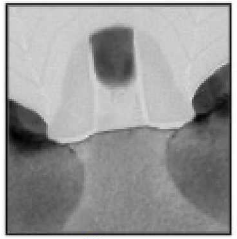
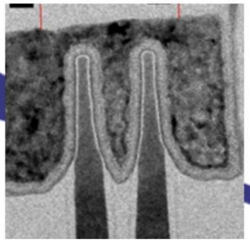
What if you could make devices atom-by-atom?

Tooling cost of successive generations climbs exponentially.



65 nm



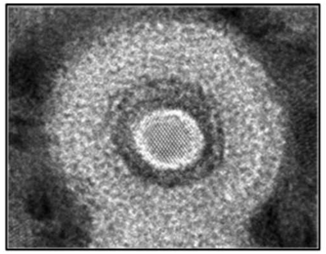
10 nm

Top-down fabrication

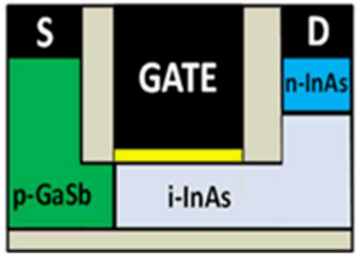
5-7 nm

Atomic Limit

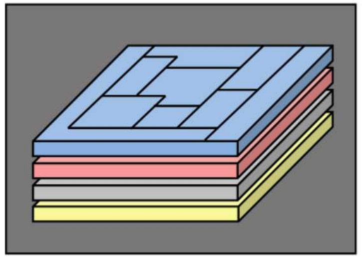
Relax manufacturability – explore opportunities in microelectronics at the atomic limit now



Nanowire Transistors

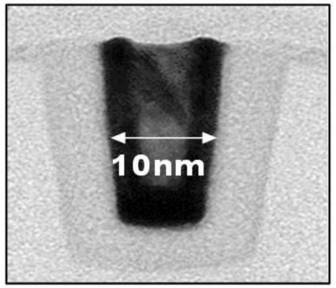


III-V Transistors

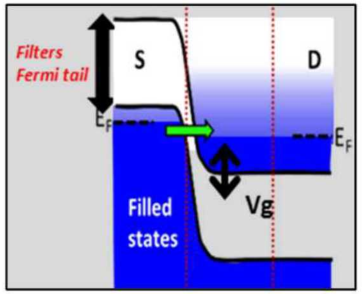


3D Stacking

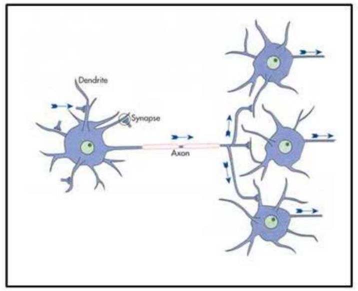
Mark Bohr, Intel 2018



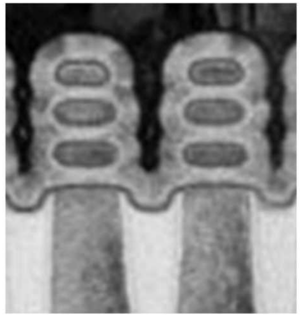
Dense Interconnects



Tunnel FETs

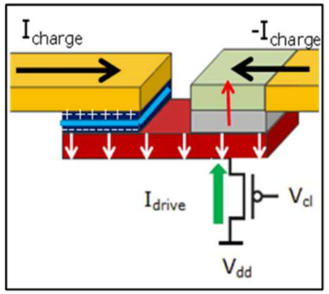


Neuromorphic Computing

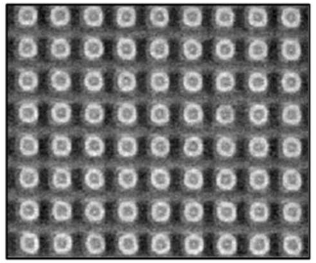


Nanosheets

Huiming Bu, IBM 2017

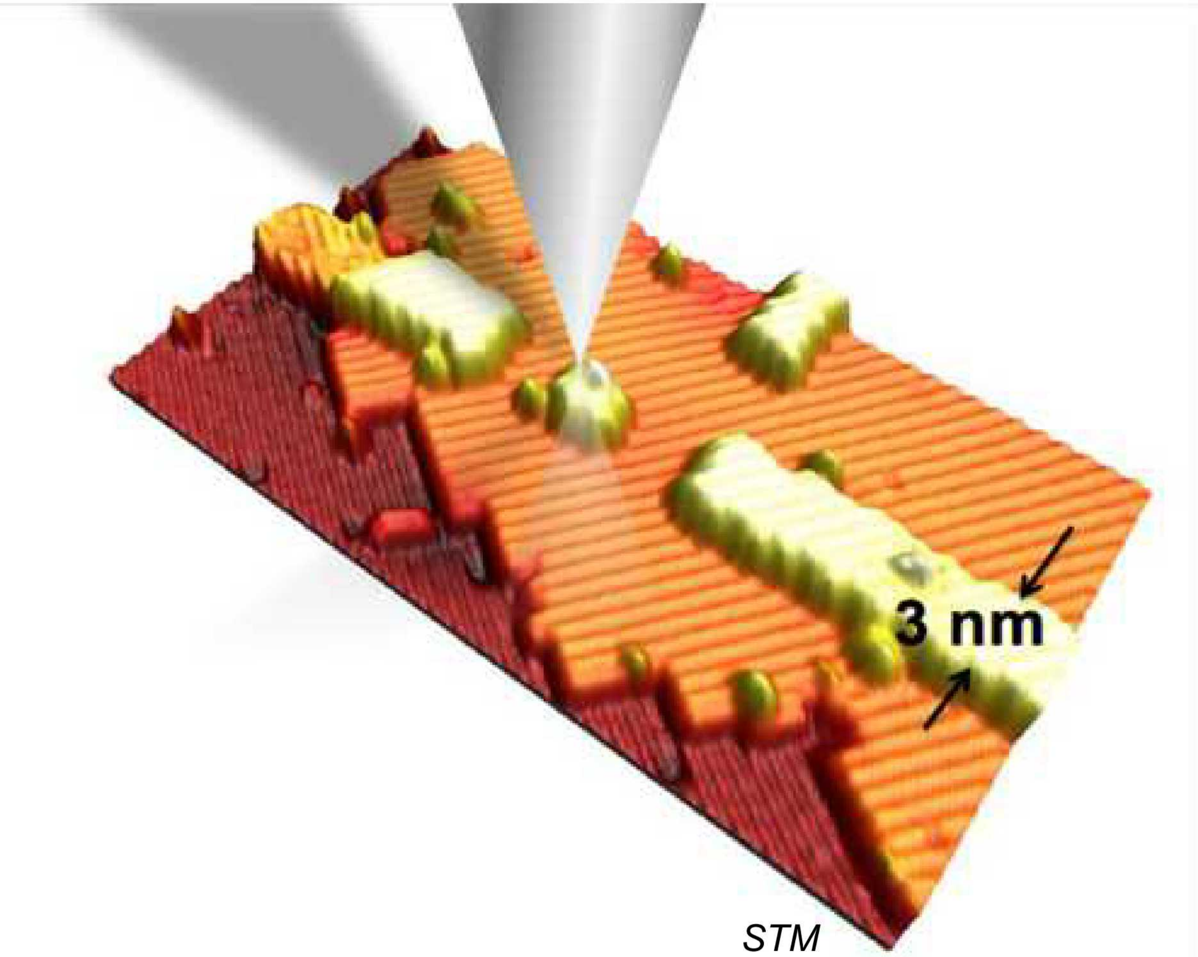


Spintronics



Dense Memory

Atomic Precision Advanced Manufacturing (APAM)



STM

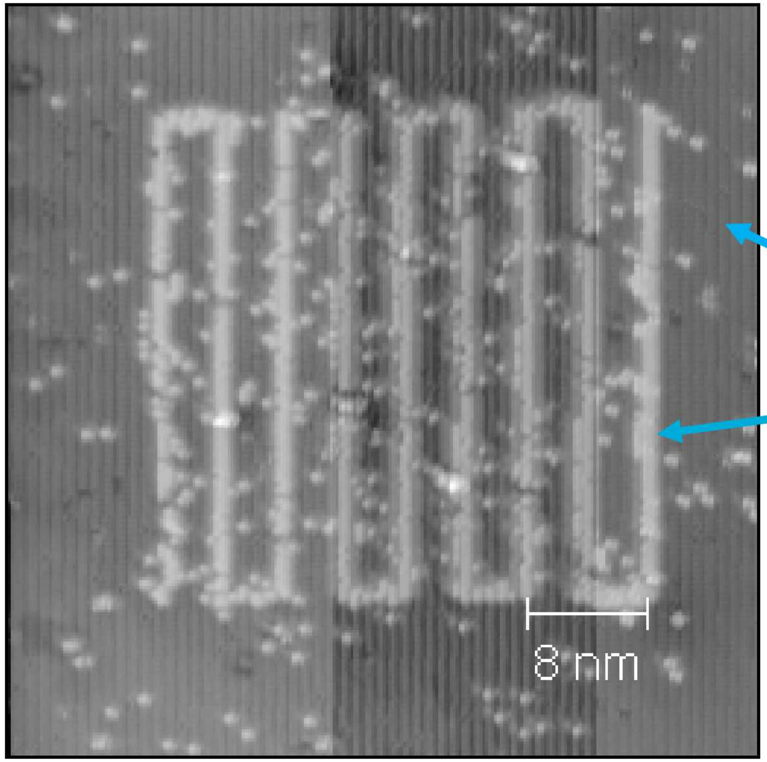
Idea: There is an unexplored opportunity to selectively incorporate molecules into chemically active parts of the silicon surface to explore the device-level microelectronics of the future

FAIR DEAL Grand Challenge

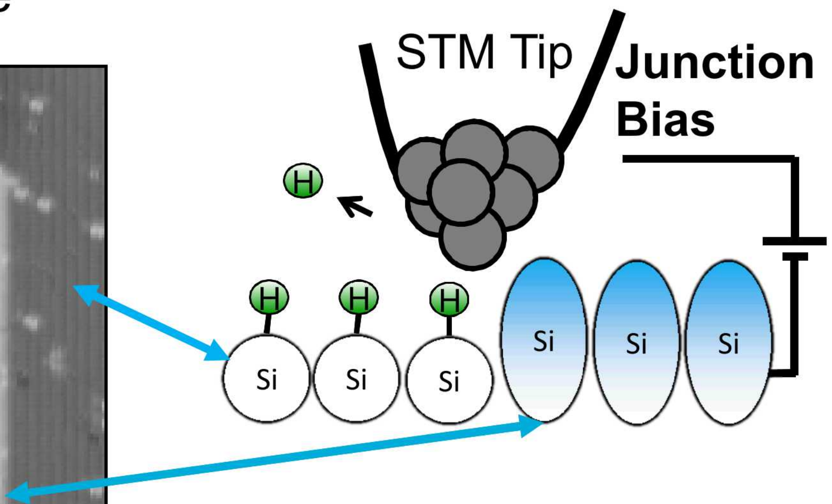
How does APAM work?

“Chemical contrast” at Si surface

- Unterminated Si: 1 reactive bond/ atom
- H-terminated Si: unreactive



STM

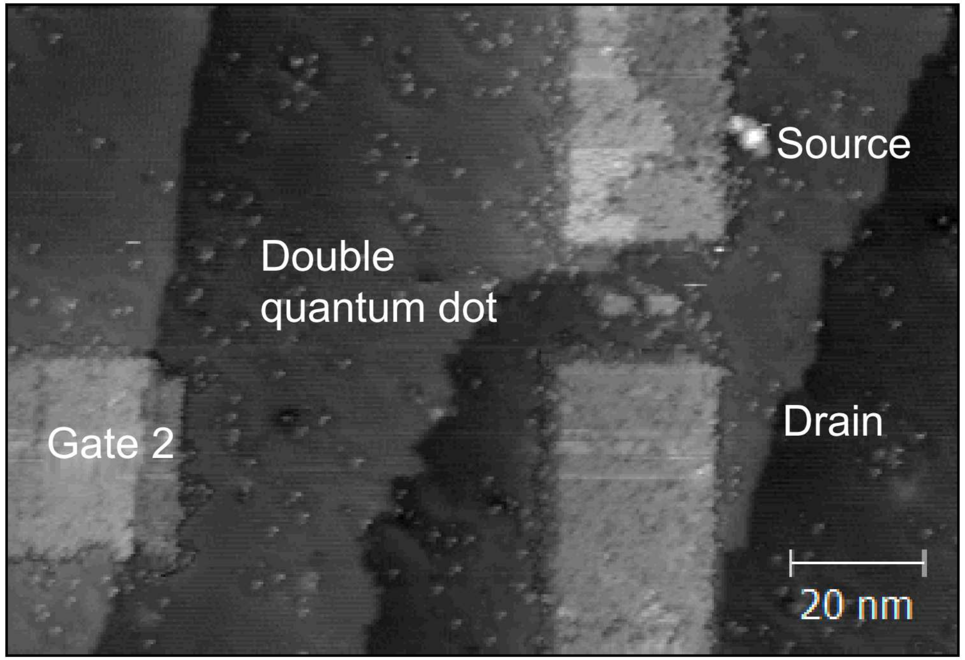


Key properties (vs. standard processing)

1. Atomic precision
2. Resist cannot be over-exposed

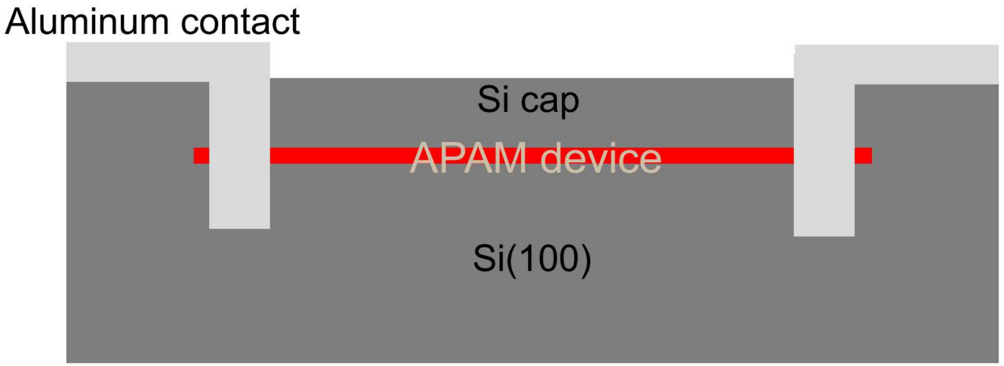
Phosphine precursor used to produce donor-based devices

Top view

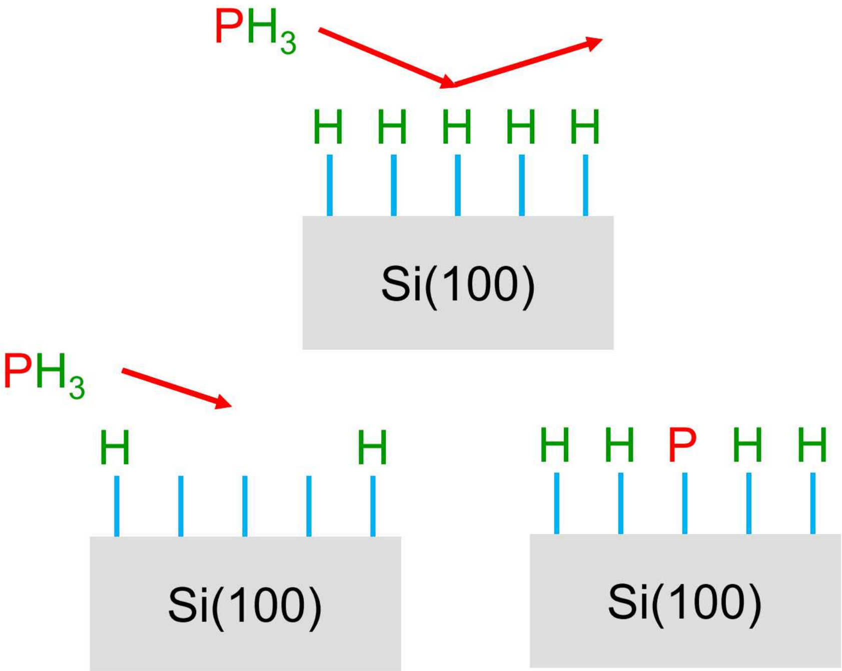


STM

Cross-section



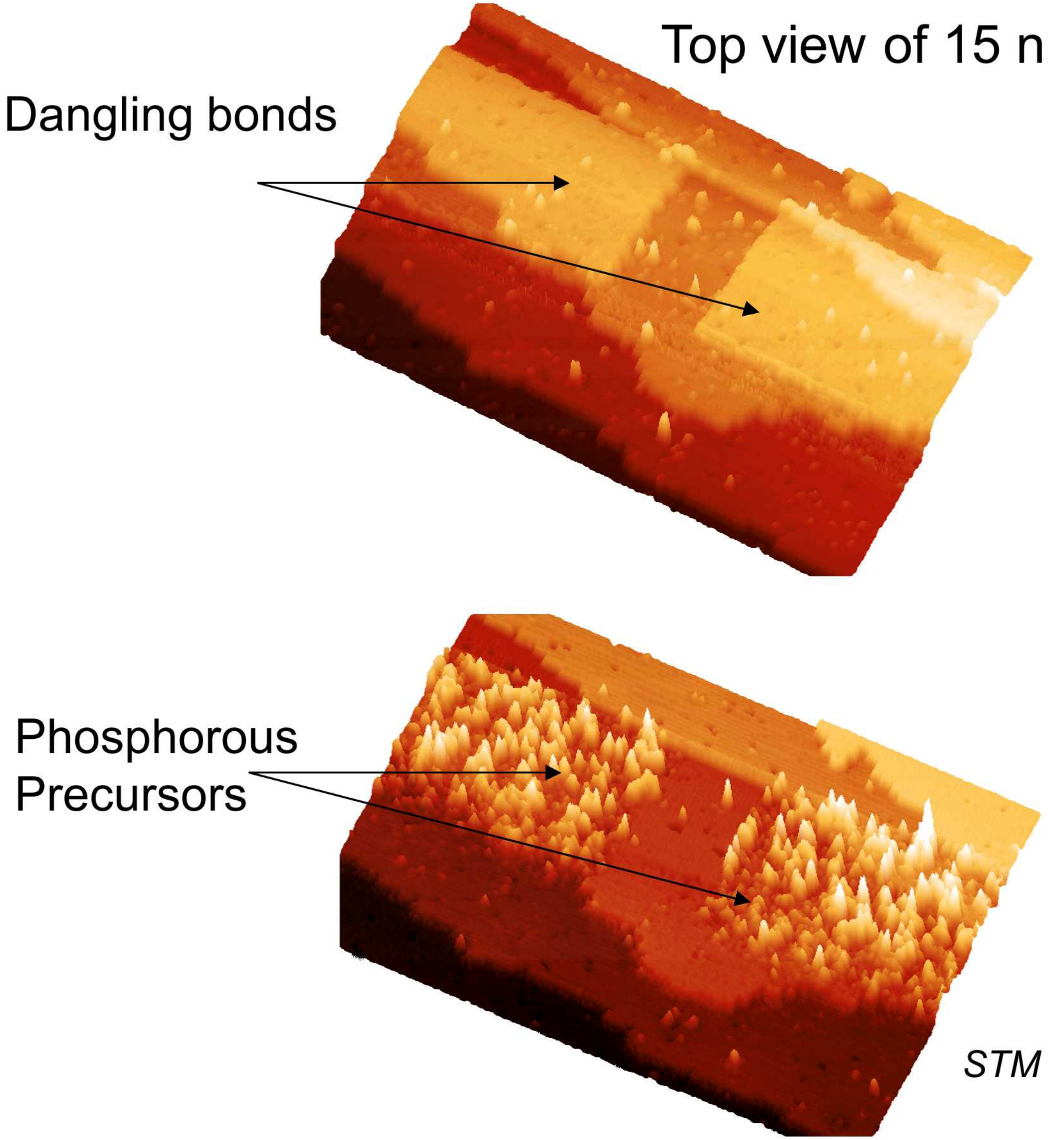
Phosphorus ‘donates’ an electron to silicon.

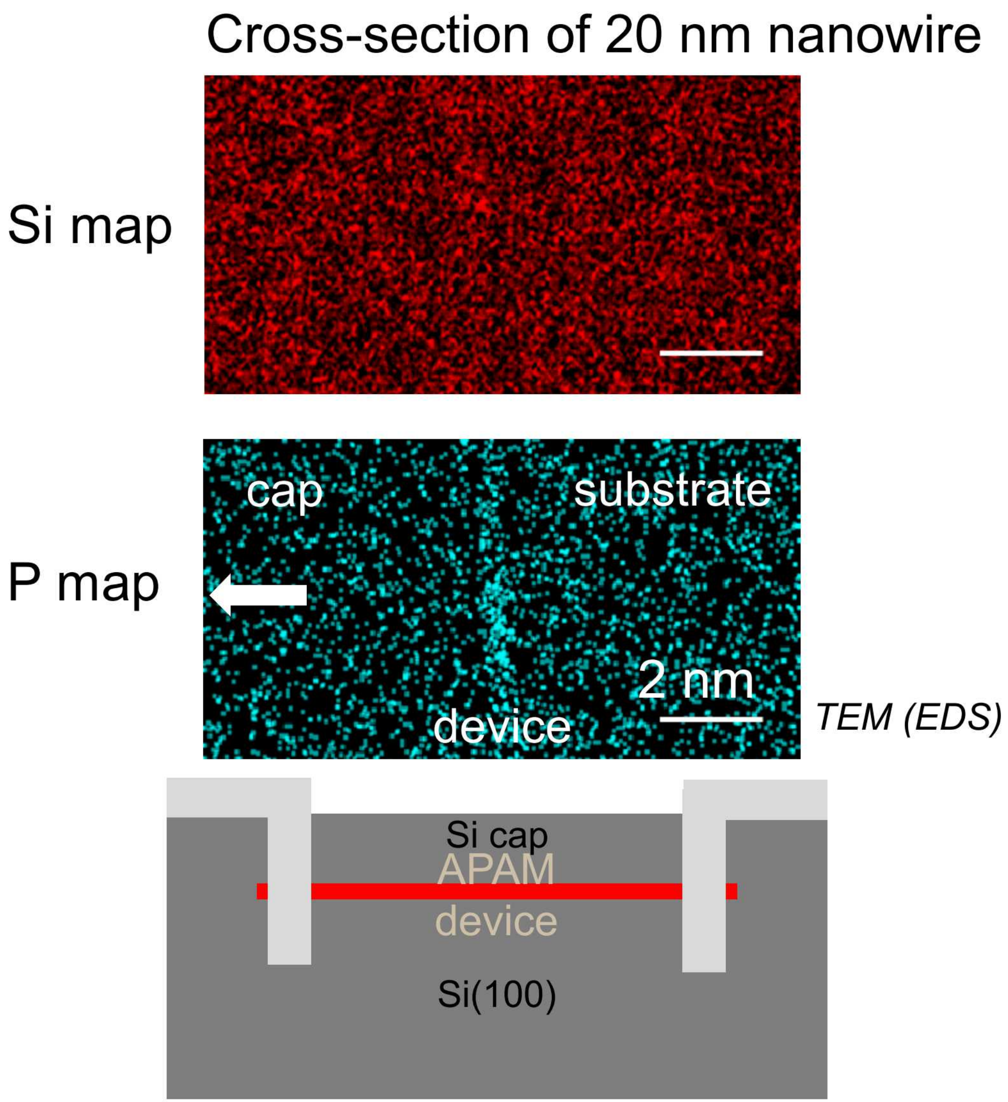


Key properties (vs. standard processing)

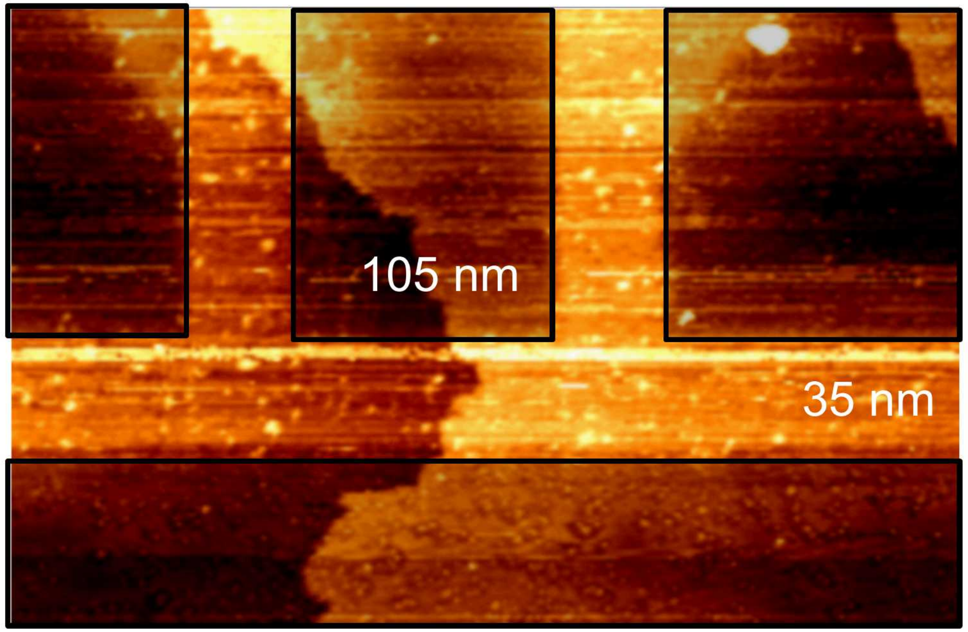
3. Chemistry corrects errors in resist
4. Extremely high density of dopants

Atomic precision device characterization

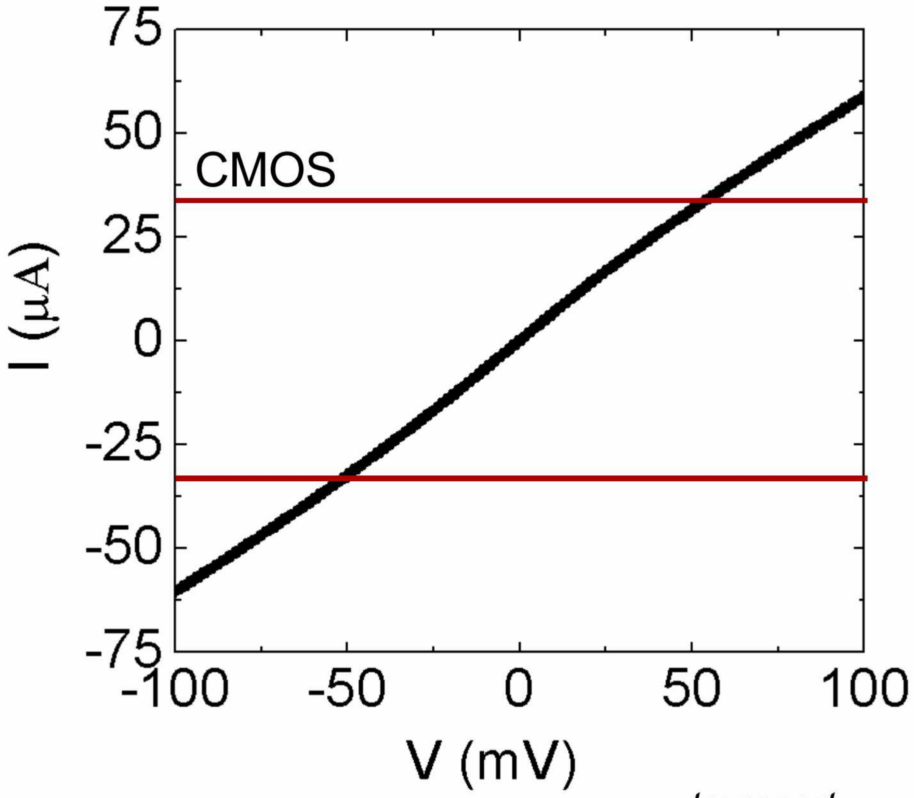




Why are APAM devices electrically interesting?



STM

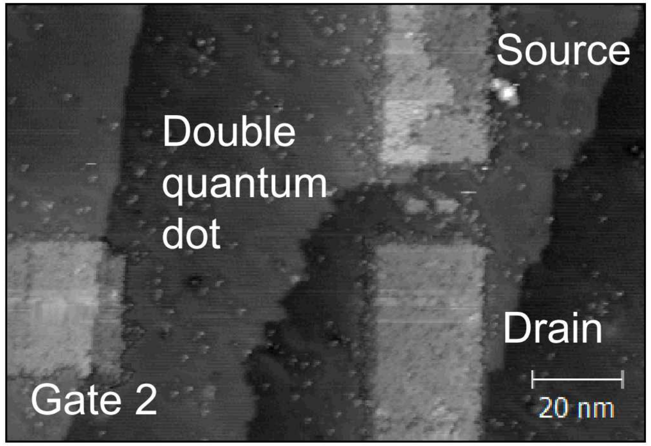


transport

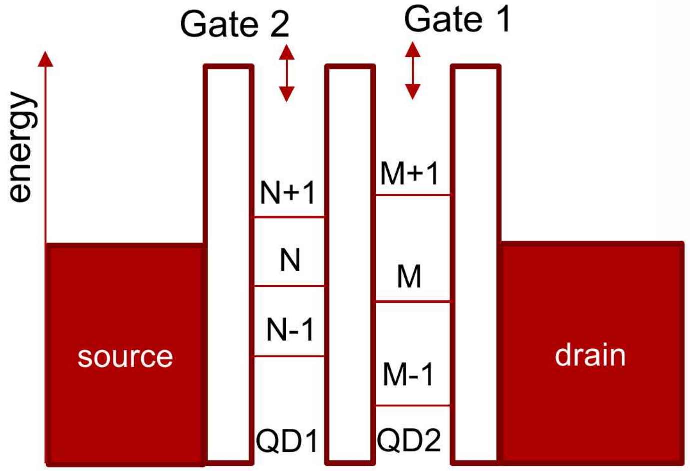
Dopant density produces an impressive current density > 1 mA/ μm.

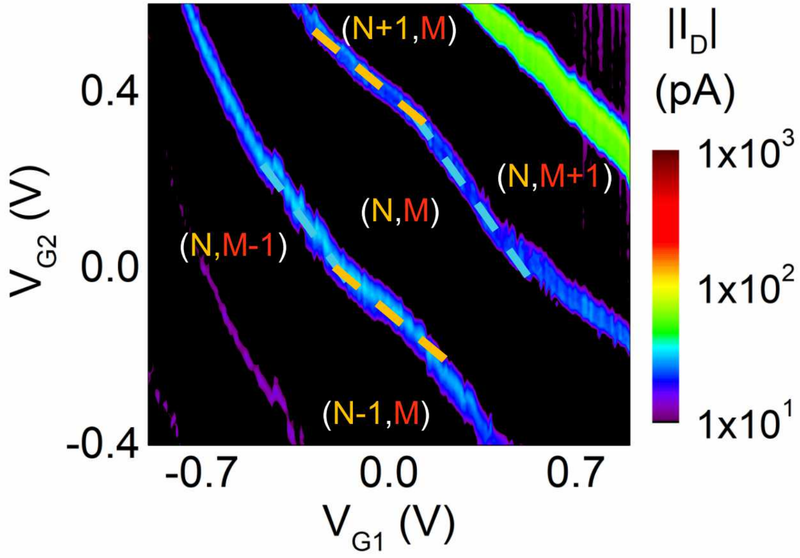
- May make a good enough switch to project CMOS to physical limit
- May be able to interface directly with MOS

Typical APAM device



STM





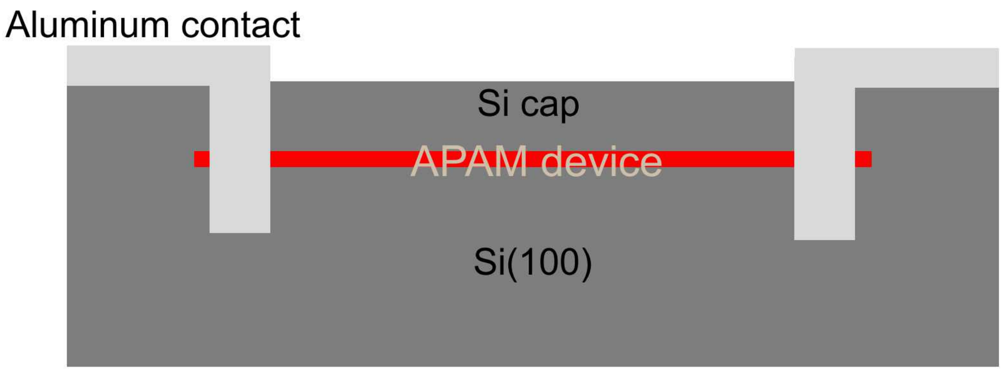
transport

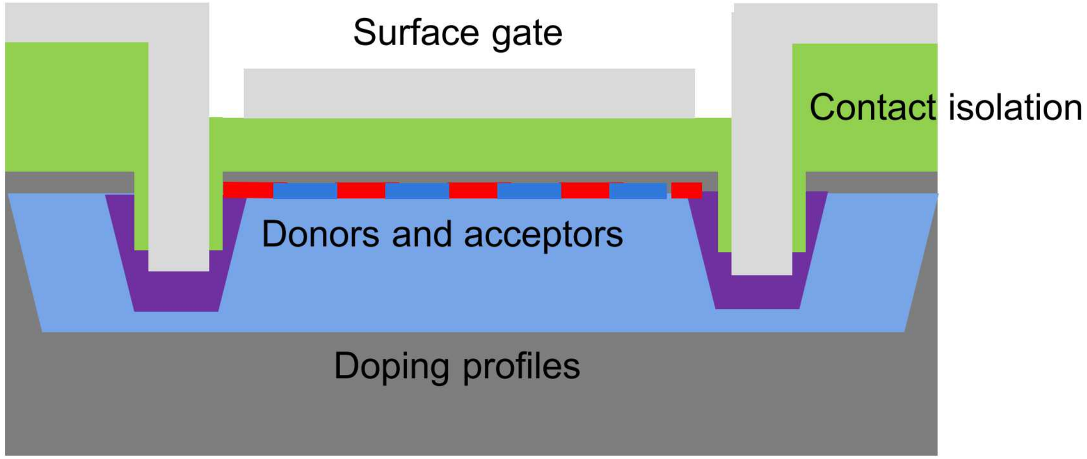
- Physics demonstration – resonant tunneling through an artificial molecule
- Very simple devices – only made of n-type regions
- Only work at cryogenic temperatures

Significant gaps for application to microelectronics

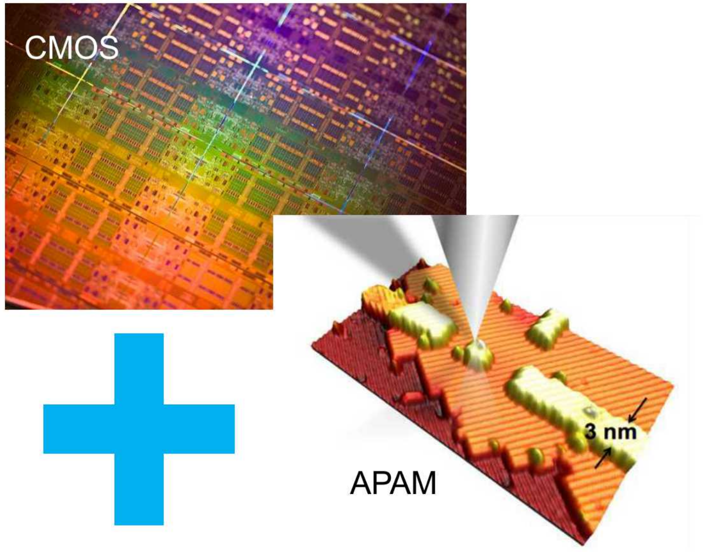
What is needed to apply APAM to digital microelectronics?

(A) Increase complexity of devices

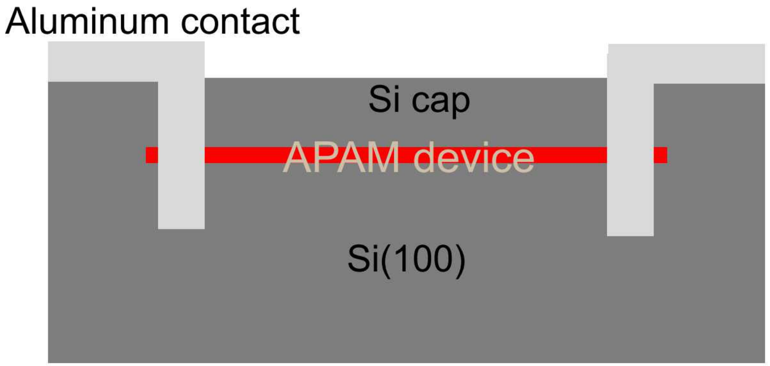


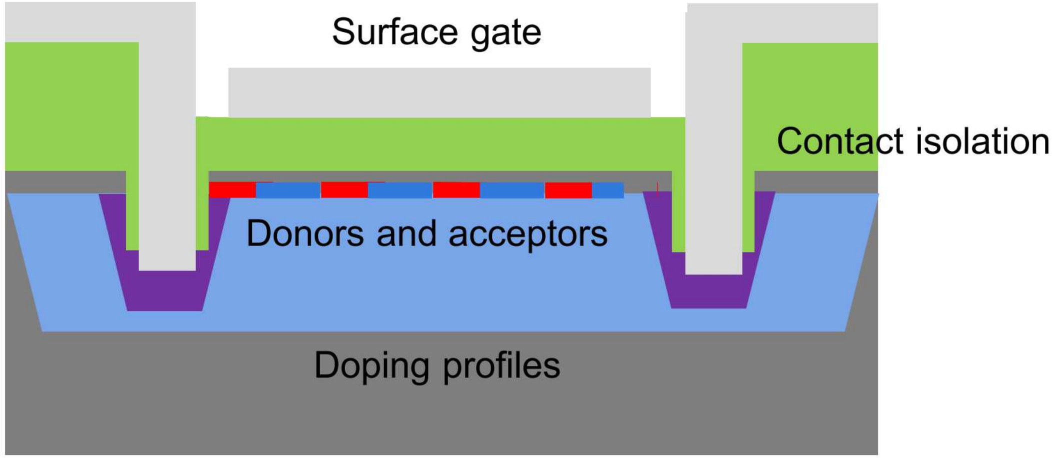


(B) Integrate with CMOS



(A) Increase complexity of devices

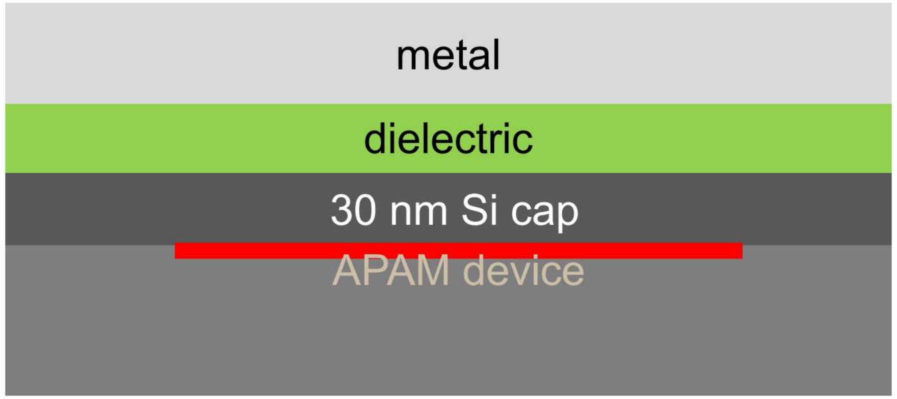


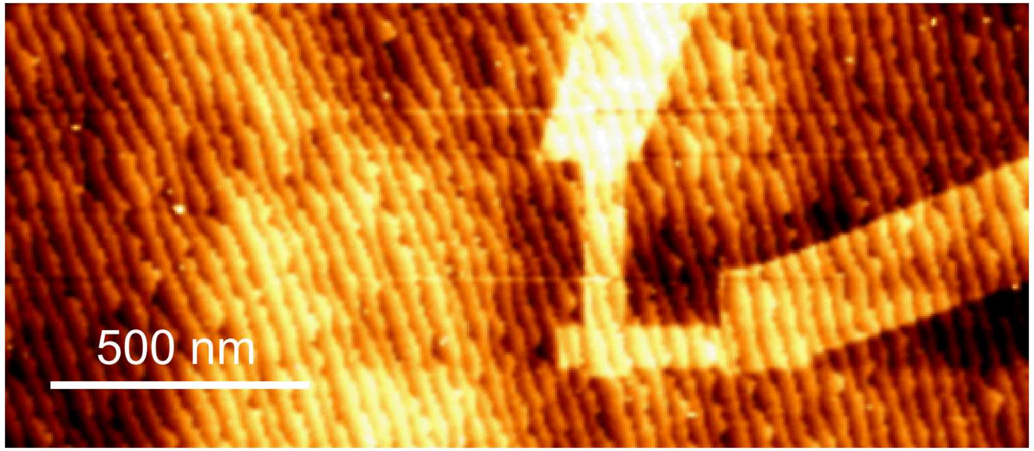


	Objective	Device component
1	**High gain**	**Surface gate**
2	Complementary devices	Donors and acceptors
3	Room temp operation	Contact isolation Doping profiles

Need surface dielectric/ metal for high gain gates

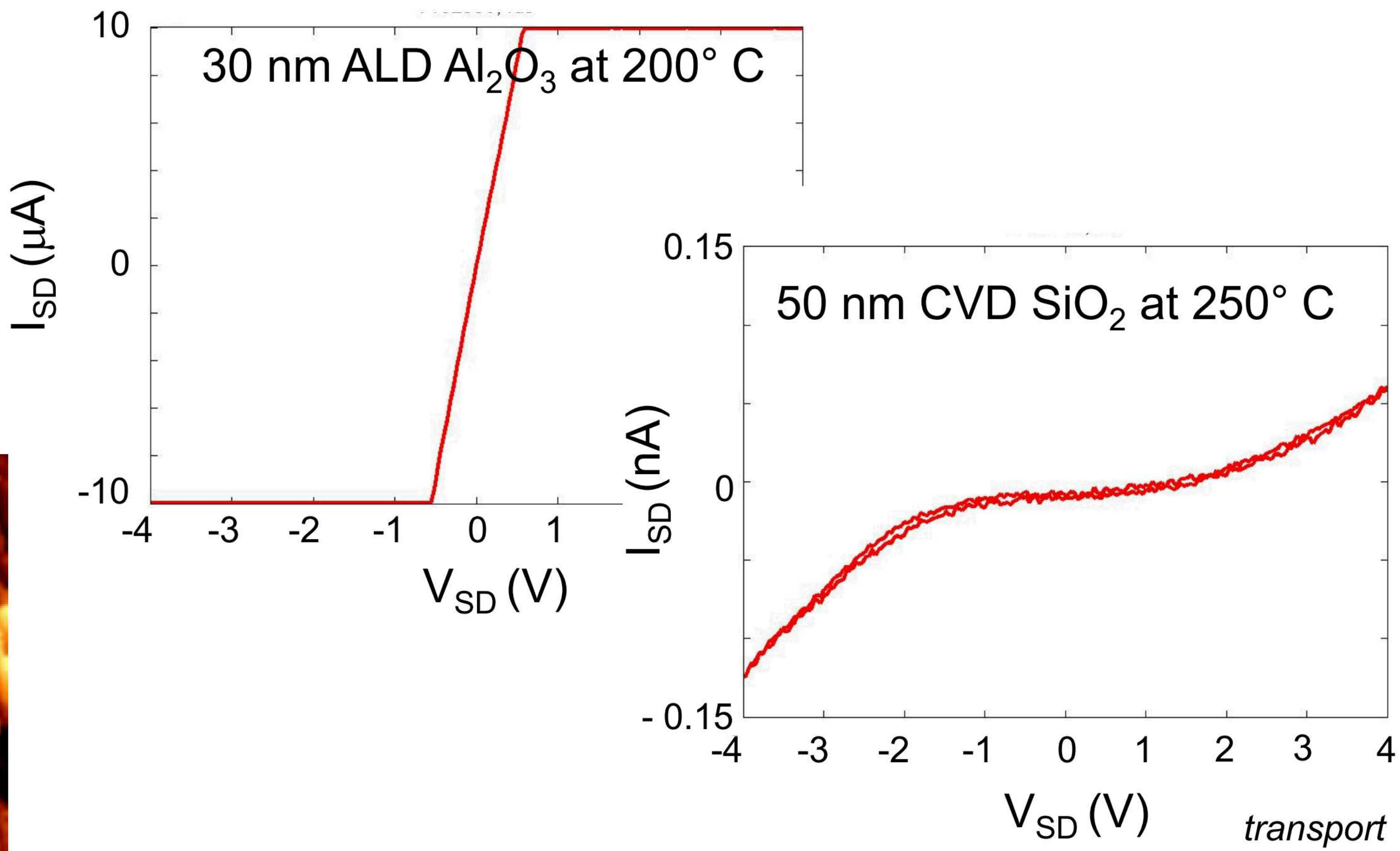
Problem: donors will diffuse due to temp.





STM

Not possible to simulate phosphorus layer
Nanowires as canaries: what processes kill nanowire?

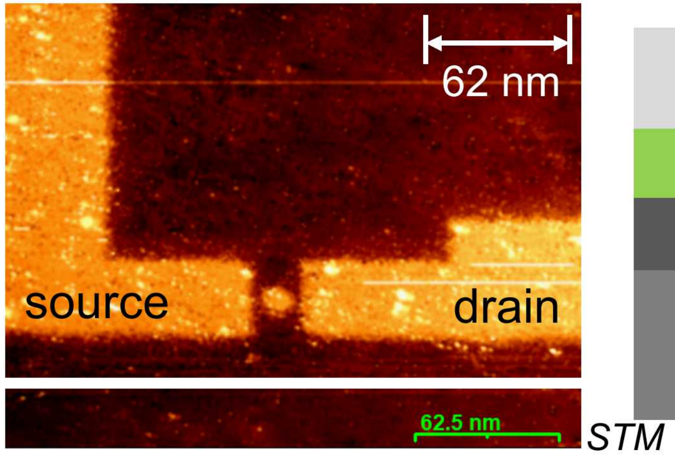


transport

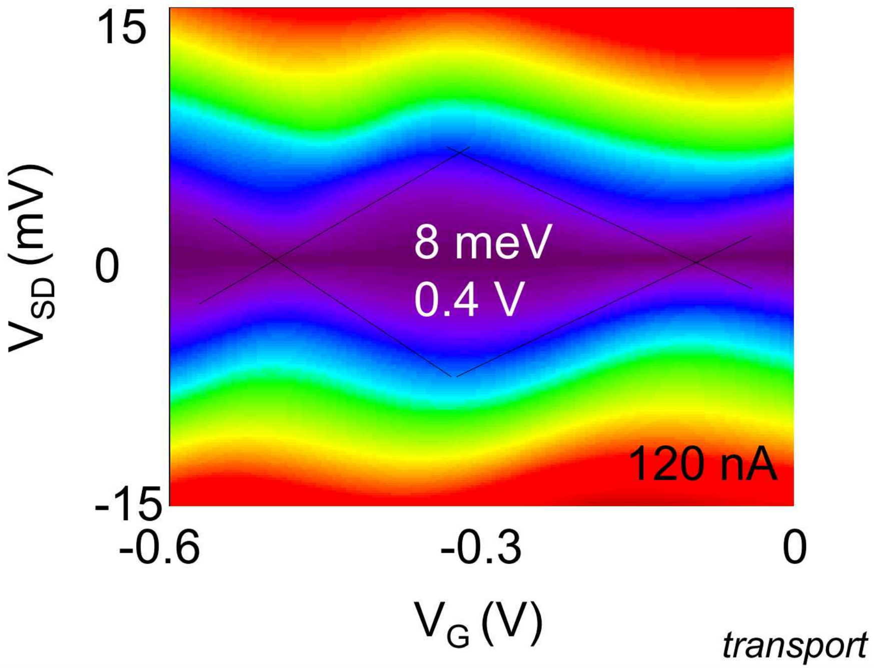
Wire survives, for ALD Al_2O_3

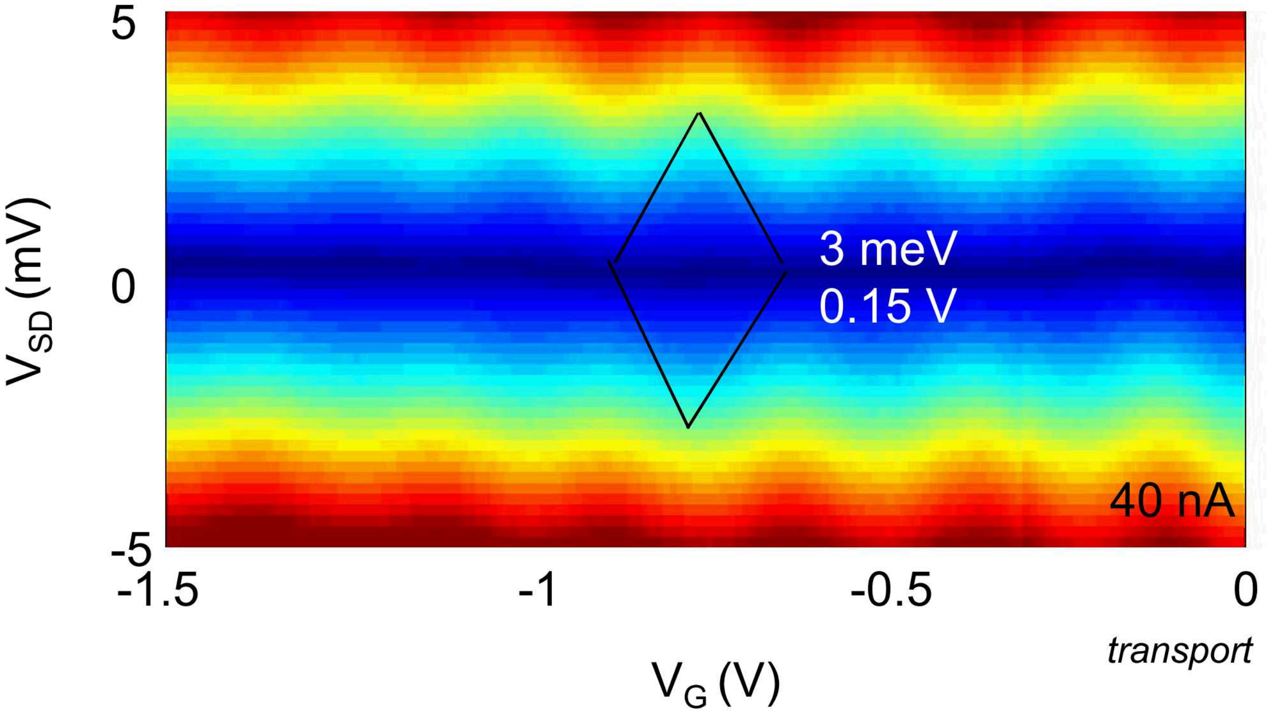
In-plane and surface gates – similar performance

World first – fab compatible
APAM gating scheme

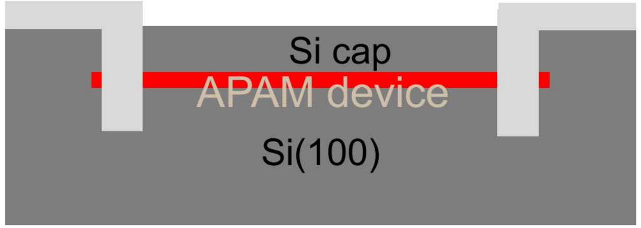


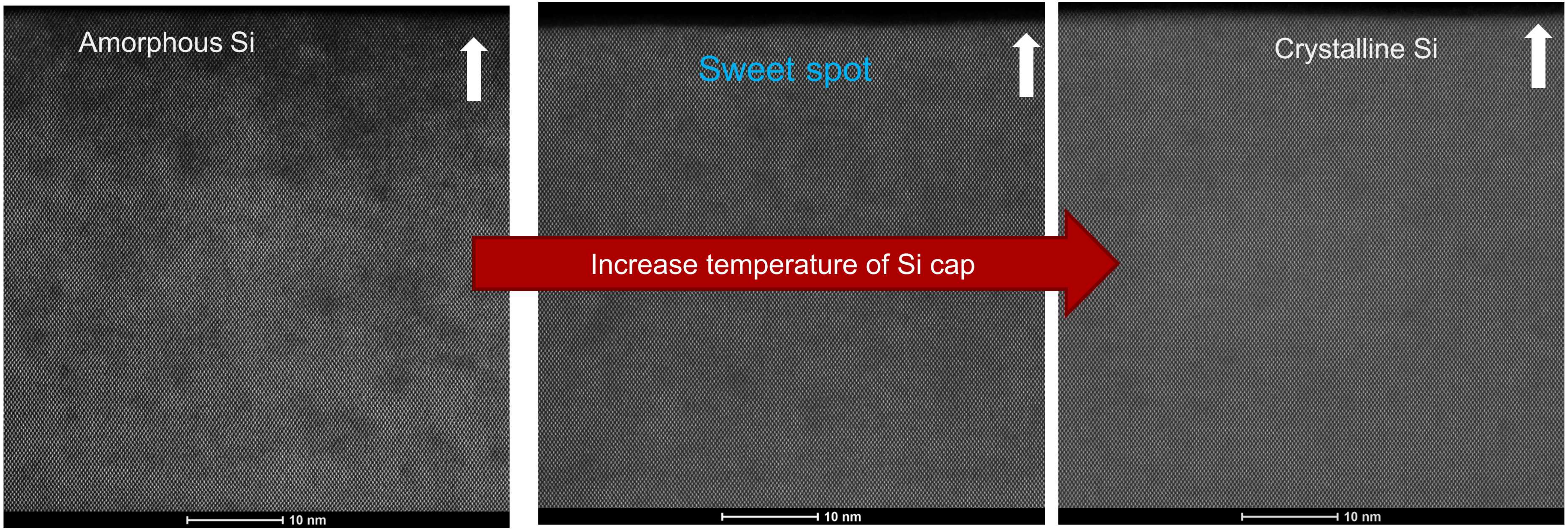
In-plane gated SET





Path forward: (1) kinetic growth of silicon cap





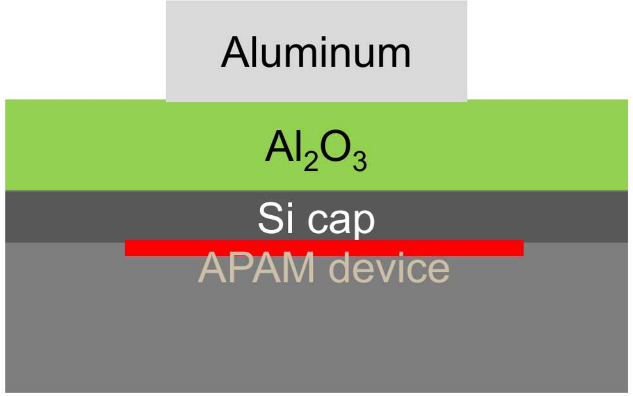
TEM

No P diffusion

No P diffusion

P diffusion

Path forward: (2) Improve gate stack



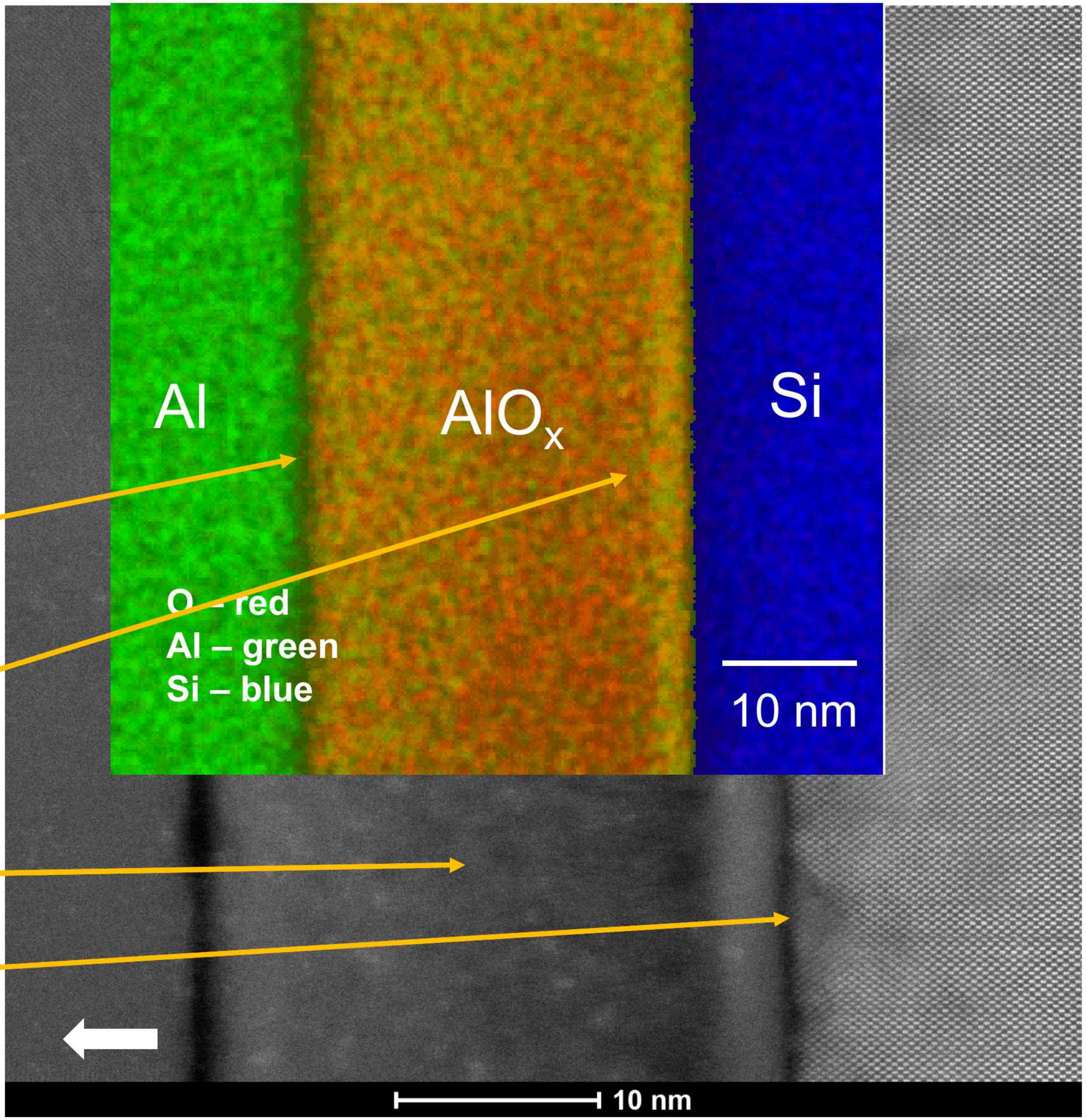
Bad interface

Bad stoichiometry

Not homogeneous

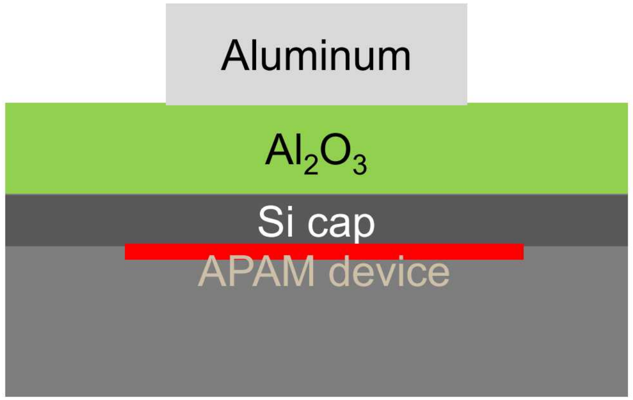
Bad interface

TEM (EDS)

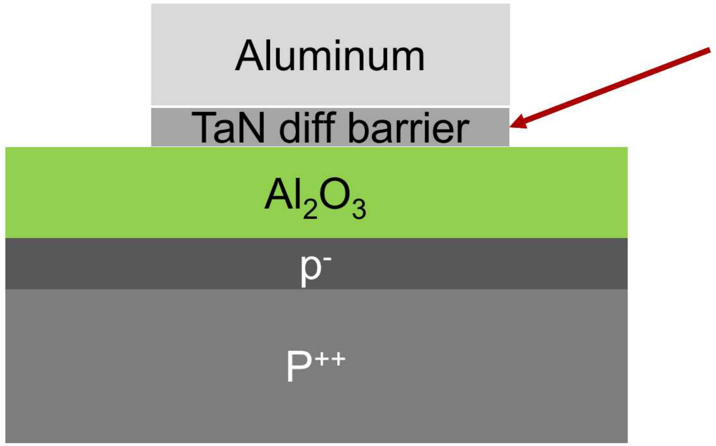


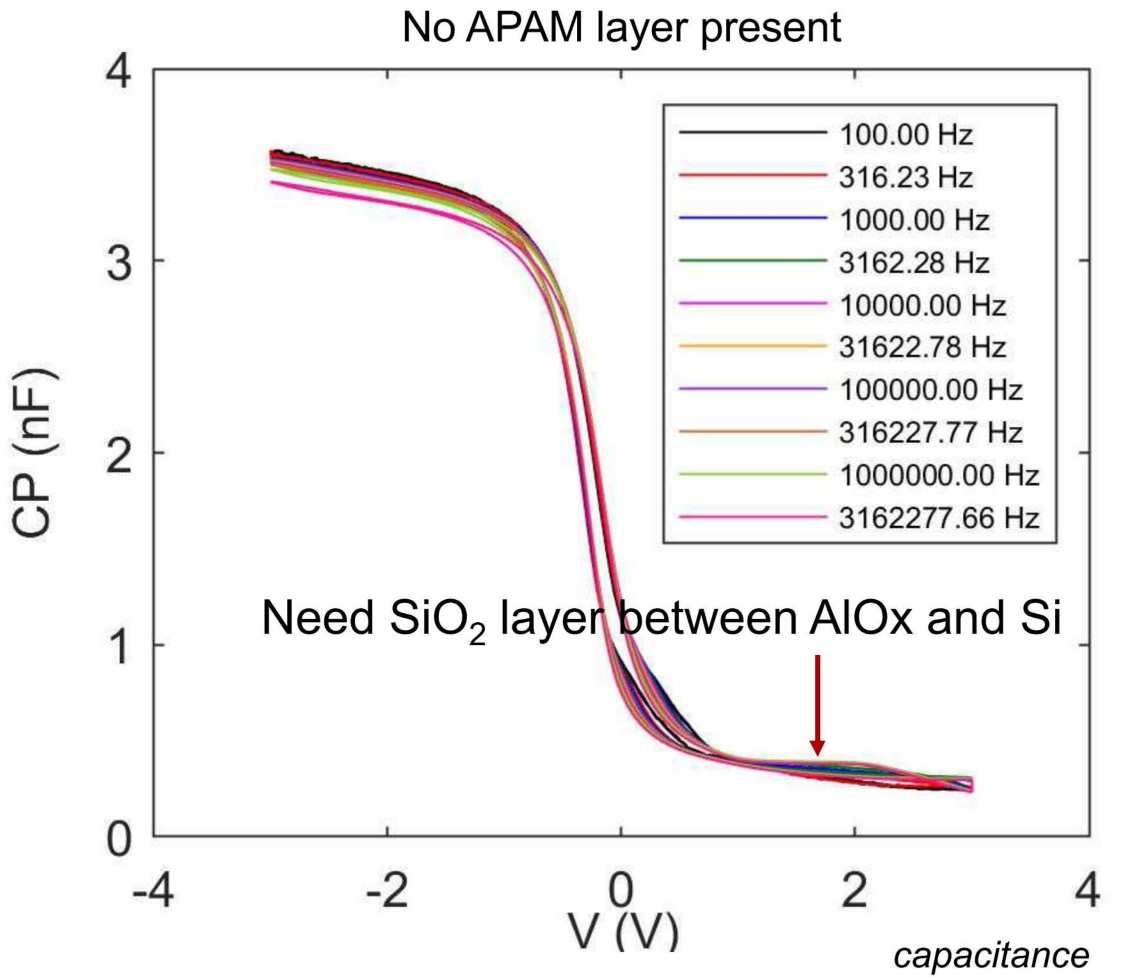
TEM

Path forward: (2) Improve gate stack



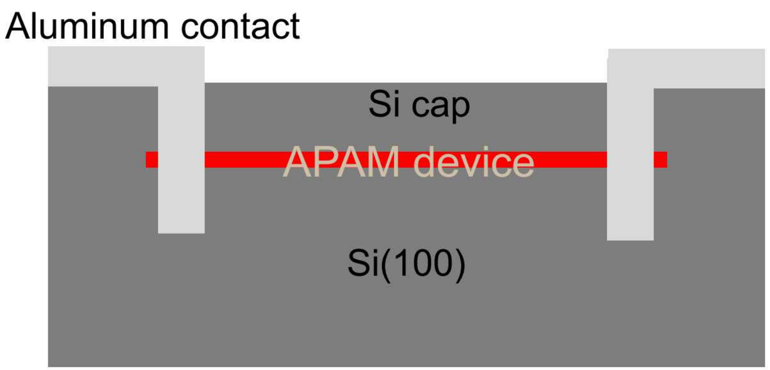
Diffusion barrier to improve interface quality

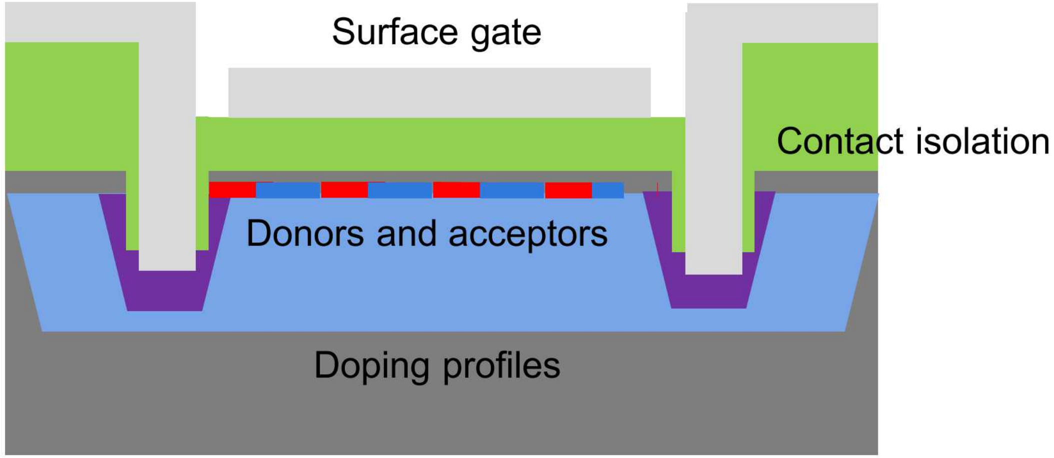




Short turnaround using CV curves on MOScaps

(A) Increase complexity of devices



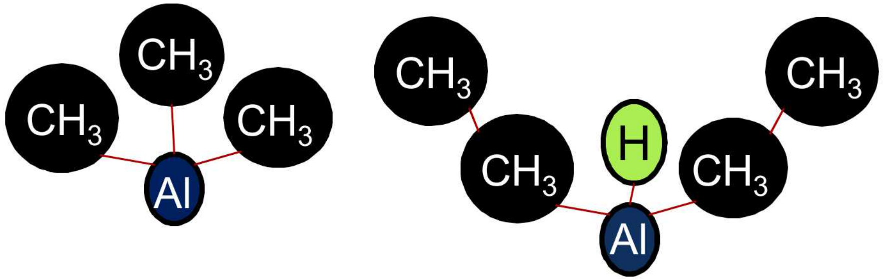


	Objective	Device component
1	High gain	Surface gate
2	**Complementary devices**	**Donors and acceptors**
3	Room temp operation	Contact isolation Doping profiles

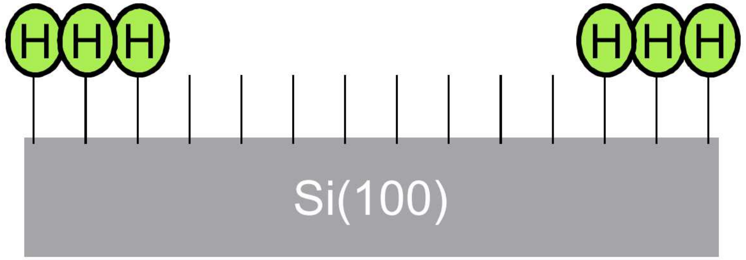
Acceptor doping for complementary devices

Precursors are generally pyrophoric, toxic, or both ← expensive to try.

Selective to resist?
Electrical quality of material?

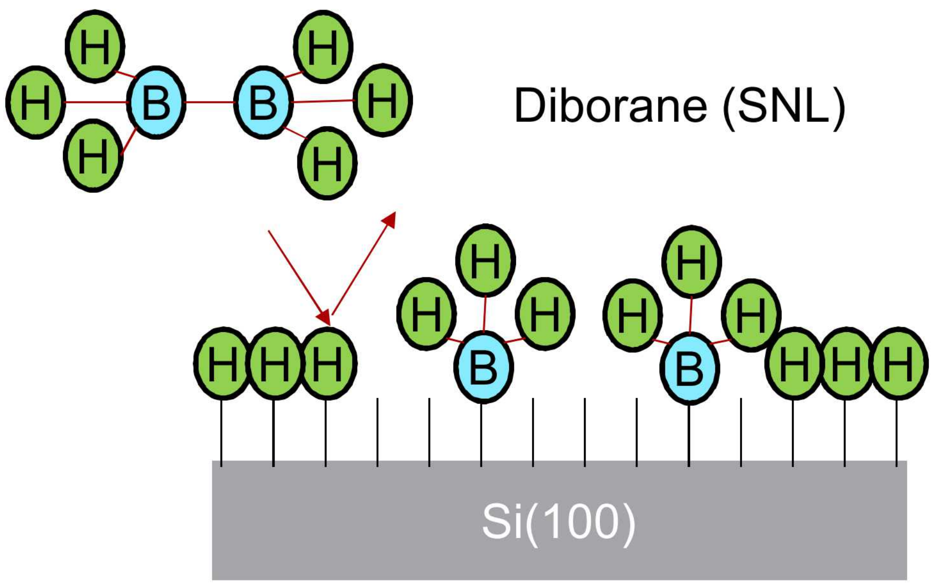


Metal-organics (Zyvex labs)

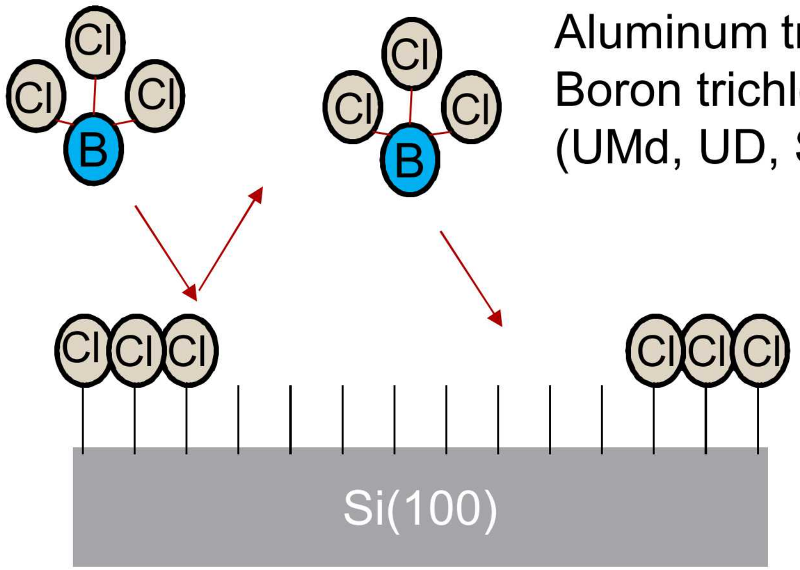


- Selective to resist (Zyvex)
- Electrical conductivity is terrible
  - Si-C bond is bad
  - Beta hydride elimination?

Acceptor doping for complementary devices



Diborane (SNL)



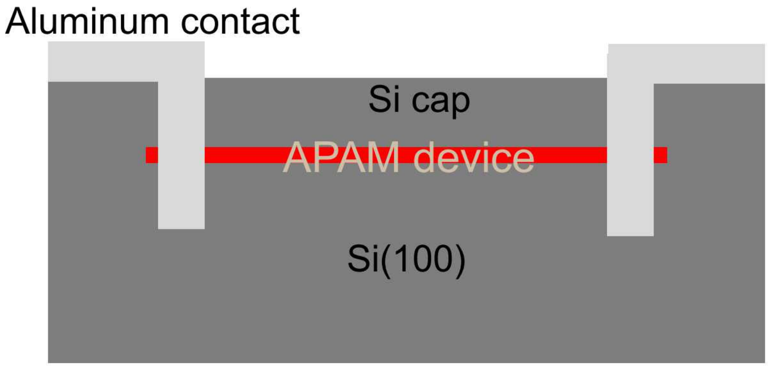
Aluminum trichloride
Boron trichloride
(UMd, UD, SNL)

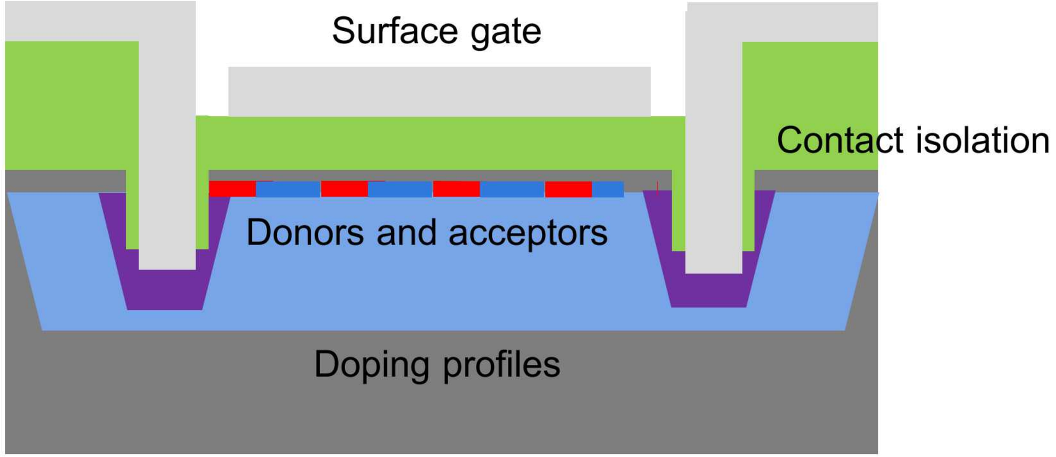
- Selective to resist (Zurich)
- Very poor mobility… inactive B.

- Selective to H resist (Delaware)
- Electrical quality:
  - Mono-dopant precursors activation ?
  - Aluminum easier to process than boron?

Chemical selectivity seems to be ‘easy’?
Hard part of problem is electrical quality?

(A) Increase complexity of devices





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1	High gain	Surface gate
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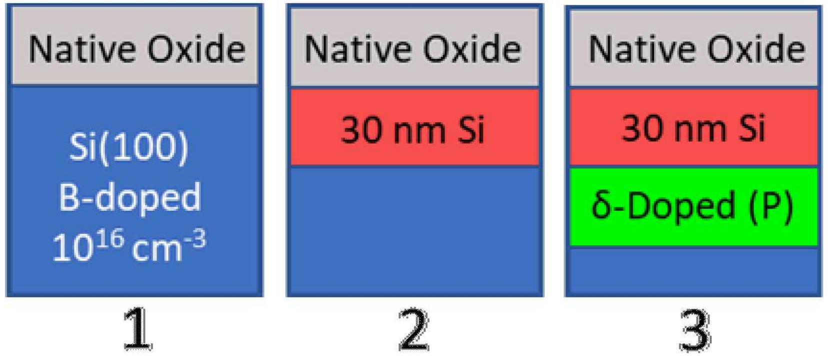
3	**Room temp operation**	**Contact isolation** **Doping profiles**

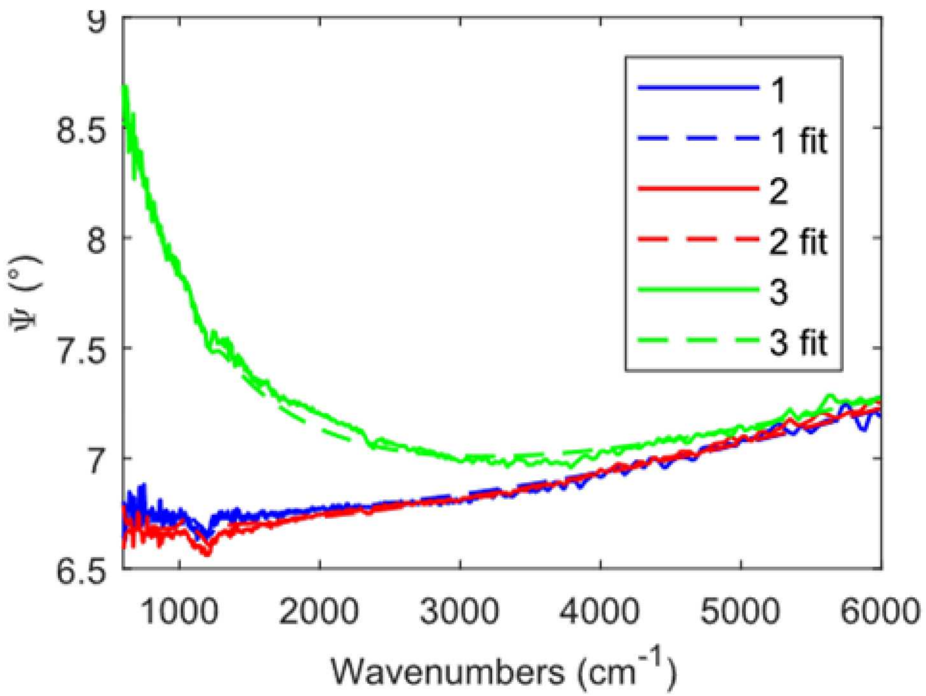
Device layer works fine at room temperature

Infrared ellipsometry

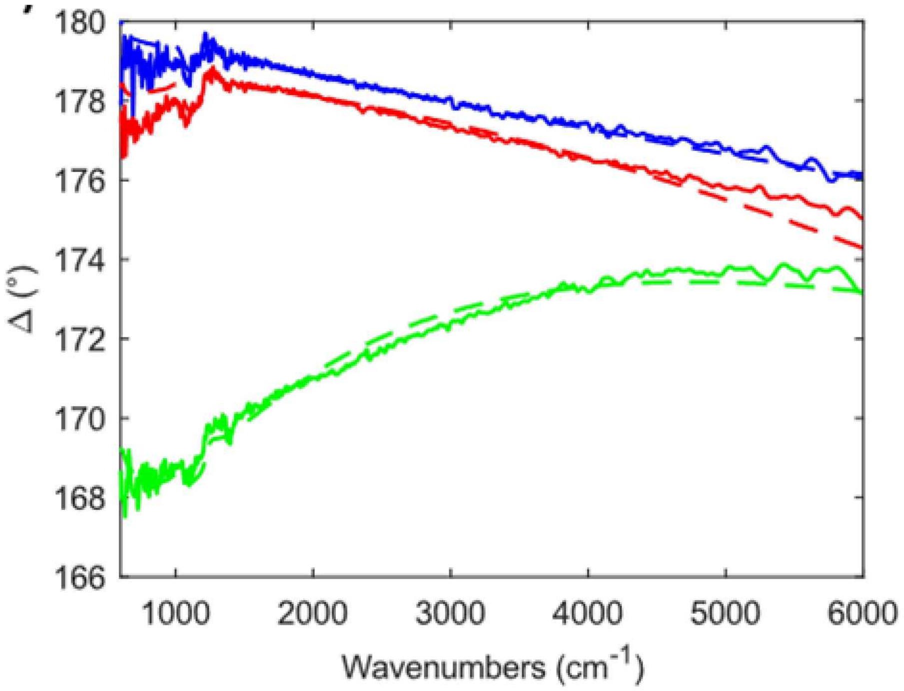
$$\tan\Psi\, e^{i\Delta} = {r_\parallel}/{r_\perp}$$



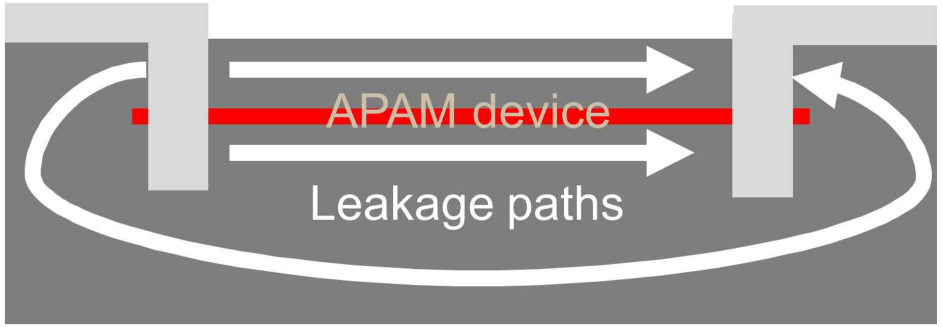
Between 4 K and 293 K, Drude conductivity only changes by factor of 2

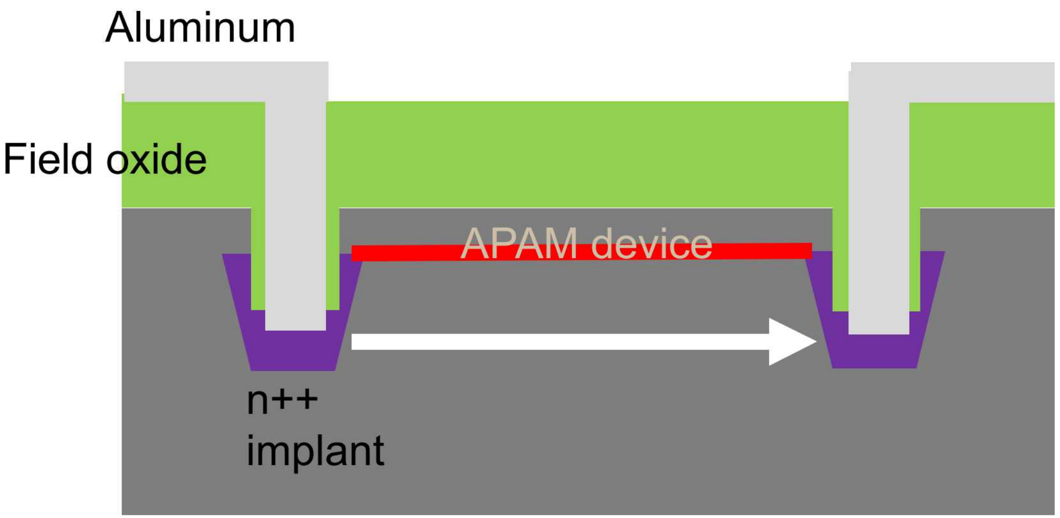


AOI: 70°



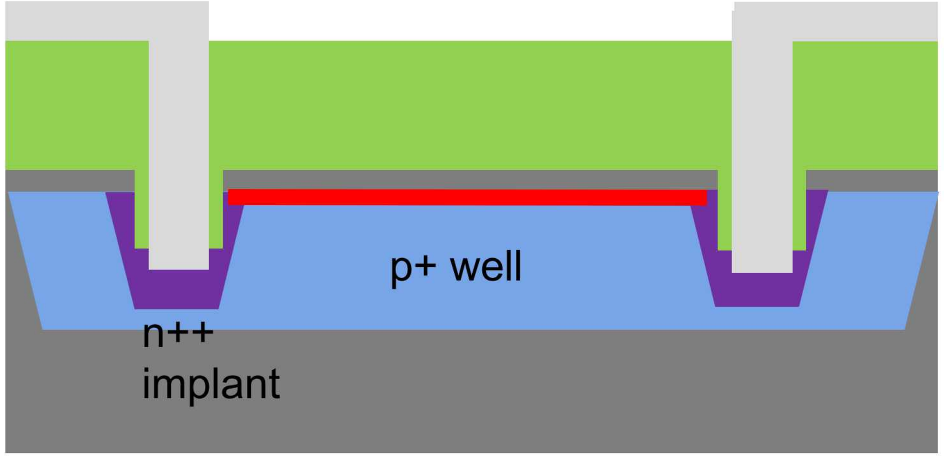
Contact isolation for room temperature operation

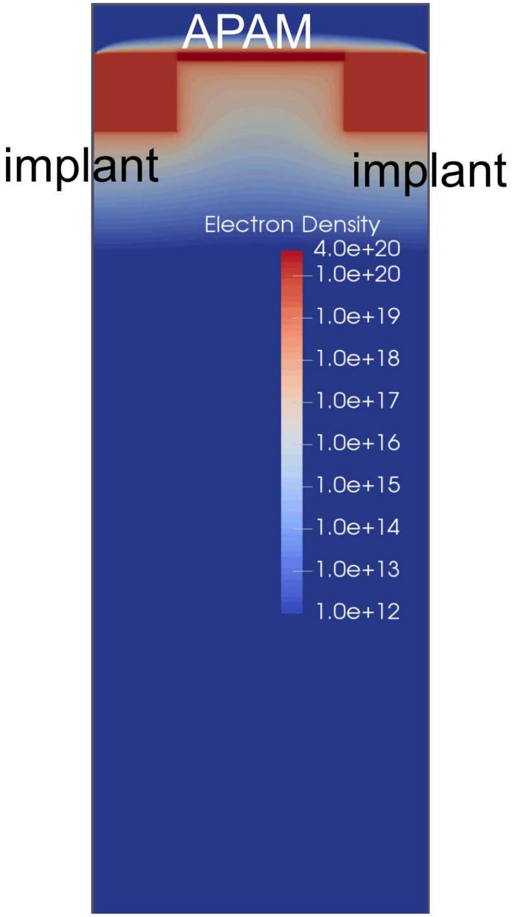


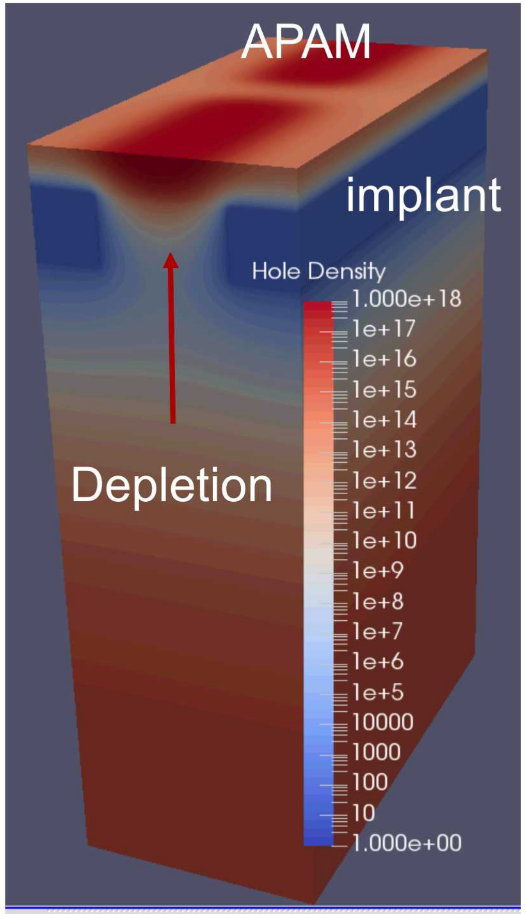


Contact isolation should remove many leakage paths

Doping profiles for room temperature operation





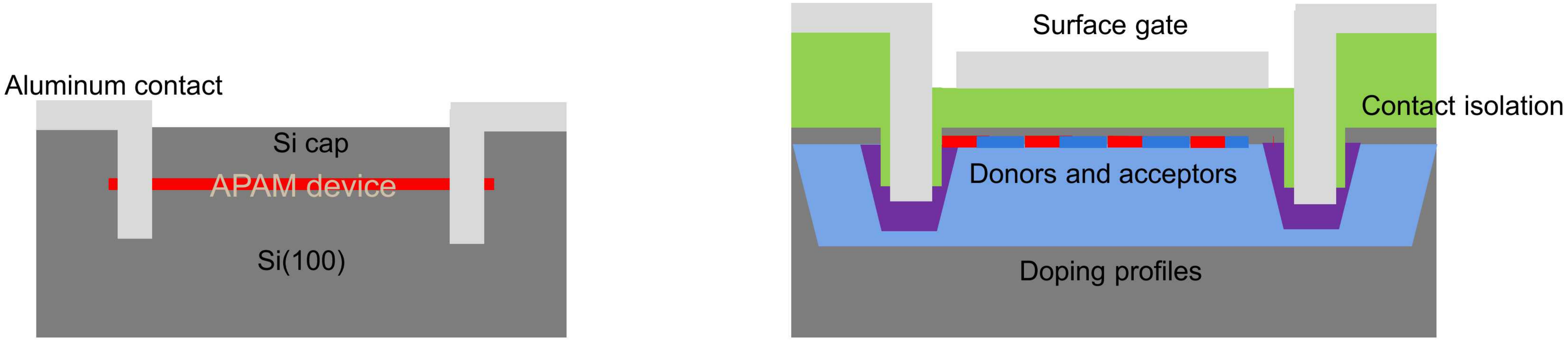


Charon (TCAD)

APAM layer depletes acceptors within 10s of nm

p-n depletion region could eliminate the other leakage path

(A) Increase complexity of devices



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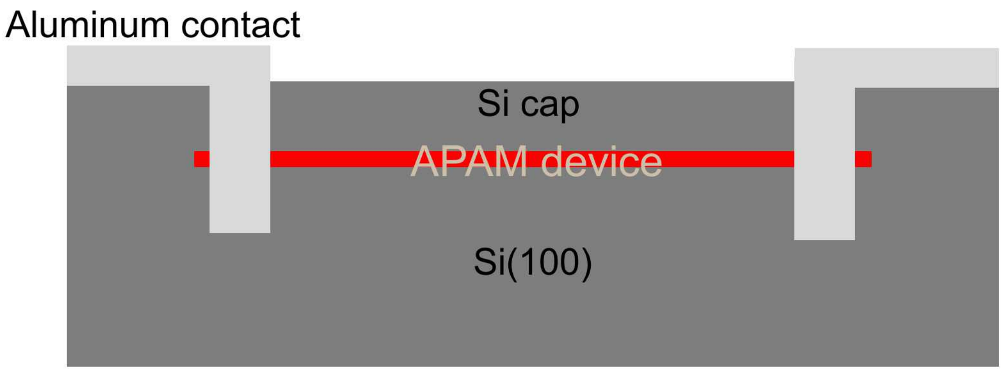
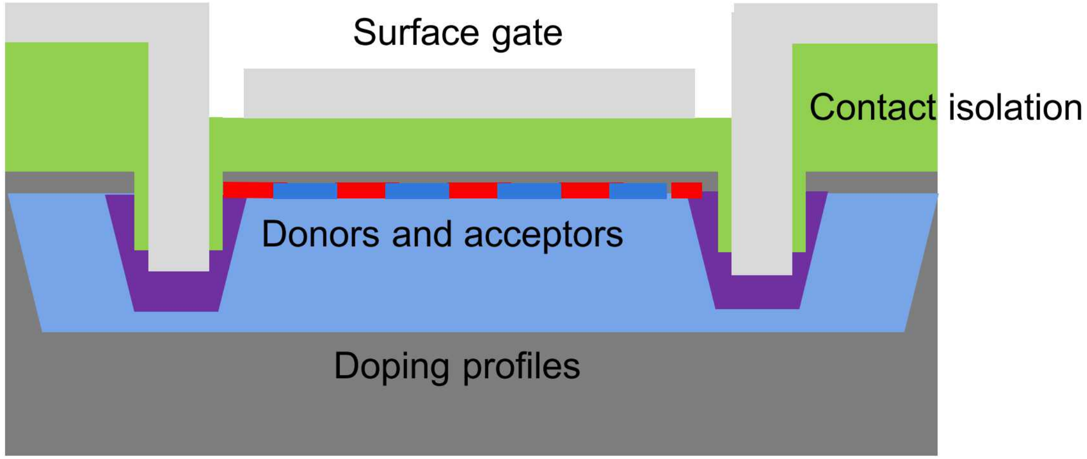
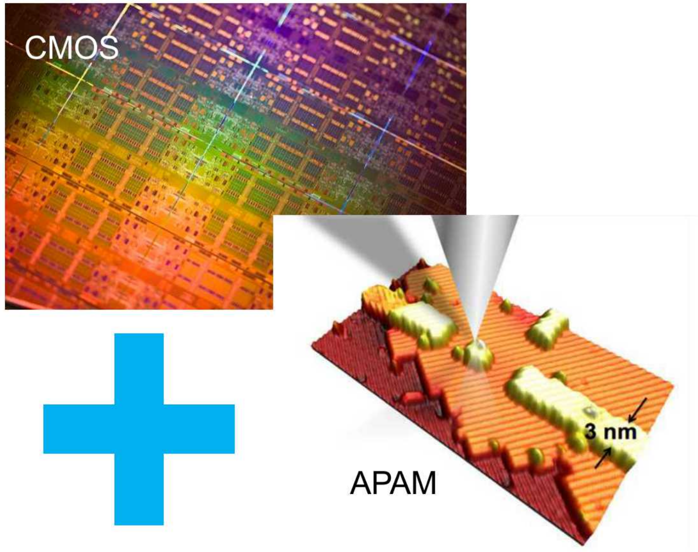
What is needed to apply APAM to digital microelectronics?

(A) Increase complexity of devices

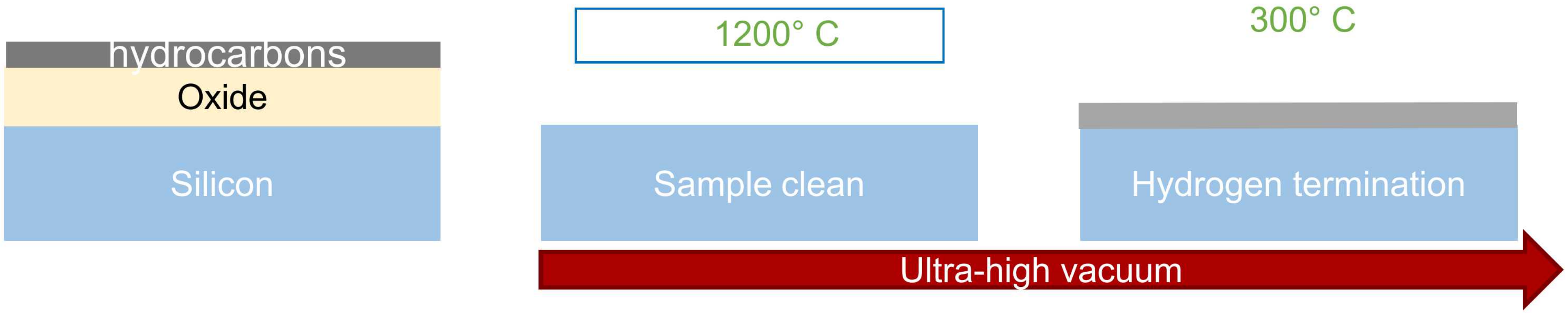




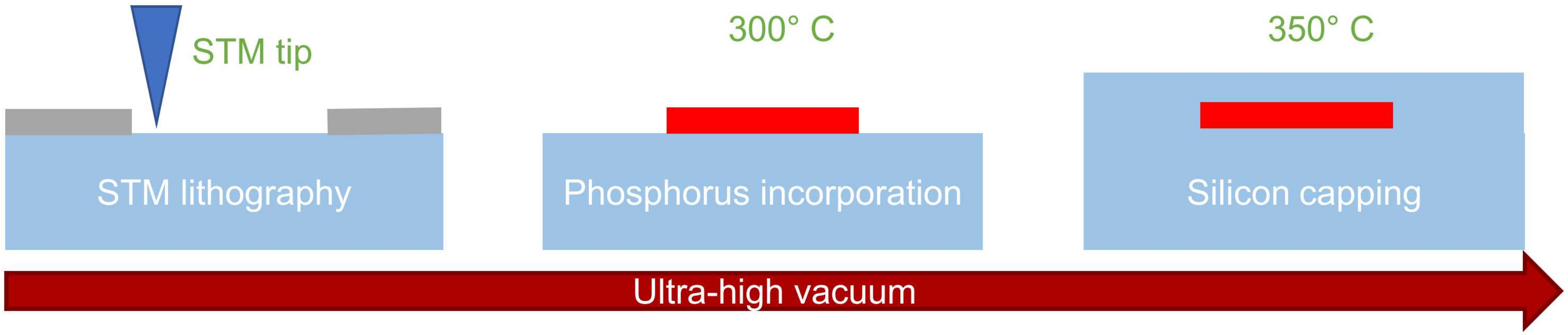
(B) Integrate with CMOS



APAM process flow

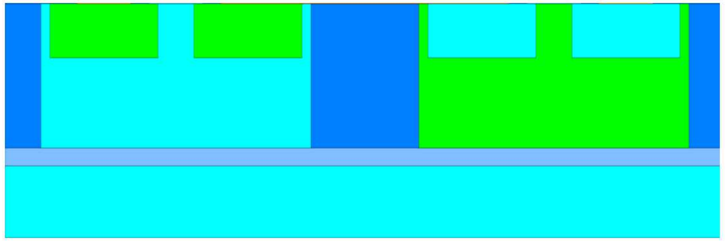


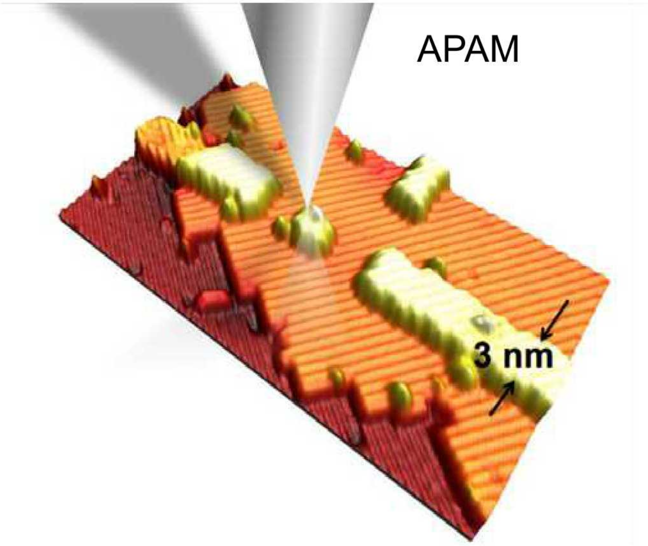
High-temperature clean destroys anything on chip before APAM.

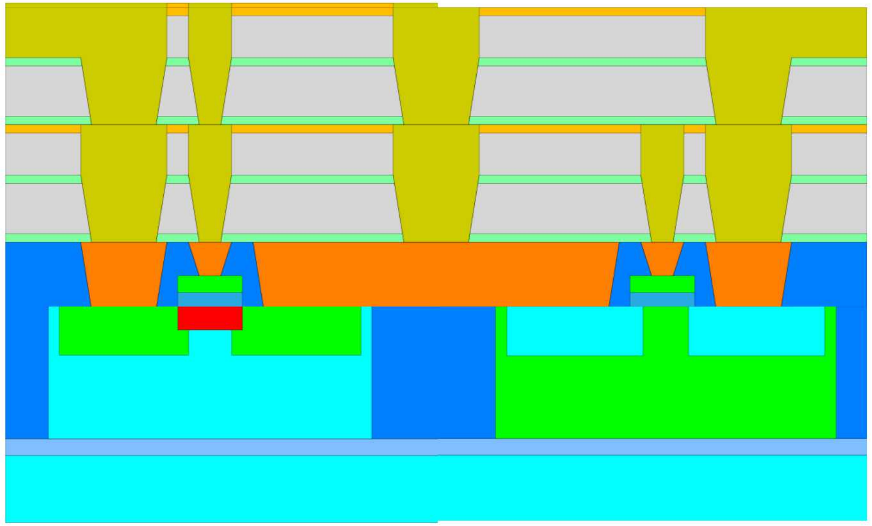


Three paths to prep sample in a different way to make it CMOS compatible.

Direct integration of APAM & CMOS







Front-end-of-line (FEOL > 850° C)

- Implants
- Oxidation (not shown)
- Polysilicon

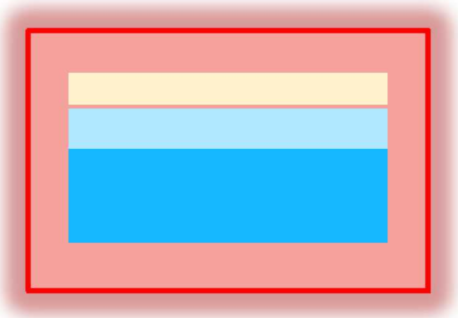
Back-end-of-line (BEOL < 450° C)

- Metallization
- Fill
- CMP

Can we fit APAM in between FEOL and BEOL?

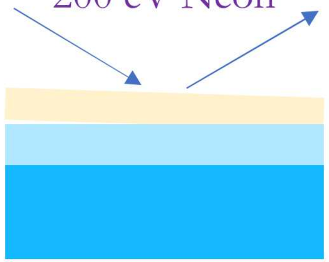
Reduced temperature sample clean

1. Less heat



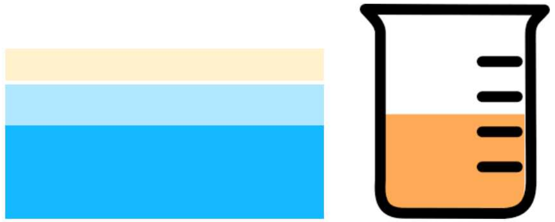
Oxide removal = 850° C

2. Ion sputtering



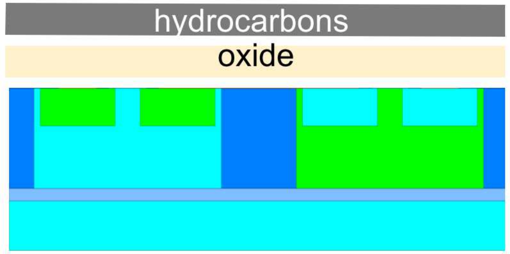
Local APAM window.

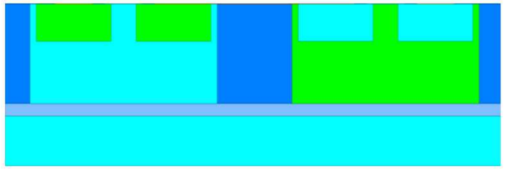
3. Wet chemistry



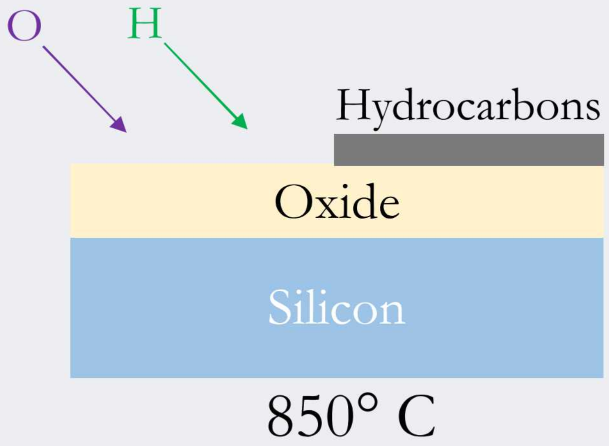
Even lower temperature = wider degree of integrability

Option 1: Reduced temperature sample clean

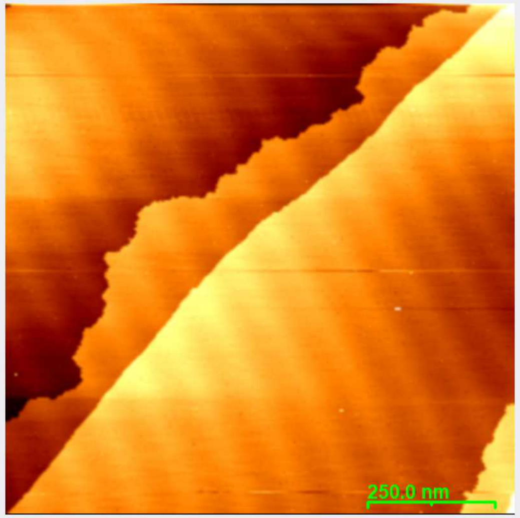


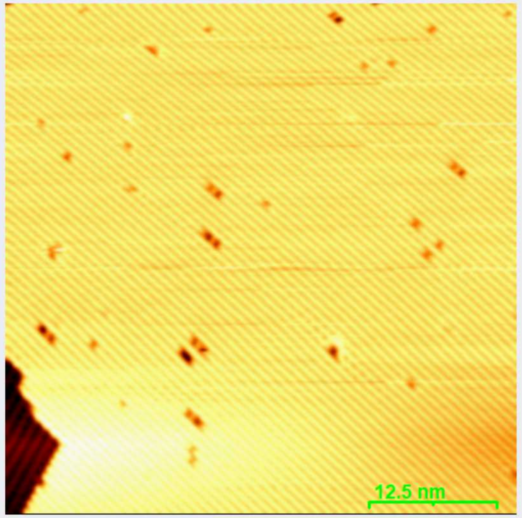


New 850° C clean: APAM can fit between FEOL and BEOL!



Ward, APL (2017)

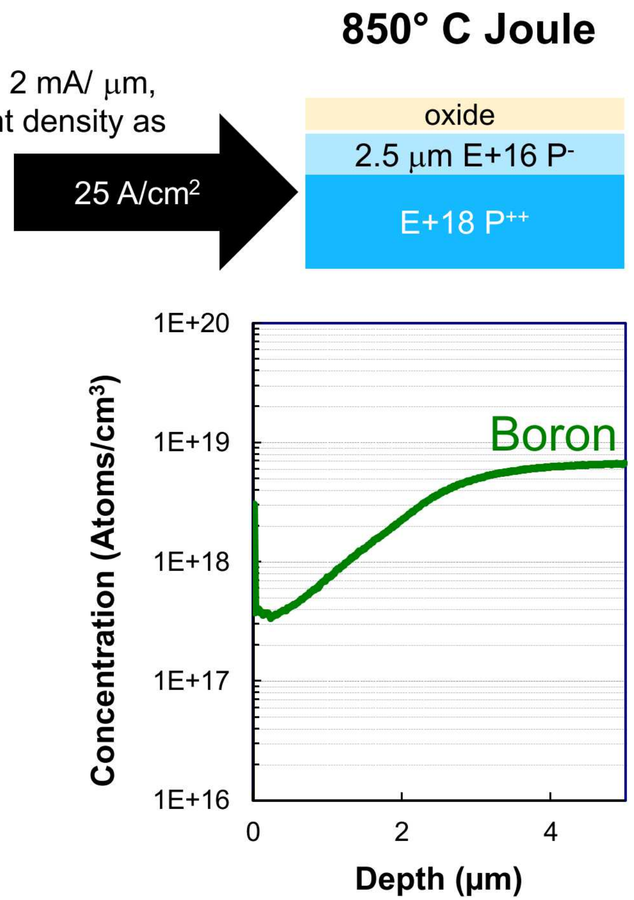




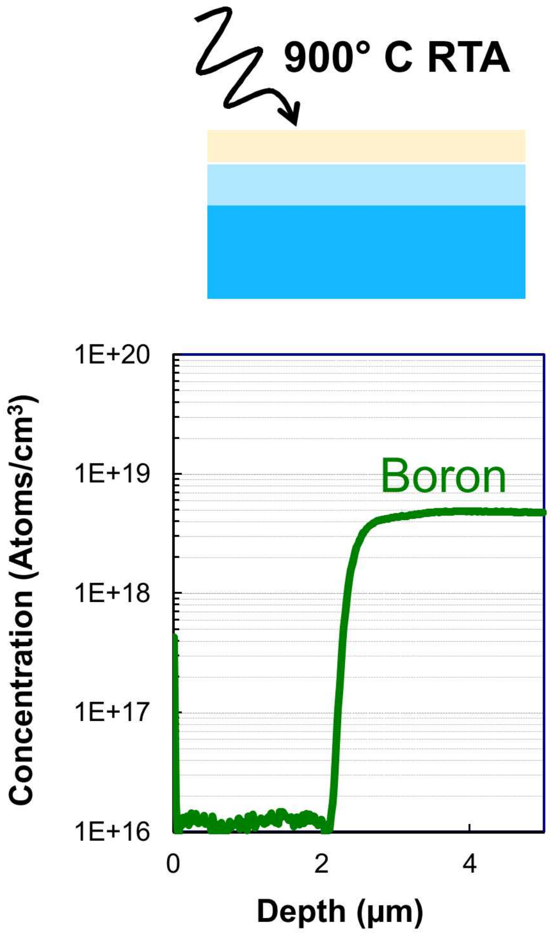
STM

Not compatible with acceptor wells!

In 2D terms, 2 mA/ μm, same current density as APAM wire!



Joule heating – acceptors 'diffuse'



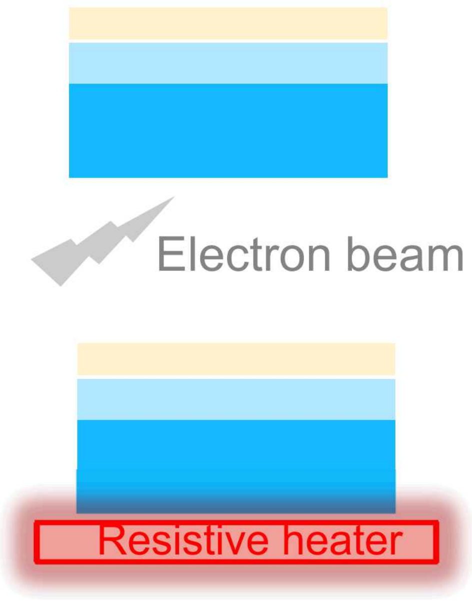
SIMS

Not viable – must take sample out of vacuum

We don't know why acceptors electromigrate like mad.

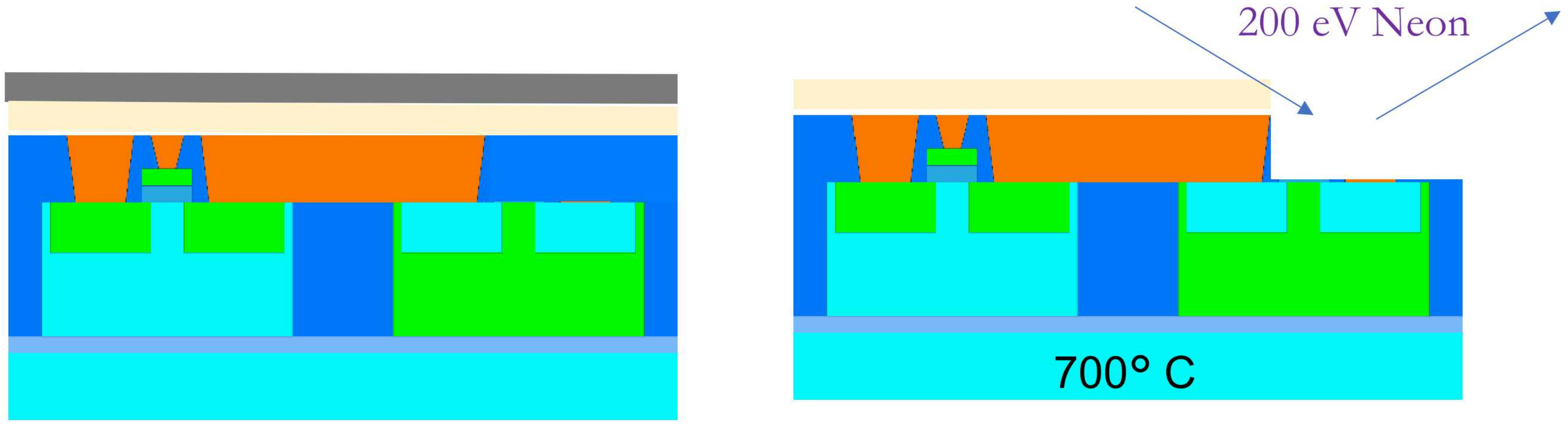
Modify APAM for Direct Integration

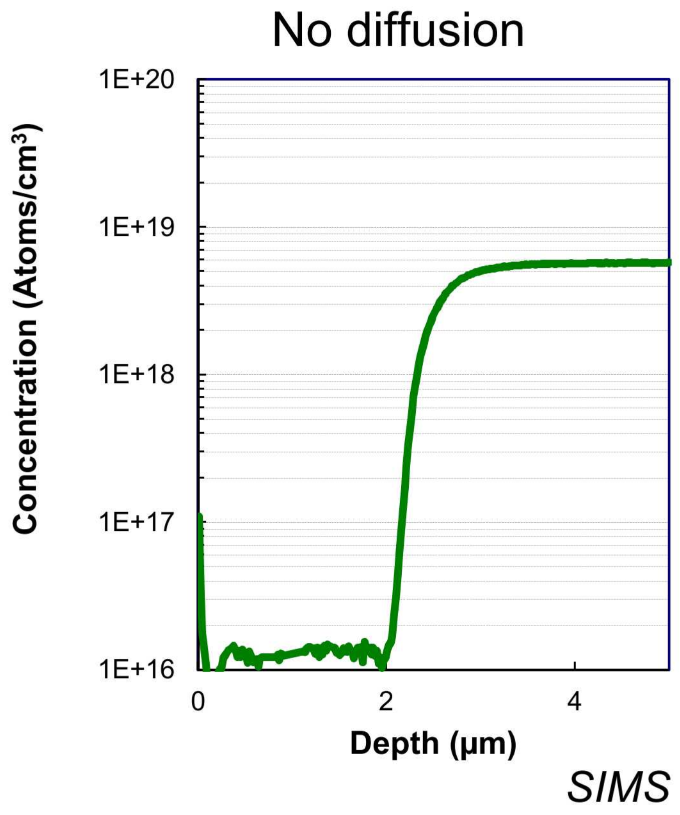
1. Heat sample with other technique



Next: effect of APAM process on CMOS circuit, effect of BEOL on APAM

Option 2: Ion sputtering for local APAM windows





Sputter off what you don't want, anneal to heal damage

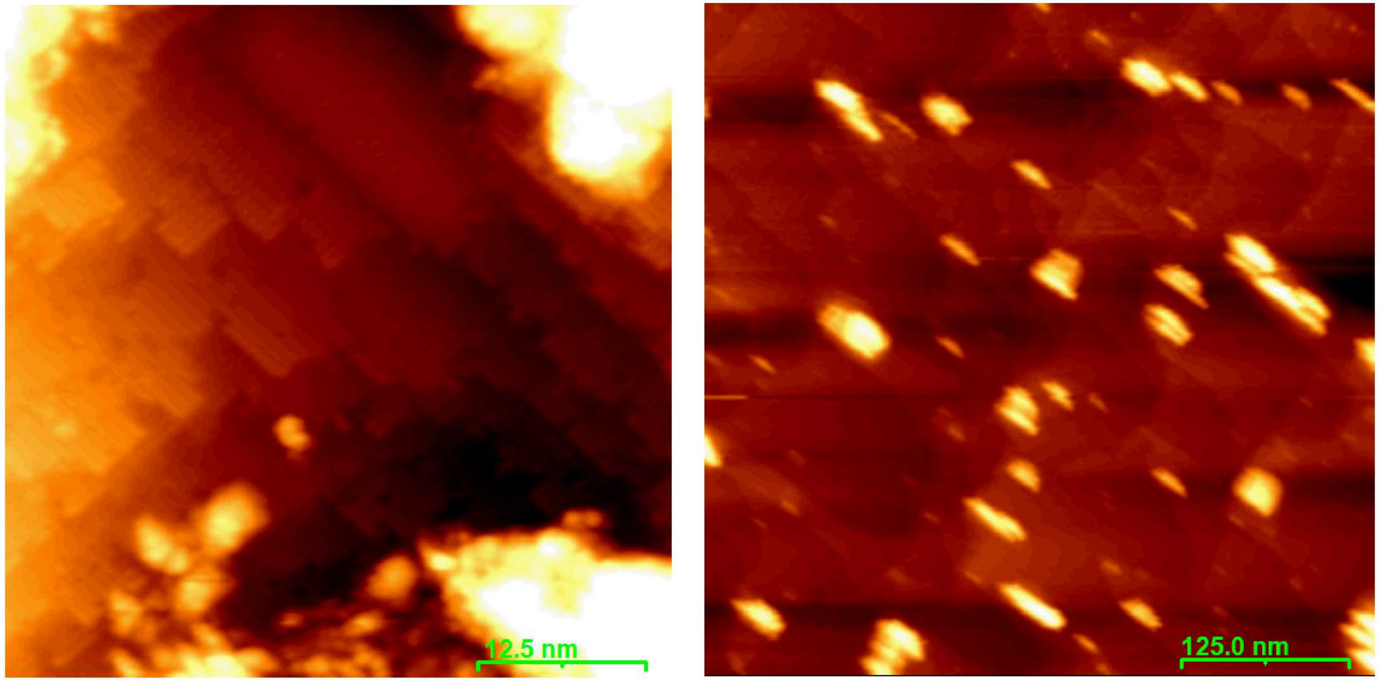
Local window: don't subject whole chip to process.

Lessons learned

(1) Amorphize faster than you remove material ← very low energies

(2) Junk is not purity of gas. ← heavy species

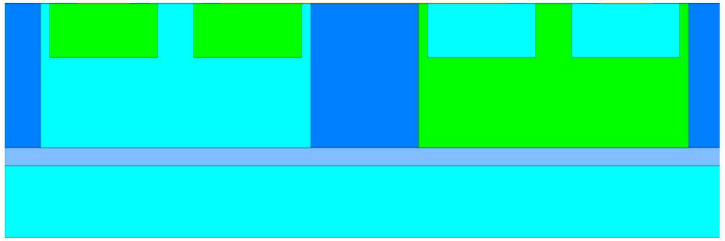
(3) Filament sources are really bad at low energies – sputtering gun onto sample.



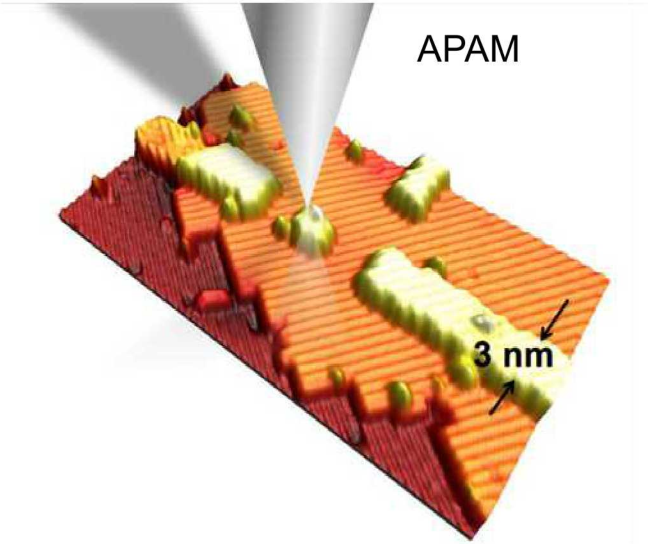
STM

Need plasma source, use Xe

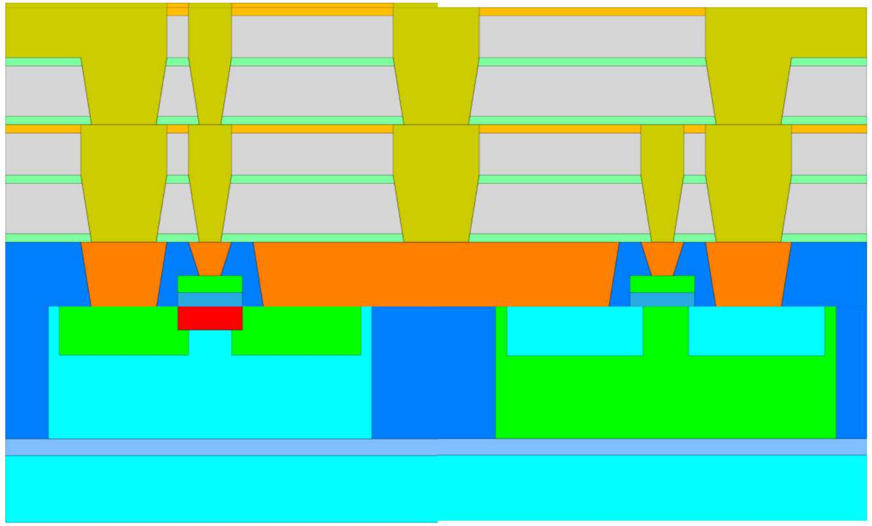
Option 3: Wet chemistry – more flexibility in integration



Front-end-of-line (~~FEOL > 850° C~~)



1200 → 200° C



Back-end-of-line ~~(BEOL < 450° C)~~

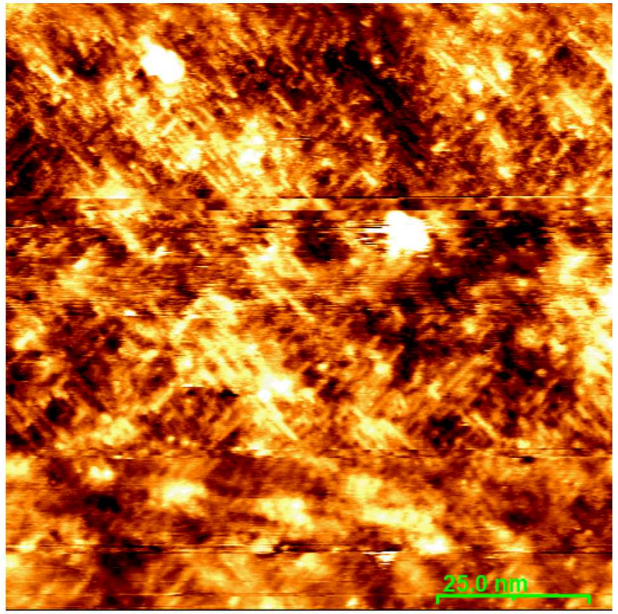
Wet chemistry

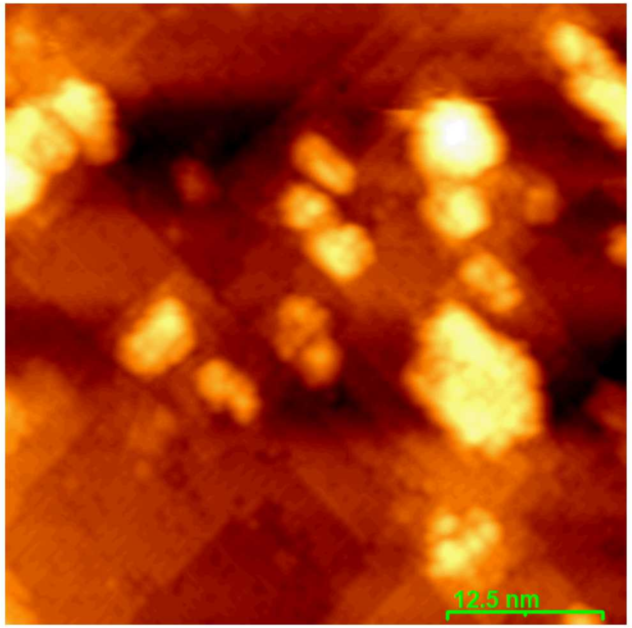
Not all FEOL is > 850° C.
Not all BEOL is < 450° C.

Wet chemistry - ambiguous

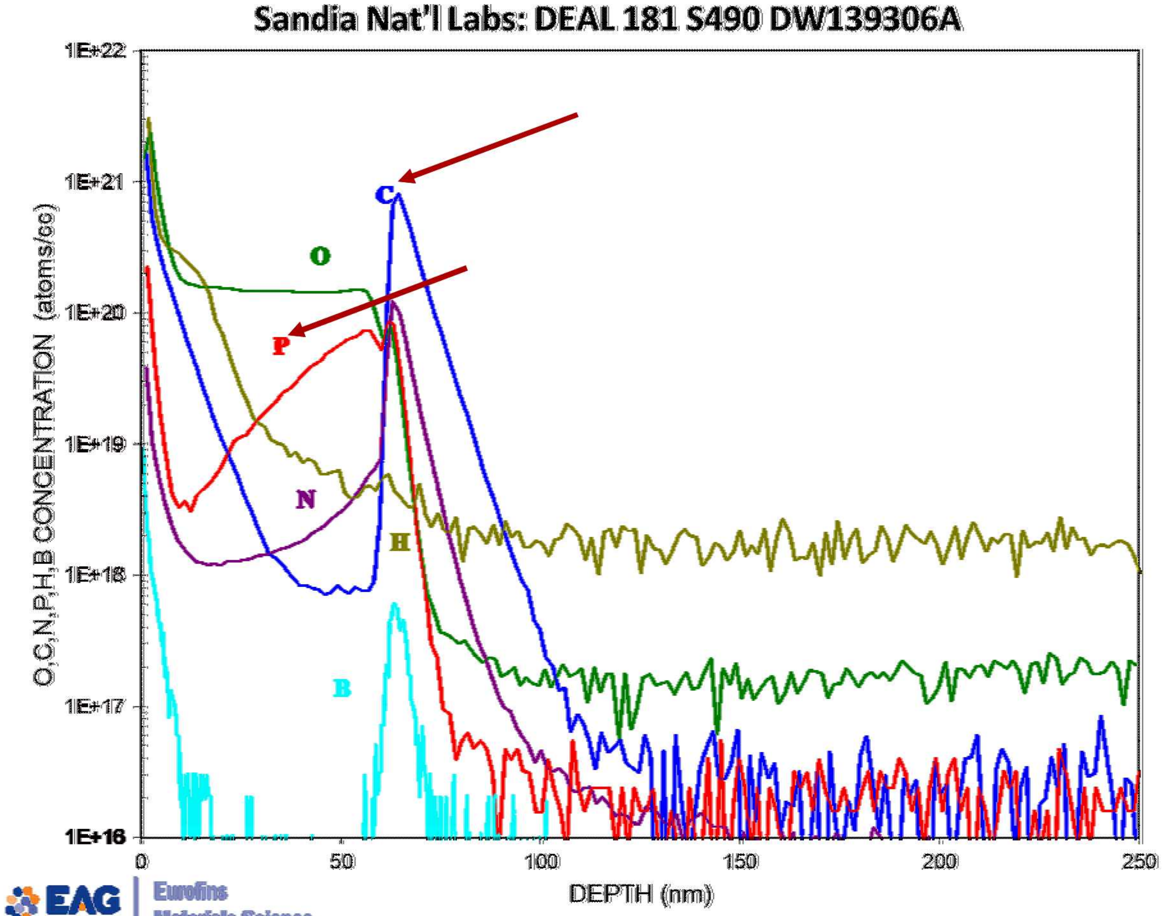
Piranha / NH_4F

Hines, J. Phys. Chem. C (2009)





After heating



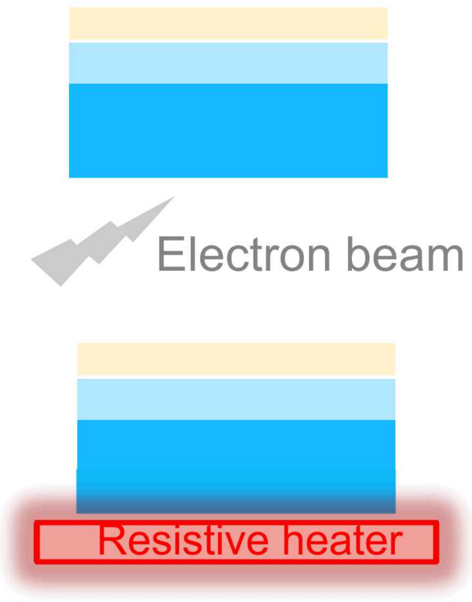
EAG Laboratories | Eurofins Materials Science

Reproduces results of paper, but it's not clean.

Cleanest low temperature processes are all reactive ion etches. (SiConi ~ 200° C)

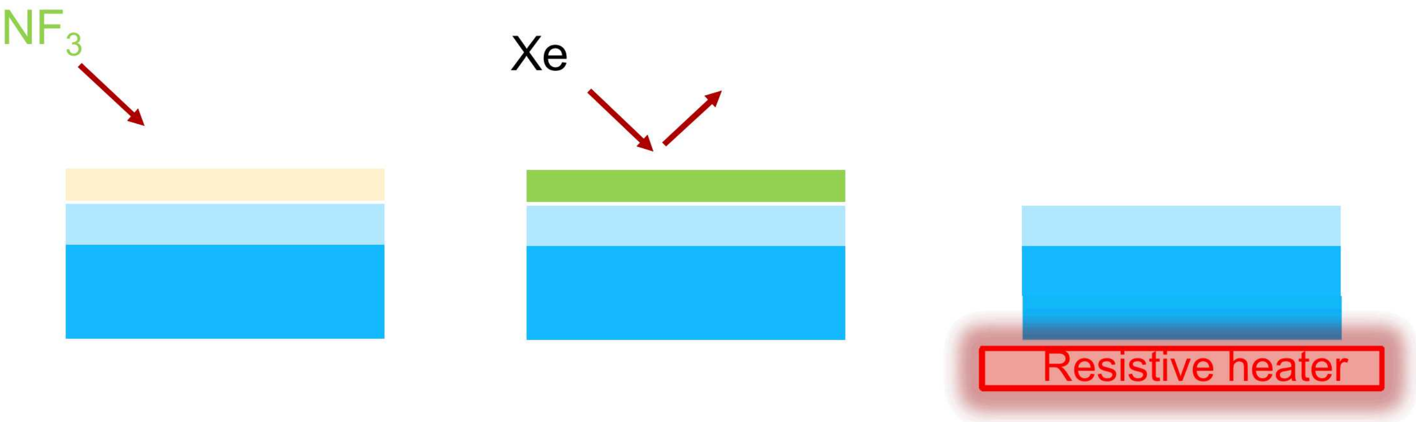
Modify APAM for Direct Integration

1. Heat sample with other technique



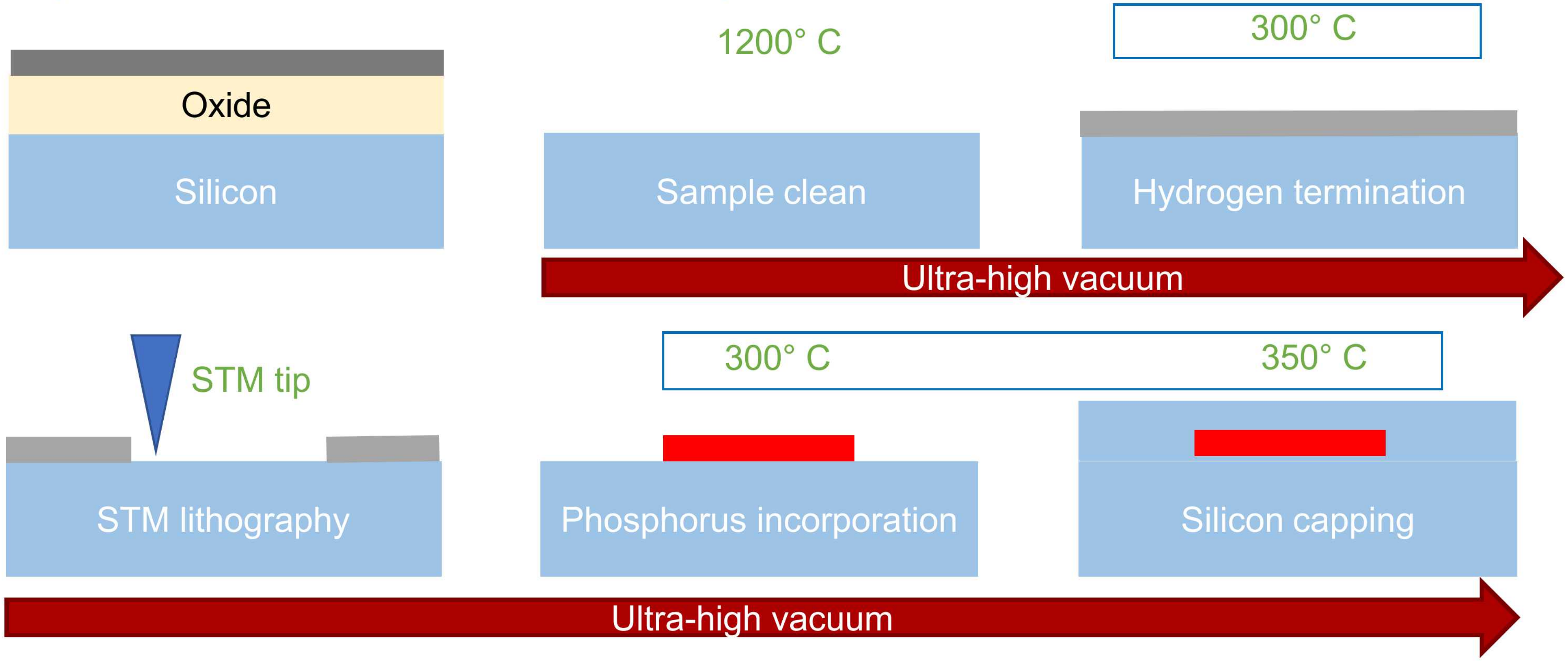
Next: effect of APAM process on CMOS circuit, effect of BEOL on APAM

2. Reactive ion etch



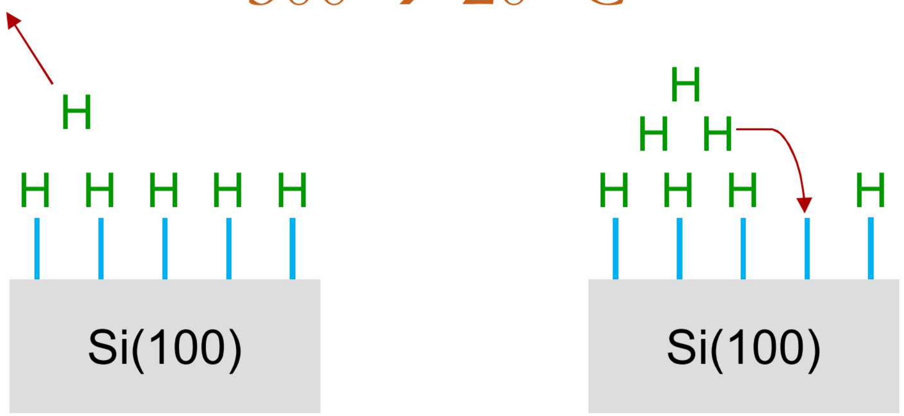
Next: make plasma-based home-made reactive ion etcher

Rest of process at reduced temperature?

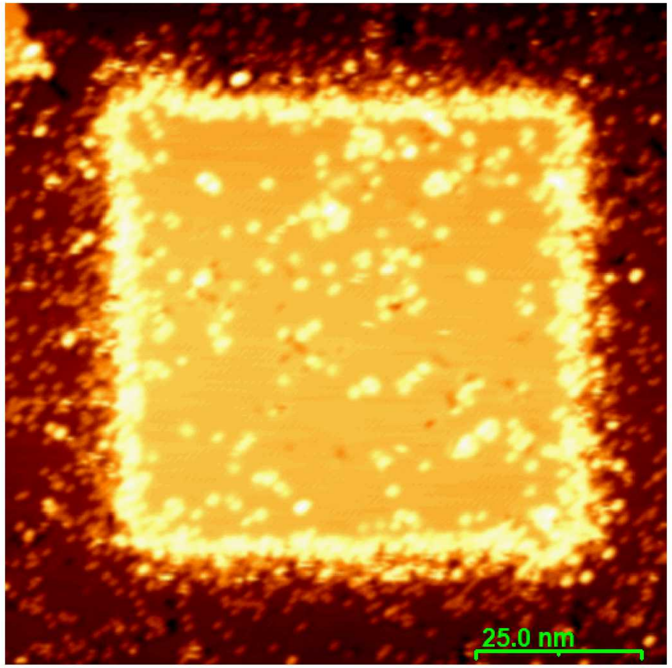


Hydrogen passivation & lithography

300 → 20° C



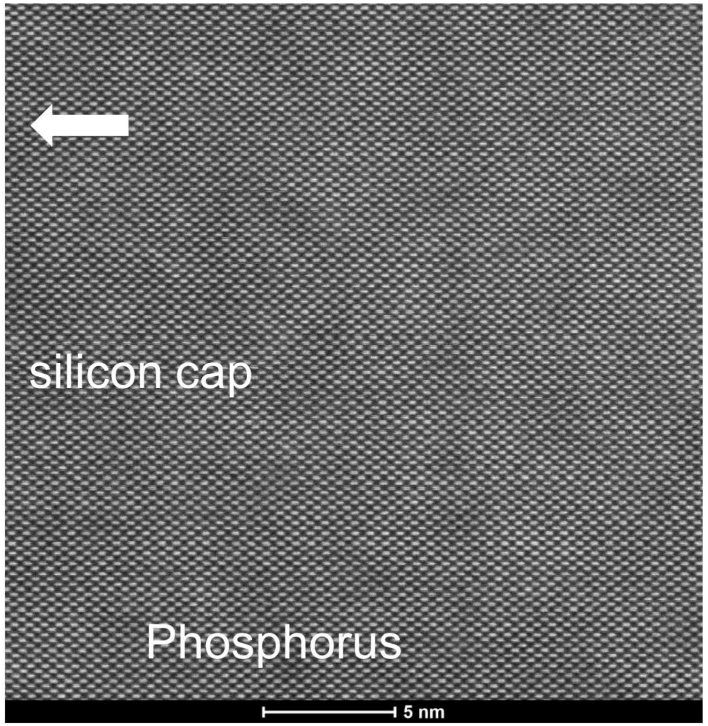
20° C: Hydrogen physisorbed on top of hydrogen passivated silicon



Lithography now requires multiple passes, but works great!

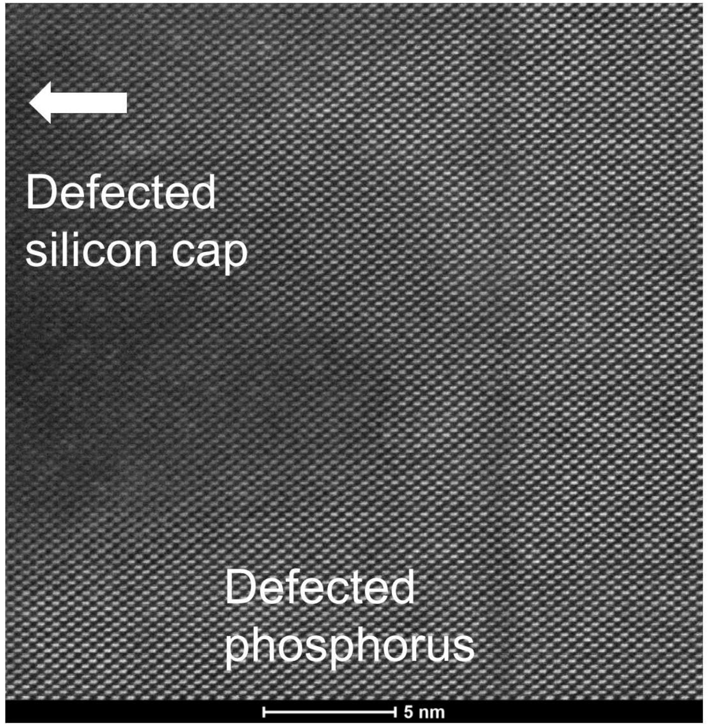
Phosphorus incorporation and capping

350 → 200° C



$n \sim 1.7 \times 10^{14}$ cm^{-2}
$\mu \sim 50$ cm^2/V-s
$\sigma \sim 2$ mS/sq.

Electrical transport at 4K not significantly affected

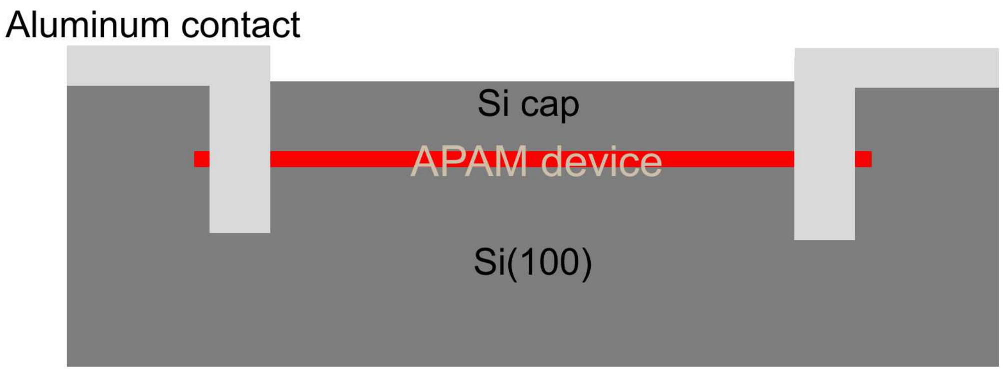


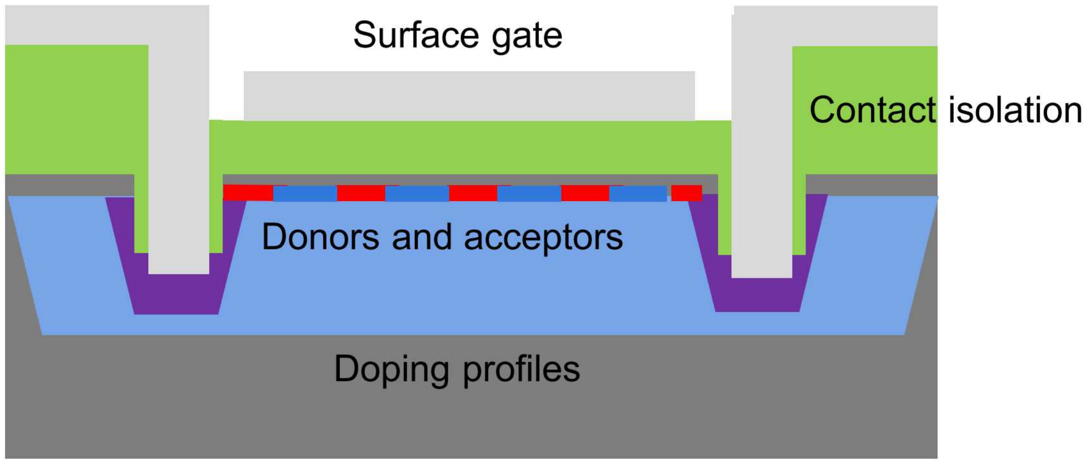
$n \sim 1.4 \times 10^{14}$ cm^{-2}
$\mu \sim 20$ cm^2/V-s
$\sigma \sim 0.6$ mS/sq.

Next: current density at room temperature across process conditions

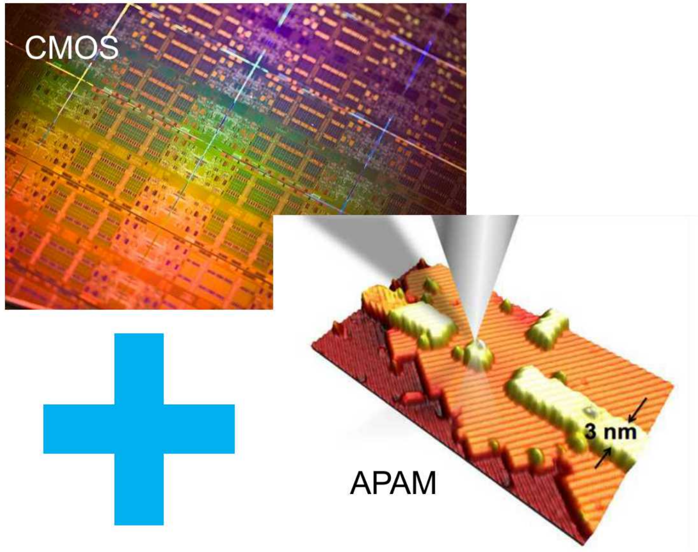
What is needed to apply APAM to digital microelectronics?

(A) Increase complexity of devices





(B) Integrate with CMOS



Thanks to the team.

Thrusts

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PM: Robert Koudelka
Deputy PM: Rick Muller

#1 APAM-enabled devices
Lead: Shashank Misra

#2 APAM modeling
Lead: Denis Mamaluy

#3 Integration
Lead: Dan Ward

#4 Application platform
Lead: George Wang

Support Team
Lead: Jennifer Woodrome
Financial: Laurel Taylor
Logistics: Lori Mann
Web: Dorean Chaleunphonh

Cross-cutting capabilities

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Microfabrication: Dan Ward, DeAnna Campbell, Mark Gunter, Philip Gamache, Steve Carr, Troy England, Reza Arghavani, Sean Smith

Modeling: Denis Mamaluy, Suzey Gao, Leon Maurer, Andrew Baczewski, Peter Schultz, Quinn Campbell, Juan Granado

Surface Science: Shashank Misra, Ezra Bussmann, George Wang, Aaron Katzenmeyer, Evan Anderson, Scott Schmucker, Esther Frederick, Fabian Pena, Dave Wheeler