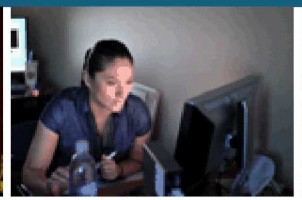
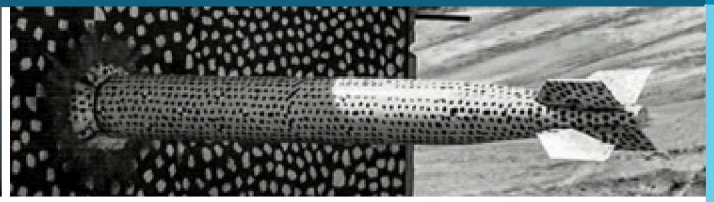
SAND2019-9133PE

GaN MISFET Trench Edge Calibrations





PRESENTED BY

Caleb E Glaser – NSME PhD Student

NANOSCIENCE & MICROSYSTEMS ENGINEERING

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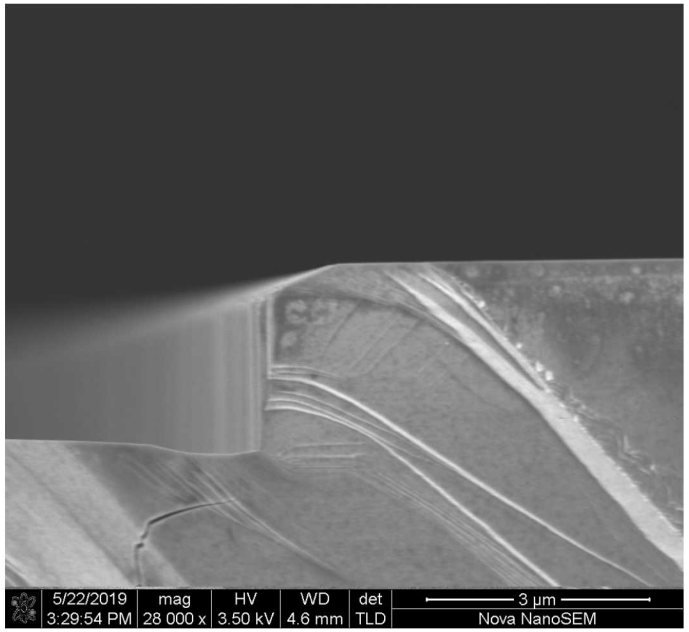
Outline

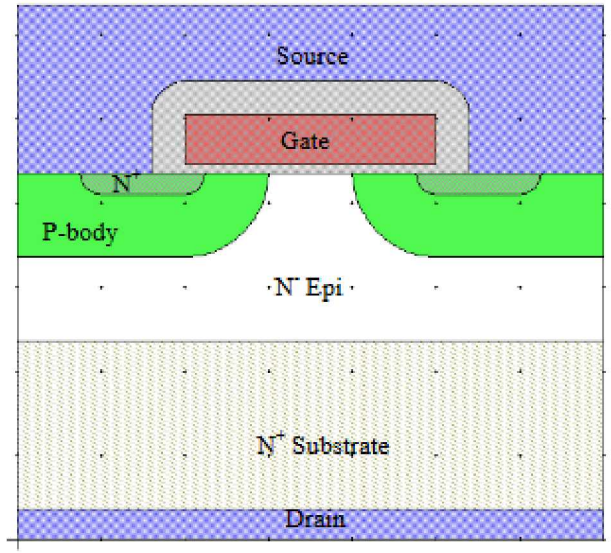
- MISFET trench design
- Trench processing steps
- Problems with trench topography
- Characterization of post etch steps
- Cause of curved trench edge
- Proposed solutions and mitigation of curved edge
- Future work



Goal of work : Determine cause of trench edge curvature and prevention

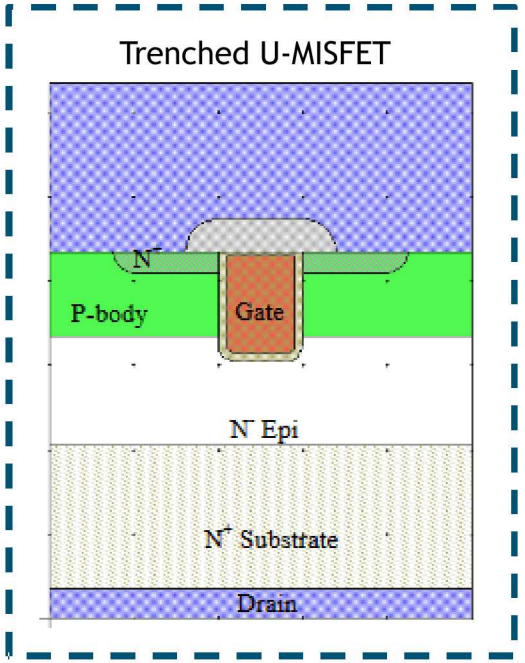
GaN MISFET Design

Planar D-MISFET



- P-body region and N+ source regions are doped using ion implantation, damaging epitaxial growth
- Channel is defined by lateral extension of junction and no voltage is required.
- Normally on – on when gate-source voltage is zero (negative voltage required to turn off)

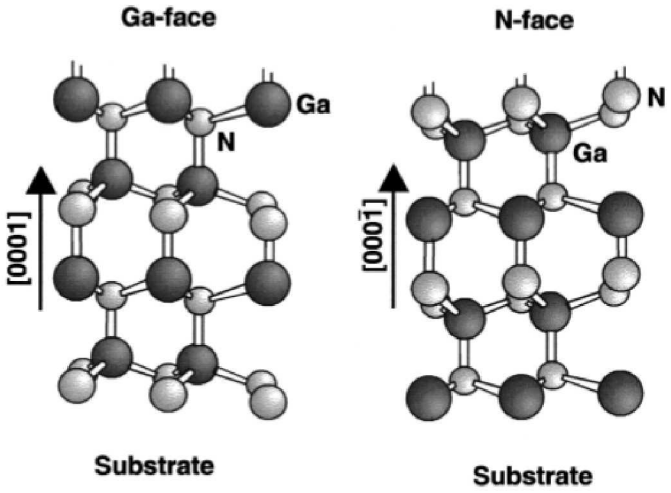
Trenched U-MISFET

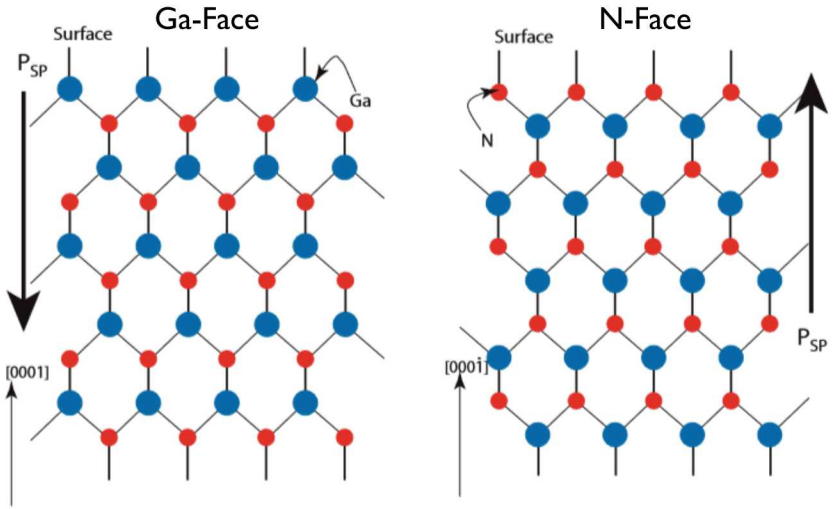


- Trench extends from surface through the N+ source and P-body into the N- Epi region.
- Can be doped during epitaxial growth without damage
- Normally off – off when gate voltage is zero (positive voltage required to turn on)

Importance of vertical trench edge

- Interface of III-V wurtzite crystals can change polarization
  - Influences charge density and electric field distribution
  - Orientation of each structure at the interface can change electrical properties
- Polarization at interface of AlGaN/GaN affects charge density of electrons and holes
  - Non-uniform trench angle alters polarization and electric field

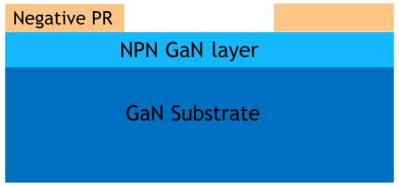




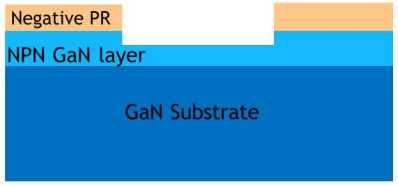
Simon, J. D. (2009). *Polarization-engineered III-V nitride heterostructure devices by molecular beam epitaxy* (Unpublished master's thesis).

U-MISFET fabrication steps

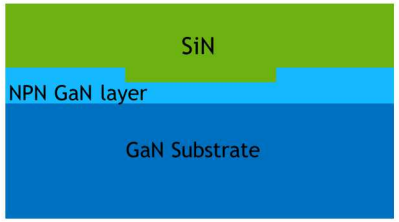
Step 1
Lithography Pattern



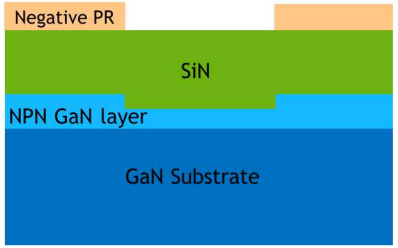
Step 2
GaICP Etch Alignment Marks



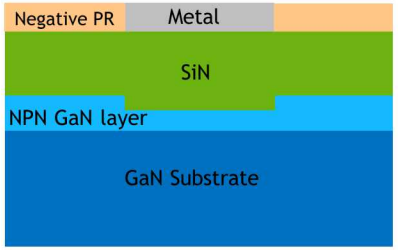
Step 3
CVD SiN Deposition



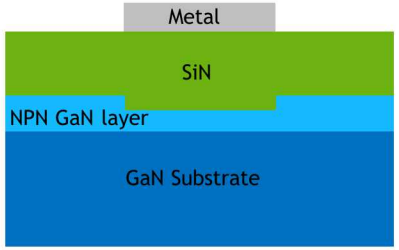
Step 4
Lithography Pattern



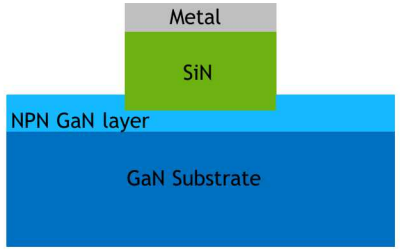
Step 5
Metal Deposition



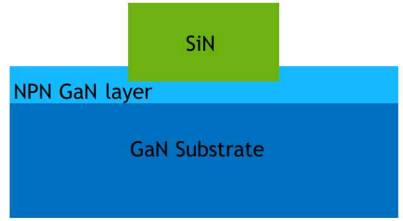
Step 6
Liftoff



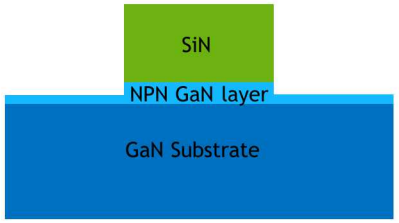
Step 7
RIE Nitride Etch



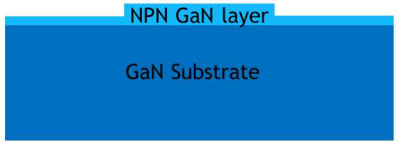
Step 8
Metal Wet Etch



Step 9
GaICP GaN NPN Etch

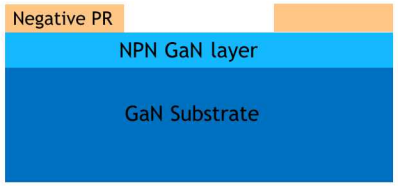


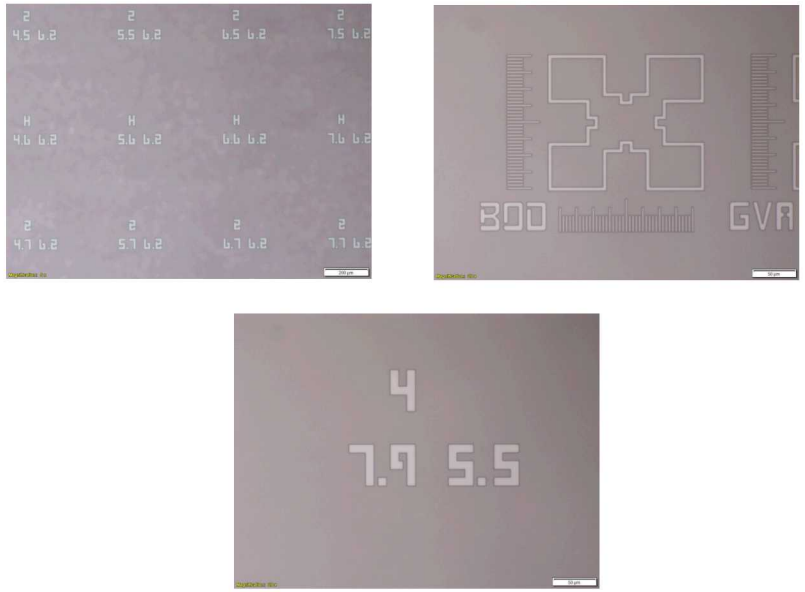
Step 10
HF SiN Removal



Fabrication steps cont.

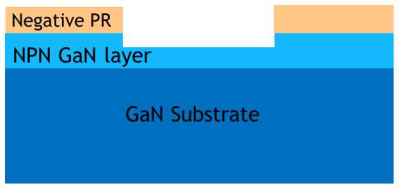
Step 1
Lithography Pattern

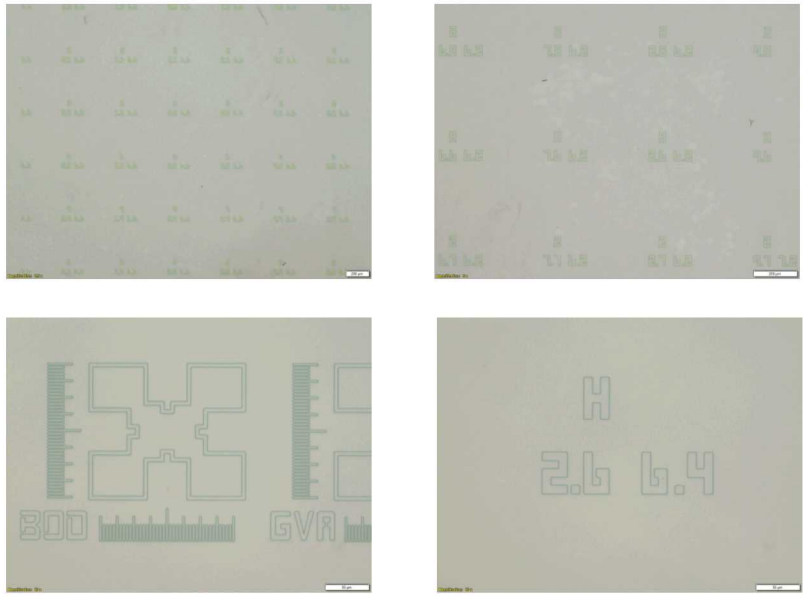




Lithography patterned using AZ 2020 negative resist (2 um thick). Selectivity of PR in GaICP is 2-3.

Step 2
GaICP Etch Alignment Marks

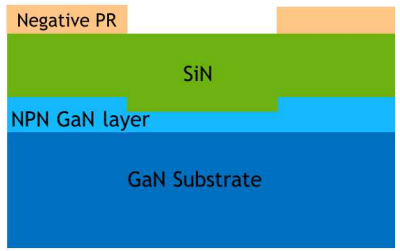




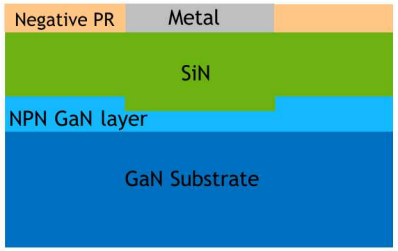
Shallow etch depth of alignment marks to 400-800 nm using BCl_3, Cl_2, and Ar. Etch time determined using cycles and calculated tool rates.

Fabrication steps cont.

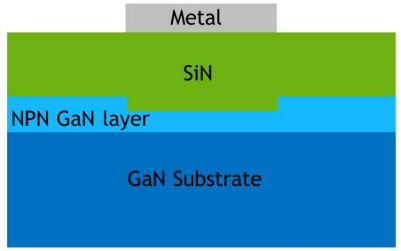
Step 4
Lithography Pattern

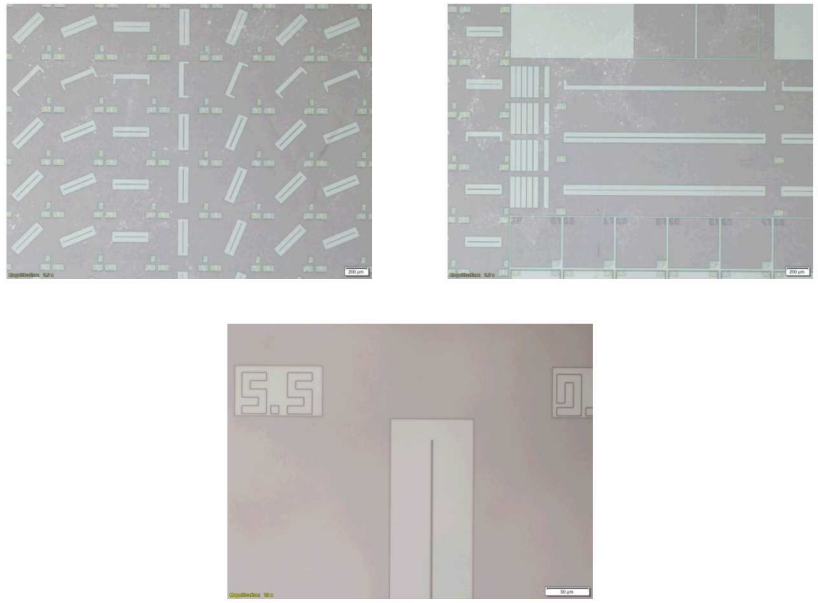


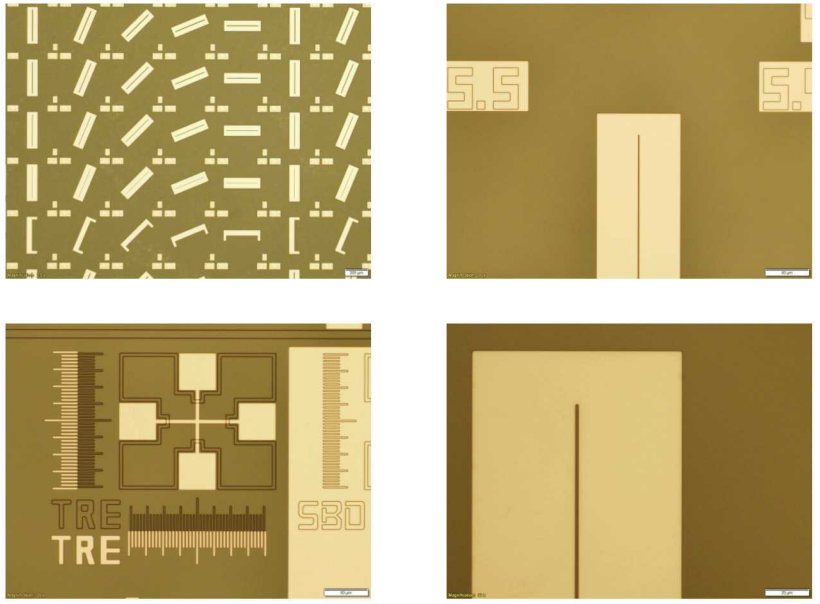
Step 5
Metal Deposition



Step 6
Liftoff



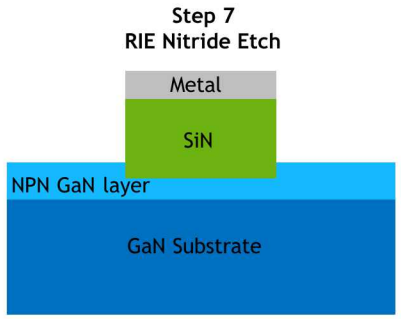


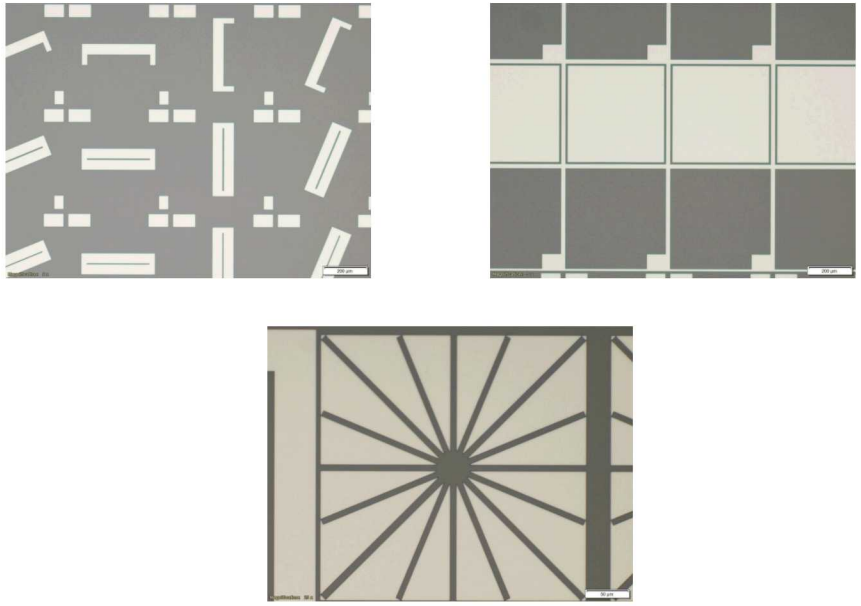


400-800 nm of SiN deposited through CVD covering alignment marks. AZ 2020 PR used to align to etched marks beneath the nitride layer.

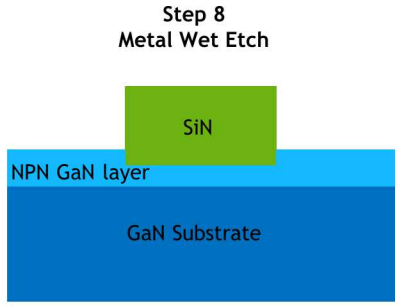
Metal deposited through evaporation with samples rotated above targets in chamber. Liftoff of pattern with acetone soak and spray.

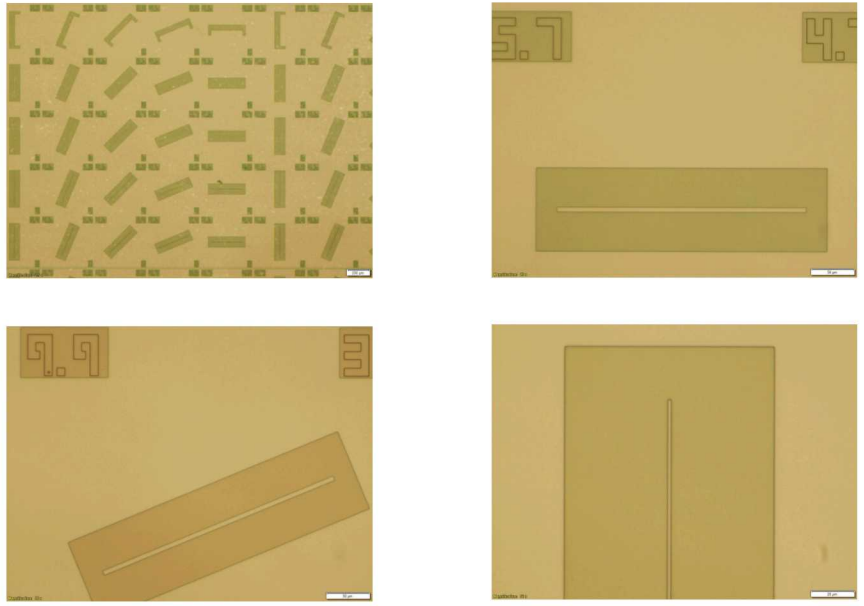
Fabrication steps cont.





Reactive ion etch used to remove SiN from the field using CF_4 and O_2.

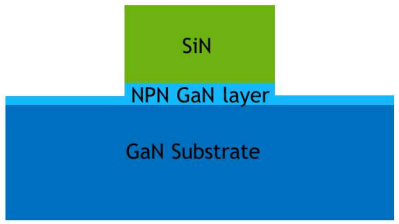


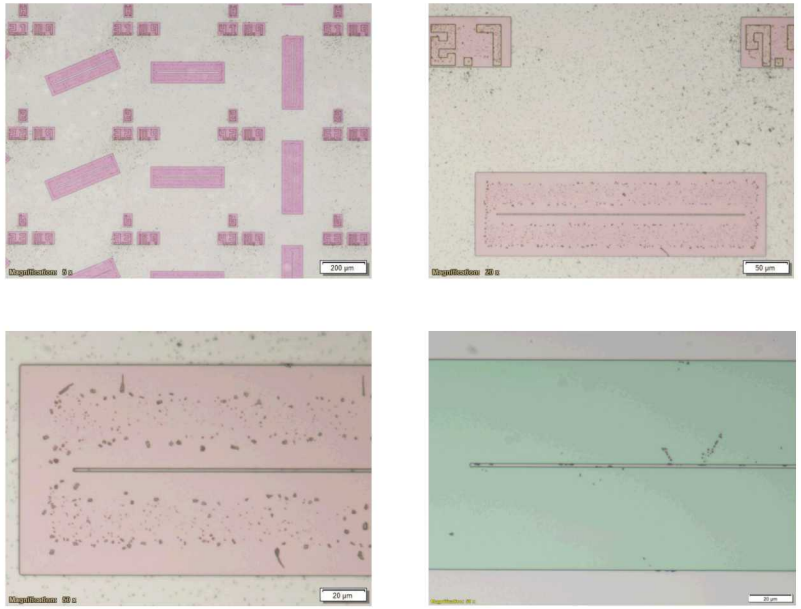


Beaker etching of metal layer to expose SiN mask on devices. Nickel etch using 2 H_2SO_4 : 1 DI. Titanium etch using 1 NH_4OH : 2 H_2O_2.

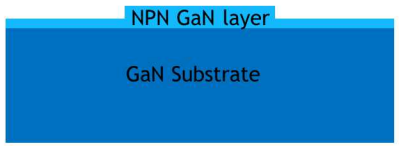
Fabrication steps cont.

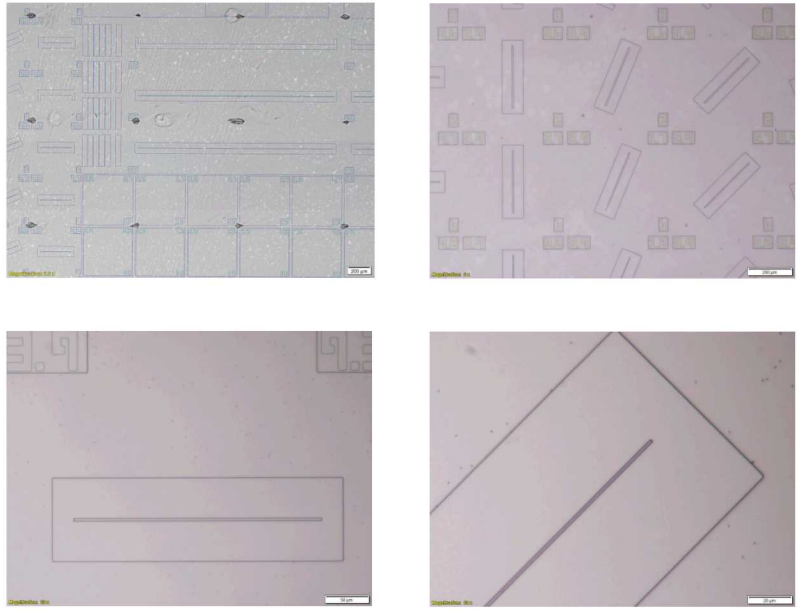
Step 9
GaICP GaN NPN Etch





Step 10
HF SiN Removal





Difference in color on devices is due to varying SiN thickness.

Beaker etching of remaining SiN on top of structures with 10 DI:1HF

Mask Selectivities

- RIE (SiN etch) - Ti/Ni Mask

Pre Etch (Å)	Post Etch (Å)	Post Mask Strip (Å)	Mask Remaining (Å)	Mask Etched (Å)	Selectivity
1681	10024	8627	1397	284	30.38
1681	9988	8743	1245	436	20.05
1681	10126	8728	1398	283	30.84
1681	10016	8754	1262	419	20.89
1635	5826	4307	1519	116	37.13
1635	5678	4312	1366	269	16.03
1635	5909	4327	1582	53	81.64

Metal Selectivity = SiN etched / Ti/Ni etched
- Mean – 33.85
- Median – 30.38

- GaICP (NPN GaN etch) – SiN Mask

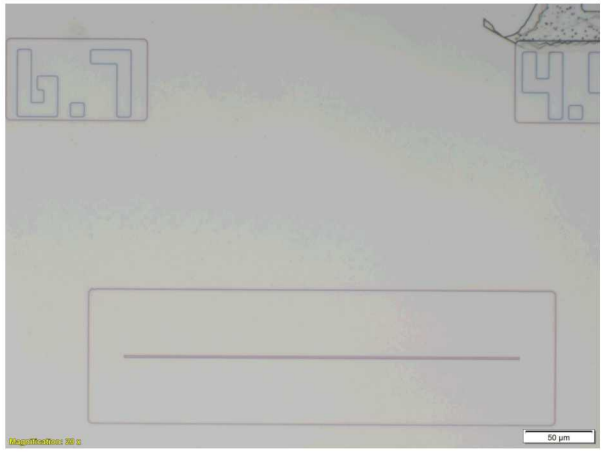
Pre Etch (Å)	Post Etch (Å)	Post Mask Strip (Å)	Mask Remaining (Å)	Mask Etched (Å)	Selectivity
8186	22000	17300	4700	3486	4.96
8186	21900	17300	4600	3586	4.82
8225	26400	22500	3900	4325	5.20
8170	26000	22300	3700	4470	4.99
4083	9554	6948	2606	1477	4.70
4085	9612	6779	2833	1252	5.41
4089	9413	6765	2648	1441	4.69
8224	26200	22500	3700	4524	4.97
8114	26000	22300	3700	4414	5.05

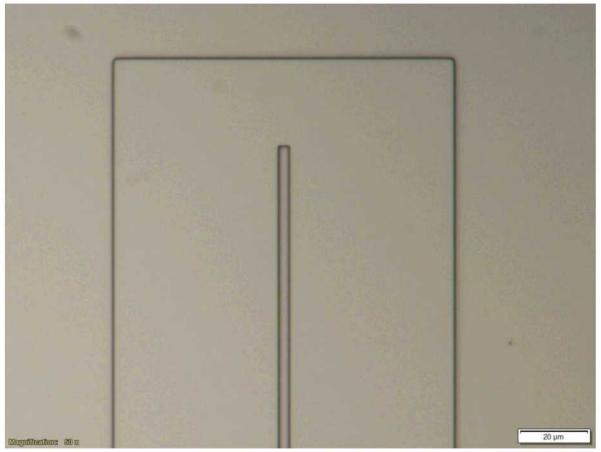
Nitride Selectivity = GaN etched / SiN Etched
- Mean – 4.98
- Median – 4.97

Note : Both masks are able to withstand their respective etch and maintain feature definition.

Chemical surface treatments

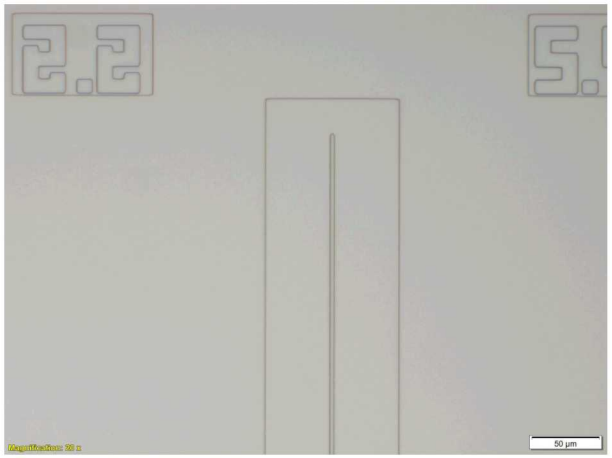
- 10:1 HF

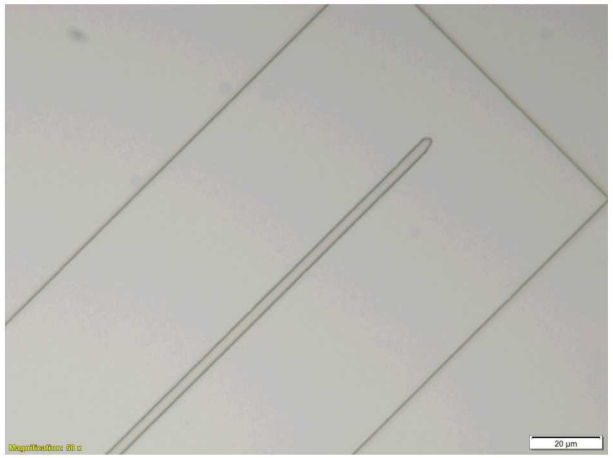




- AZ 400K developer at 80 ˚C
  - Potassium borate based buffered solution
  - Can be used both to develop PR and chemically treat the surface to remove etch damage from GaICP
  - Needed to create vertical sidewall

- AZ 400K Developer

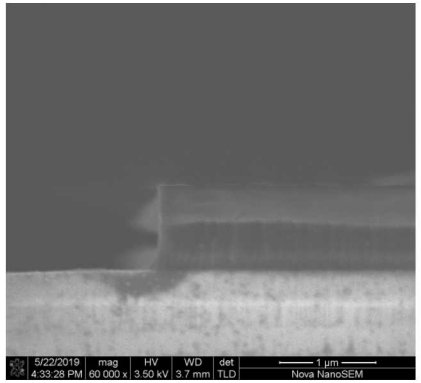


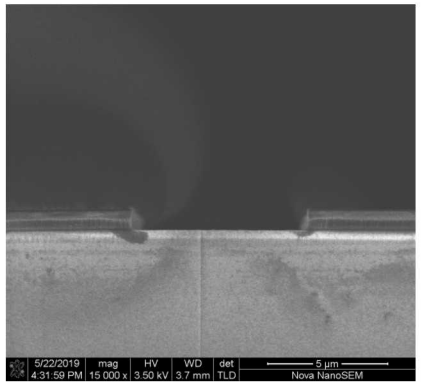


- Both HF and Developer treatment optically do not change the device structure or integrity.

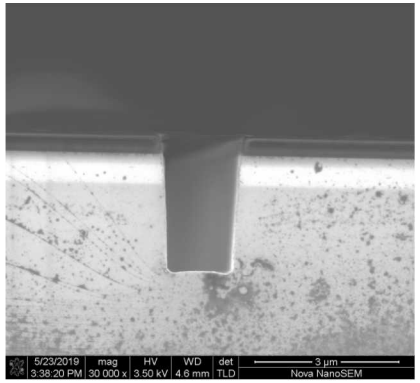
Cause of curved trench edge

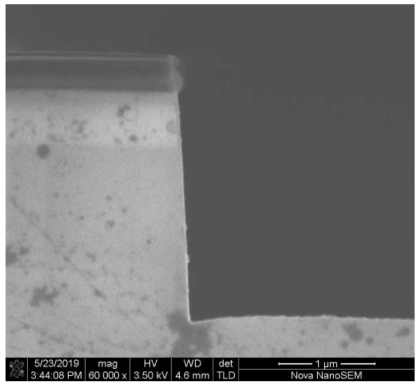
SiN RIE Etch only



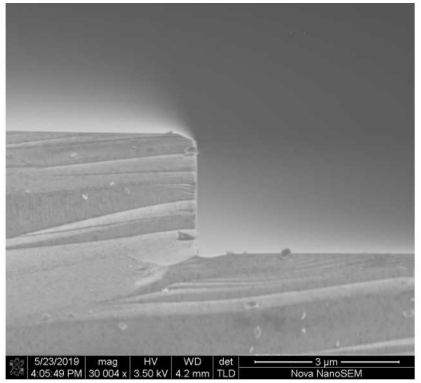


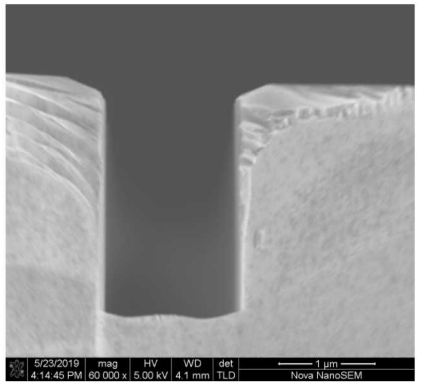
RIE + GaICP Etch



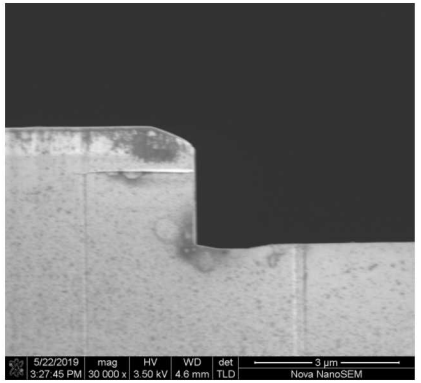


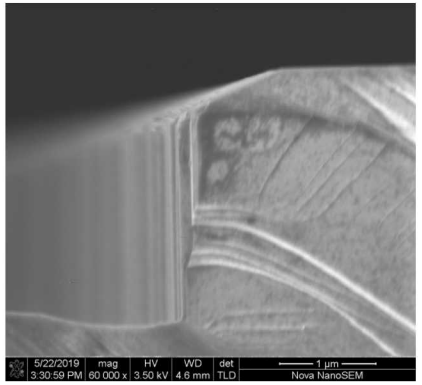
RIE+GaICP+10 min AZ 400K





RIE+GaICP+60 min AZ 400K



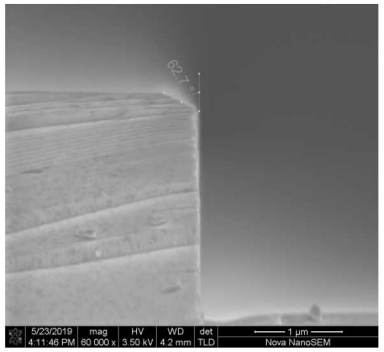


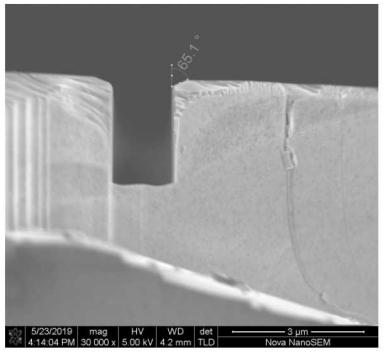
Cause of curved edge → AZ 400K developer

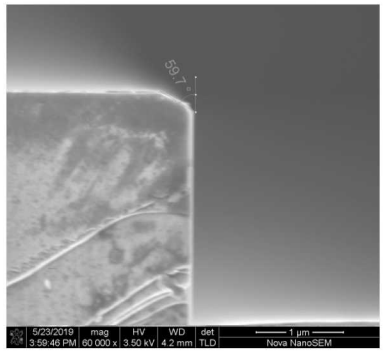
Increased time in solution → Increased edge curve

Angular dependence on etch time

10 min AZ 400K

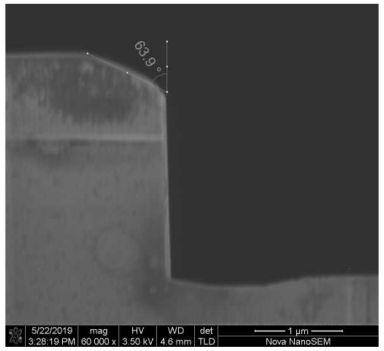


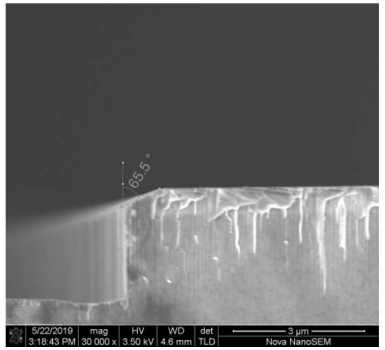


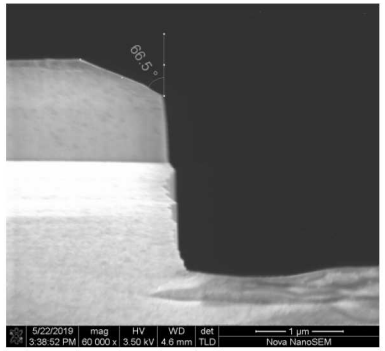


Mean angle ≈ 63°

60 min AZ 400K







Mean angle ≈ 65°

Angle of trench edge remains constant with increasing AZ 400K treatment time

Mitigation of curved step

Identified approaches to reduce curved edge

- Increase thickness of N layer and reduce AZ 400K time
  - Reduces impact of curve and distance etched into P layer
  - Maintain removal of etch damage
- Crystallographically oriented alignment marks
  - Etch alignment marks to exposed plane for alignment of subsequent mask layers
  - Can be very difficult to reach maintain adequate alignment

Summary

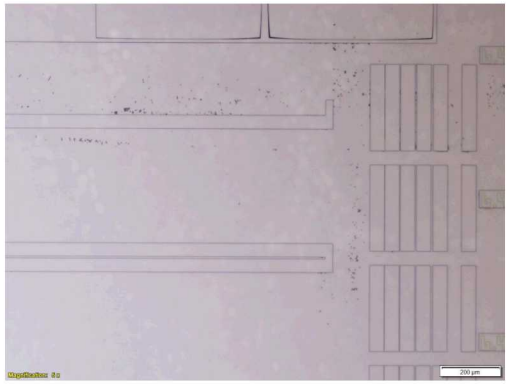
- Trench U-MISFET chose since it avoids implantation damage and is normally-off
- Vertical trench required to minimize polarization along AlGaN/GaN sidewall interface
- AZ 400K found to be cause of curved trench edge
  - Needed to remove surface damage from GaICP etch and make vertical sidewall
- Increased 400K time increases curved edge
  - Angle remains constant (65˚)
- Reduction of curved edge through increasing top N layer and reduction of AZ 400K time

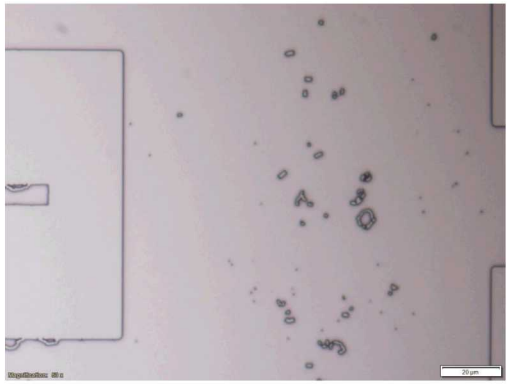
Future Work

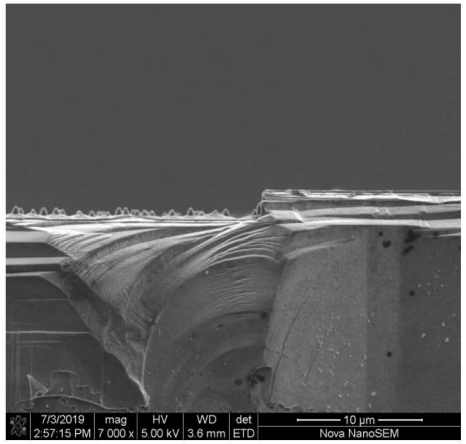
- Optimization of gate dielectric process
  - Interface trap densities
  - Analyze varying the dielectric use
- Fab simple devices to characterize process
  - Optimize design of devices to increase voltage and current performance

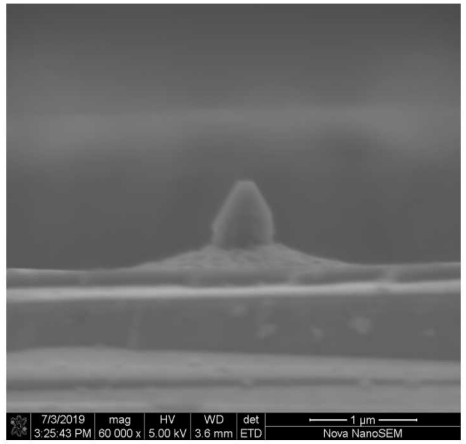
Additional problems

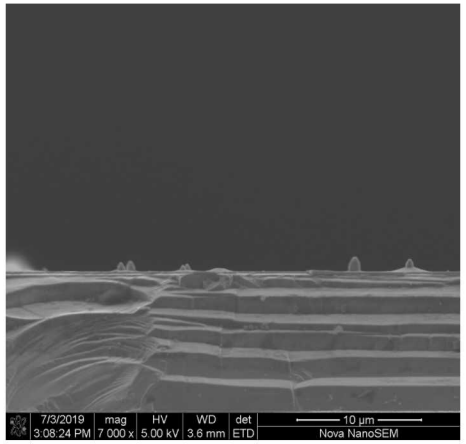
- Pyramidal/cone-shaped contaminants found along trenches after HF SiN removal
- Contamination uniform across wafer, but increased near devices parallel to wafer flat



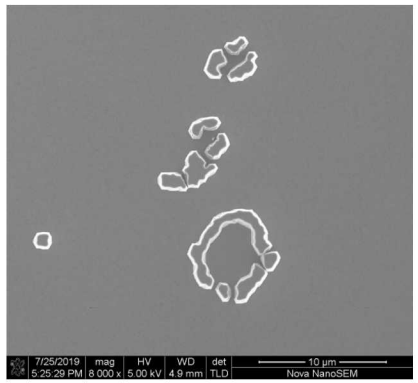


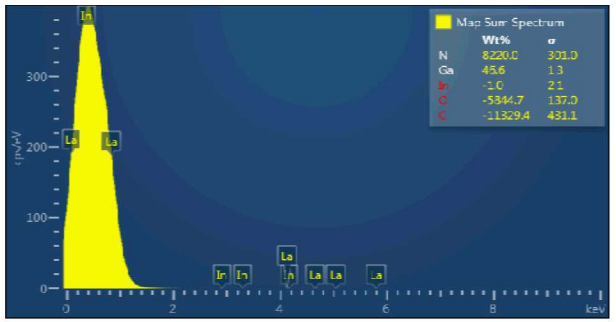




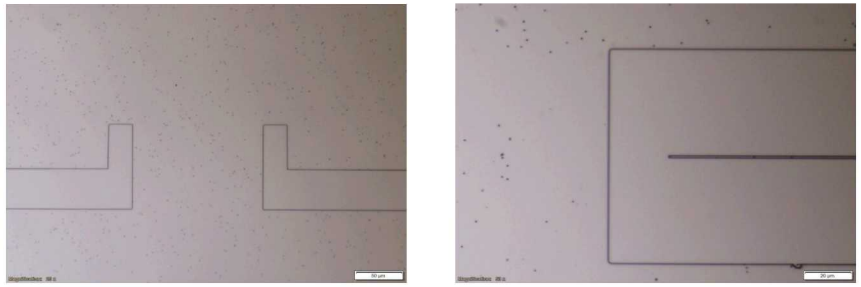


Additional problems cont.

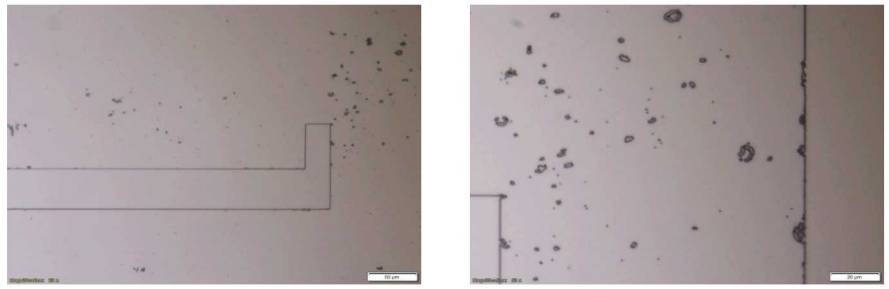




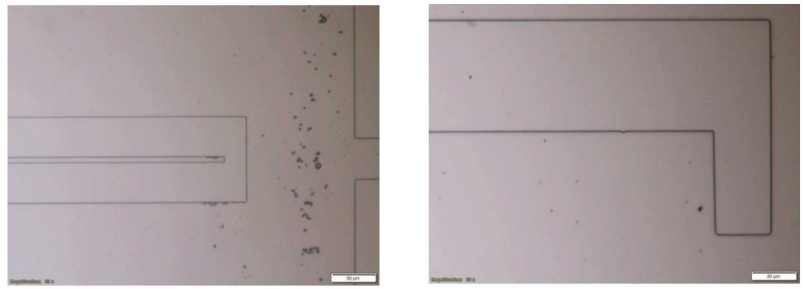
- EDX data inconclusive
  - Contamination appears to be organic
- Various cleaning methods used to reduce contamination



5 min O_2 Ash



10 min HCl



5 min Ash (O_2, N_2O, CO_2)