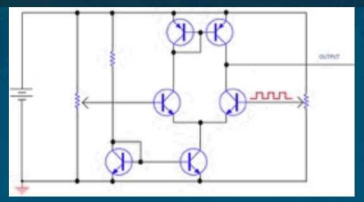
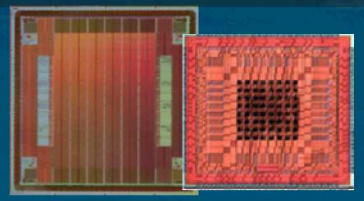
SAND2019-7962PE

AMS Verification Technologies and Flow for enabling POSH SoCs





PRESENTED BY

Eric Keiter, PI

Sandia National Laboratories

SAND2018-XXXX C

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Outline

Part 1: Xyce open source circuit simulator (Sandia)

`http://xyce.sandia.gov`

Part 2: FGPA Hardware Emulation (Yale)

The Xyce Analog Circuit Simulator

SPICE-Compatible syntax (Berkeley 3f5)

Not "Fast SPICE"

Two versions, **Serial** and…

Distributed Memory Parallel (MPI-based)

Unique solver algorithms

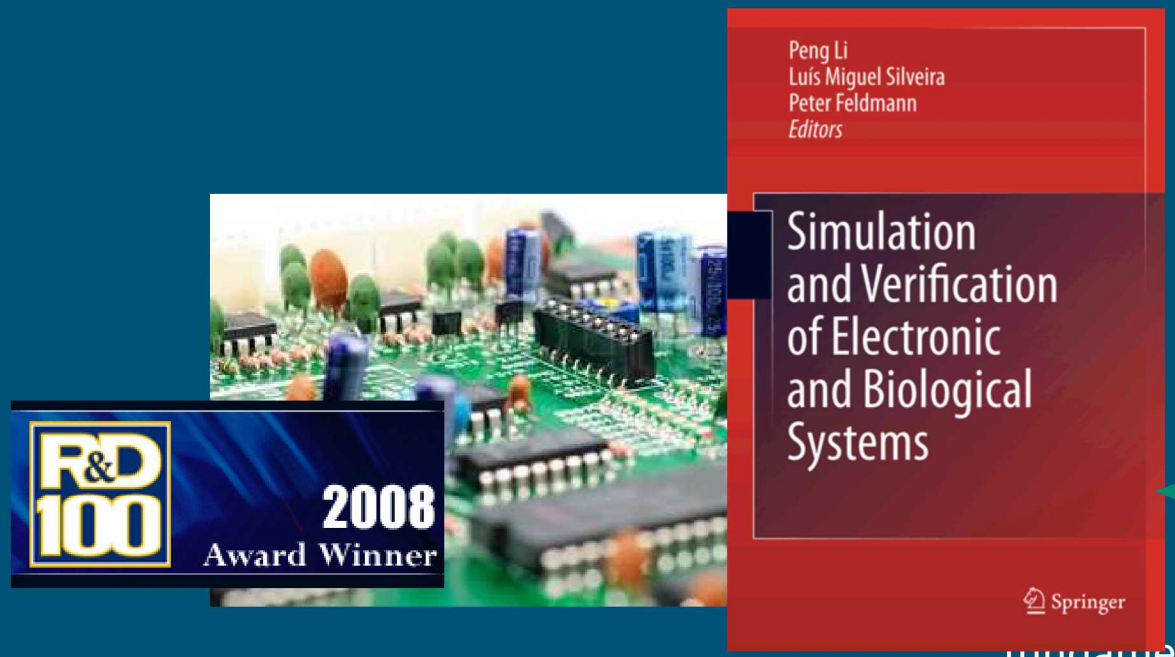
Industry standard models

Non-traditional models
- Neuron/synapse
- TCAD (PDE-based)

Open Source, GPLv3
- Since September of 2013 (Xyce 6.0)

Xyce Release 6.11.1
- June, 2019; 24th major release
- >4.700 registered downloaders

http://xyce.sandia.gov



Keiter, et al., "Parallel Transistor-Level Circuit Simulation"

fundamental research

Xyce Capabilities

Typical

DC, Transient, AC, Noise
- .DC, .TRAN, .NOISE, .AC (and .STEP)

Post Processing:
- Fourier transform of transient output (.FOUR)
- Post-simulation calculation of simulation metrics (.MEASURE)

Output (.PRINT)
- Text Files (tab or comma delimited)
- Probe (PSPICE)
- Gnuplot, TecPlot, RAW (SPICE 3f5)

Analog Behavioral Modeling

Expressions, functions, parameterizations…

Others

Harmonic Balance Analysis (.HB)
- Steady state solution of nonlinear circuits in the frequency domain

Random Sampling Analysis
- Executes the primary analysis (.DC, .AC, .TRAN, etc.) inside a loop over randomly distributed parameters

Sensitivities
- Computes sensitivities for a user-specified objective function with respect to a user-specified list of circuit parameters ($\partial O/\partial p$…)
- DC or Transient
- E.g., an output voltage's dependence on a capacitance

Obtaining Xyce

Xyce at Sandia

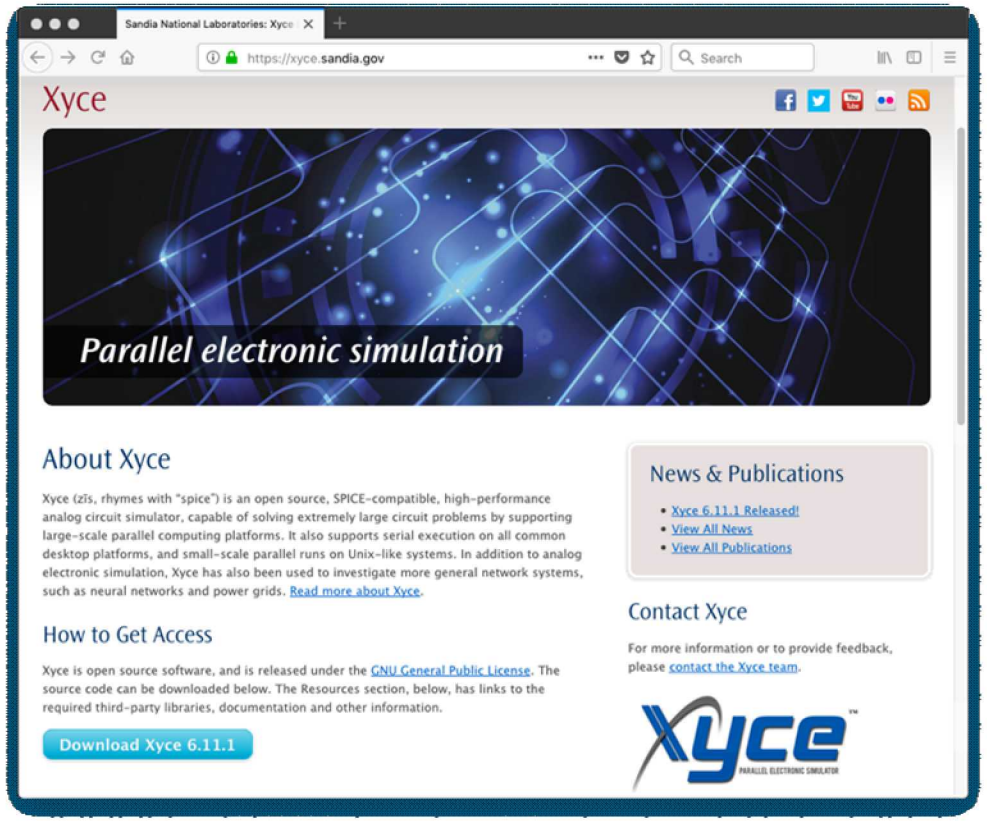
- **Binary executables** for Windows, OSX and Red Hat Enterprise Linux 6 & 7
- **Xyce** release source code, **build instructions** and more…

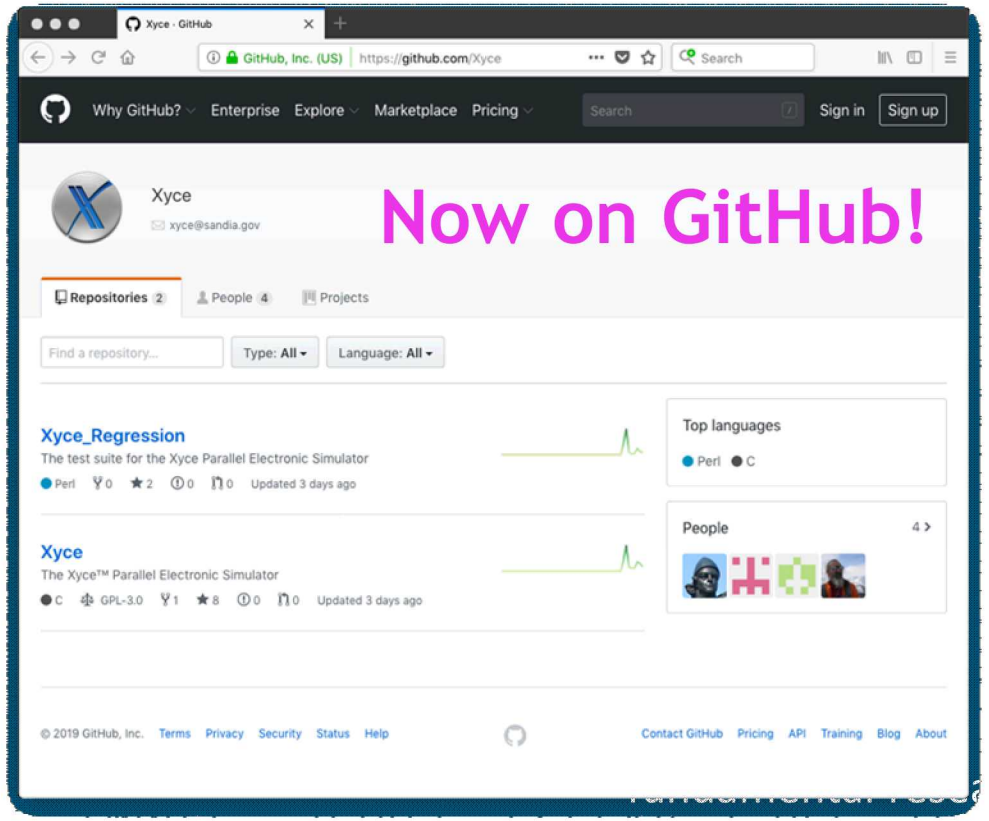
https://xyce.sandia.gov

GitHub

- For the latest **stable changes** to the **source code** between releases

https://github.com/xyce





Resources on the Sandia Site

Go to our website: Click on the download button, fill out form

At download page, many resources are available.

- **Binary executables** for Windows, OSX and Red Hat Enterprise Linux 6 & 7
- **Xyce Source code** and **build instructions**
  - If you do this, follow instructions carefully.
  - You must build the Trilinos library with the EXACT options we specify.
  - https://trilinos.org/
- **Regression test suite** (several thousand tests)
- **Documentation**
  - Users guide
  - Reference guide
  - Mathematical Formulation
  - Release notes
  - FAQ
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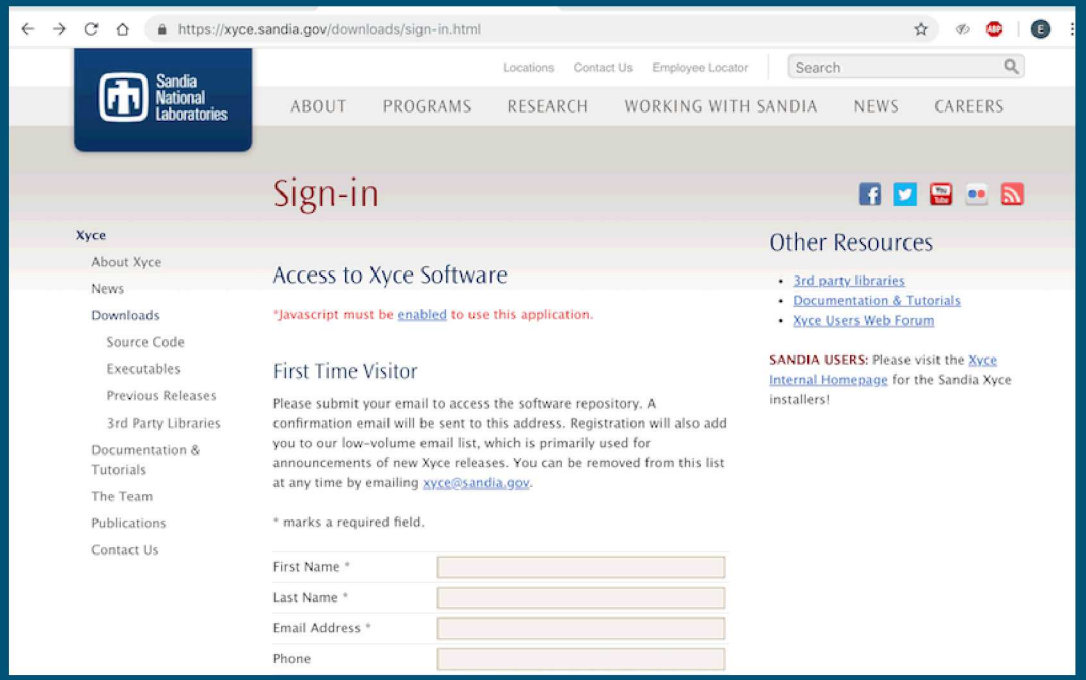

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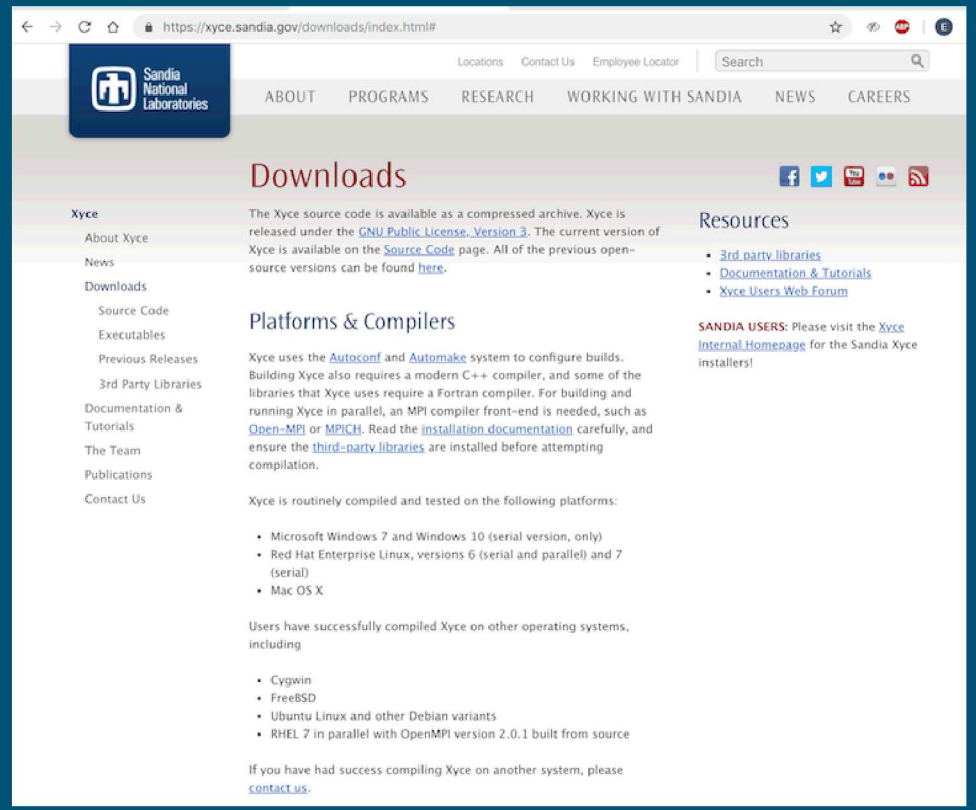

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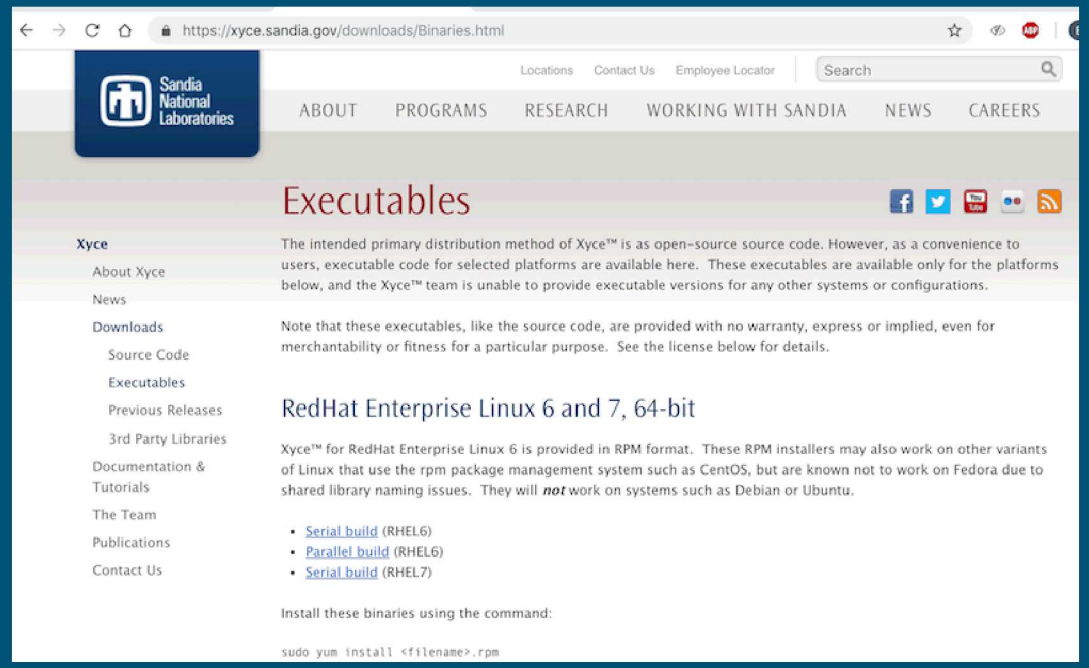

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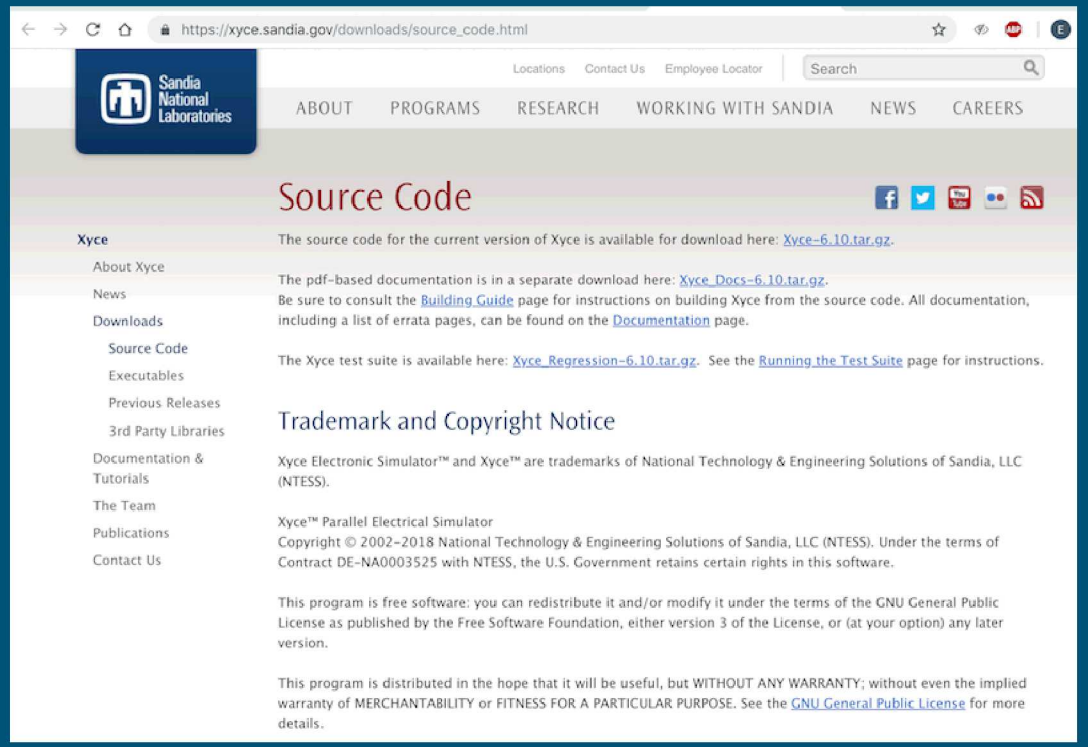

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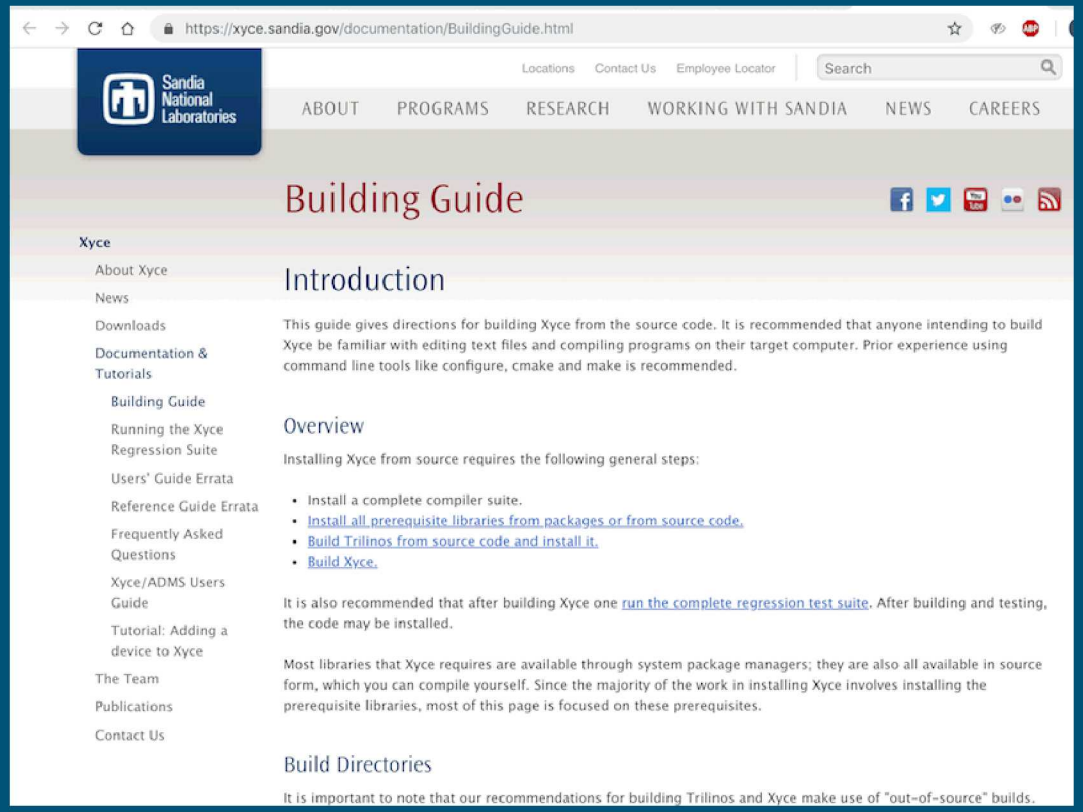

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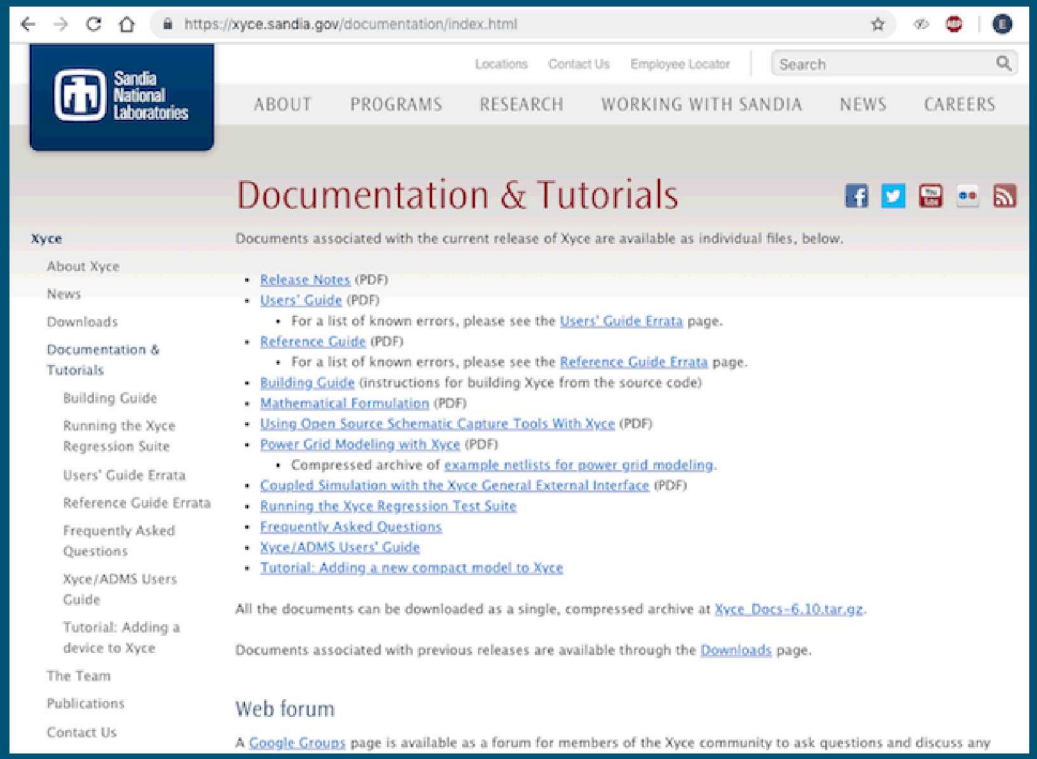


Xyce Release 6.11.1 Highlights

Initial S-parameter Analysis capability, including support for the P (port) device

HSPICE compatibility improvements

- Charge-based capacitor model
- Pattern (PAT) source function
- Parsing compatibilities (X for 10^6, nested delimiters, C-style ternary expressions, e.g.)
- `-hspice-ext` command line option for certain Xyce-incompatible HSPICE features

Improvements of .MEASURE

- .AC analysis now supported
- Added MEASFAIL, MEASDGT and MEASOUT

Parameter sensitivities

- .AC analysis now supported
- Transient direct sensitivities can now be processed using .FOUR

Performance enhancements and bug fixes

- Up to 4× speed enhancements for some simulations

HSPICE-to-Xyce Translations

HSPICE compatibility is the initial solution for making PDKs available to Xyce

Application Note available on the Xyce website

- Differences between HSPICE and Xyce (syntax and features)
- Viewing Xyce output files in WaveView
- A step-by-step guide for translating HSPICE to Xyce

The Xyce team has successfully translated

- GF 14nm PDK
- GF 65nm PDK
- and can help other performers with similar translations.

XDM Translator

- A tool for automatically translating HSPICE (& PSpice) netlists into Xyce syntax
- Should handle most translation tasks, with incompatible lines highlighted
- Available with the Xyce 7.0 release

Xyce 7.0

"Coming Soon"

Major features

XDM

Initial CMake refactor

- Improved ease of compiling Xyce on all platforms
- Robust against variations in third-party libraries, particularly Trilinos
- Streamlined and faster configuring on all platforms

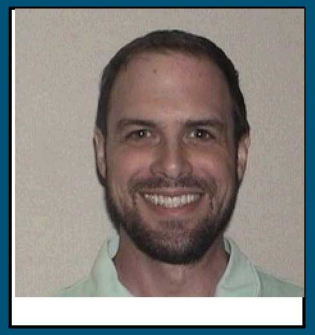
Also

- More HSPICE compatibility improvements
- More performance improvements

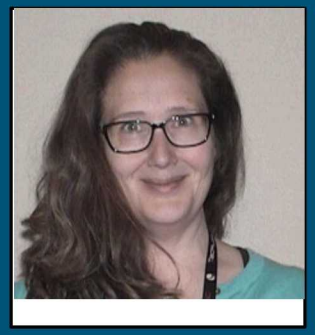
Xyce Resources

This week, we are here:

Eric Keiter, Sandia
- Circuit simulation, Xyce
- UW-Madison, Plasma Simulation



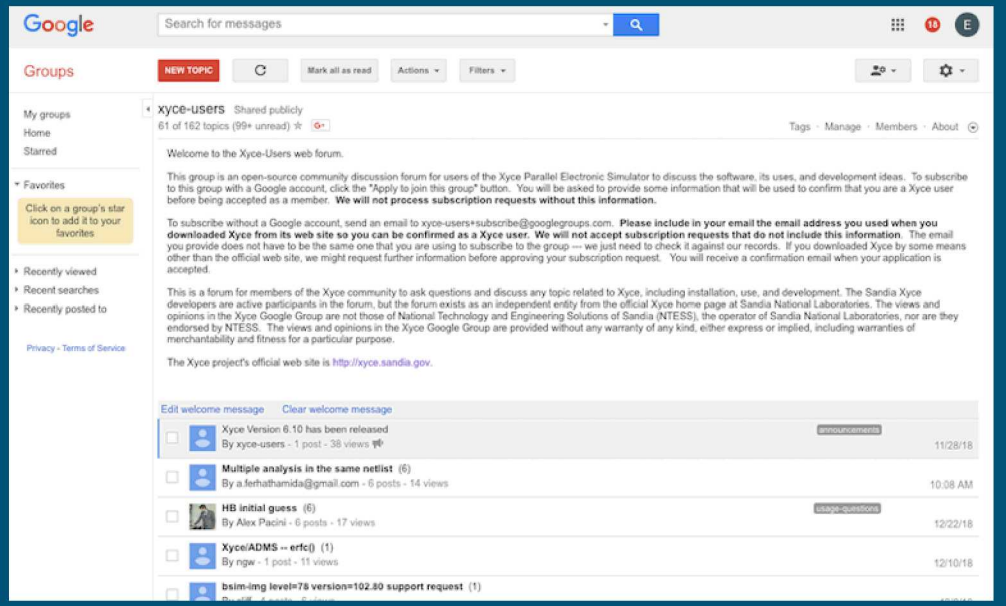
Jason Verley, Sandia
- Circuit simulation, Xyce
- Colorado School of Mines, Solid-State Physics



Heidi Thornquist, Sandia
- Parallel algorithms
- Linear solvers
- Model order reduction
- Rice University, Applied Math

After this week:
- Tutorial Videos (on documentation website)
- Feel free to contact us (me) directly
- Xyce mailing list: **xyce@sandia.gov**
- Xyce google group:

https://groups.google.com/group/xyce-users



Xyce Team Acknowledgements

Eric R. Keiter

Thomas V. Russo

Richard L. Schiek

Heidi K. Thornquist

Ting Mei

Jason C. Verley

Peter E. Sholander

Karthik V. Aadithya

…and many others

Contact:

`http://xyce.sandia.gov`
`xyce@sandia.gov`

Google Group Forum:

`https://groups.google.com/group/xyce-users`

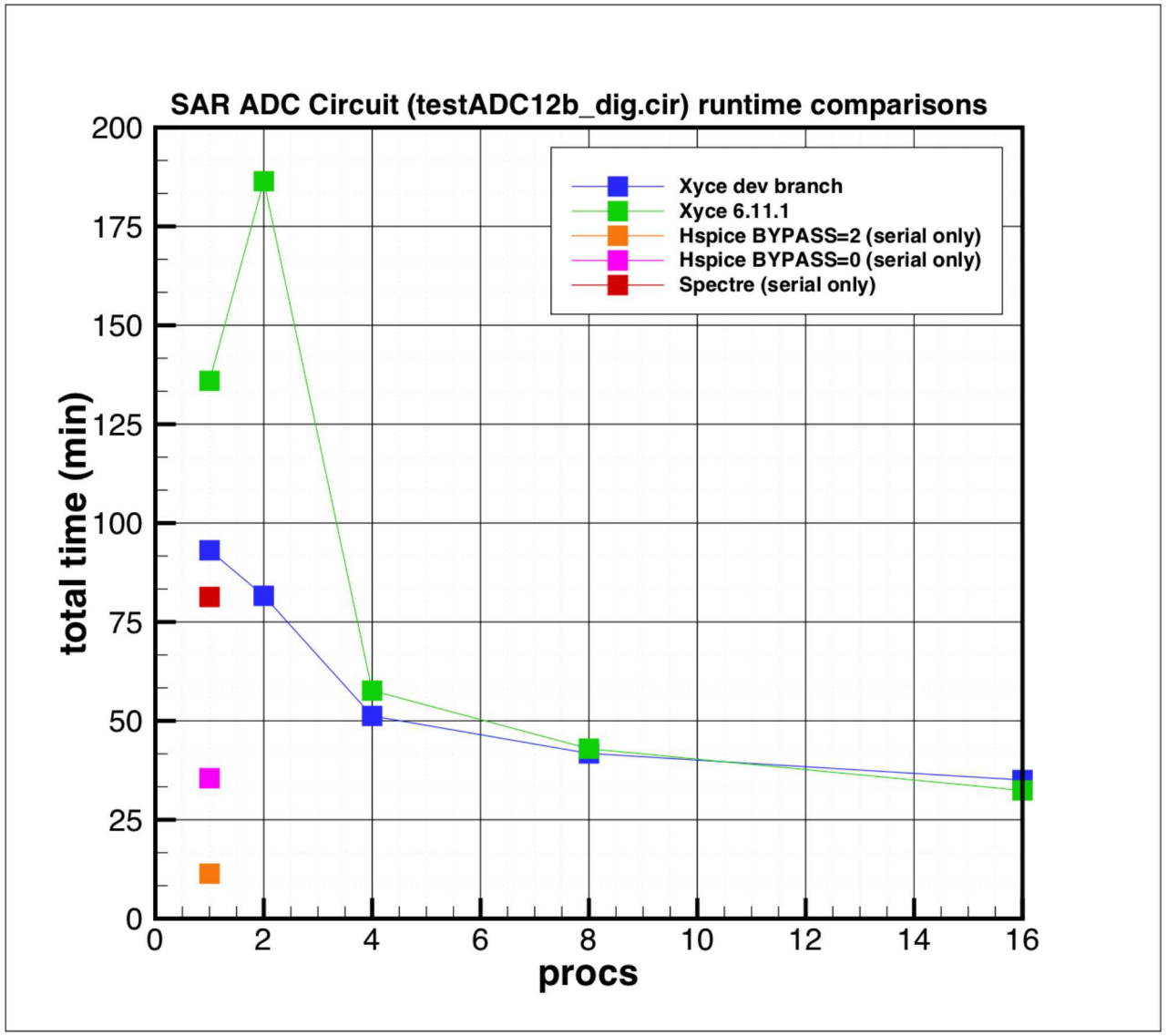
fundamental research

Xyce Demo

SAR ADC timings, Xyce vs Hspice and Spectre

Recent efficiency improvements to Xyce have brought it close to Spectre for one processor.

Still work to do to catch Hspice. Some of the difference is due to BYPASS, which is present in Hspice, but not Xyce or Spectre.



Comparison of SAR ADC Result, Xyce vs Hspice

Results match well. RMS Errors small

RMS relative error in v(sync) is 0.0434905680015374%

RMS relative error in v(po<0>) is 0.0232474456164593%

RMS relative error in v(po<1>) is 0.023581461963474%

RMS relative error in v(po<2>) is 0.025830825117 86%

RMS relative error in v(po<3>) is 0.0240096727254828%

RMS relative error in v(po<4>) is 0.0166525520072121%

RMS relative error in v(po<5>) is 0.00929693070847055%

RMS relative error in v(po<6>) is 0.0309201017241085%

RMS relative error in v(po<7>) is 0.0230237794341722%

RMS relative error in v(po<8>) is 0.0259005260949305%

RMS relative error in v(po<9>) is 0.0175662606806119%

RMS relative error in v(po<10>) is 0.00940986678122403%

RMS relative error in v(po<11>) is 0.00976999004888706%