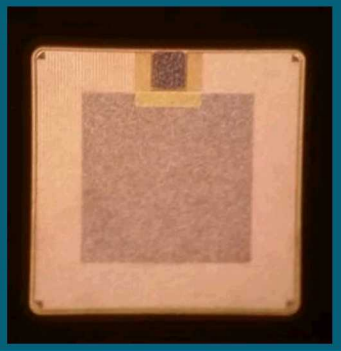
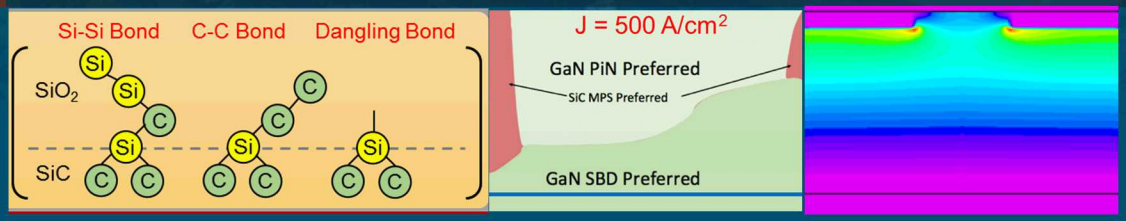
SAND2019-7248PE

VTO Electric Drivetrain Consortium Keystone #1: Power Electronics Device Research Strategy Overview





Bob Kaplar

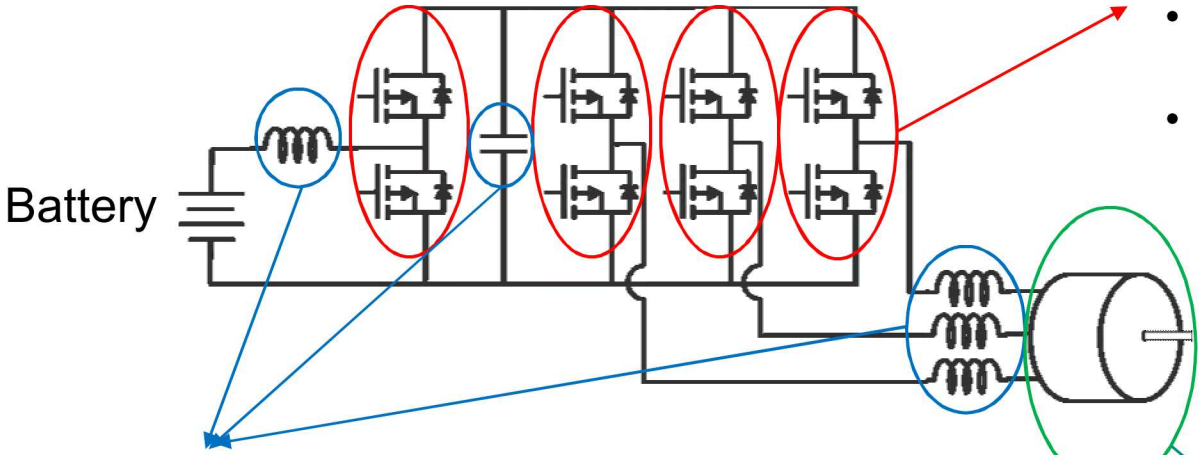
Sandia National Laboratories

June 25, 2019

Objectives

- Power electronics density target = 100 kW/L
- Power target = 100 kW (1.2 kV / 100 A devices)
- Cost target = $6/kW
- Operational lifetime target = 300k miles
- Barriers:
  - Commercial SiC devices may not be designed specifically for automotive environment
  - Commercial GaN HEMTs (lateral devices) are typically low-voltage (< 650 V), questions exist concerning reliability (heteroepitaxy)
  - Relative immaturity of vertical GaN devices (performance and reliability)
  - Relative immaturity of passive materials relative to semiconductors (performance / reliability)

Approach – System Level View



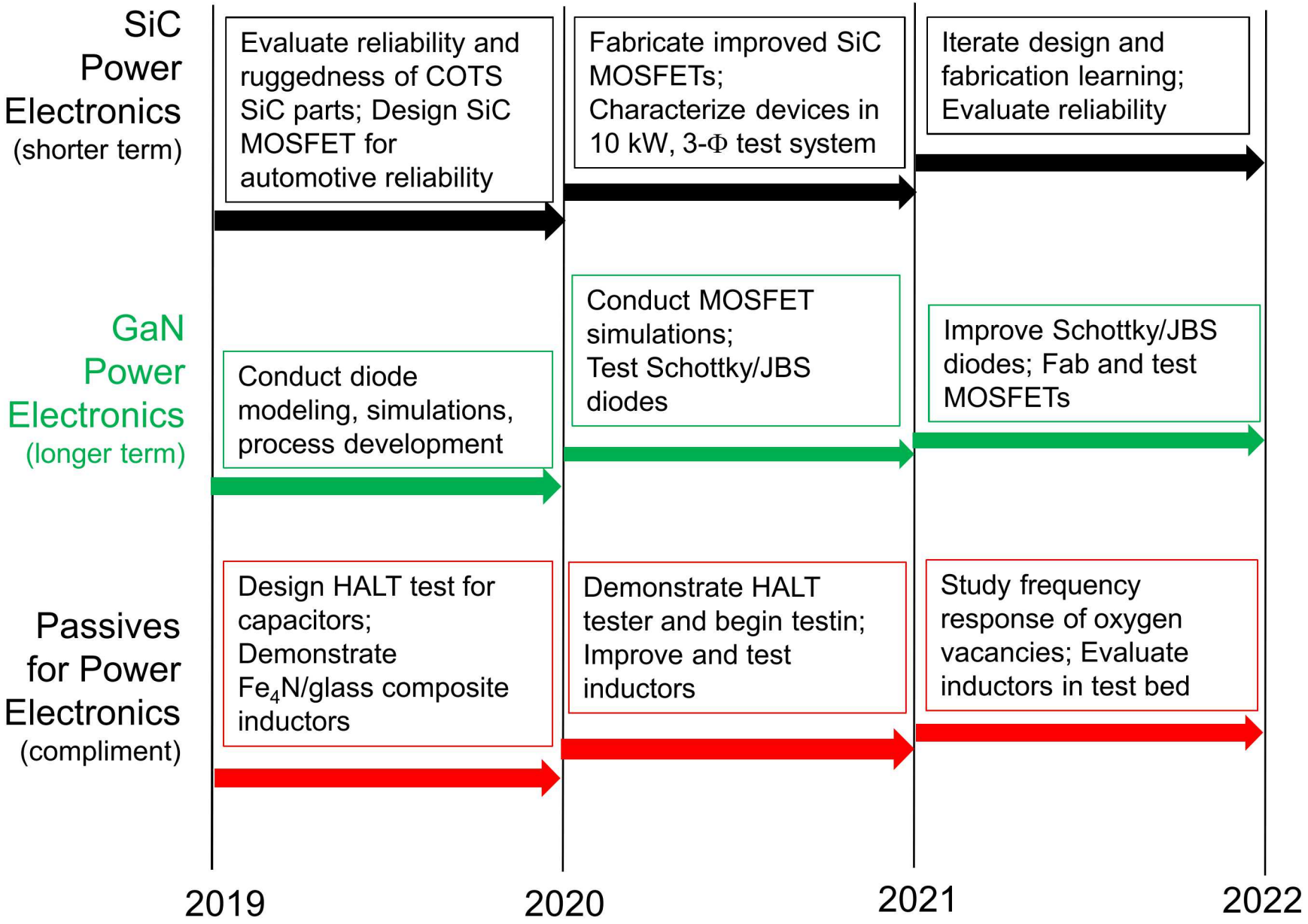
- Power Electronic Devices:
  - SiC or GaN-based
    - Higher critical E-field
  - Higher-frequency operation
    - Increased power density
    - Reduced size / weight

- Passives for Power Electronics
  - Composite materials for improved inductors
  - Improved capacitor lifetime, operating modes
  - Higher-frequency operation
  - Reduced size / weight

- Advanced Motor Designs:
  - Increased power density
  - Higher speed operation
    - Reduced size / weight

- Characterization efforts at each point in the system:
  - Power electronic devices, passives, motors
- Consortium efforts span multiple levels within system design

Approach – Materials for Power Electronics



Consortium Device Team

- Sandia power electronics team
  - Vertical GaN devices: Greg Pickrell, Andy Allerman, Mary Crawford, Jeramy Dickerson, Andrew Binder
  - Device subcontractors: Jon Wierer (Lehigh), Jim Cooper (Purdue/Sonrisa)
  - SiC, power converters, and passives: Jack Flicker, Jason Neely, Lee Rashkin, Todd Monson, Jon Bock
- SiC devices (design / fab / test)
  - Anant Agarwal (Ohio State), Woongje Sung (SUNY)
- Lateral GaN devices
  - Shadi Shahedipour-Sandvik (SUNY)
- GaN device testing
  - Victor Veliadis (NCSU)

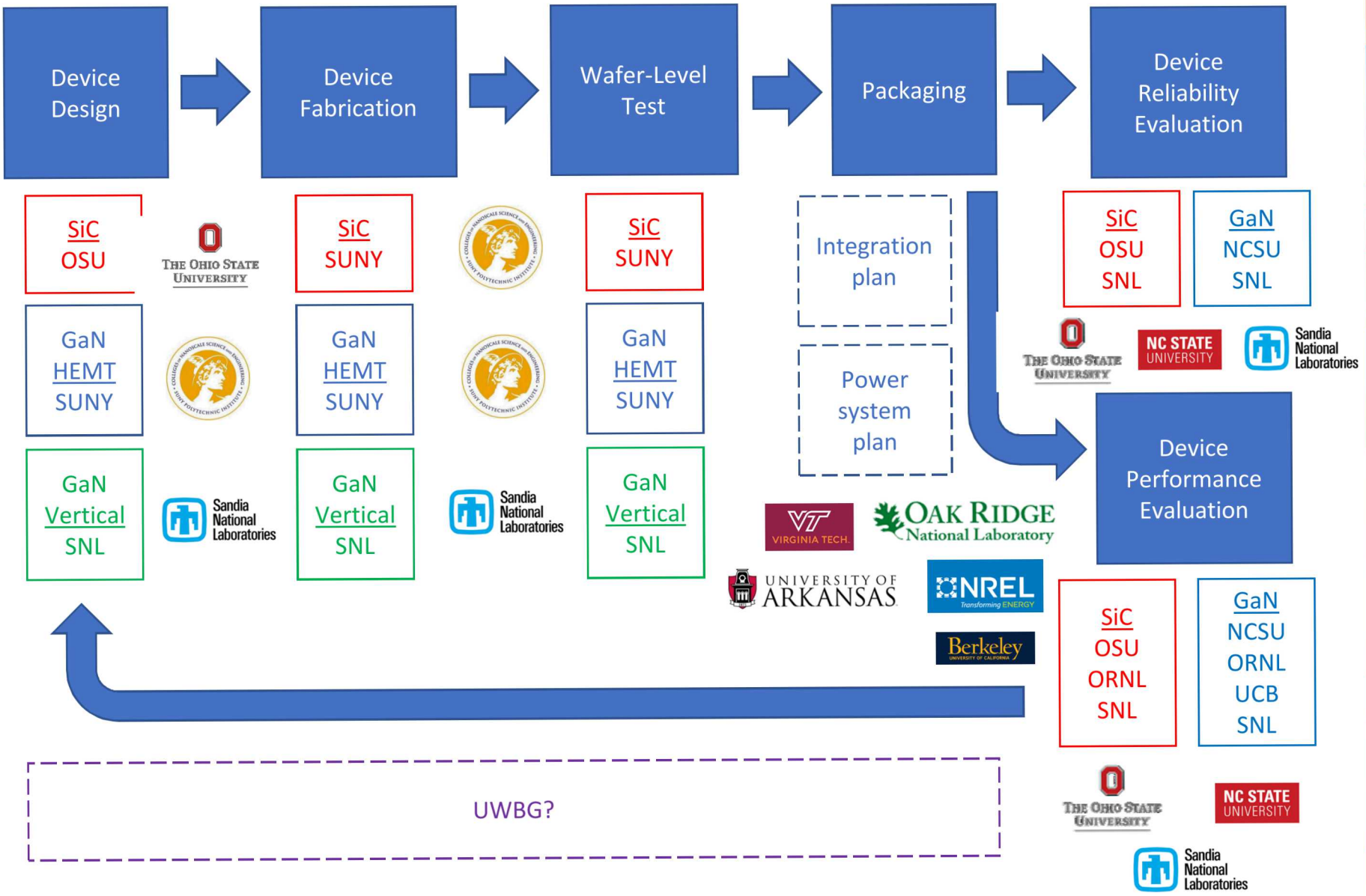
Sandia National Laboratories

SUNY Poly Albany Campus

The Ohio State University

NC State University

Consortium Coordination for Devices



Approach – SiC Power Electronics

- SiC is still young … but several electric traction drive products have recently featured SiC devices
- Improving the performance of SiC devices is likely to increase its adoption
- Achieve consortium goals within project timeline

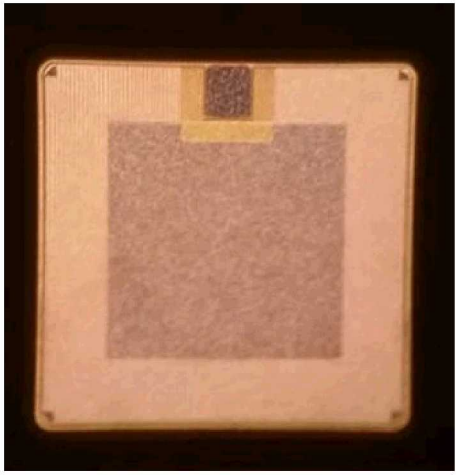
PD550 Si IGBT Inverter
9 kW/L

Gen-1 SiC Inverter
18 kW/L
- **Requires 1/3 the space**

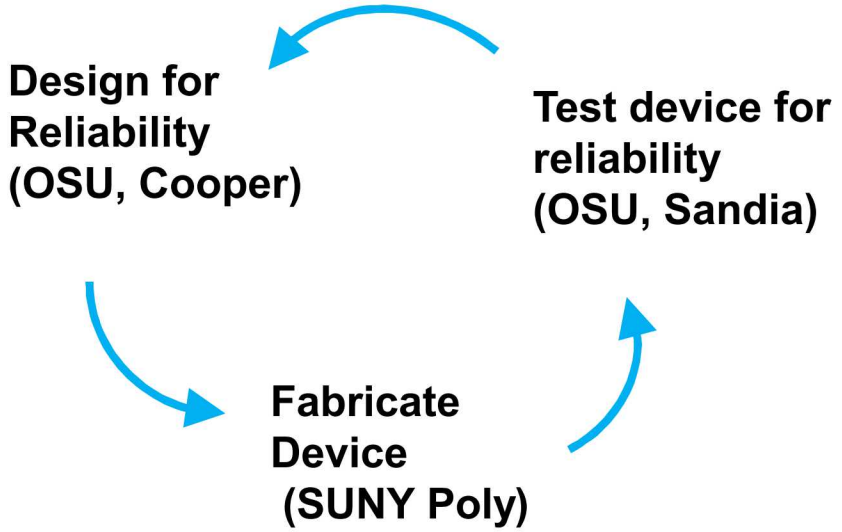
SiC Device Strategy

- SiC is one path to Power Electronics target **(shorter term)**
  - SiC has some commercial maturity and a larger manufacturing base
- SiC device designs may not target automotive applications
  - Cost and performance emphasized over reliability
  - High temp. operation causes issues with threshold voltage (< 1 V at 150 C junction temp.)
  - Gate oxides and channel length designs not optimized for automotive environment
- Focus on ***design for reliability*** within cost targets
- Performance and reliability evaluation
  - Characterize new device designs under relevant use scenarios

MOSFET Die

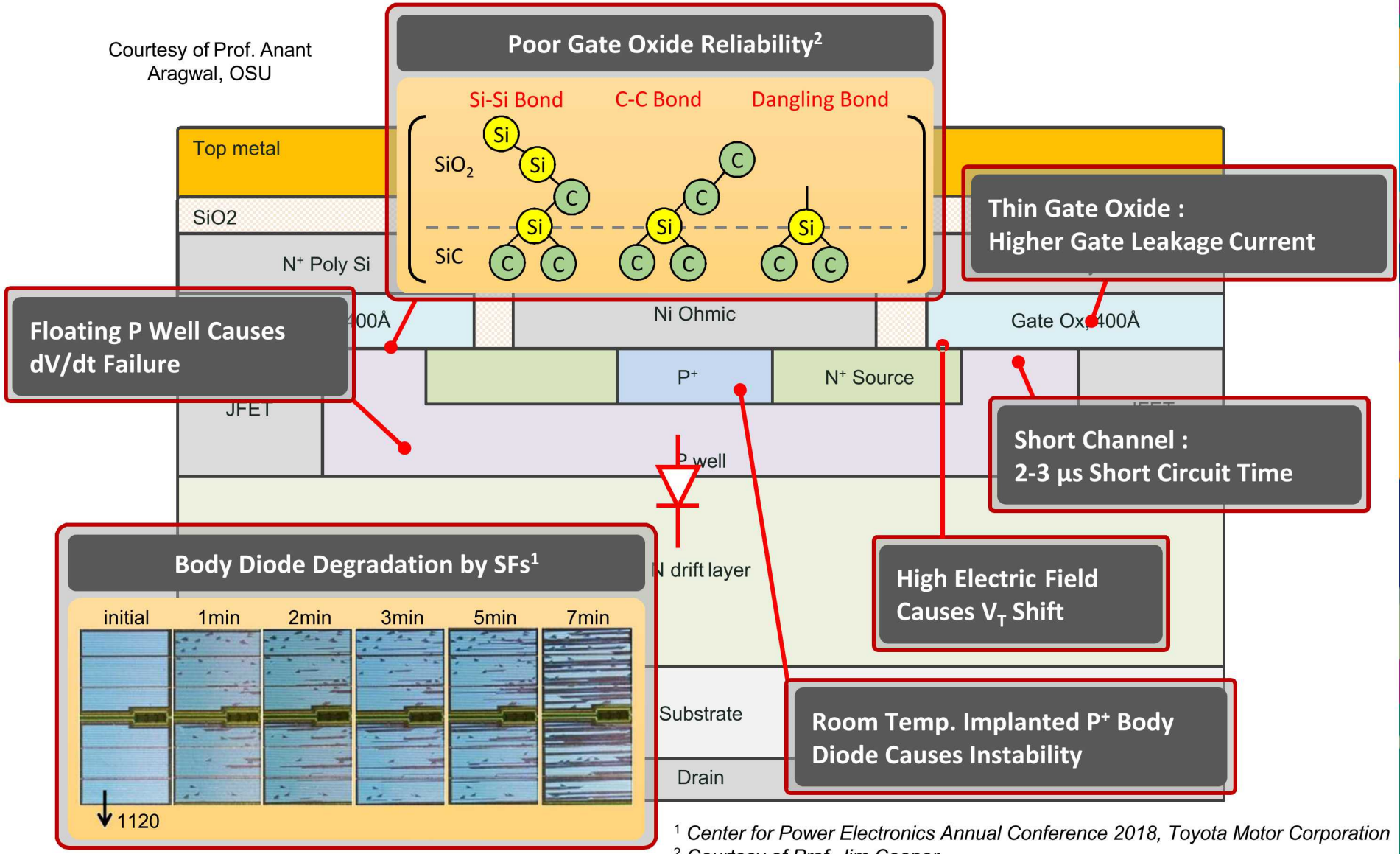


Courtesy of Prof. Woongie Sung, SUNY



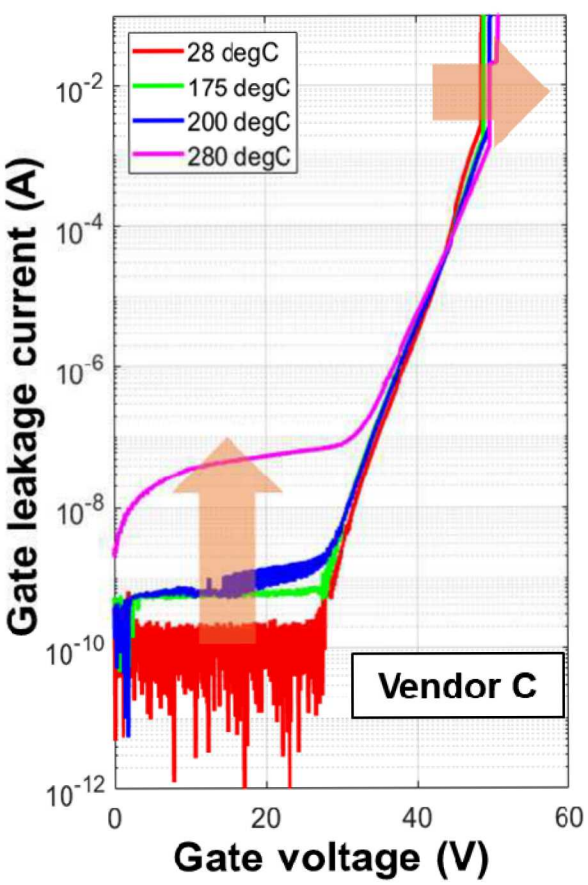
SiC Device Reliability – Issues

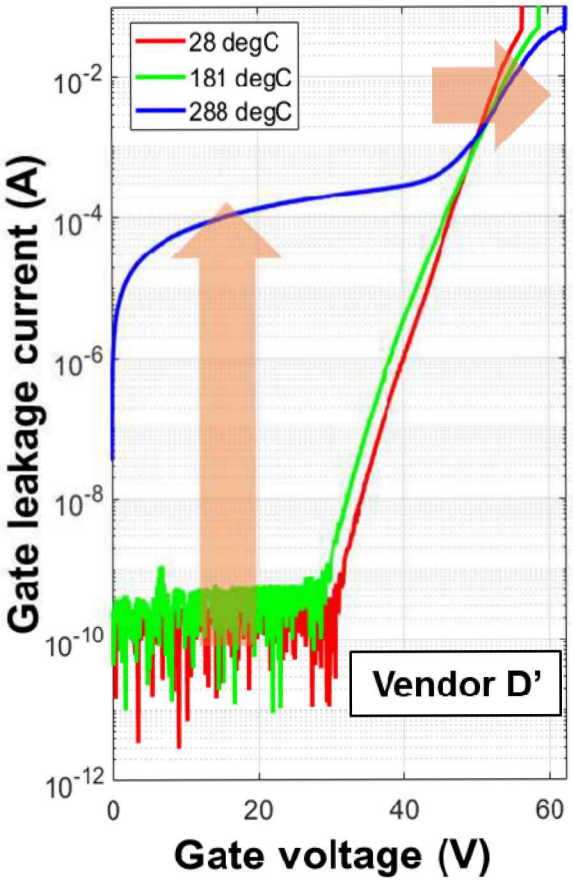
Courtesy of Prof. Anant Aragwal, OSU

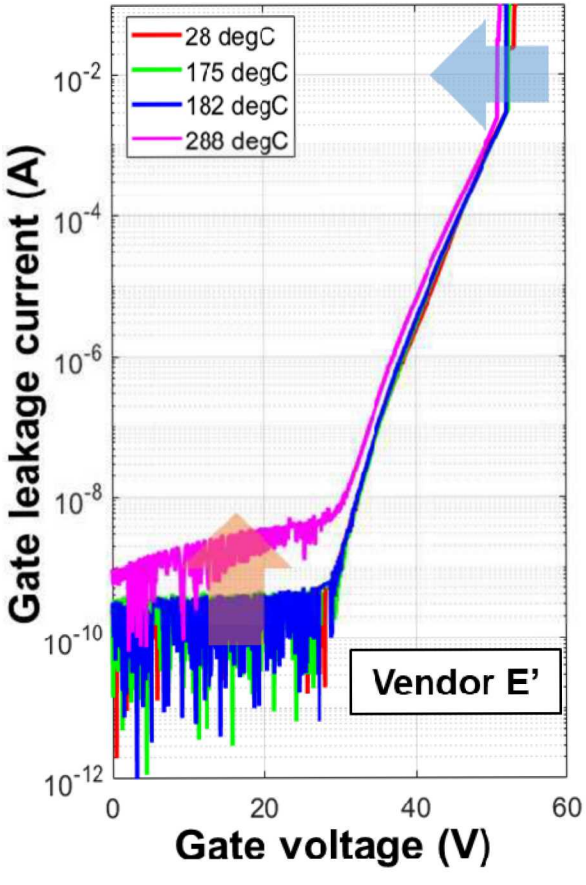


[1] *Center for Power Electronics Annual Conference 2018, Toyota Motor Corporation*
[2] *Courtesy of Prof. Jim Cooper*

SiC Device Reliability – Gate Current Example





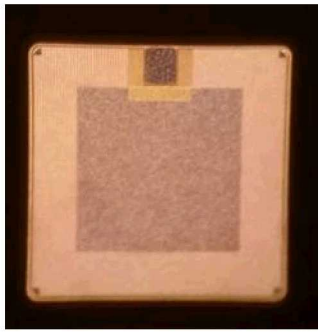


Work in Progress up to 300°C

Courtesy of Prof. Anant Aragwal, OSU

SiC Cost Targets

- Targets should be achievable by 2023
- Estimates of chip cost for a 1.2 kV / 100 A MOSFET with an integrated JBS diode (chip size 6 × 6 mm^2)



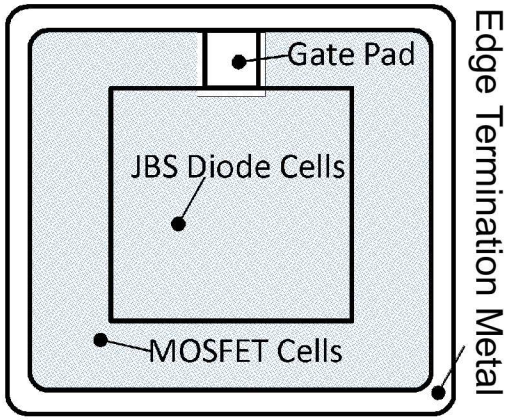
Courtesy of Prof. Woongje Sung., SUNY

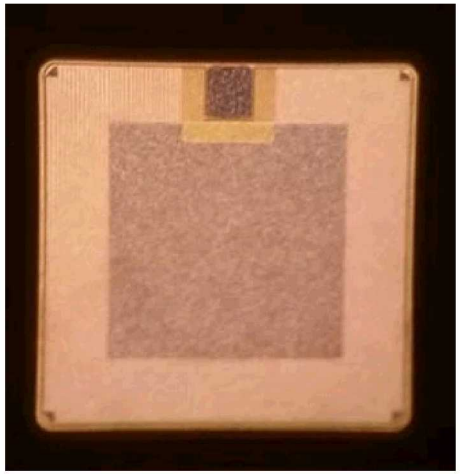
	R&D Phase (2018)	Low volume (2020) 10,000 chips per year	Moderate volume (2023) 1 million chips per year	200mm substrate with Moderat volume (2023~)
Cost per Amp	**27¢/Amp**	**10¢/Amp**	**2.8¢/Amp**	**1.85¢/Amp**
Cost of 150 mm SiC substrate	$2500	$1700	$500	$750
Process cost per wafer	$5000	$1500	$500	$500
Cost per 100 A die	$27	$10	$2.8	$1.85
Total number of chips on a wafer excluding a 2 mm zone around the substrate	400	400	400	750
Yield	70%	80%	90%	90%
Number of functional die per wafer	280	320	360	675

Courtesy of Prof. Anant Agarwal, OSU

SiC Device Fabrication

- Reliability/ruggedness evaluation of commercial and SUNY Poly devices
  - Ohio State, Sandia
- Evaluate devices in 10 kW, 3-phase test system
  - Stress devices in realistic drive cycle scenario (e.g. 10 minute hill climb)
- Devices fabricated by SUNY Poly
  - High-performance, high-reliability 900-1700 V SiC JBS diode integrated MOSFETs
  - Devices to be fabricated at a commercial foundry

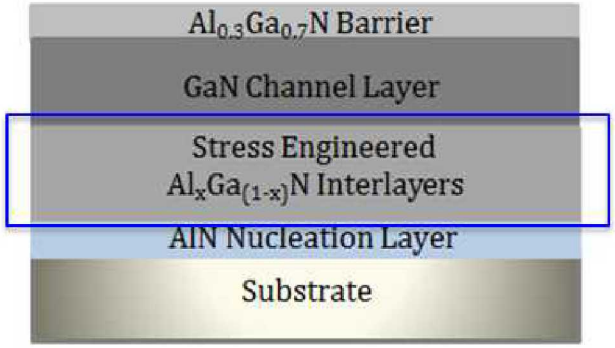




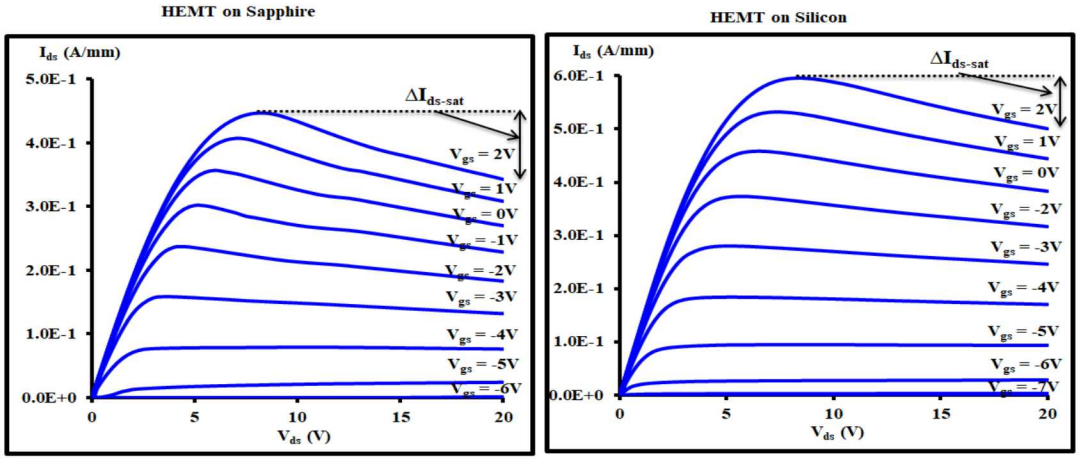
Courtesy of Prof. Woongie Sung, SUNY

Lateral GaN Power Devices

- AlGaN/GaN HEMT is the most mature GaN power device, but continues to suffer from less-than-ideal reliability due mainly to growth on foreign substrates (e.g. SiC, Si, Sapphire)
- Consortium work will focus on growth and fabrication of AlGaN/GaN HEMTs on native GaN substrates

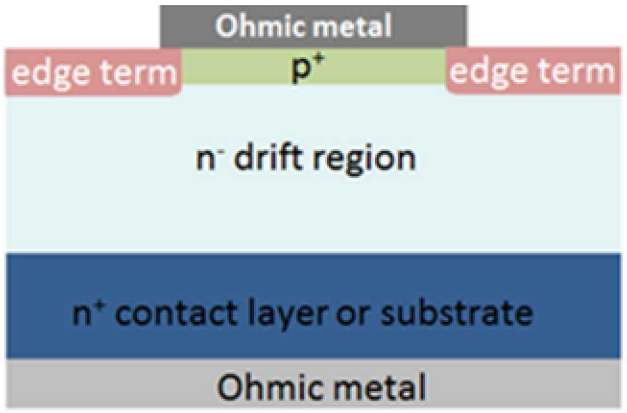


- Eliminate strain engineered layers by growing on native GaN substrates
  - Lower defect density is expected to lead to better device performance and reliability

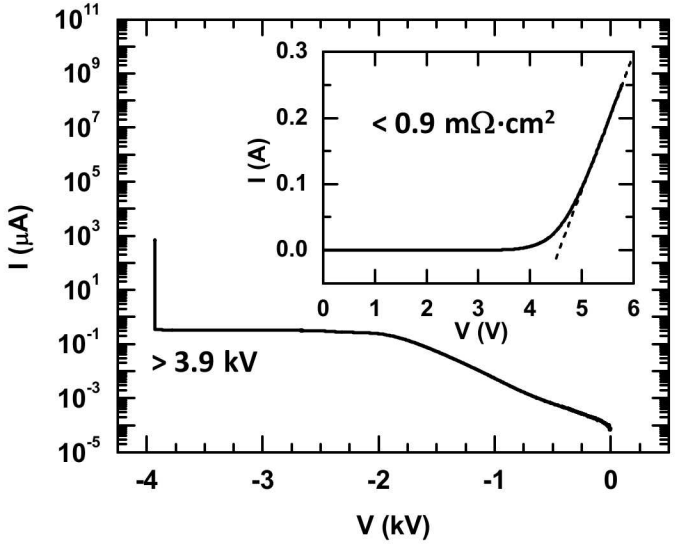


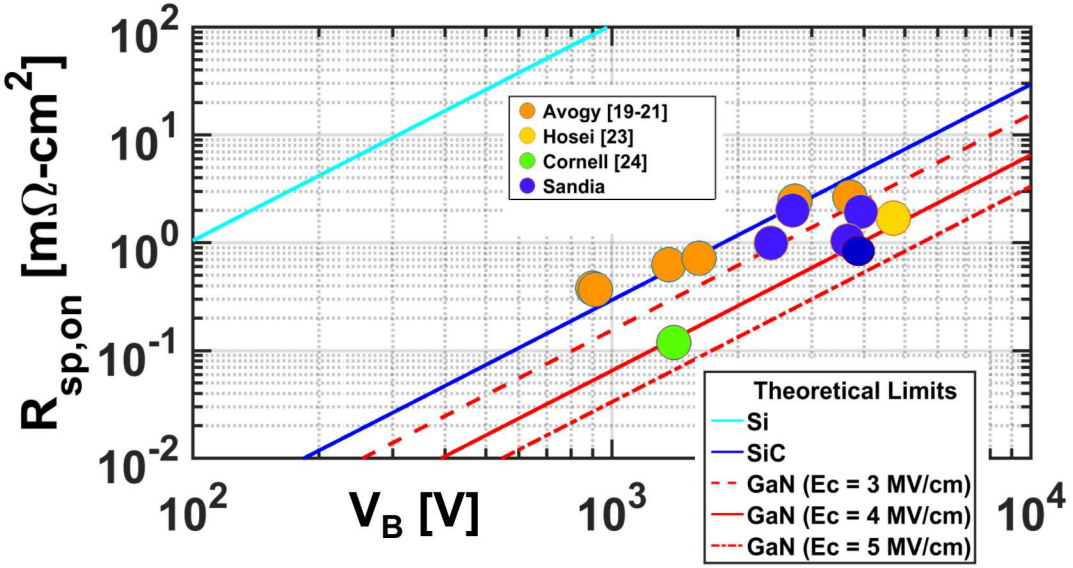
Courtesy of Prof. Shadi Shahedipour-Sandvik, SUNY

Vertical GaN Power Devices



- Vertical device architecture enables higher breakdown voltages
  - Similar to Si and SiC power devices
  - Better performance due to higher critical electric field for GaN
- Less mature – Challenges exist with substrates, growth, and processing

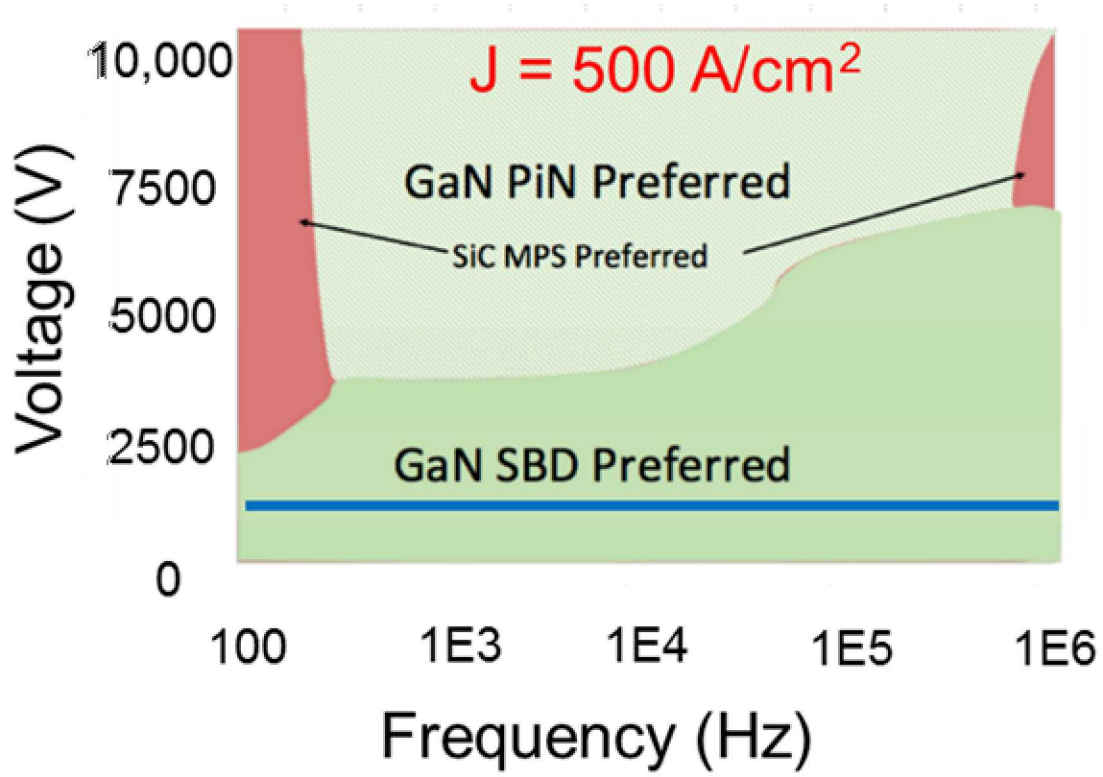




A. Armstrong et al., Elec. Lett. 52(13), 1170 (2016)

System Benefits for Vertical GaN

System evaluation of **diode power dissipation vs. diode type** for given operating regime (reverse voltage, forward current density, frequency), T = 300 K

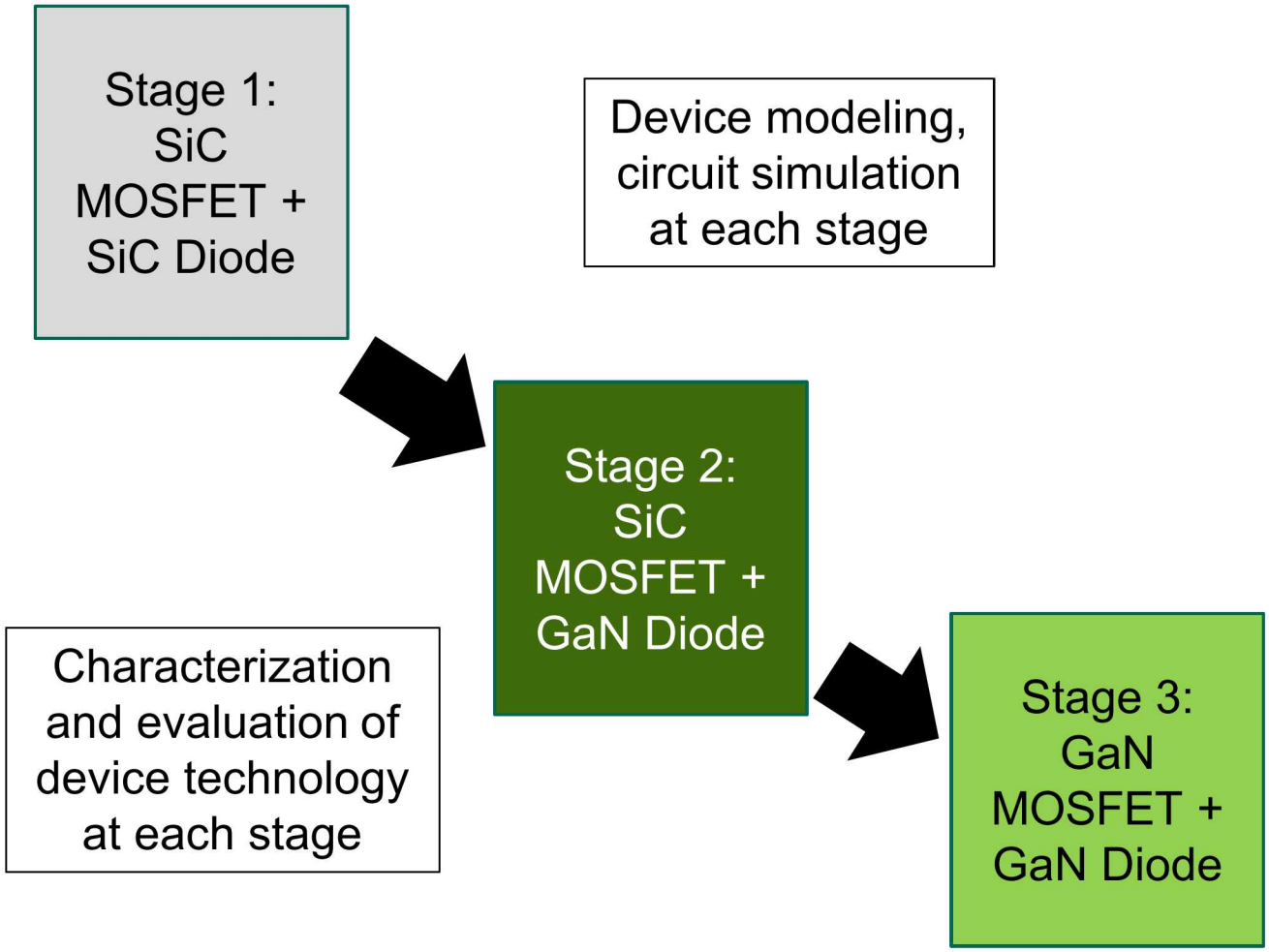


- **Lower R_{on} for GaN SBD and JBS diodes drive expected performance benefits**
- **Target operating voltage for EDT power devices: 1200 V (blue line)**

J. Flicker and R. Kaplar, IEEE WiPDA, Albuquerque, NM (2017)

Evolution of Vertical GaN Devices

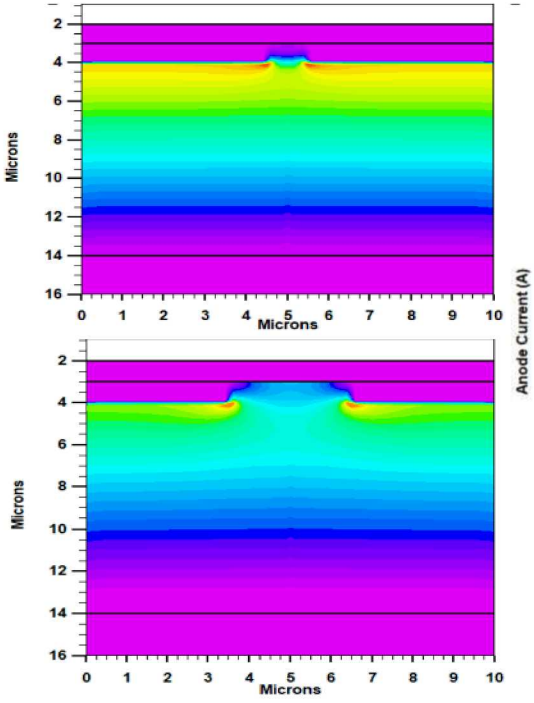
Follow successful commercial model of **staged** device integration from Si + SiC development



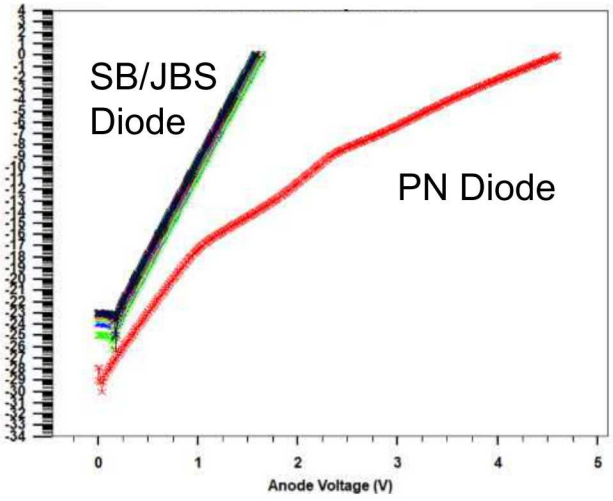
Progress on GaN Vertical Devices

- Decision to focus resources in first year on the vertical GaN diode
  - Allows staged combination with SiC transistors.
  - Schottky Barrier (SB) and Junction Barrier Schottky (JBS) diodes
- Modeling/Simulation is underway
  - Have developed SB diode models in Silvaco simulation software
  - JBS diode models are under development

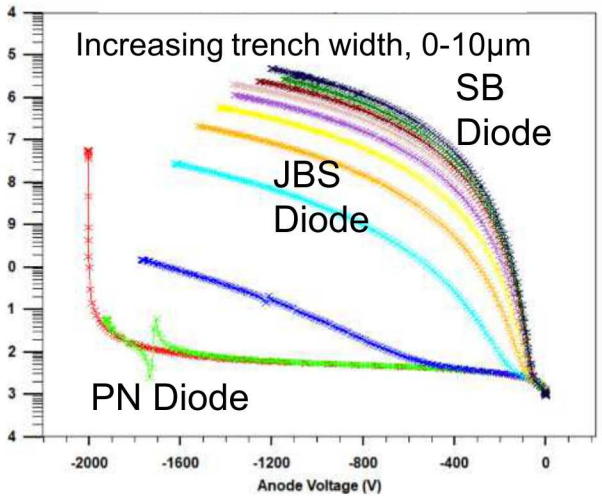
E-field – Planar JBS



JBS - Forward IV



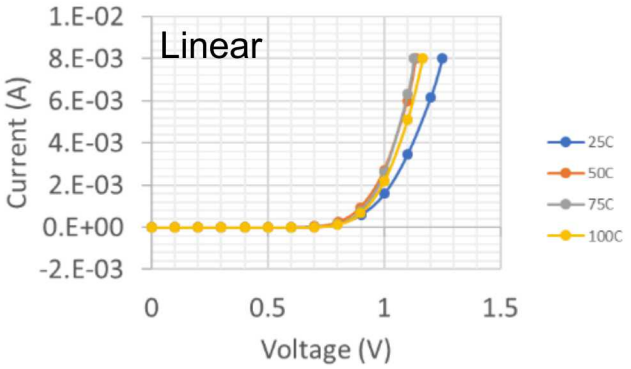
JBS - Reverse IV

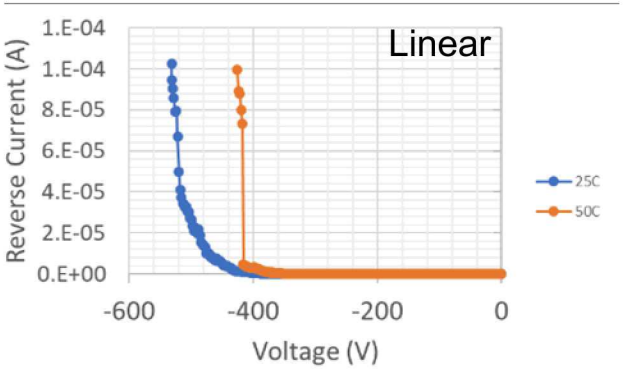


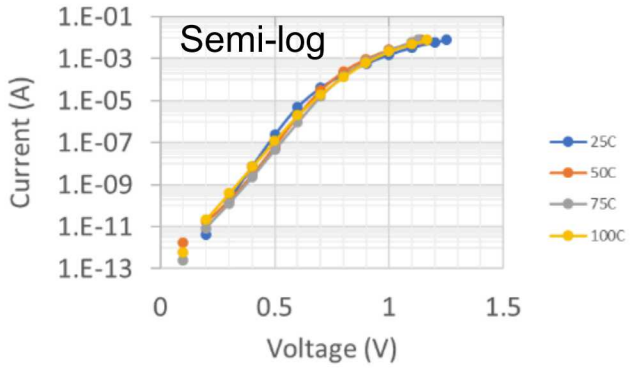
Progress on GaN Vertical Devices

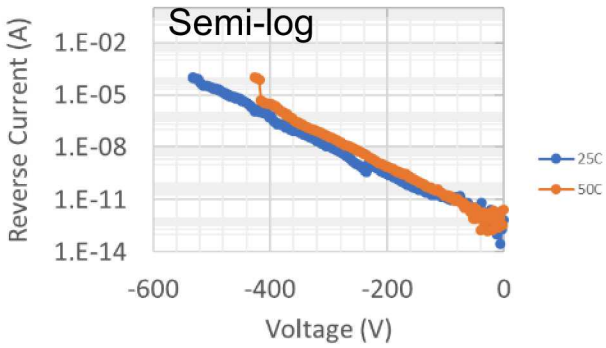
- Gen1 GaN SB Diodes **demonstrated**
  - SB diodes are being characterized and used to calibrate models
  - Focus on good Semiconductor-Metal interface for Gen1 devices
- Mask designs for JBS diode development **completed**
  - Exploring different design strategies
  - Using SiC devices to understand current scaling methods

SB Diode IV over Temperature

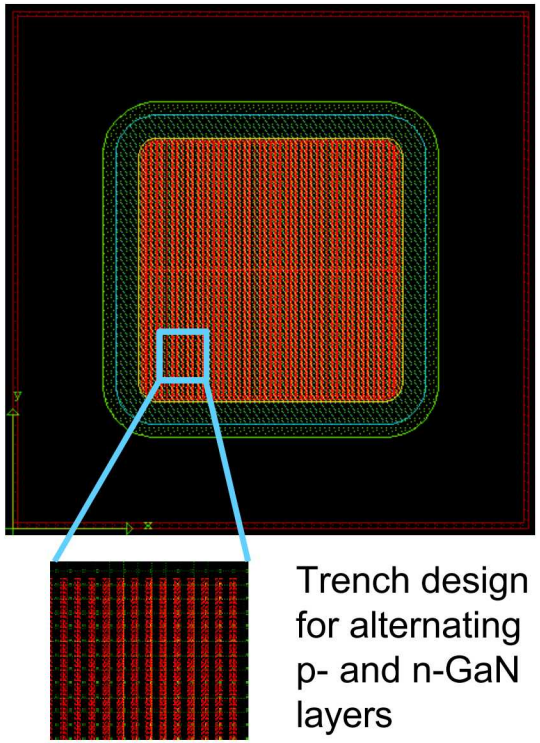








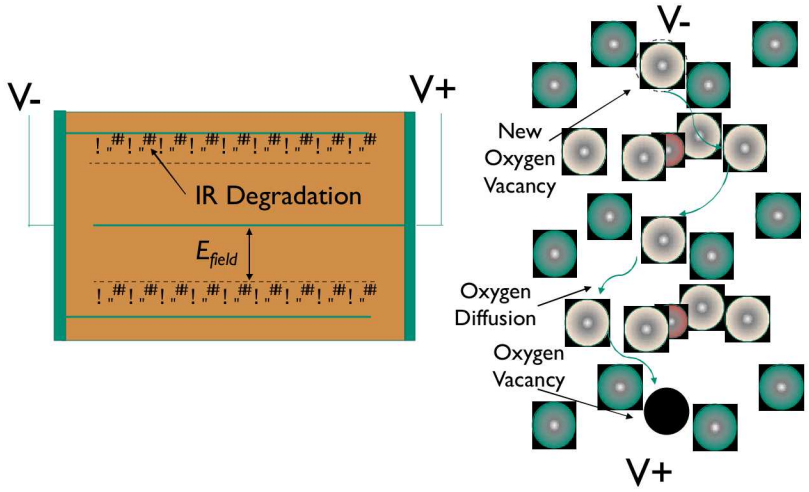
JBS Diode Mask

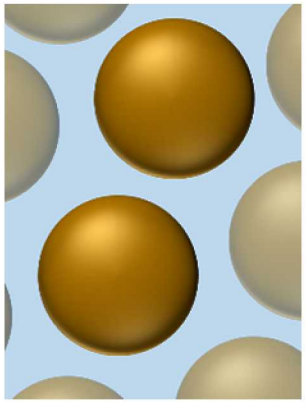


Trench design for alternating p- and n-GaN layers

Passive Materials for WBG Power Electronics

- Innovate passive materials for high-frequency power electronics
  - Improve ceramic capacitor performance and reliability
  - Increase frequency of magnetic materials and reduce size of inductors
  - Increase power density through integration (vs. discrete components)



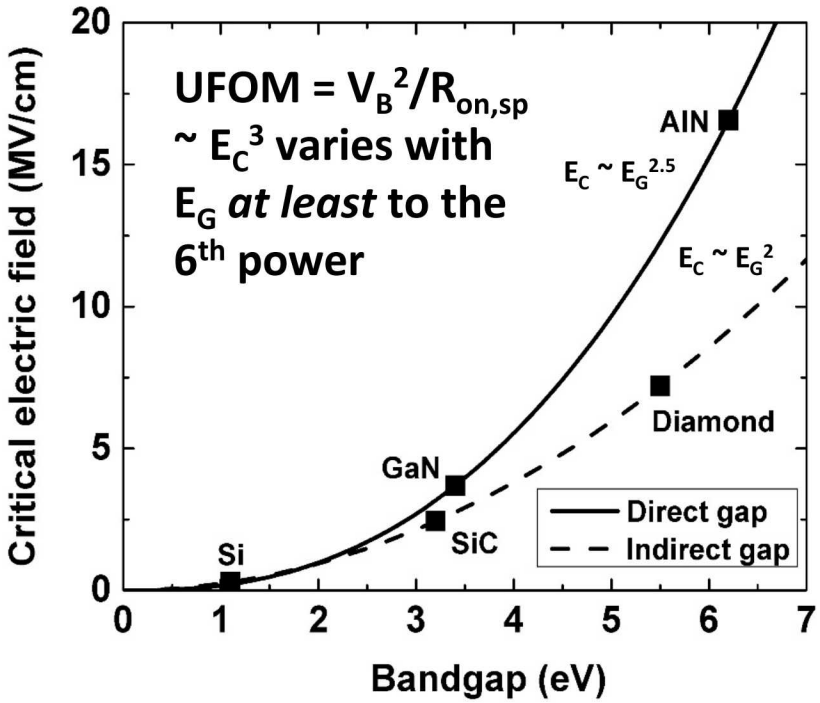


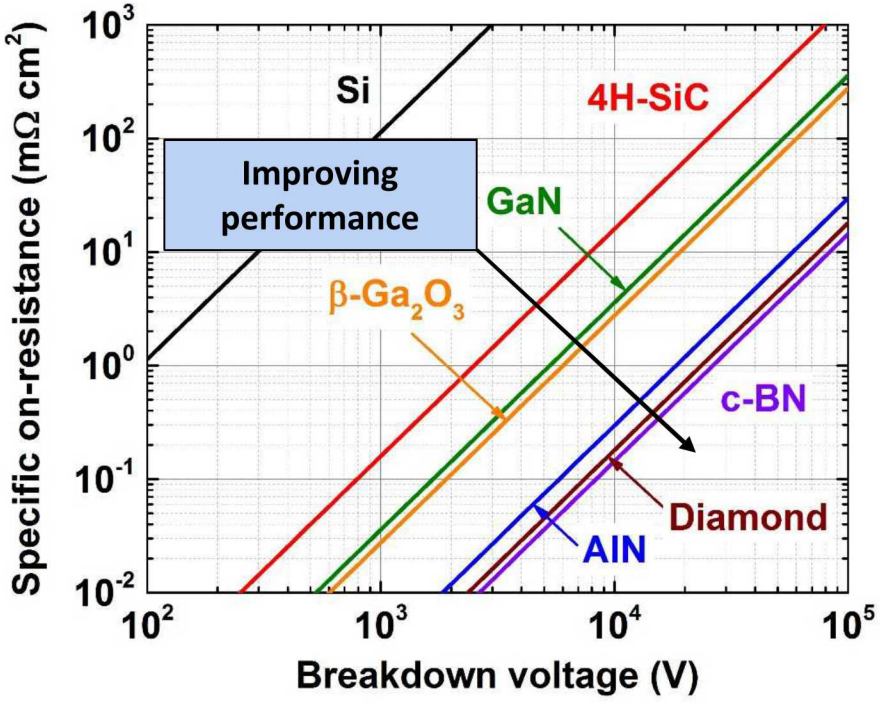
With permission from Getty Images

- **Ceramic capacitor aging caused by oxygen diffusion toward anode and accumulation of oxygen vacancies at cathode**
- **Bipolar switching at ~10x the rated voltage and 125°C above the rated temperature can increase the lifetime**

- **Inductor designs may be improved with tailored Fe_4N composites**
  - **Smaller size**
  - **Higher-frequency operation**
  - **Operating temperatures up to 200°C**

Future Work: UWBGs?





Strong dependence of E_C on E_G leads to better performance

Unipolar FOM = $V_B^2/R_{on,sp} = \varepsilon\mu_n E_C^3/4$

Hudgins et al., *IEEE Trans. Pwr. Elec.* 18, 907 (2003); J. Y. Tsao et al., *Adv. Elec. Mat. Adv. Elec. Mat.* 4, 1600501 (2018)

Summary

- **Systems-level view has identified key areas to focus on for device development**
  - **Wide-bandgap power devices – SiC and vertical GaN devices are main efforts, with some work on lateral GaN**
  - **Close coordination between Sandia, other DOE labs, and key universities**

- **SiC device improvement will be driven through "design for reliability" approach with performance metrics and cost in mind**
  - **Iterative cycles of design, fab, and performance and reliability evaluation across partner institutions**

- **GaN device development is underway**
  - **System-level benefits being evaluated**
  - **HEMT effort focused on reliability**
  - **Vertical GaN Schottky and JBS diode work is in progress**
  - **Vertical GaN MOSFET work starting**

- **Suitable passive components are required to take full advantage of WBGs**