SAND2019-6902PE

20 kV Gallium Nitride Electromagnetic Pulse Arrestor for Grid Reliability

Sandia National Laboratories
R. Kaplar, A. Allerman, B. Gunning, G. Pickrell, M. Crawford, A. Armstrong, J. Dickerson, A. Binder, J. Flicker, J. Neely, O. Aktas (EDYNX), J. Cooper (Sonrisa)

Naval Research Laboratory / NIST
K. Hobart, T. Anderson, A. Koehler, M. Tadjer, J. Gallagher, M. Ebrish, M. Porter (NPS)

Stanford University
S. Chowdhury

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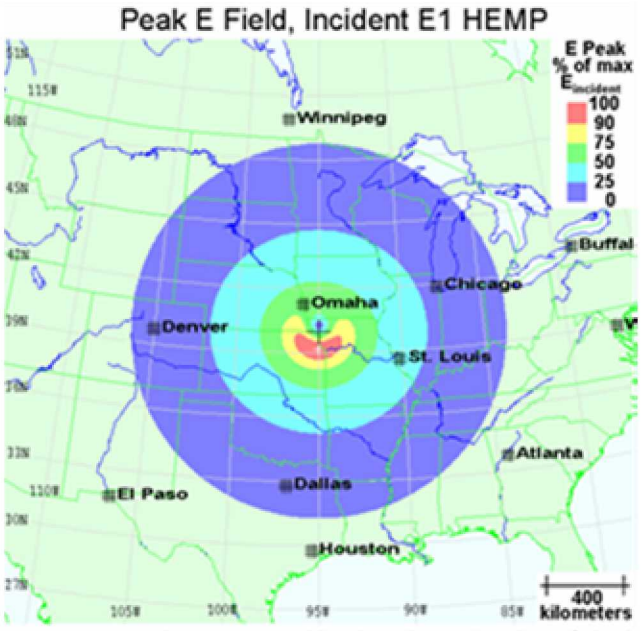
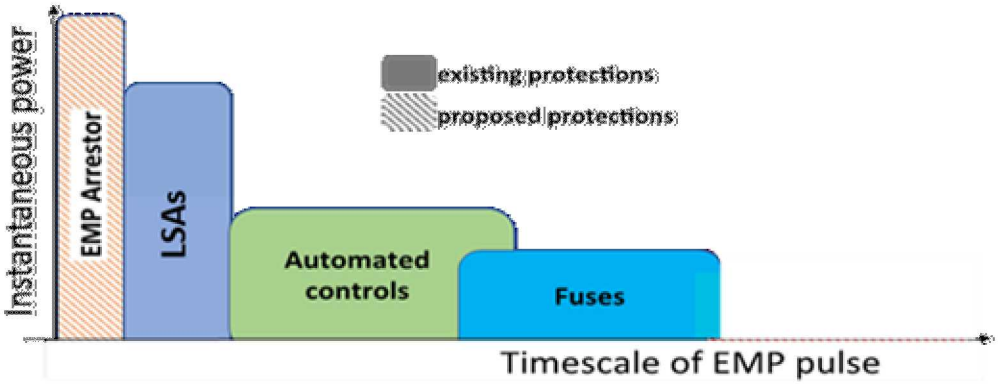
Protection for the Electric Grid Project Objectives



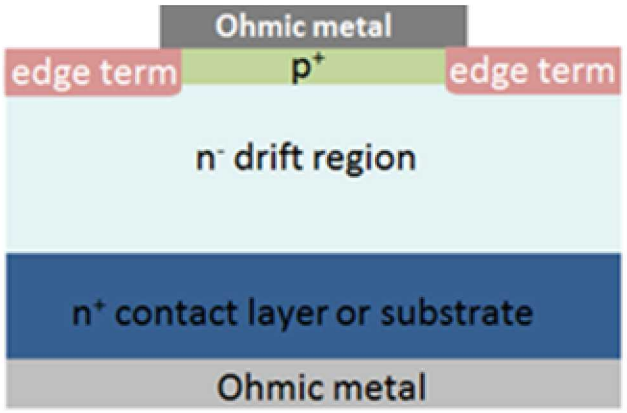
- Electromagnetic pulses are a threat to the grid
  - Very fast E1 component (< 1 μs)
  - Unaddressed by current SOA technology (LSAs)



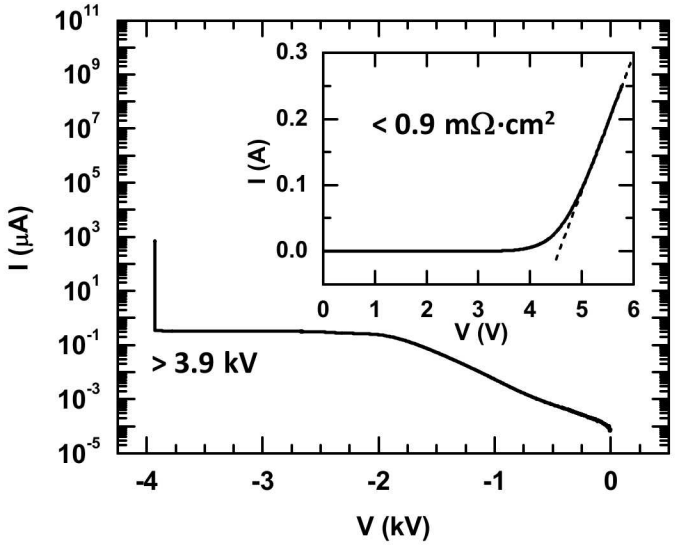
- Protection is generally needed for MVDC grid-connected systems

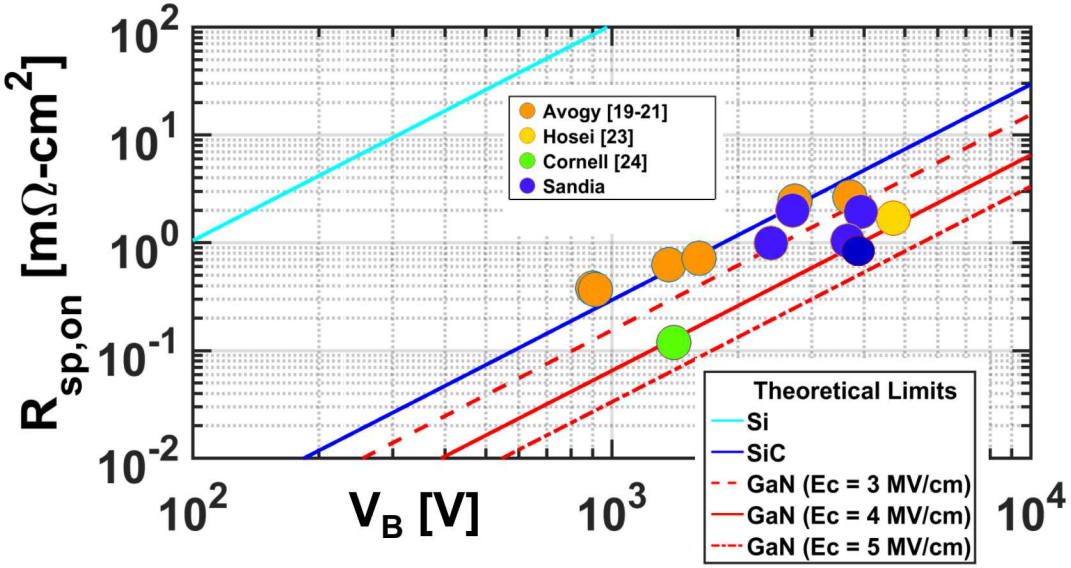
J. S. Foster Jr. et al., "Report of the Commission to Assess the Threat to the United States from Electromagnetic Pulse (EMP) Attack: Critical National Infrastructures," *Defense Technical Information Center* (2008).

Vertical GaN Technology



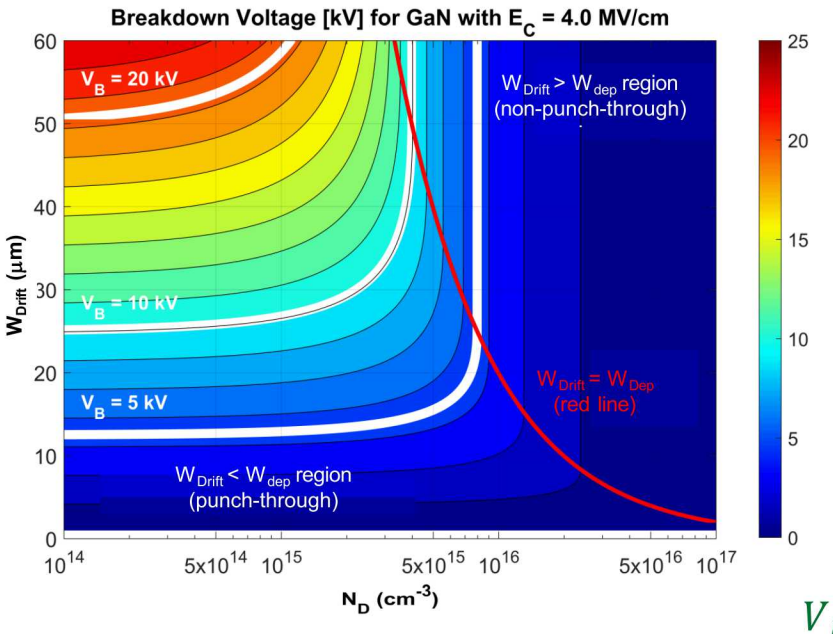
- **Extend the limits of vertical GaN power device technology**
  - **Increase V_B by 4x from today's SOA**
  - **Challenges: Thick drift region, low net doping, edge termination**
- **Establish a domestic foundry process for vertical GaN power devices**



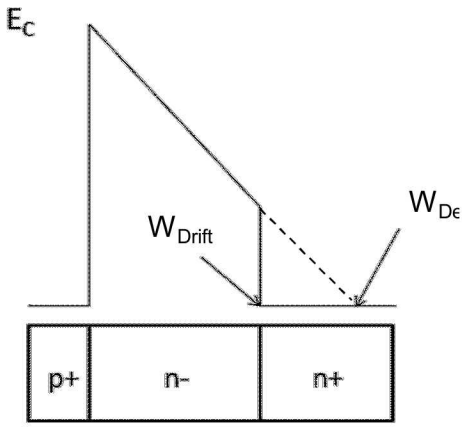


A. Armstrong et al., Elec. Lett. 52(13), 1170 (2016)

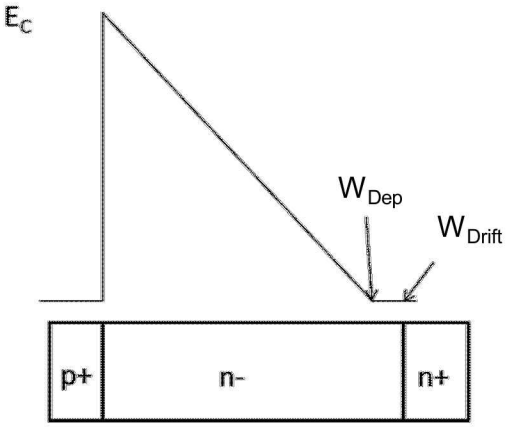
Epitaxy and Doping



Punch-Through
$W_{Drift} < W_{Dep}$



Non-Punch-Through
$W_{Drift} \geq W_{Dep}$

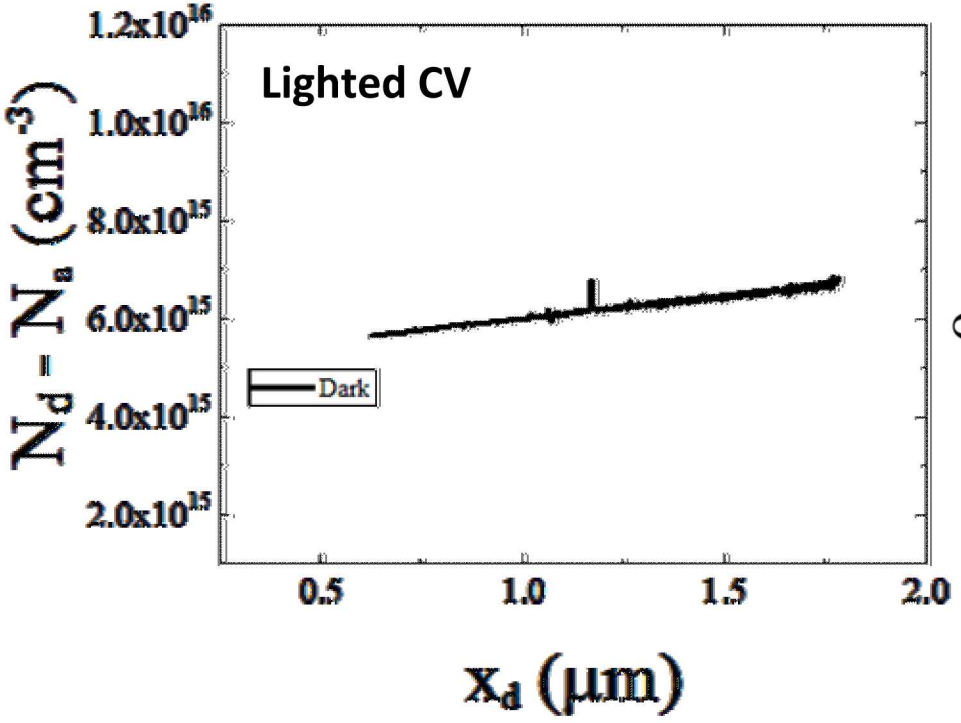


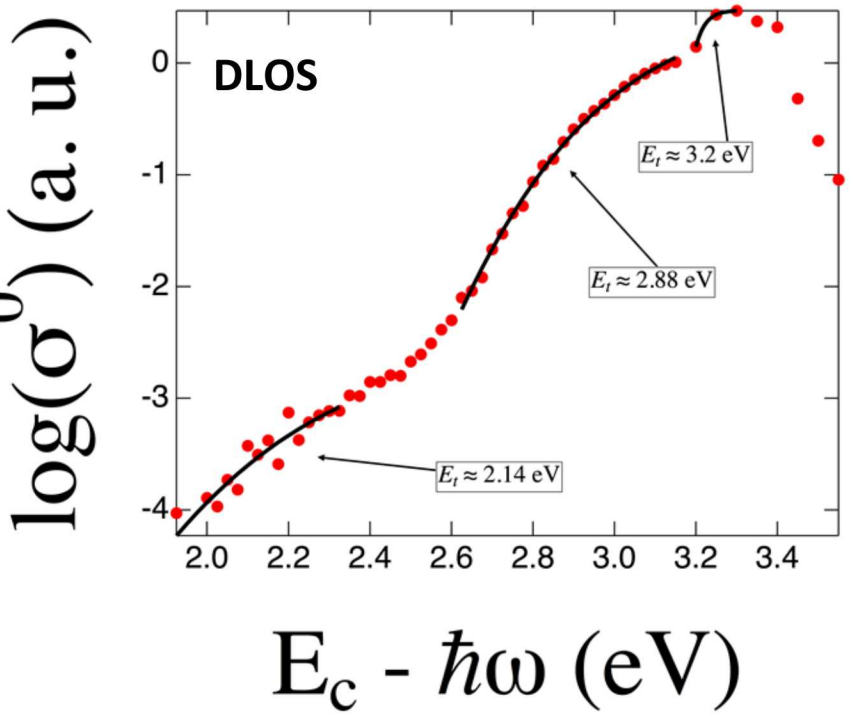
$$V_{br} = E_C W_{Drift} - \frac{qN_D W_{Drift}^2}{2\varepsilon}$$

$$V_{br} = \frac{\varepsilon E_C^2}{2qN_D}$$

- **Need N_D = low-10^{15} cm^{-3}, W_{Drift} = 50-100 μm for 20 kV breakdown**
- **Optimal unipolar FOM achieved for $W_{Drift} = 3V_B/2E_C$**

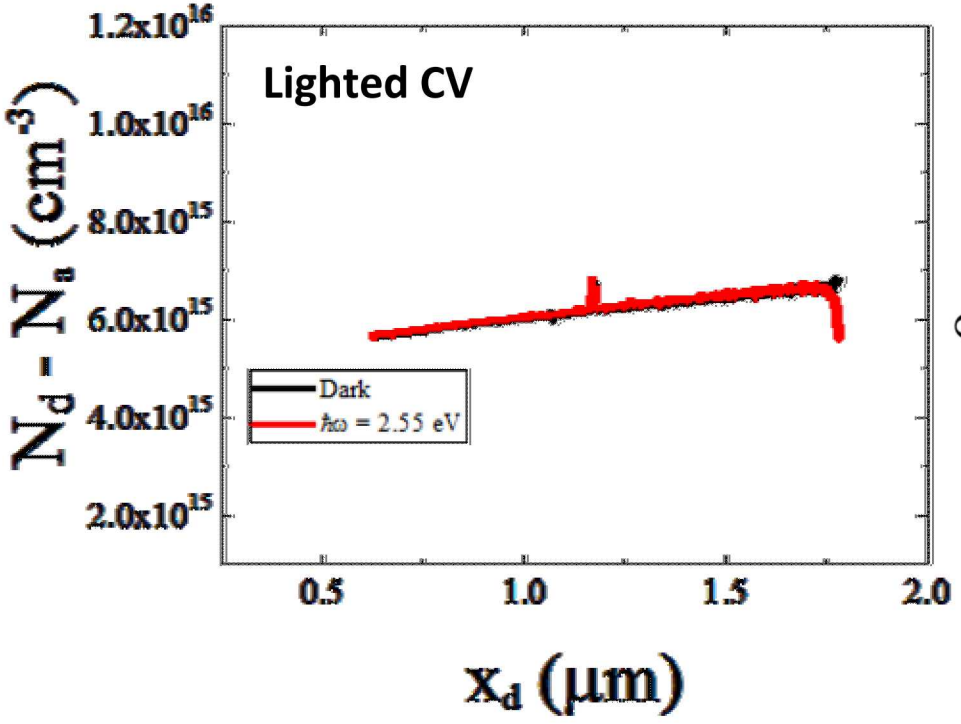
Epitaxy and Doping

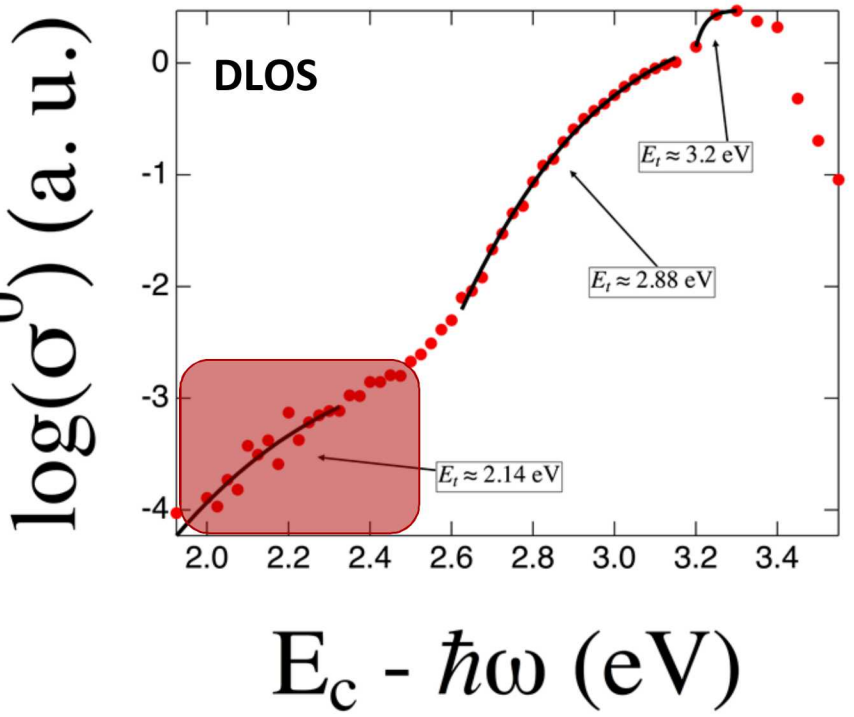




M. P. King et al., Applied Physics Letters 109, 183503 (2016)

Epitaxy and Doping

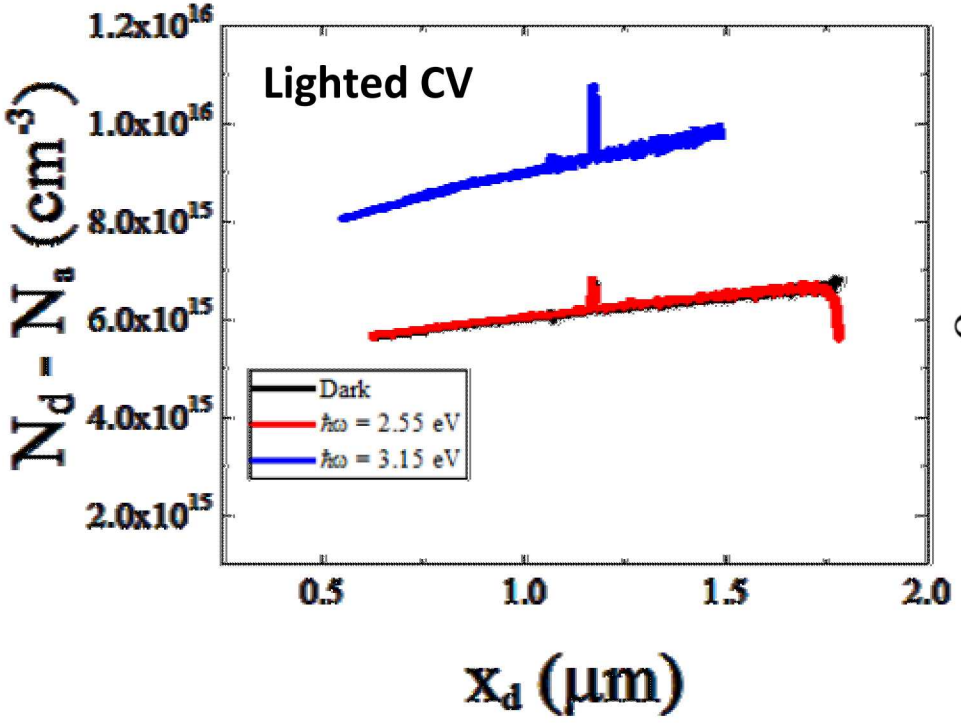


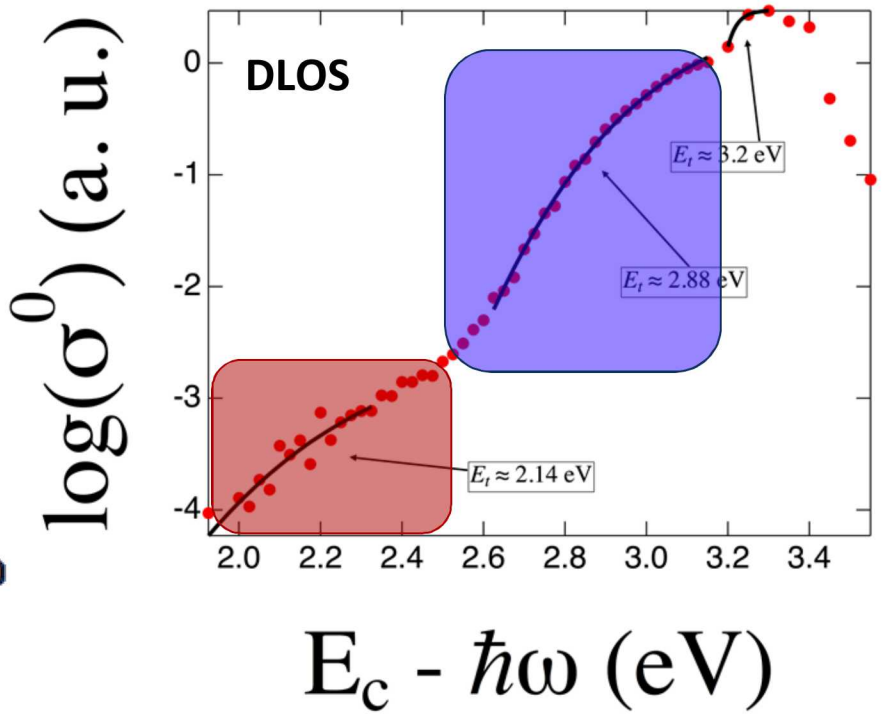


- **Small response from E_C – 2.14 eV level, $N_T \approx 3\times10^{13}$ cm^{-3}**

M. P. King et al., Applied Physics Letters 109, 183503 (2016)

Epitaxy and Doping

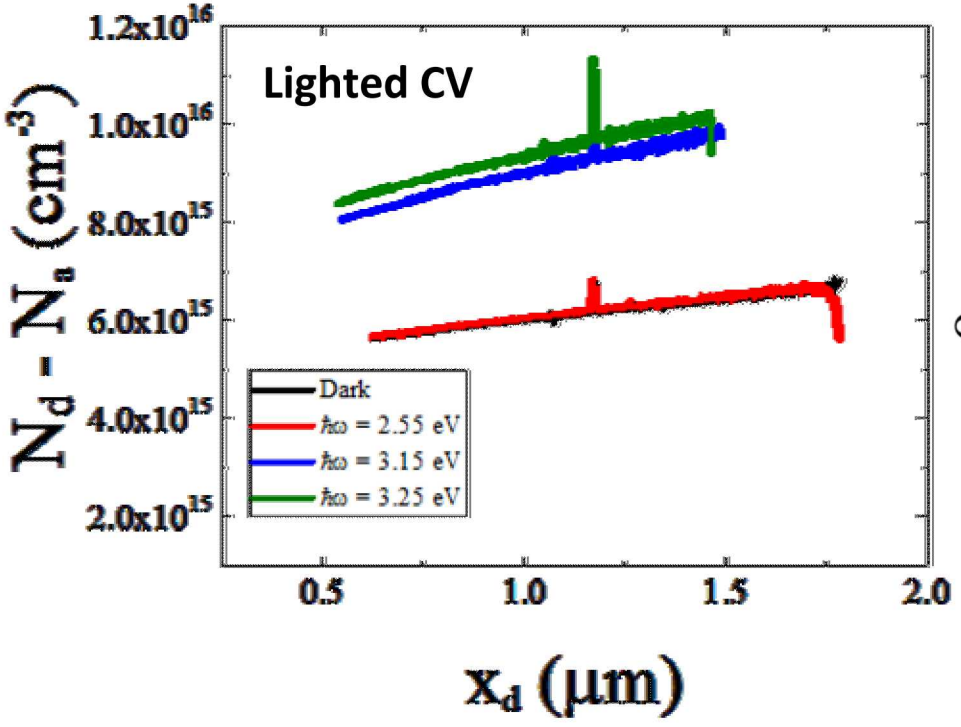


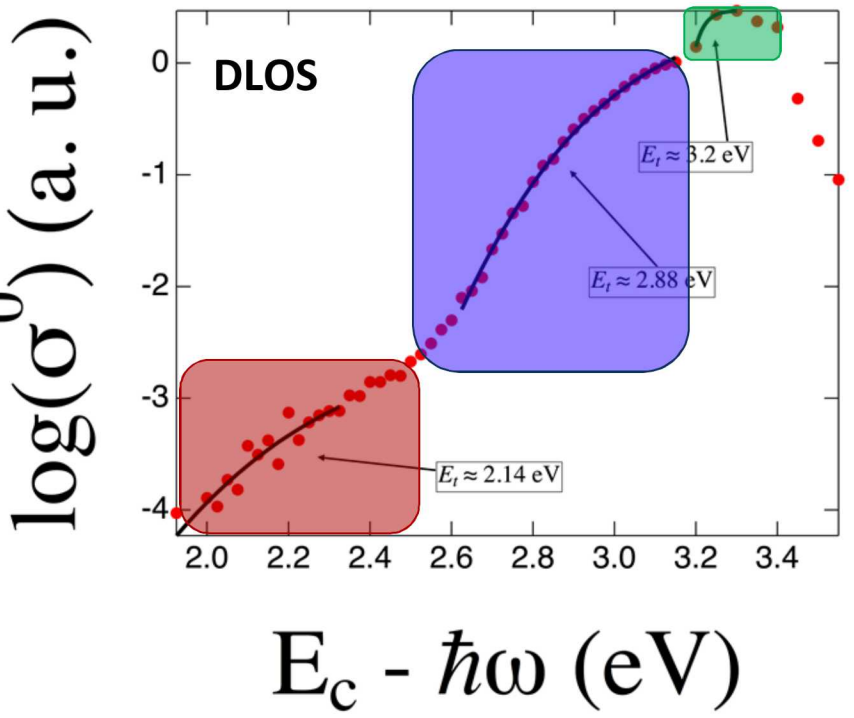


- Small response from E_C – 2.14 eV level, $N_T \approx 3\times10^{13}$ cm^{-3}
- E_C – 2.88 eV level is the primary compensating defect, $N_T \approx 2\times10^{15}$ cm^{-3}

M. P. King et al., Applied Physics Letters 109, 183503 (2016)

Epitaxy and Doping





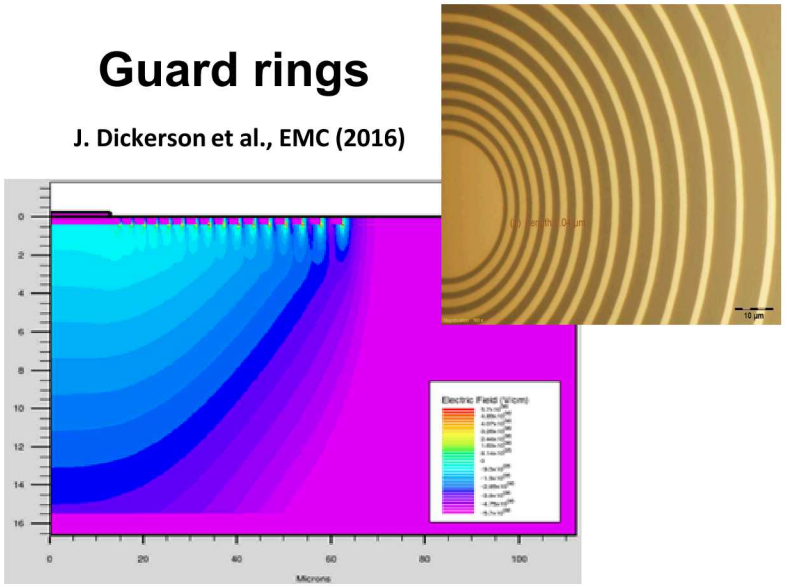
- Small response from $E_C - 2.14$ eV level, $N_T \approx 3\times10^{13}$ cm^{-3}
- $E_C - 2.88$ eV level is the primary compensating defect, $N_T \approx 2\times10^{15}$ cm^{-3}
- $E_C - 3.20$ eV level is a secondary compensating defect, $N_T \approx 5\times10^{14}$ cm^{-3}

M. P. King et al., Applied Physics Letters 109, 183503 (2016)

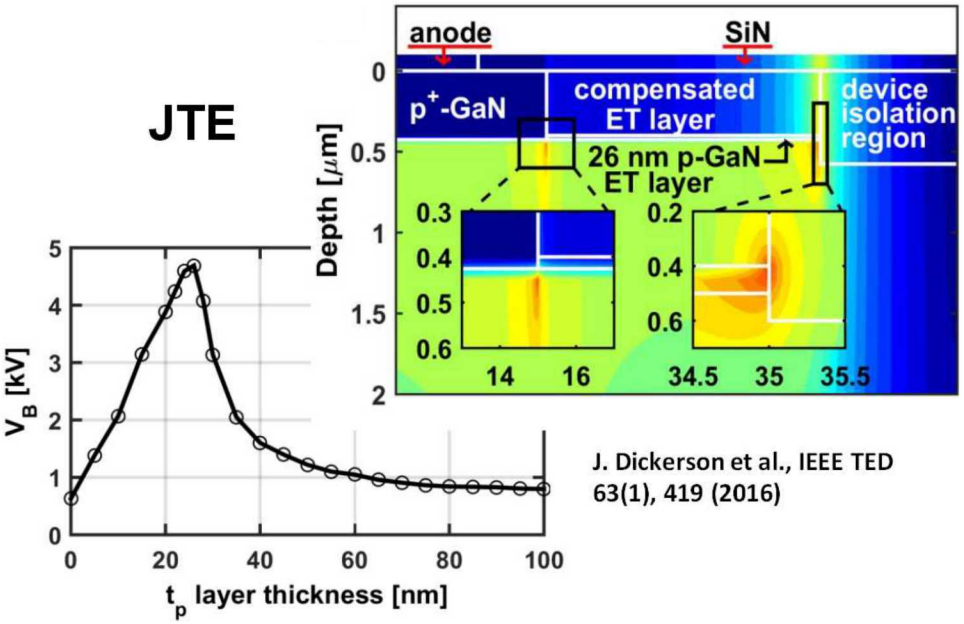
Edge Termination

Guard rings

J. Dickerson et al., EMC (2016)

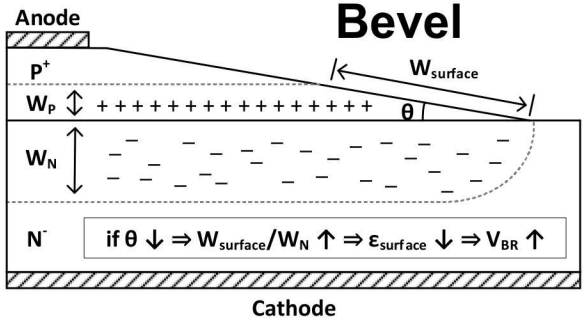


JTE



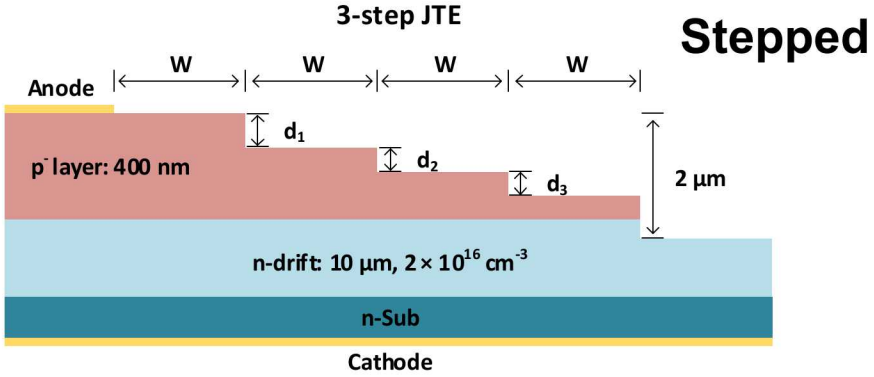
J. Dickerson et al., IEEE TED 63(1), 419 (2016)

Bevel



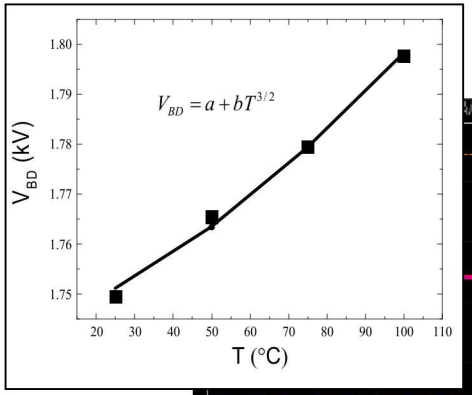
A. Binder et al., submitted to WiPDA (2019)

Stepped

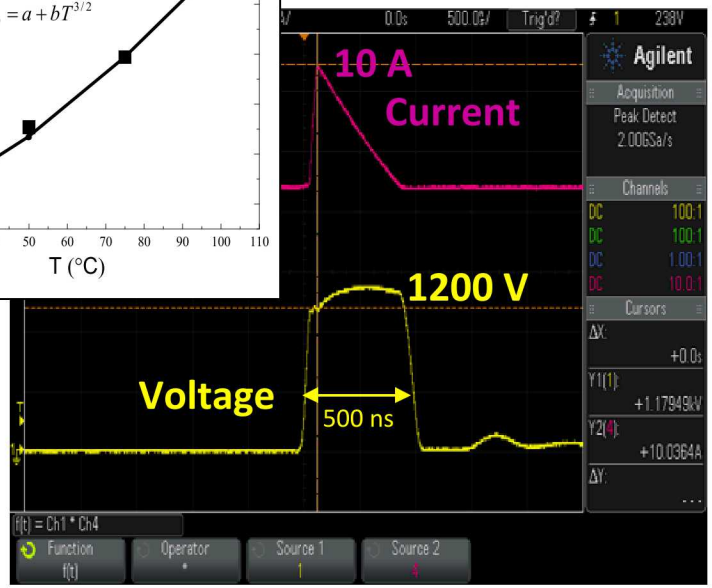


Fast Avalanche Response

- **Will quantify breakdown physics, including time response**
  - **Avalanche ruggedness is key – avalanche breakdown previously demonstrated, but need to better understand physics**
  - **Existing reverse-recovery test system will be upgraded to measure time response of avalanche breakdown**

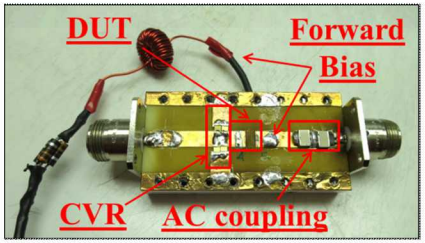


M. P. King et al., IEEE TNS 62(6), 2912(2015)



O. Aktas and I. C. Kizilyalli, IEEE EDL 36(9), 890 (2015)

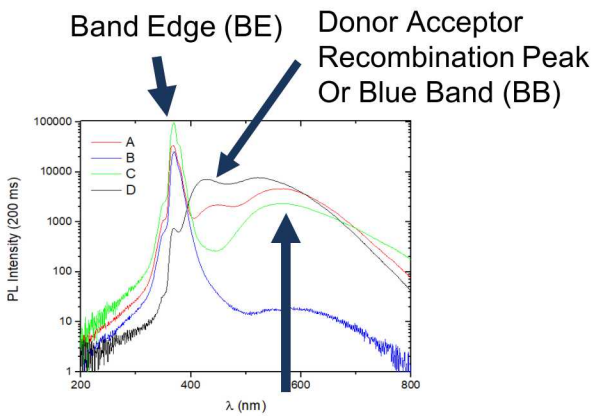
D. L .Mauch et al., IEEE TPE 32(12), 0333 (2017)

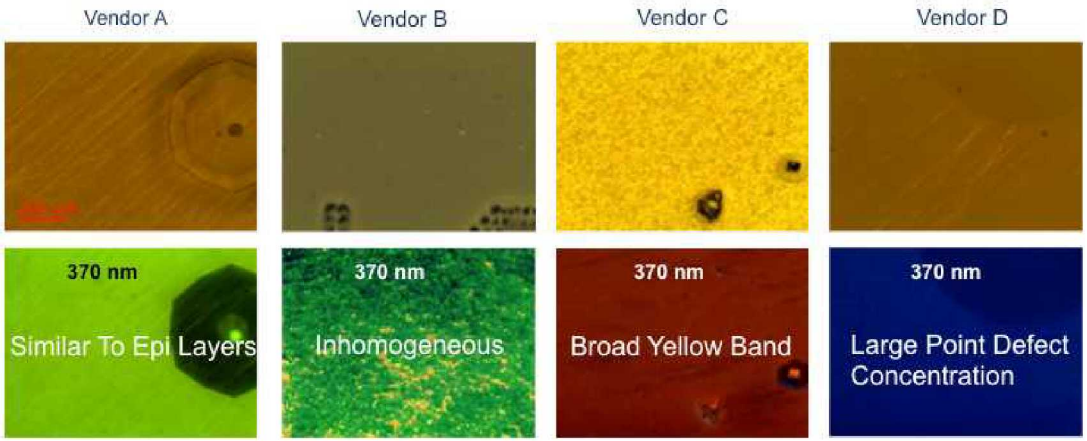


Substrate Characterization

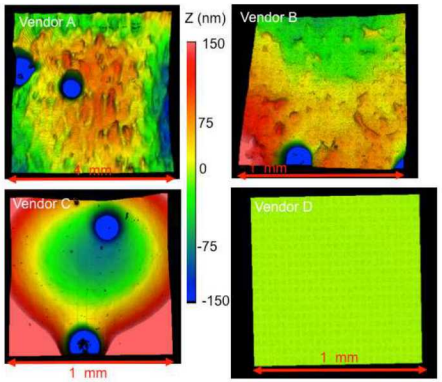
Project Objectives

PL Spectrum/Imaging

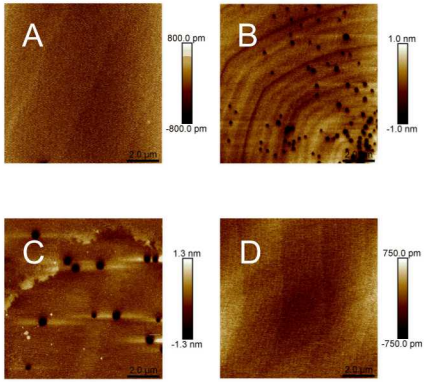




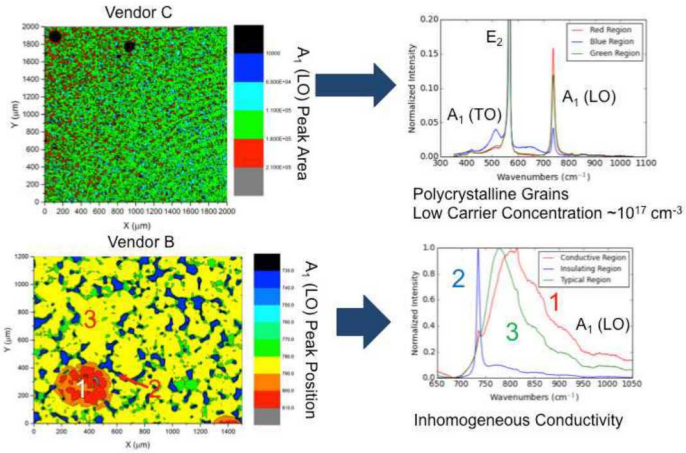
Zygo Surface Scan



AFM



Raman Spectroscopy/Mapping



Goal: Non-Destructive, Wafer-Scale Mapping Techniques for Rapid Screening

Substrate Evaluation

Project Objectives

As-Received Wafer Spec

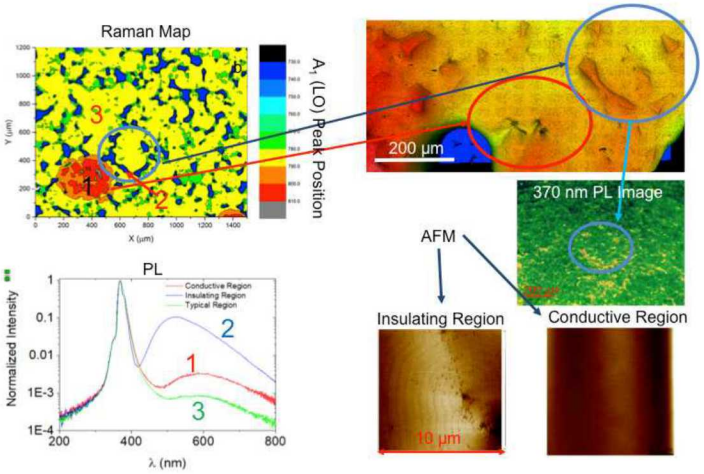
Sample ID	BOW (μm)	Resistivity	Offcut
A	-12	Not supplied	-0.39° to m
B	-5	19 mΩ-cm	0.5°
C	80	Not supplied	0.65°
D	8	1 mΩ-cm	0.3° to m 0 to a

Extracted from Detailed Characterization

Sample ID	Optical Profilometry Roughness	AFM Roughness	XRD Offcut	Raman Carrier Concentration	KSA Bow	XRD (002) FWHM Rocking Curve	Problem Issue	PL band edge to midgap ratio	Median E_2 Raman Shift (cm^{-1})	Median E_2 Raman FWHM (cm^{-1})
A	25.9 nm	0.217 nm	0.377°	10^{17}-10^{18} cm^{-3}	6.6 μm	54''	Large Polishing Roughness	7.25	567.5 +/- 0.2	3.58 +/- 0.06
B	22.7 nm	0.323 nm	0.487°	Inhomogeneous	2.3 μm	90''	Inhomogeneous Conductivity	1163	568.1 +/- 0.1	5.8 +/- 0.2
C	37.0 nm	0.389 nm	0.081°	< 10^{17} cm^{-3}	Large	179''	Grain Boundary Defects	41	567.2 +/- 0.1	4.6 +/- 0.3
D	0.85 nm	0.128 nm	0.503°	> 10^{19} cm^{-3}	3.8 μm		Stress Cracks	0.097	567.0 +/- 0.1	3.46 +/- 0.08

	White Light Interferometry	Raman Spectroscopy	Photoluminescence/SIMS
Vendor A $$$	-50 μm Ridges -Large Long Range Roughness 0.217 nm - 25.9 nm	-Inhomogeneous Conductivity in C-Plane Direction -Uniform Raman Map	-50 μm Ridges -Blue Band Luminescence (C, Mg, or Zn Defects) -PL Similar To Epi Layers
Vendor B $$	-Amorphous Ridge and V Defects	-Inhomogenous Conductivity in plane	-Insulating Ridges at Orange Spots -Low Vacancy and C complexes concentration
Vendor C $	Large Bow	-Low Carrier Concentration -Polycrystalline Grain Boundaries	-High Silicon Concentration
Vendor D $$$$	-Stress Cracks -Low Long Range Roughness 0.128 nm - 0.85 nm	-Large Carrier Concentration -Uniform Raman Map	-Blue PL image- Point Defects

Significant variation at all scales - within wafer, wafer-to-wafer, and vendor-to-vendor




or (Don't Waste Your Grower's Time!!!)

J.C. Gallagher, et. al. J. Cryst. Growth 506, 178-184 (2019)

Pilot Production at NRL/NIST

Incoming Wafers

Evaluation at NRL (Pass/Fail)
- Hg Probe
- Raman
- PL spectrum/map
- PL image/map
- Zygo

Metrology at NIST
- Hg Probe
- Zygo

Fabrication

NRL
- PCM evaluation
- Short loop process development

NIST
- Multi-wafer runs with established process flow
- Mid-process metrology and PCM test (Pass/Fail)
- Target 4 wafers/month

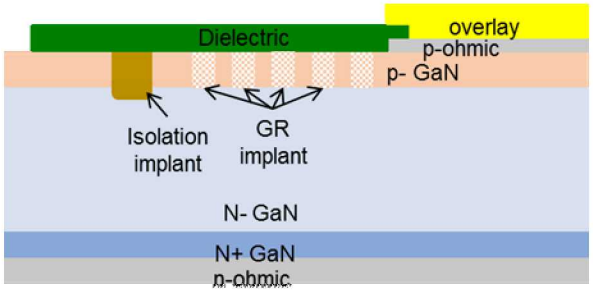
External
- Ion implantation
- Wafer thinning

Testing/Reliability

NRL
- Electrical test, wafer mapping, yield analysis (Pass/Fail)
- EL imaging to study termination performance
- Select parts to be packaged for reliability testing
- EL imaging before/after reliability and stress testing

EDYNX
- HTRB/HTOL
- Packaging

Device Cross-Section (~1 mm^2)

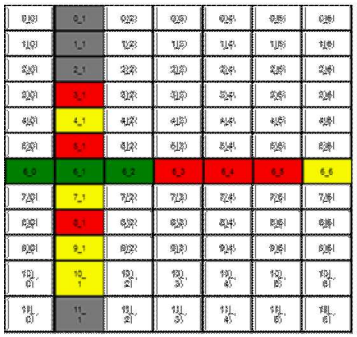


Tools at NRL
MDC Hg Probe
Heidelberg MLA150
Temescal E-beam
AJA Sputterer
Oxford Cl-ICP
Oxford PECVD

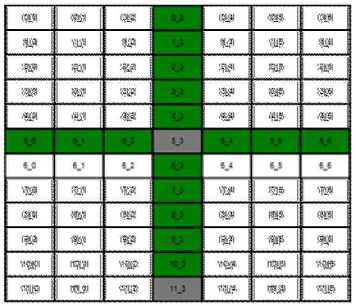
Tools at NIST
Four Dimensions Hg probe
Heidelberg MLA150
ASML Stepper
Denton E-beam Evaporator
Denton Sputter Deposition
Oxford Cl-ICP
PlasmaTherm PECVD

Device Characterization

Wafer #1



Wafer #2

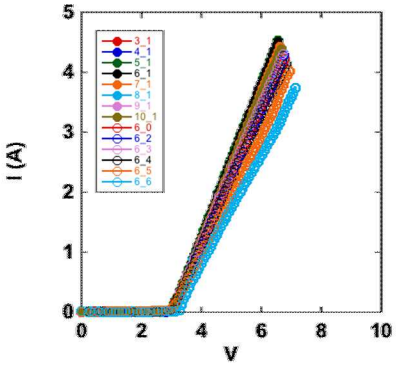


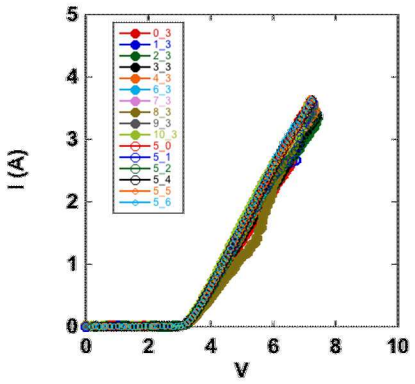
= Fail (I_{-50V} > 100 uA)

= OK (I_{-1000V} > 1 uA)

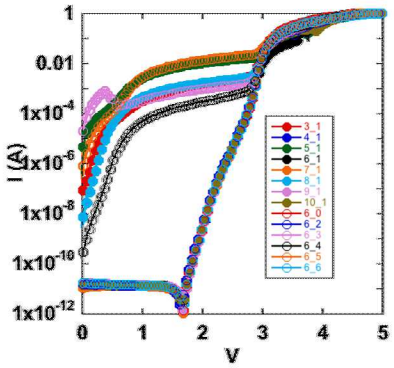
= Good (I_{-1000V} < 10 nA)

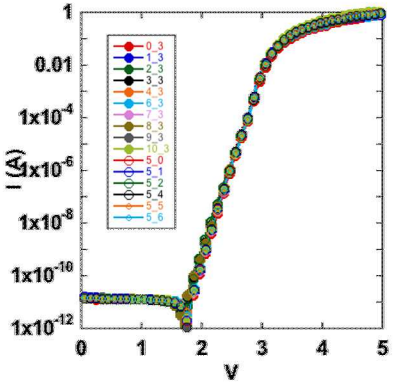
Forward I-V (linear)



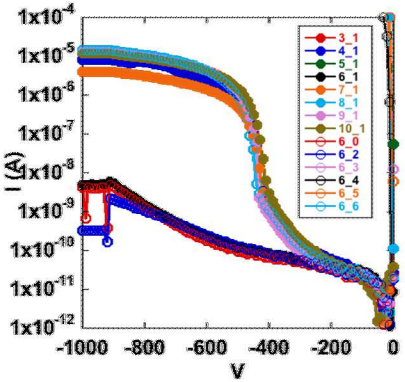


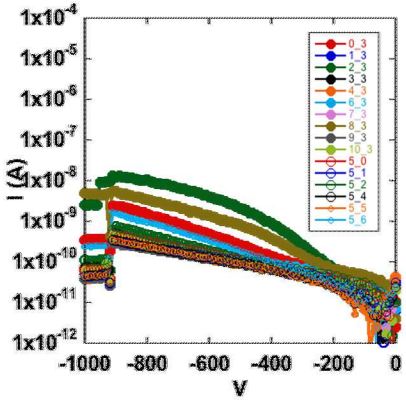
Forward I-V (log)





Reverse I-V (log)



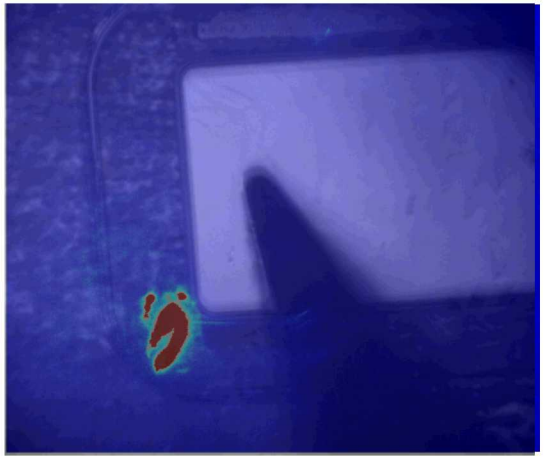


Metrics:

- Forward Current (>500 A/cm^2)
- ON-Resistance (<1.3 mΩ-cm^2)
- Turn-On Voltage (<3.5 V)
- Leakage Current (<1 mA/cm^2)
- Breakdown Voltage (1.2 → 3.3 → 6.6 kV)

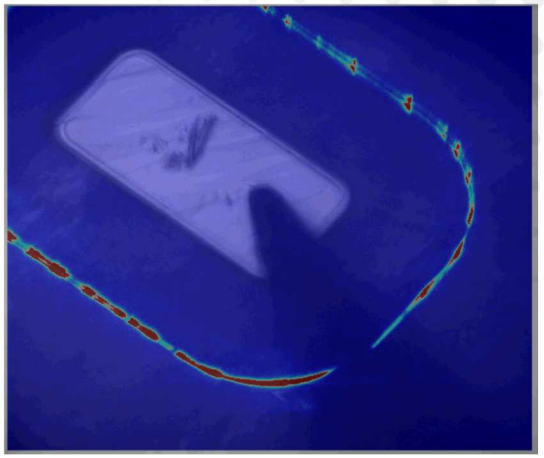
- Significant variation at all scales - within reticle, wafer-to-wafer…
- Quantify yield using auto probing for wafer-scale mapping and data analysis

Breakdown Analysis / FA



Wafer #1 - Unoptimized design

- High field at corner of device
- Large spread in BV across die
- Dominated by localized defects

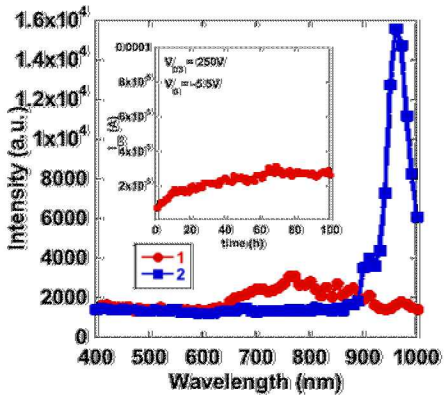


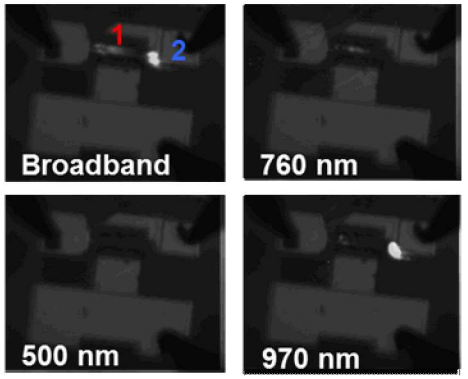
Wafer #2 - Improved termination

- Uniform field spreading along edge of device
- Tight grouping of BV across die

NRL Vacuum Probe Station

- Hyperspectral Imaging
- 20 kV test capability
- 250 – 1000 nm imaging range, 2 nm resolution
- Broadband and Monochromatic Imaging modes
- Wavelength sweep capability to extract spectra

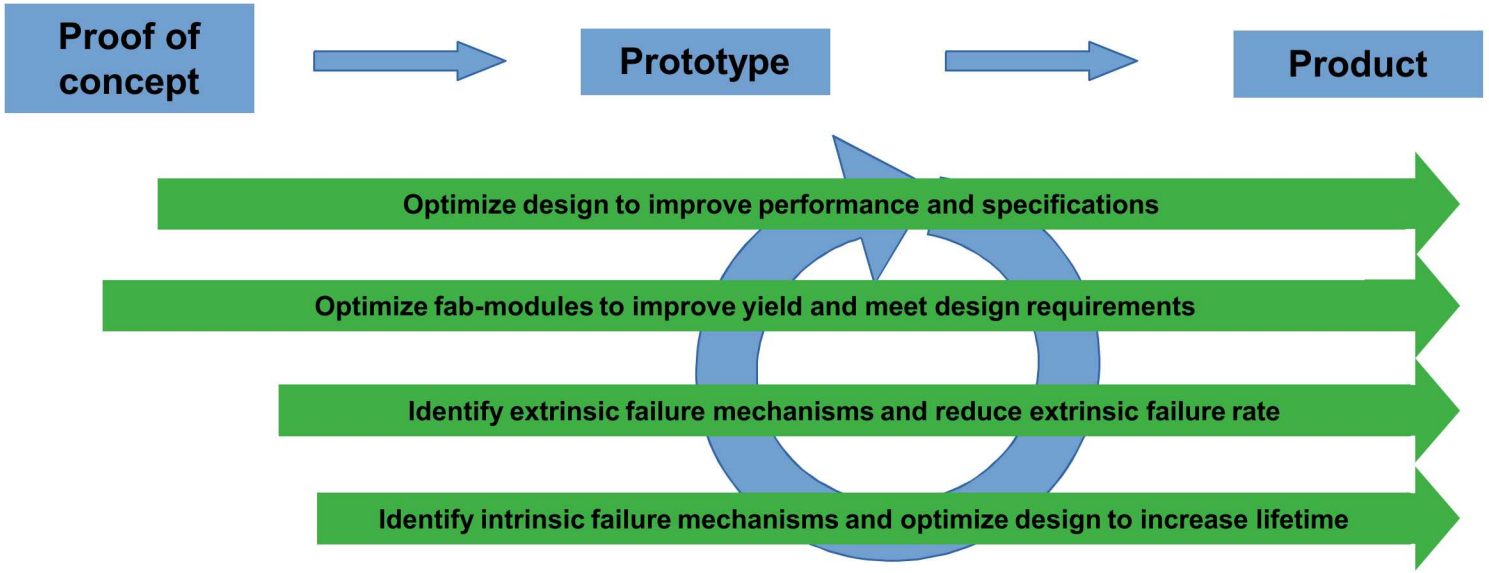




Hyperspectral Imaging of GaN HEMTs

Reliability Evaluation and Failure Analysis

Reliability evaluation helps shorten the product development cycle even when employed during early stages



Methods Used:

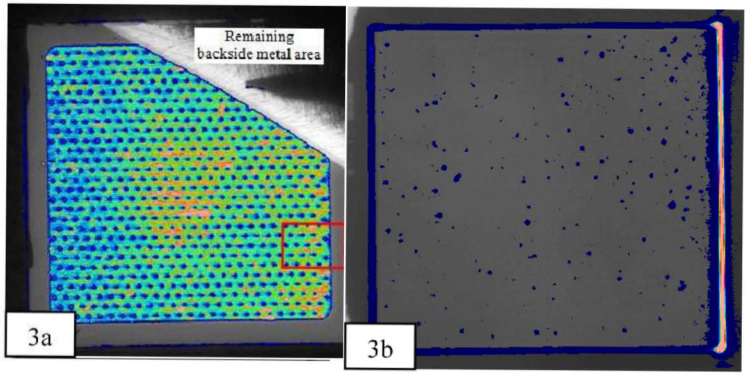
- Short-term stability
- Step-stress
- Failure analysis
- Reliability lifetime evaluation
- Failure-mode identification
- Failure analysis

Foundry process and reliability test / FA integrated in tightly-coupled cycle for fast learning

Reliability and FA Capabilities

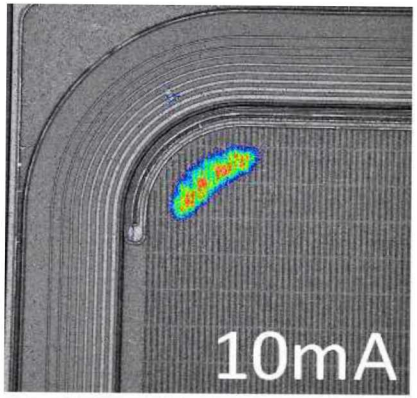
Project Objectives

- **Reliability analysis**
  - **Short-term stress**
  - **Step-stress**
  - **Long-term HTRB, HTOL**
  - **Lifetime estimation**
- **Failure analysis**
  - **Decap**
  - **DFIB, SEM, TEM, EDX, EBIC**
  - **Emission microscopy**
  - **AFM, XPS, PL, CL**
- **Packaging**
  - **High-voltage, high-current packaging**
- **Test and stress capabilities**
  - **Up to 20 kV DC, 100 A DC**
  - **Time monitoring of long-term transients (> 100 ms)**
  - **High-temperature ovens (150 C)**
  - **Cooled oil bath for HTOL stress**
  - **Parametric testing (packaged parts – DC and pulsed)**



Rupp et al., ISPSD 2012

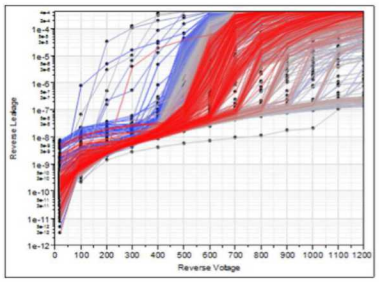
van Meerbeek et al.,
ISPSD 2012



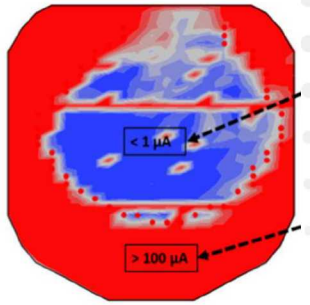
GaN PN Diode Reliability

Project Objectives

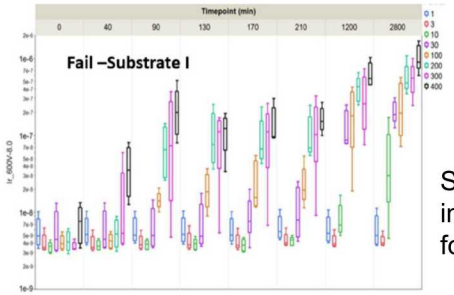
- **Known factors:**
  - **Substrate type (HVPE GaN vs others) [1]**
  - **Substrate supplier [2]**
  - **Current-induced diffusion of H [3]**
- **Possible factors (extrapolated from HEMTs):**
  - **TDDB-like effects in GaN [4]**
  - **Interaction of contacts with GaN surface under bias and/or temperature [5]**
  - **Dynamic effects [6]**
  - **Hot-electron effects [7]**
- **Proposed plan**
  - **Start with evaluation of existing devices**
    - **Establish baseline condition and range of behavior**
    - **Establish wafer-sort limits**
  - **Package and test devices**
    - **1.2, 3.3, 6.5 kV**



I_R-V_R curves for all diodes on a wafer reveal outliers and trends [1]



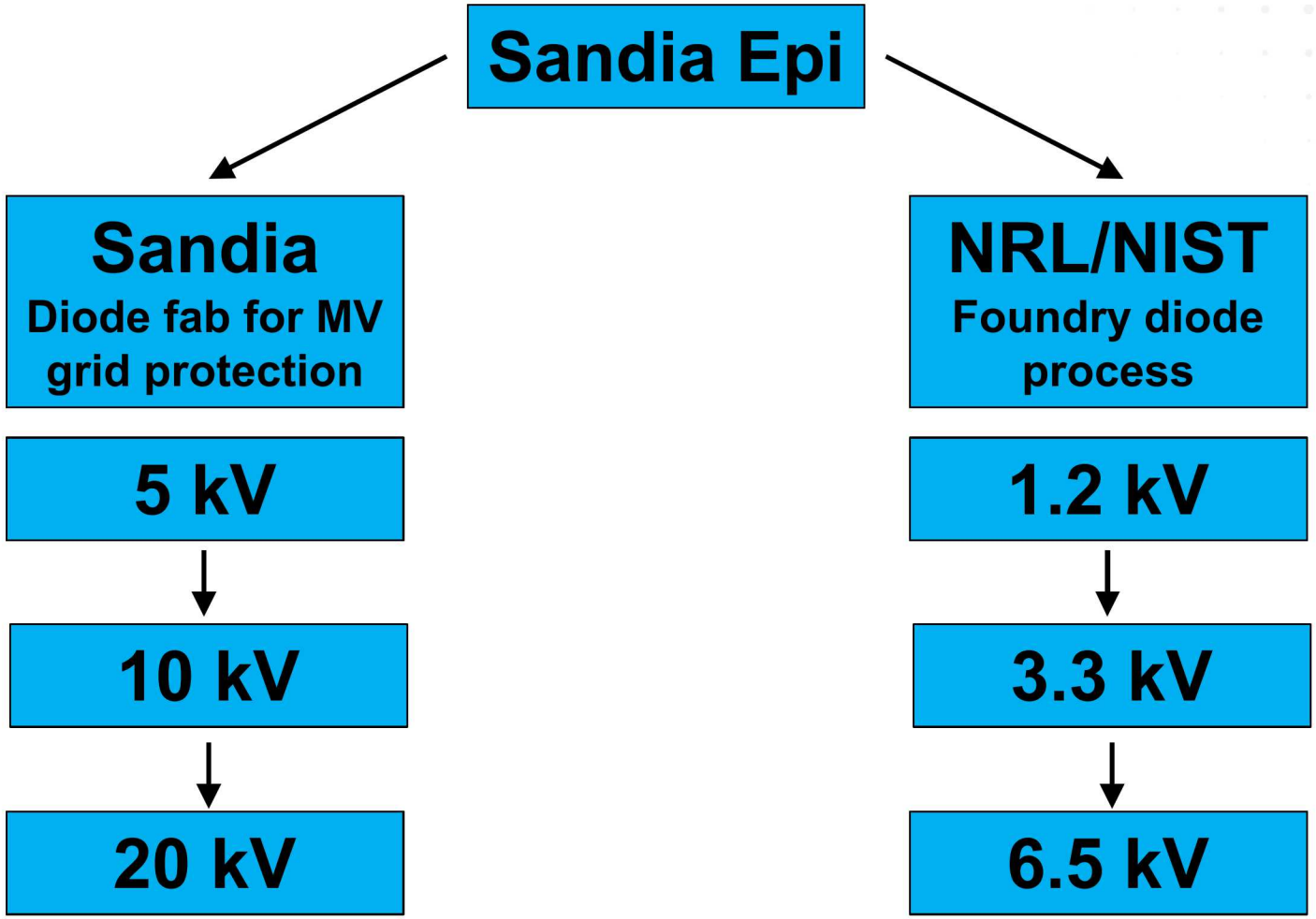
Wafer map of IR shows possible link to wafer non-uniformity [1]



Statistical analysis of increase in IR after forward-bias stress [1]

[1] Kizilyalli et al., IEEE TED 62(2), 414 (2015)
[2] Travis Anderson, private communication
[3] Fabris et al., Microelectronics Reliability 88, 568 (2018)
[4] M. Borga et al., IEEE TED 64(9), 3616 (2017)
[5] D. Marcon et al., Microelectronics Reliability 52, 2188 (2012)
[6] D. Bisi et al., IEEE TED Oct. 2013.
[7] Brazzini et al., IEEE TED 64(5), 2155 (2017)

Device Progression



Year 1 Technical Milestones

Quarter	Description
2	Complete setup of reliability testing capability suitable for 6.5 kV diodes. Test system using existing 1.2 kV diodes.
3	Demonstrate controllable n-type doping in a > 30 μm thick epitaxial GaN layer on a GaN substrate suitable for a 5 kV diode. Concurrently develop epi for 1.2 kV diode to be processed in foundry.
3	Evaluate edge termination approaches based on numerical simulation and compatibility with processing capability. Down-select to best design and optimize for 1.2 and 5 kV diodes.
4	Modify existing reverse-recovery setup to characterize fast avalanche response. Test system using existing 1.2 kV diodes.

Early setup of unique testing capabilities, coupled with development of epi/processing suitable for high-voltage diodes, are key

Initial Device Metrics

Metric	Value (NRL/NIST, Q5)	Value (Sandia, Q6)
Breakdown voltage	≥ 1.2 kV	≥ 5 kV
Area	≥ 1 mm^2	≥ 1 mm^2
Yield	≥ 50% (≥ 1 wafer/lot)	NA
Forward current density	≥ 500 A/cm^2	≥ 330 A/cm^2
Differential on-resistance	≤ 1.3 $m\Omega\ cm^2$	≤ 7.7 $m\Omega\ cm^2$
Turn-on voltage	≤ 3.5 V	≤ 3.5 V
Leakage current density	≤ 1 mA/cm^2 @ 80% of rated V_B	≤ 1mA/cm^2 @ 80% of rated V_B

Will establish device designs and processing capability in year one to meet these goals in year 2

Team Structure

Sandia National Laboratories

Sandia
- Epitaxial growth
- Device design, processing, and test
- MV grid applications

EDYNX
- Reliability and failure analysis

Sonrisa
- Device design

U.S. NAVAL RESEARCH LABORATORY

NRL/NIST
- Foundry process
- Failure analysis

Stanford
- Device design
- Back-side processing
- Breakdown analysis

Sandia

Team

Bob Kaplar – PI, Power devices

Andy Allerman – Epitaxial growth

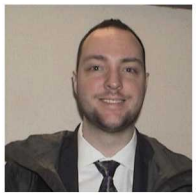
Brendan Gunning – Epitaxial growth

Greg Pickrell – Device processing and test

Mary Crawford – Device processing and test

Andy Armstrong – Defect spectroscopy

Jeramy Dickerson – Device design

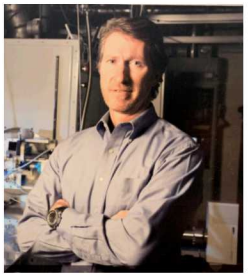


Andrew Binder – Device design

Jack Flicker – Grid applications

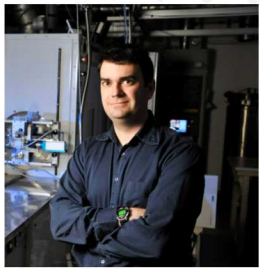
Jason Neely – Grid applications

NRL/NIST



Karl D. Hobart – Failure analysis

Travis J. Anderson – Device processing, electrical testing, failure analysis



Marko J. Tadjer – Device processing

Andrew D. Koehler – Electrical testing, failure analysis

- **Postdoctoral Fellows: James Gallagher and Mona Ebrish – Electrical testing, failure analysis**
- **PhD Student (NPS): Matt Porter – Failure and breakdown analysis**

Stanford / EDYNX / Sonrisa

Srabanti Chowdhury (Stanford) – Device design, processing, and breakdown analysis

Ozgur Aktas (EDYNX, Sandia subcontractor) – Reliability testing and failure analysis

Jim Cooper (Sonrisa, Sandia subcontractor) – Device design

Commercial Objectives

- **Project will mature fast MV grid protection devices**
  - **Will fill a gap in protection against fast E1 EMP components**
  - **Other MV protection applications (e.g. MO V replacement)**
  - **Potentially can save the cost of a major grid failure**
- **Foundry process**
  - **Establish key building blocks in first steps towards a domestic commercial vertical GaN foundry**
  - **Will encourage small companies to invest in vertical GaN technology**
  - **Will help increase demand for GaN substrates, improving their availability, quality, and uniformity, and reducing their cost**
  - **Eventual parity in substrate and processing cost with SiC will achieve lower costs for vertical GaN, due to area scaling resulting from higher critical electric field**

Conclusions

- Project will advance the state-of-the-art ion vertical GaN devices
  - 20 kV breakdown is 4x higher than today's SOA
  - Immediate target application is MV grid protection
  - Establishment of foundry process will make key baseline processes reproduceable and accessible, reducing costs and accelerating technology adoption
- Key challenges
  - Thick, low-doped GaN epitaxial layers are a key challenge and require expertise and investment in fundamental growth and doping/defect physics
  - Design and processing of edge termination structures will also be a key challenge
  - Reliability characterization and failure analysis will be closely coupled with foundry process in iterative learning cycles
- Solutions will leverage broad expertise of the team