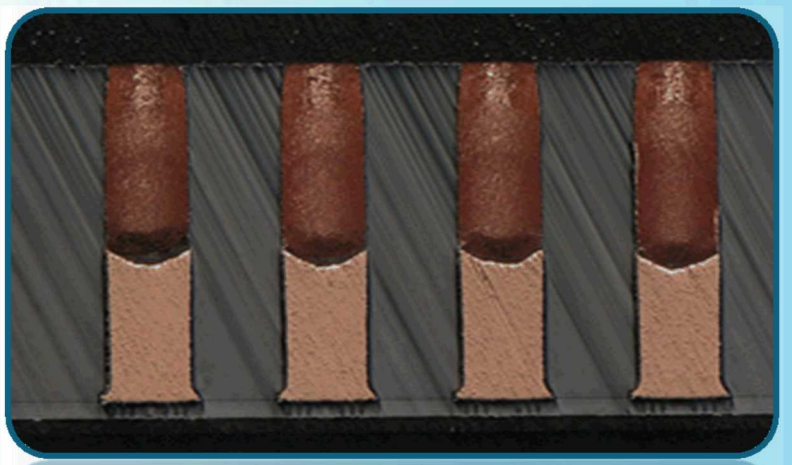
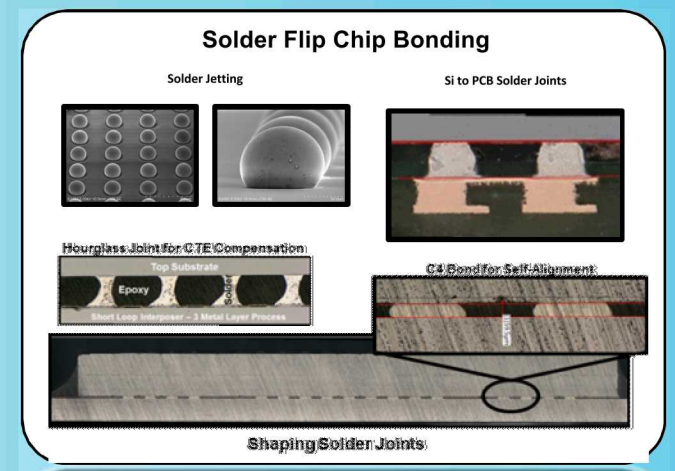
SAND2019-3994PE

Utilizing Electroplating for 2.5D and 3D Integration –

Through Silicon Vias and Fine Pitch Micro Bump Formation





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505 263 1095

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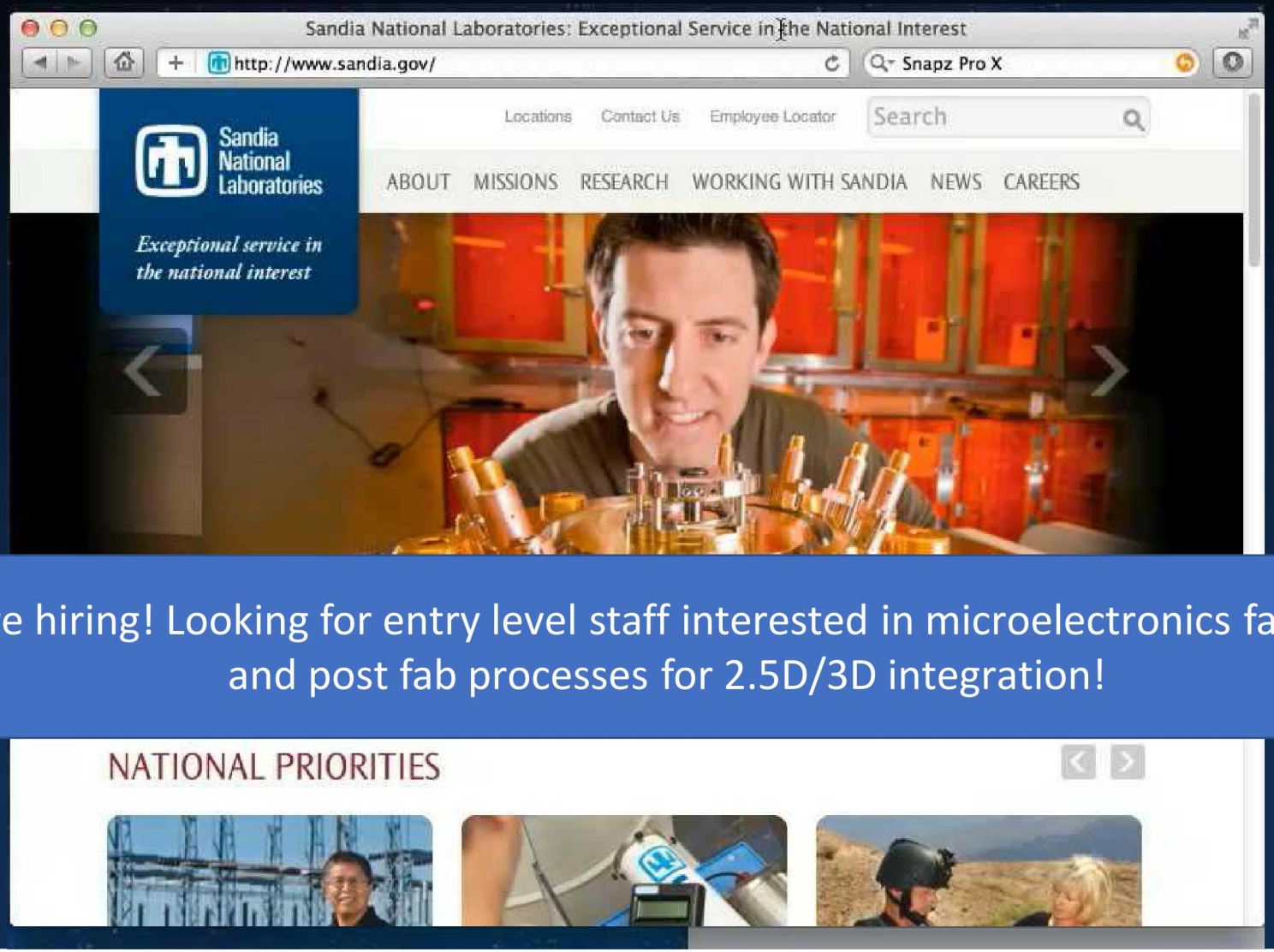
How to Apply - sandia.gov/careers

Advanced Search & Job Agent/email notification



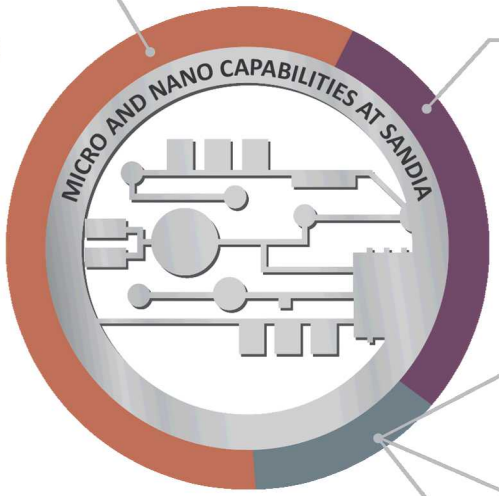
We are hiring! Looking for entry level staff interested in microelectronics fabrication and post fab processes for 2.5D/3D integration!

Microsystems Engineering Sciences Applications (MESA) Center Overview

Unique Facilities Differentiate Sandia's Micro/Nano R&D

MESA

MICROSYSTEMS
ENGINEERING SCIENCES
AND APPLICATIONS



CDC

COUNTERFEIT
DETECTION CENTER

CINT

CENTER FOR INTEGRATED
NANOTECHNOLOGIES

IBL

ION BEAM LABORATORY

ACRR

ANNULAR CORE
RESEARCH REACTOR

- Only source for custom strategic rad-hard microelectronics
- Largest government-owned foundry
- FFRDC with the broadest and deepest micro and nano expertise [derived R&D-product delivery work mix]

What is MESA?

- Microsystems Engineering Sciences Applications (MESA) is a $462M FFRDC-based development and production facility for any microsystem component or technology that cannot or should not be obtained commercially.

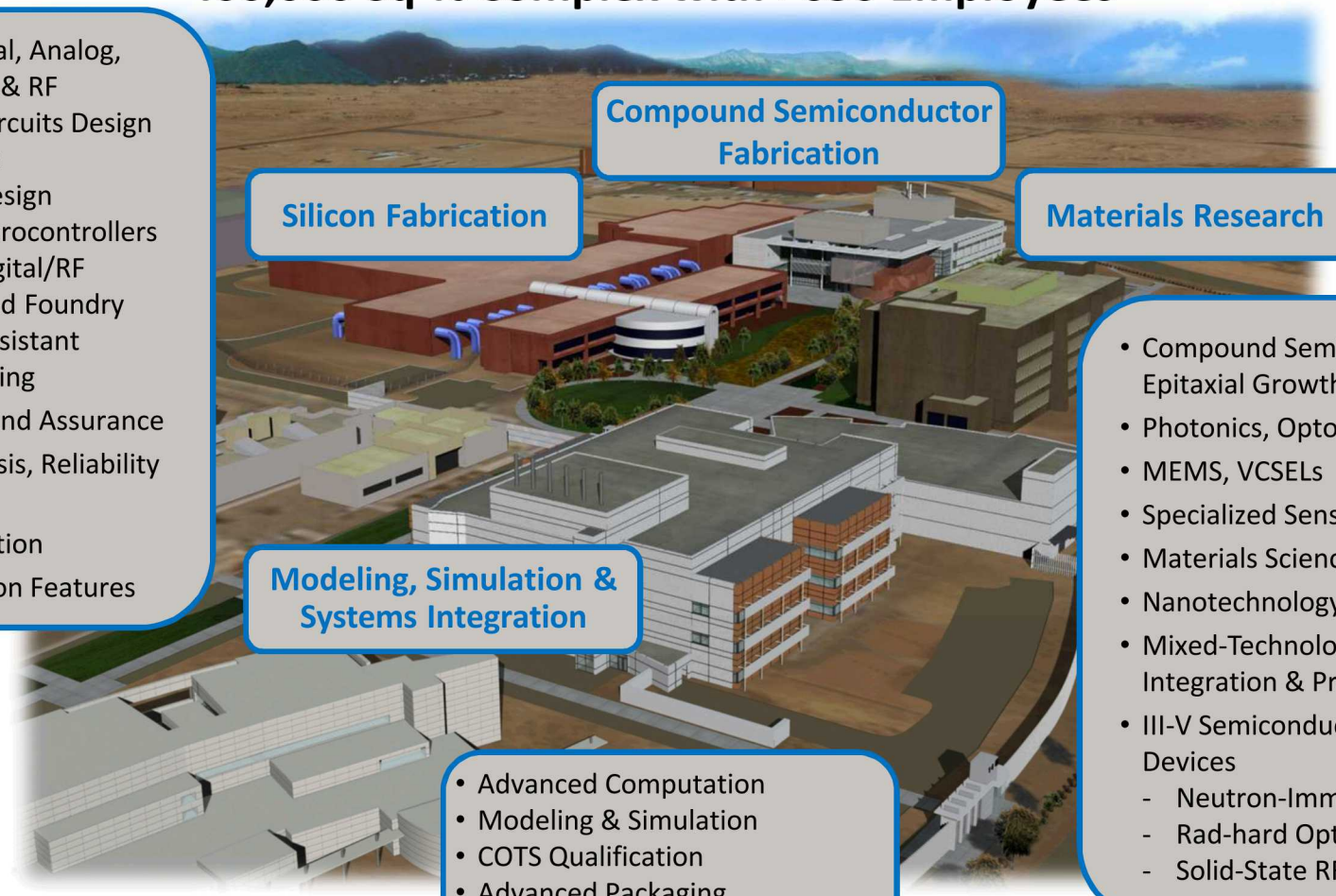
- MESA Develops and Delivers:
  - Strategic radiation-hardened custom integrated circuits (ICs)
  - Digital/Analog/Mixed-Signal/RF ICs
  - Trusted Products and Designs
  - 5-Level MEMS
  - III-V Compound Semiconductors
  - Optoelectronic/Photonic Devices
  - High-speed/RF Electronics
  - Heterogeneous Integration
  - Failure Analysis/Reliability Physics
  - Advanced Packaging
  - Specialized Sensors

MESA bridges science to systems, providing an environment where multidisciplinary teams create ***microsystems-enabled*** solutions to our nation's most challenging problems.

Microsystems and Engineering Sciences Applications (MESA)

400,000 Sq-ft Complex with >650 Employees

- Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design & Fabrication
- Custom IC Design
  - Secure microcontrollers
  - Analog/Digital/RF
  - IBM Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects and Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features



- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test

- Compound Semiconductor Epitaxial Growth
- Photonics, Optoelectronics
- MEMS, VCSELs
- Specialized Sensors
- Materials Science
- Nanotechnology, Chem/Bio
- Mixed-Technology Integration & Processing
- III-V Semiconductor Devices
  - Neutron-Immune HBT
  - Rad-hard Optical Links
  - Solid-State RF Devices

Sandia's MESA (Microsystems and Engineering Sciences Applications) Fabs

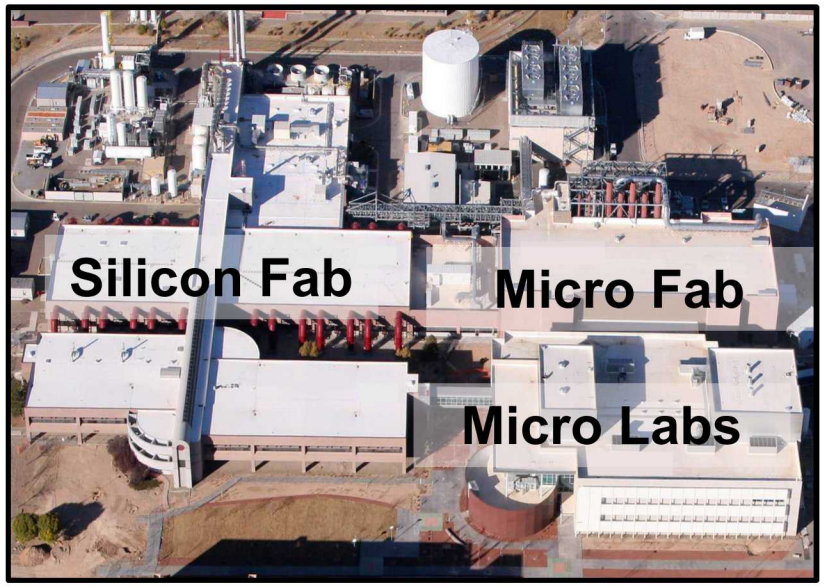
Silicon Fab

- **Over 13,000 ft^2 of Class 1 Clean Room**
- **Rad Hard CMOS Microelectronics**
- **MEMS**
- **Si Photonics, Optical Waveguides**
- **Ion Traps**

Micro-Fab

- **15,000 ft^2 of Class 10/100 Clean Room**
- **Compound Semiconductors**
- **Vertical Cavity Lasers, Modulators**
- **RF Electronics & Photonics**
- **Post Silicon Wafer Processing**
- **3D Integration**

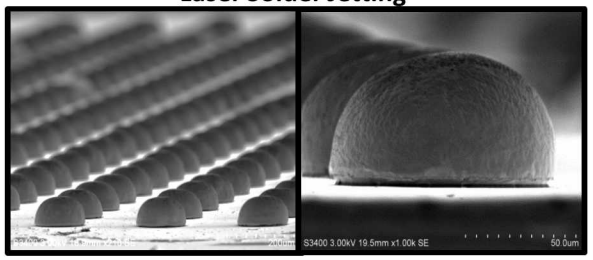
Micro Labs



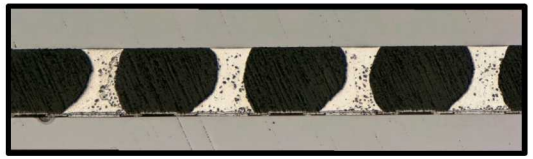
Flip Chip Bonding
Solder Jetting, Cu Pillars, Au and In Bumps

- Highly flexible R&D level solder bump deposition and rework
- D2D and D2W reflow attachment
- C4 flip chip
- Solder joint shaping
- Au thermocompression bonding
- Indium bump bonding
- Cu pillars

Laser Solder Jetting

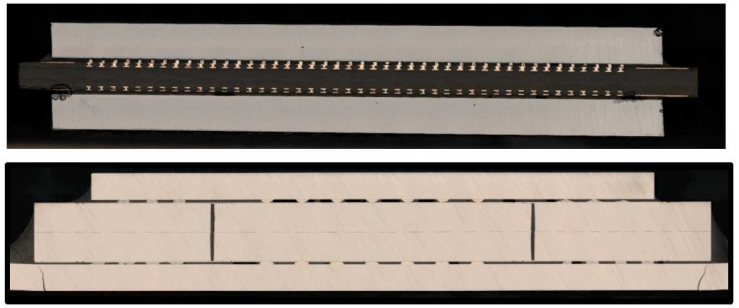


Solder Joint Shaping for Managing CTE Mismatch

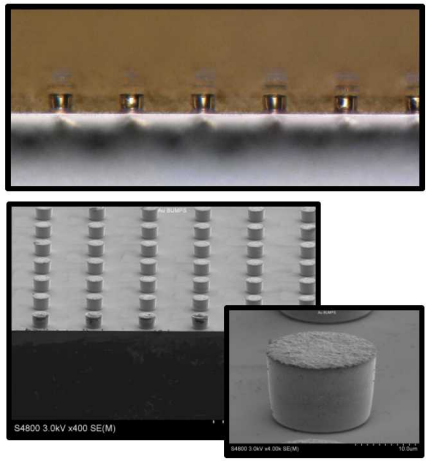


$Y=\frac{\Delta\alpha\Delta T}{h}$ Y = Strain, Δα = delta CTE, ΔT = delta temp, h = height of solder joint

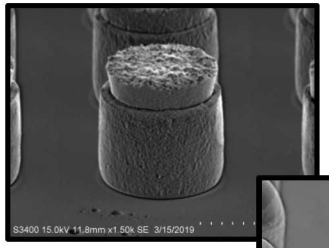
Multi-Chip Stacking



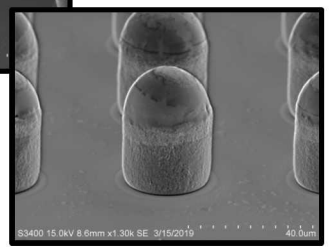
Electroplated Au Bumps



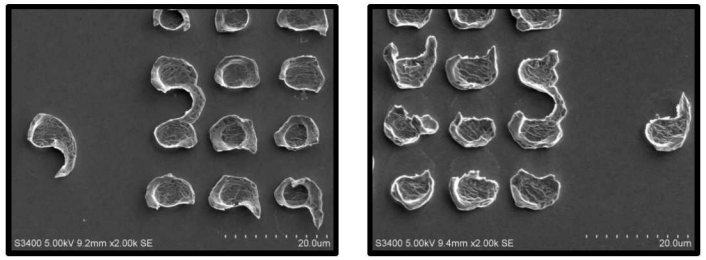
SnAg Capked Cu Pillar

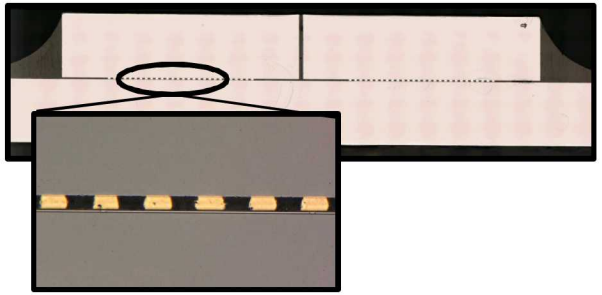


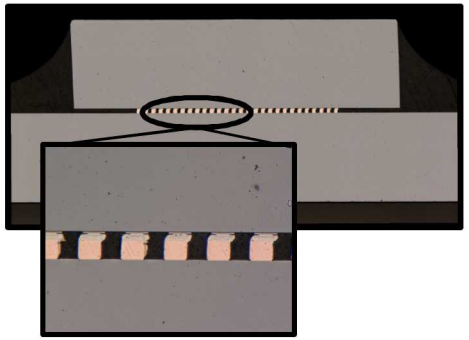
SnAg Reflow



Corresponding Sites of De-bonded Indium Bumps



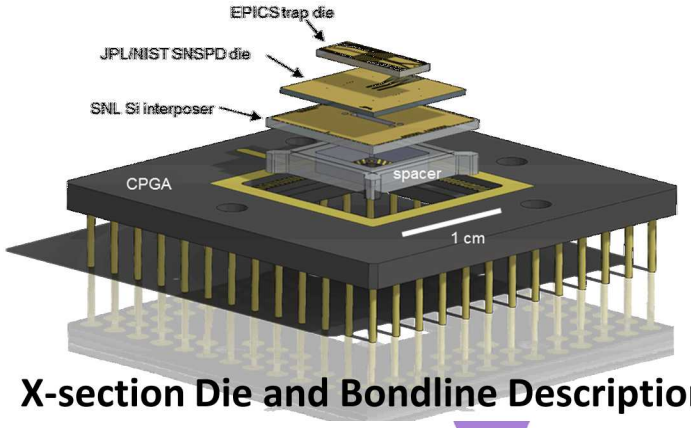




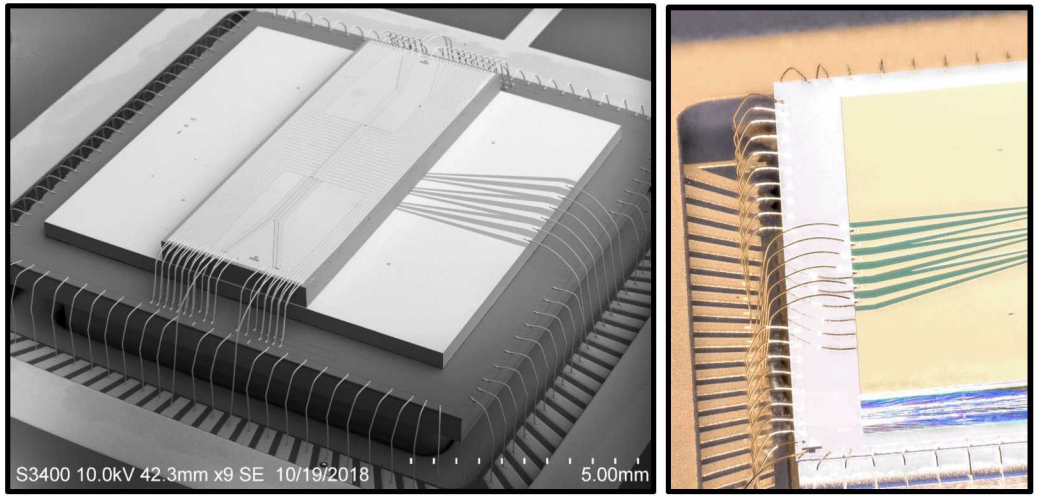
EPICS (*Extreme Performance Ion Trap-cavity System)*
Heterogeneous Integration Approach

- **Collaboration between SNL/JPL/NIST/Duke Univ.**
- **Combine SNSPD (superconducting nanowire single photo detector) with an optical cavity and microfabricated ion trap for enhanced ion detection**
- **Solder, epoxy, and indium bonds used to connect these 5 components with 4 different wirebond profiles for full connectivity**

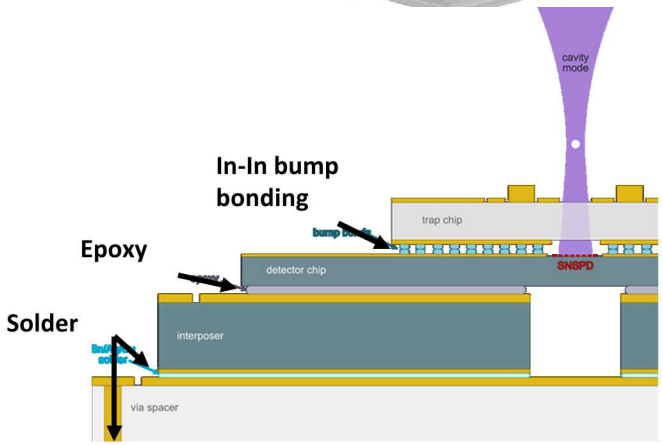
Packaging CAD Rendition



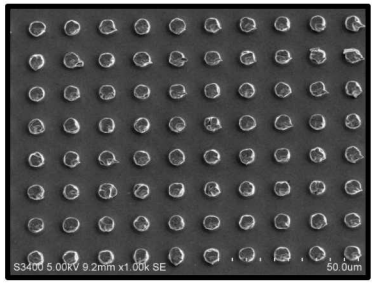
SEM of Final Assembled Device



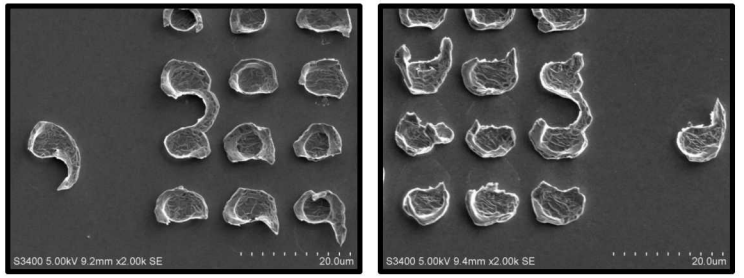
X-section Die and Bondline Descriptions



Indium microbumps



Corresponding sites of de-bonded die

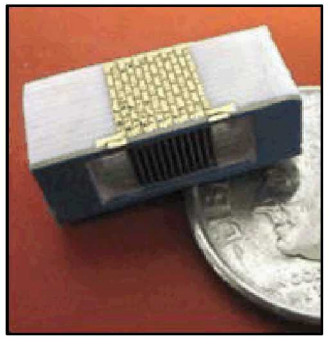


Jungsang Kim, *ECE, Physics and CS Department, Duke University*
Varun Verma, Sae Woo Nam, *National Institute for Standards Technology*
Emma Wollman, *Jet Propulsion Laboratory*
Christian Arrington, Andrew Hollowell, Patrick Finnegan Peter Maunz, *Sandia National Laboratories*

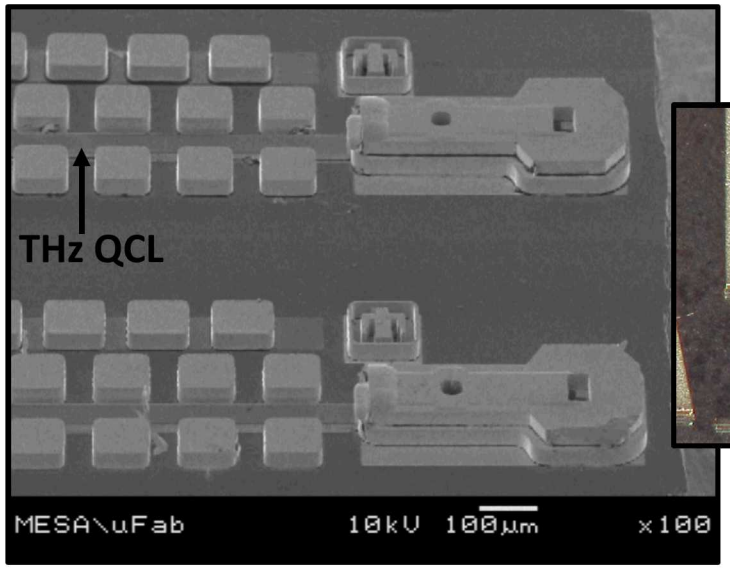
Plating Applications

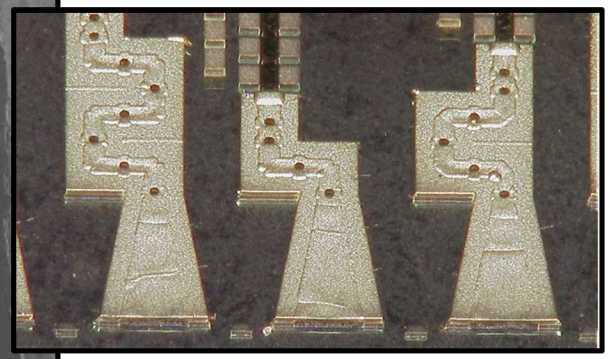
Masking achieved through unique fixturing and controlled polymer deposition




3-D Integrated Gold THz Waveguides

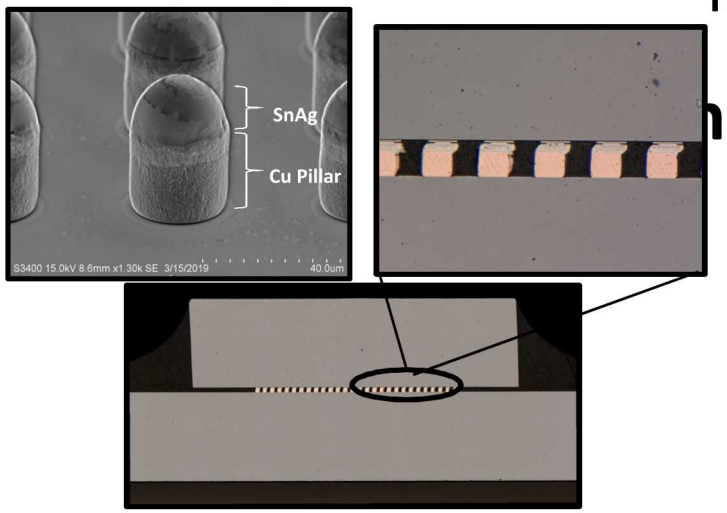




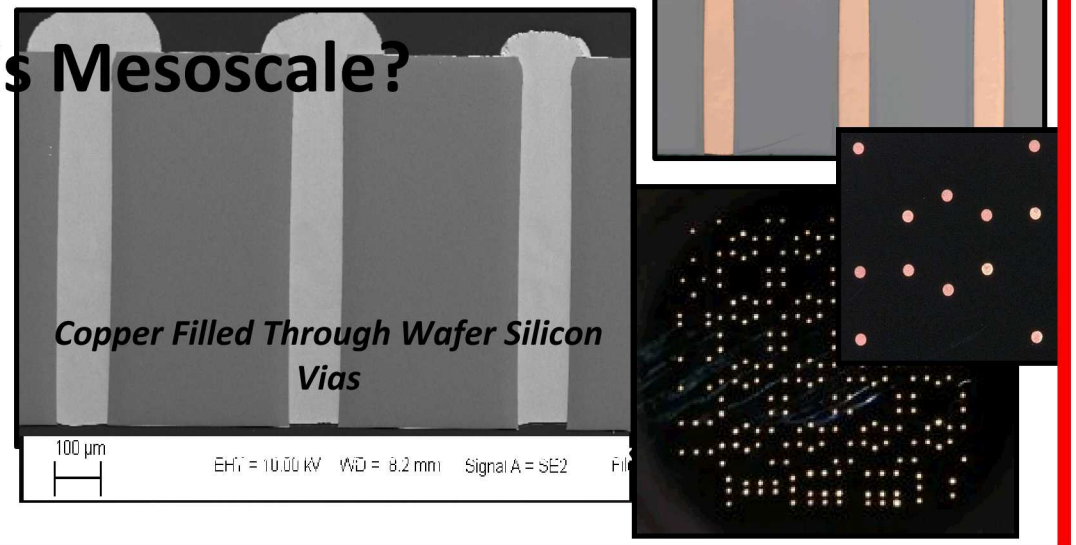
Mesoscale Fabrication
Filling, Forming, and Coating

What is Mesoscale?

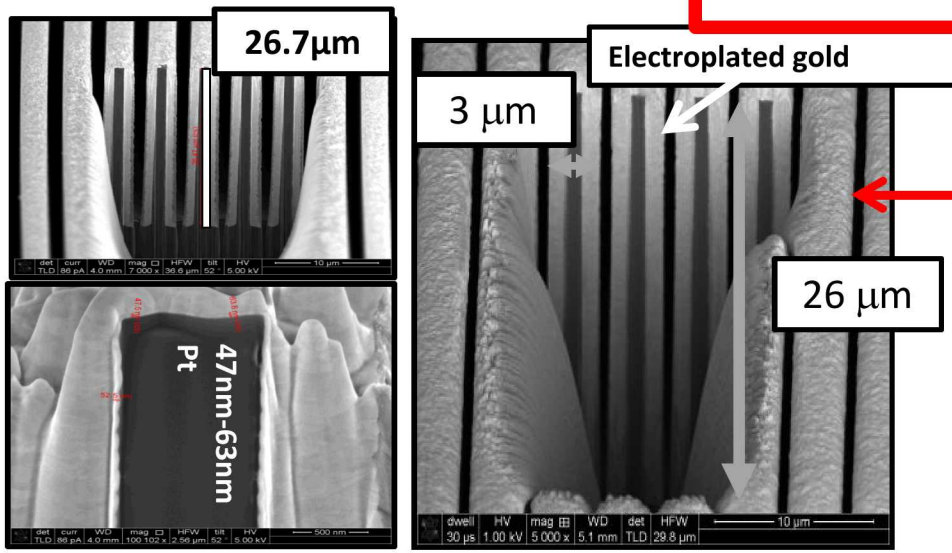
Cu Pillar µ-Bumps



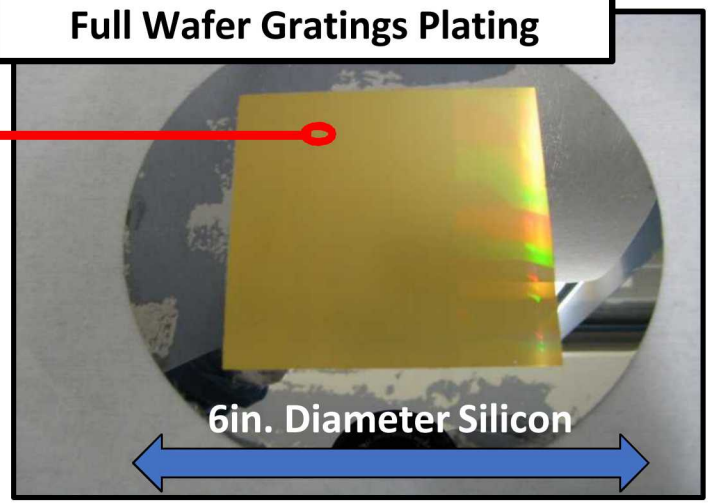
Through Full Substrate Via Filling



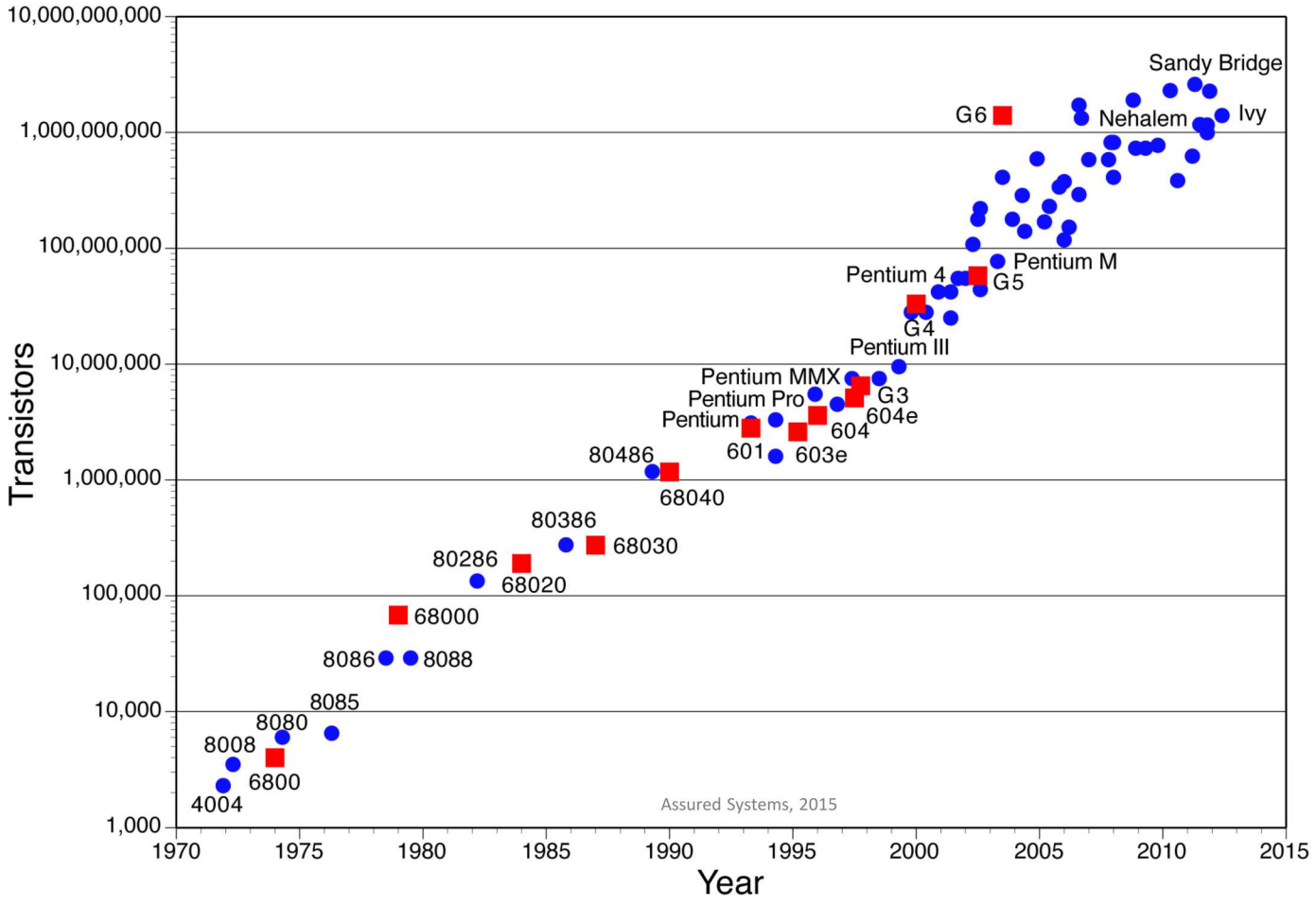
Precision Electro-coating



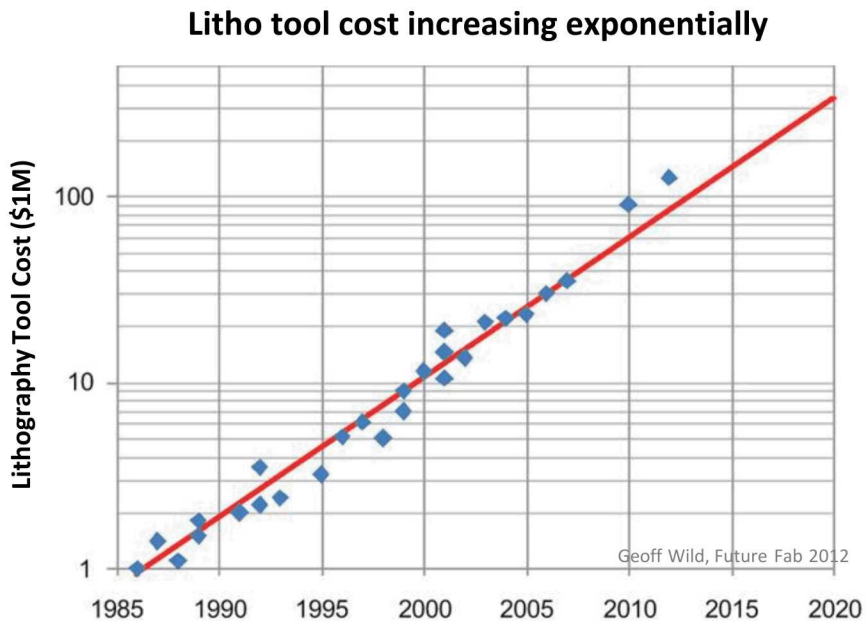
Full Wafer Gratings Plating

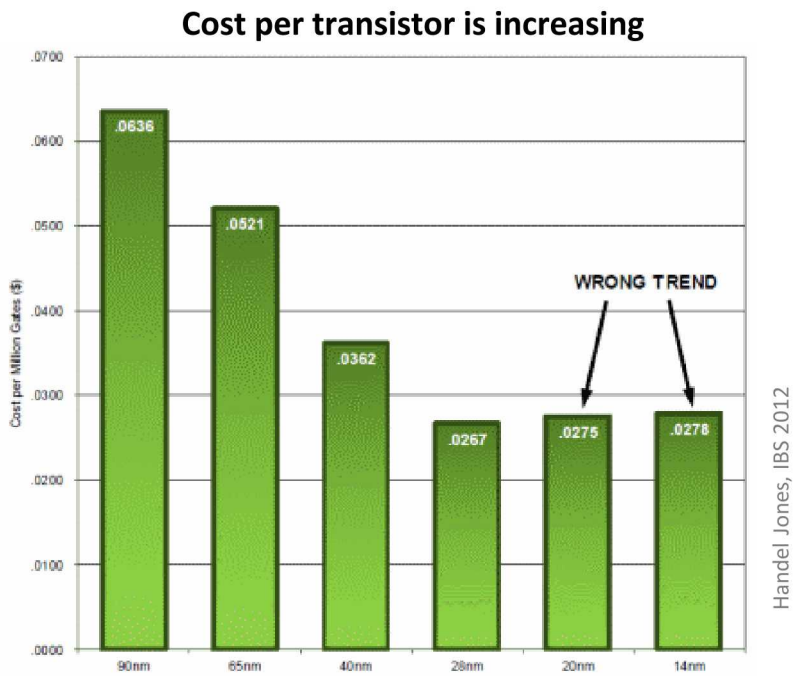


Moore's Law: Marching Towards 0nm!

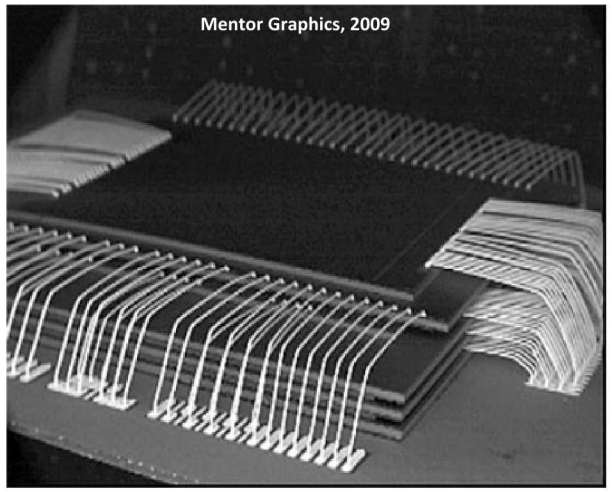


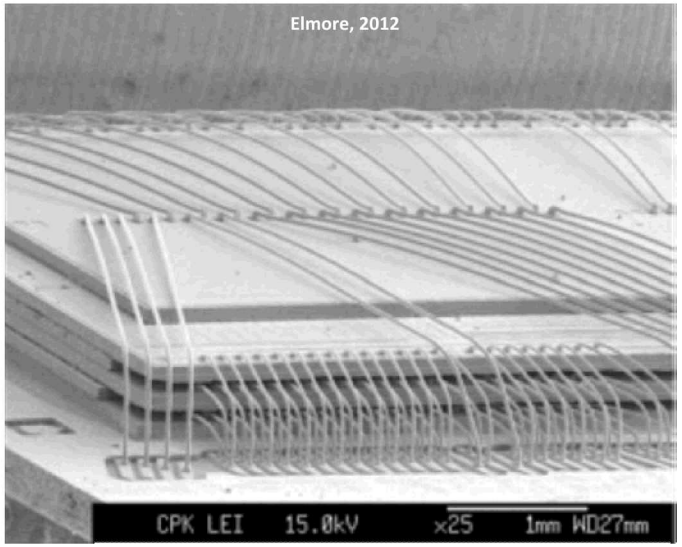
Moore's Law: Not So Fast…

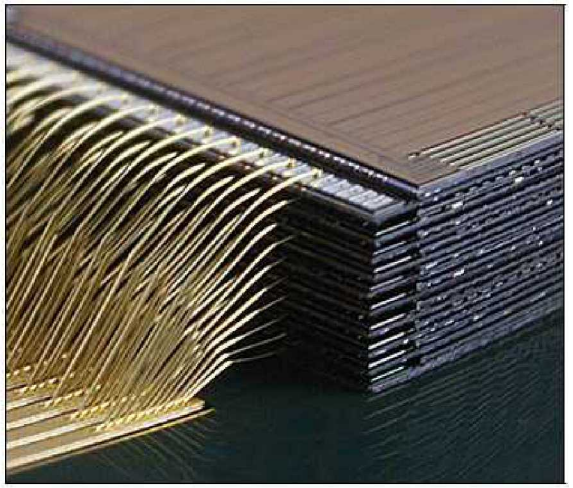


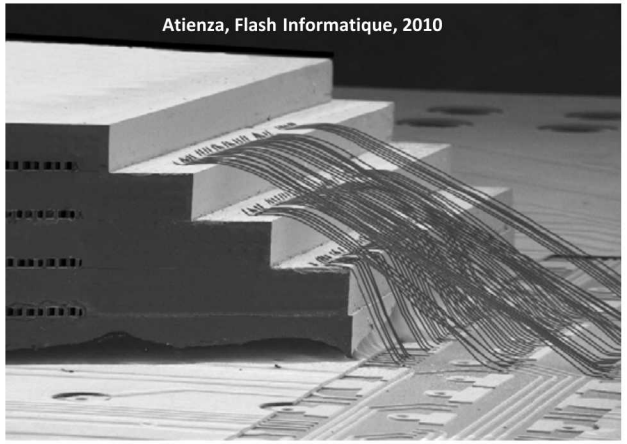


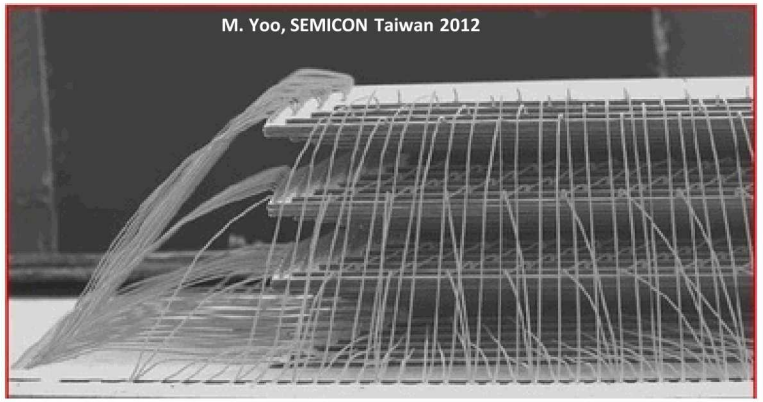
One Way to Increase Bandwidth…

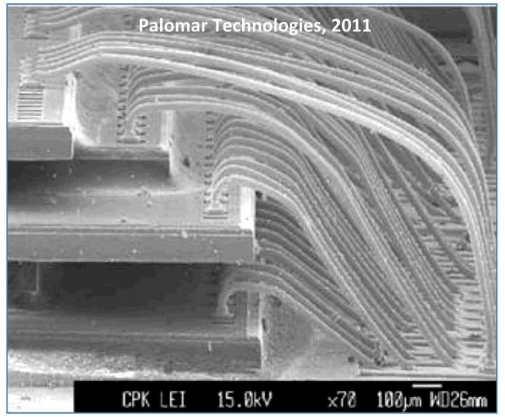




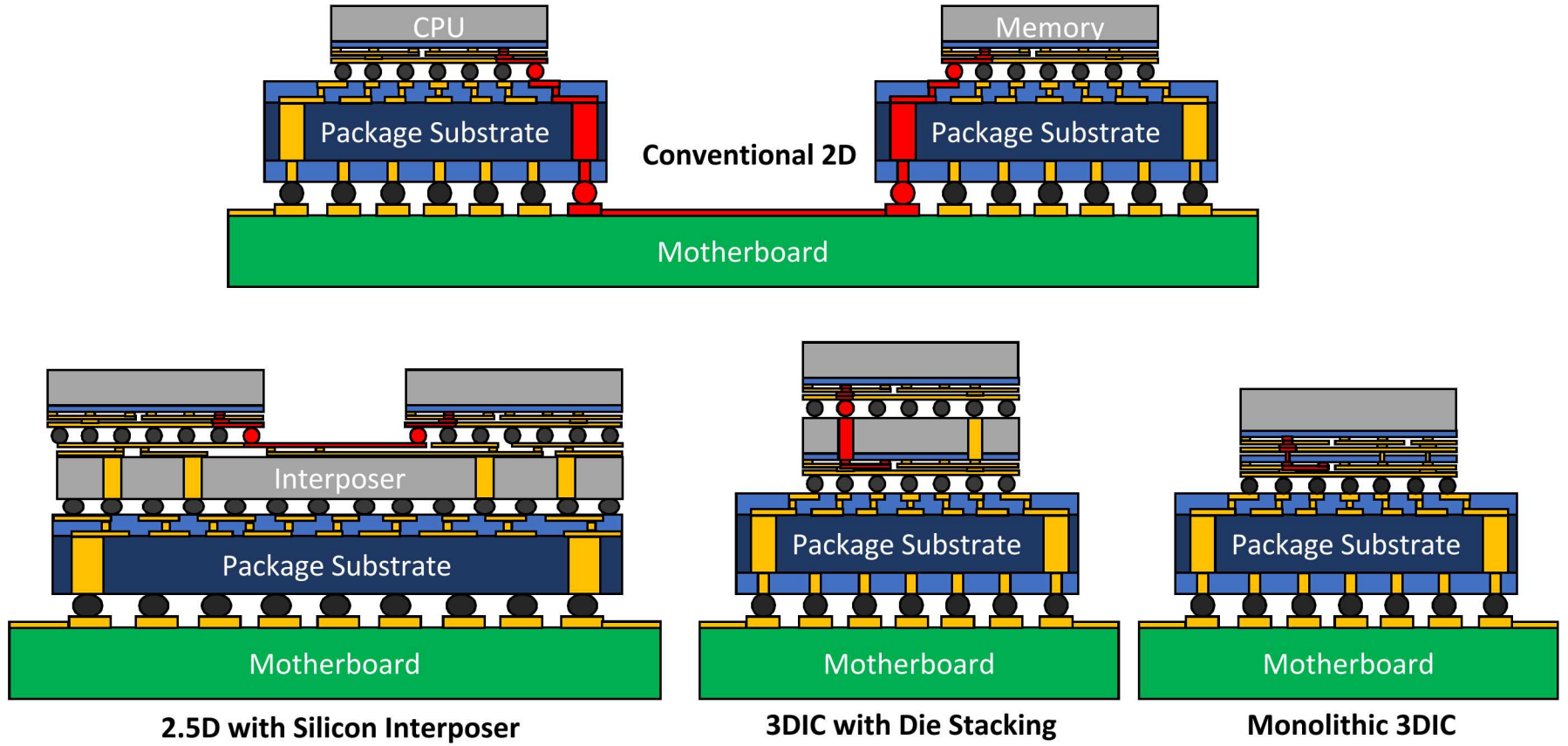








3D Integration Landscape



Through Substrate Vias (TSVs) for MEMS Devices

Benefits of TSVs

- **Increase I/O per area**
- **Improved thermal sinking**
- **Reduced electrical parasitics**
- **Simplified design and assembly**

Cu TSVs vs Doped Si TSVs

Material	Doped Si	Copper
Resistance single TSV	$40\,\Omega$	$0.8\,\mathrm{m}\Omega$
Thermal conductivity	$150\ \frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}$	$400\ \frac{\mathrm{W}}{\mathrm{m}\cdot\mathrm{K}}$

MEMS TSVs Integration with SOI Substrates

TSV-First[1]

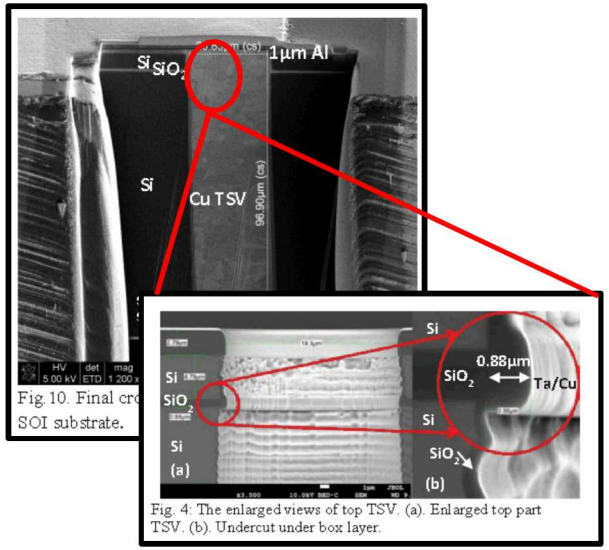


Fig. 10. Final cr
SOI substrate.

Fig. 4: The enlarged views of top TSV. (a). Enlarged top part TSV. (b). Undercut under box layer.

TSV-Last[2]

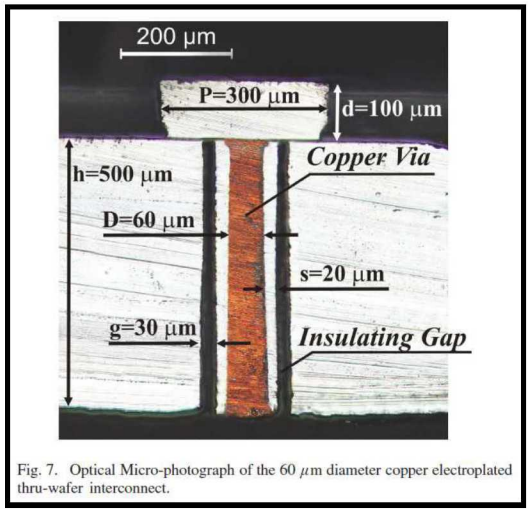


Fig. 7. Optical Micro-photograph of the 60 μm diameter copper electroplated thru-wafer interconnect.

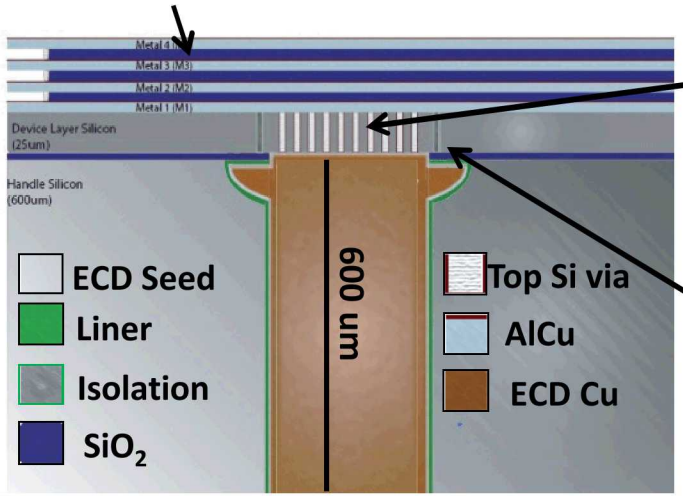
Sandia's TSV Requirements

- **Via-Last TSVs**
- **Full Thickness Si Wafers**
  - **Maintain radius of curvature**
  - **Maintain large mass for accelerometers**
- **Void free fill**

1. G-K. Lau et. al "Process Integration and Challenges of Through Silicon Via (TSV) on Silicon-On-Insulator (SOI) Substrate for 3D Heterogeneous Applications." 17th Electron. Packaging Tech. Conf., (2015).
2. A. Efimovskaya, et. al "Double-Sided Process for MEMS SOI Sensors with Deep Vertical Thru-Wafer Interconnects." Journal of Microelectromechanical Systems, Vol. 27, No. 2, April 2018

Hybrid W Via First, Cu Via Last Approach for SOI Substrates

Multi-layer routing (SUMMiT-V or BEOL CMOS)

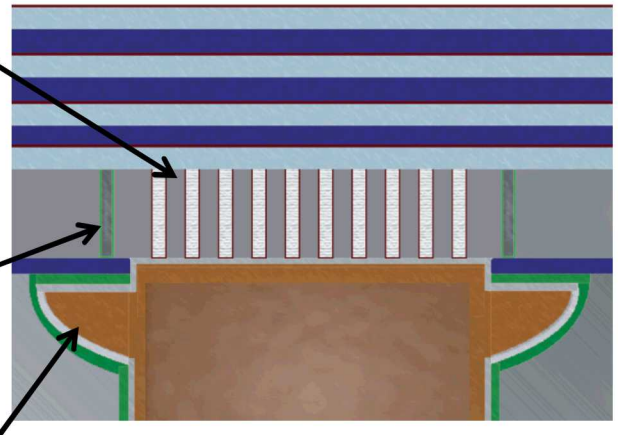


100 um

W vias to connect Cu TSV through BOX and top Si layer

Isolation trench to insulate the vias from the device Si layer

Notch from ion reflection is difficult to insulate and fill with Cu



TSV-First[1]

Su… …l from a conformal ALD Pt seed

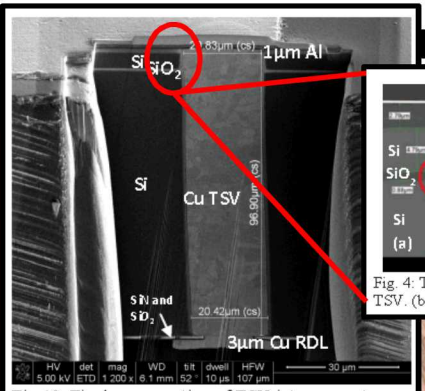


Fig. 10. Final cross-section of TSV interconnect on SOI substrate.

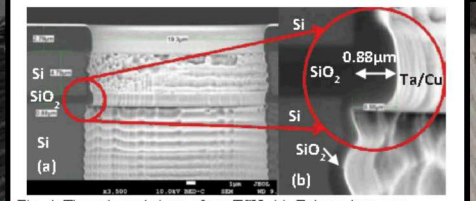
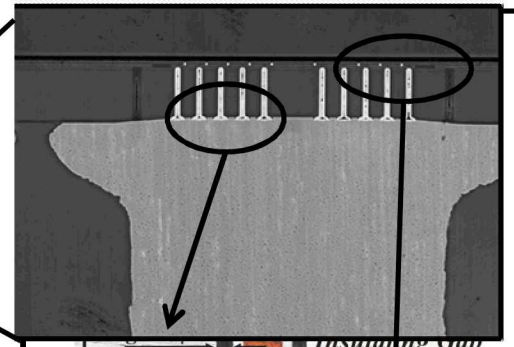
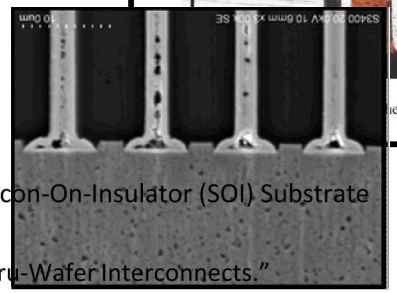
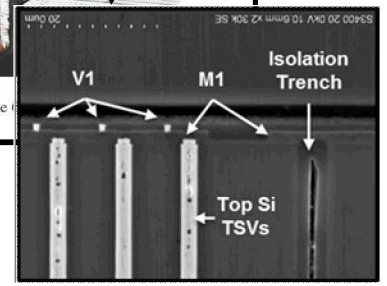


Fig. 4: The enlarged views of top TSV. (a). Enlarged top part TSV. (b). Undercut under box layer.

TSV-Last[2]







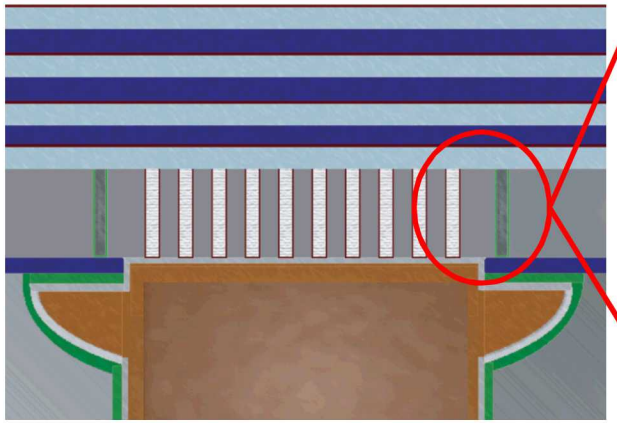
1. G-K. Lau et. al "Process Integration and Challenges of Through Silicon Via (TSV) on Silicon-On-Insulator (SOI) Substrate for 3D Heterogeneous Applications." 17th Electron. Packaging Tech. Conf., (2015).

2. A. Efimovskaya, et. al "Double-Sided Process for MEMS SOI Sensors with Deep Vertical Thru-Wafer Interconnects." Journal of Microelectromechanical Systems, Vol. 27, No. 2, April 2018

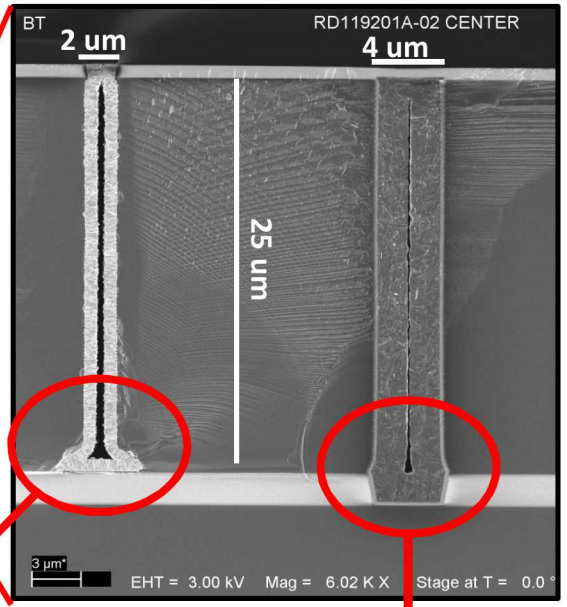
Conduction and Isolation Across the Device Layer Si

ALD Pt
Al_2O_3 Liner
Isolation Trench
SiO_2

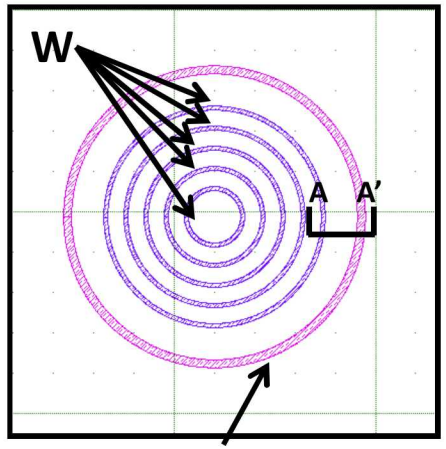
W TSV
AlCu
ECD Cu
Passivation



Cross section A-A’

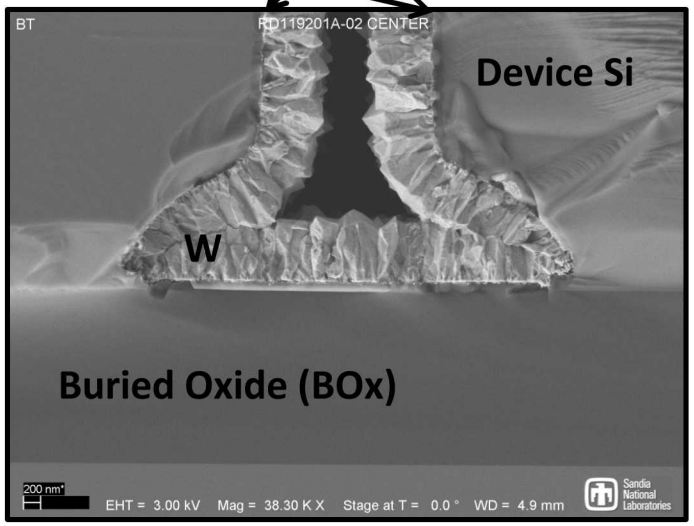


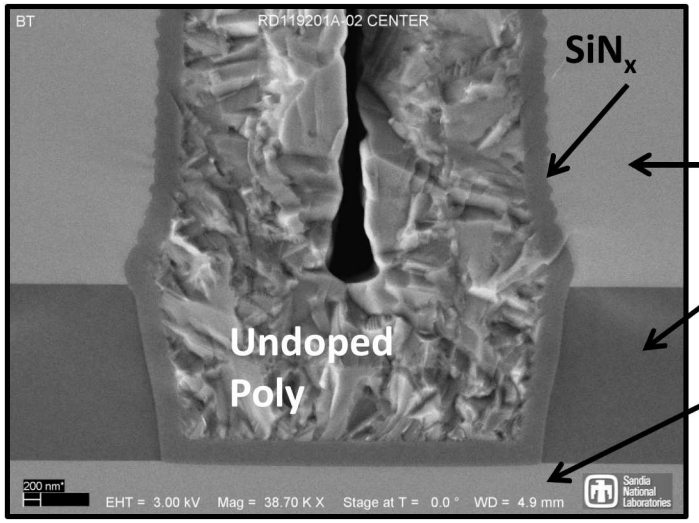
Device Si Layout



Isolation Trench

Degenerately doped Poly Si



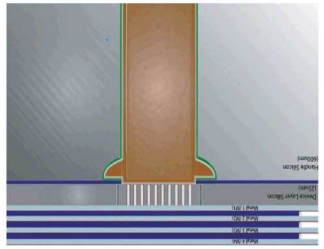


Device Si

BOx

Handle Si

TSV Insulating Liner



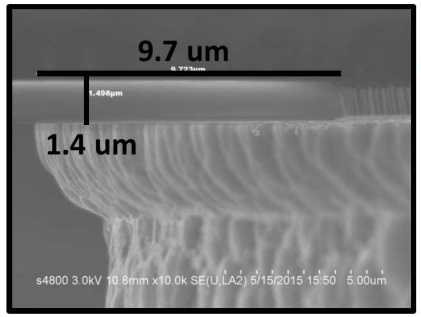
ALD Pt
Liner
Isolation Trench
SiO_2
W TSV
AlCu
ECD Cu
Passivation

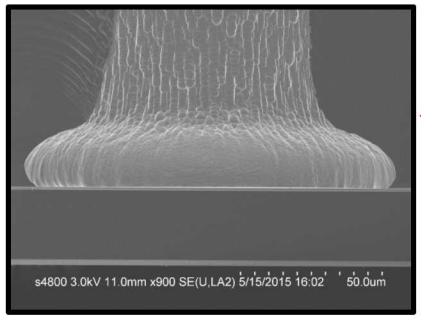
Insulating Liner Constraints

- Must be conformal
- Temperature can't exceed 450C
- Sufficient breakdown voltage

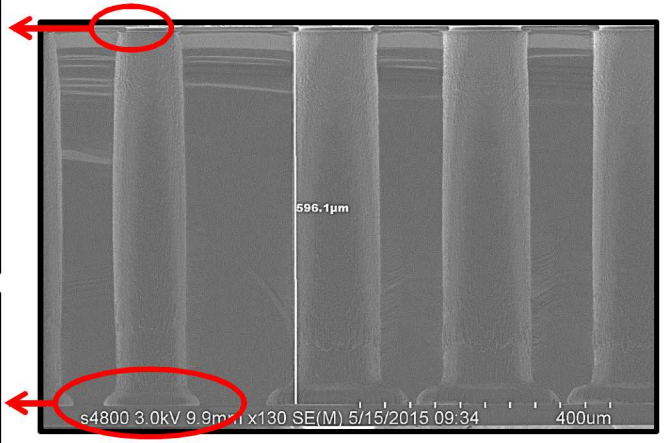
Liner Options

- ~~Sputter deposited insulator (SiO_2, Al_2O_3, etc.)~~
- Low Temp Oxide (LTO)
- ~~ALD Al_2O_3~~





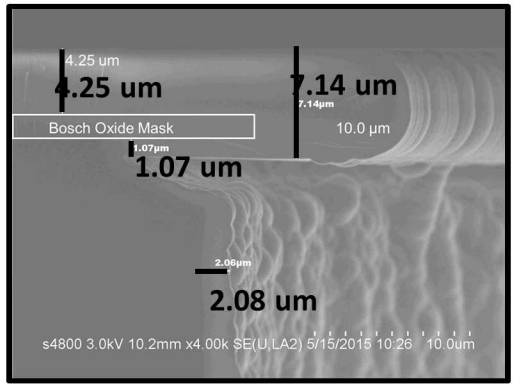
Substantial hardmask undercut

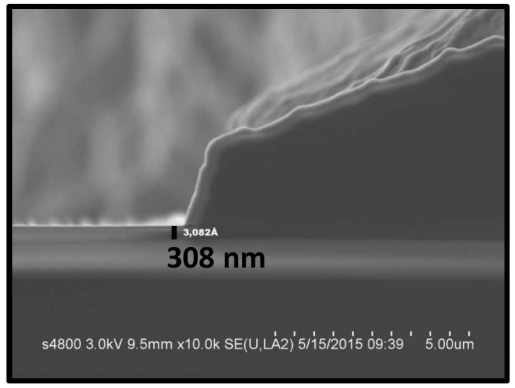


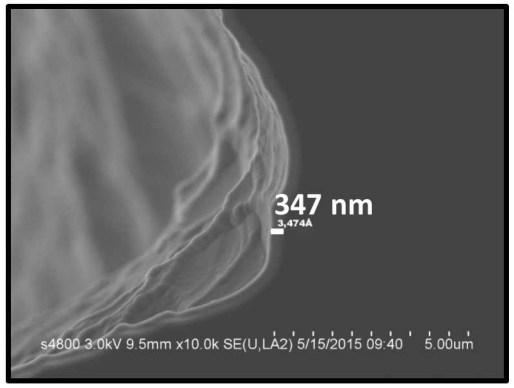
TSV Etch Cross Section

Using the BOX as an etch stop results in notching

Low Temperature Oxide Cross Section

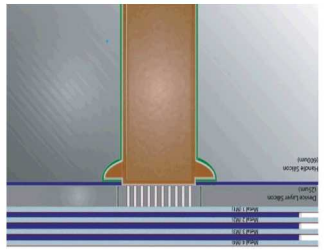






- LTO does conform around the hardmask undercut
- Uniformity is not optimum: 4.25um deposition on top surface and 300nm deposition at the bottom of the TSV

TSV Insulating Liner



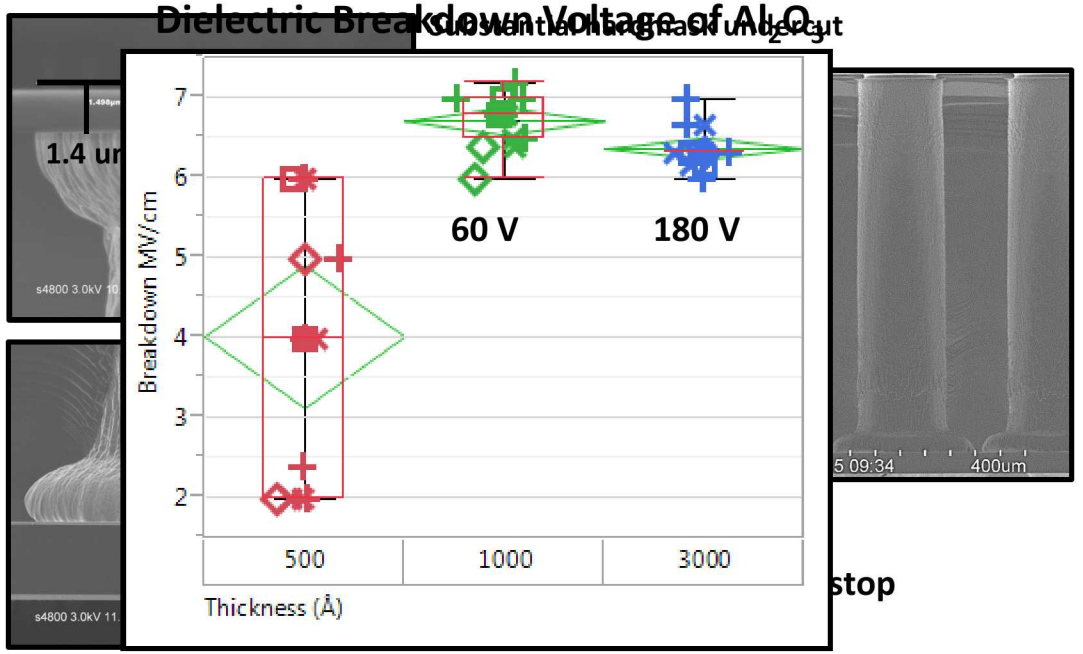
ALD Pt
Liner
Isolation Trench
SiO_2
W TSV
AlCu
ECD Cu
Passivation

Insulating Liner Constraints

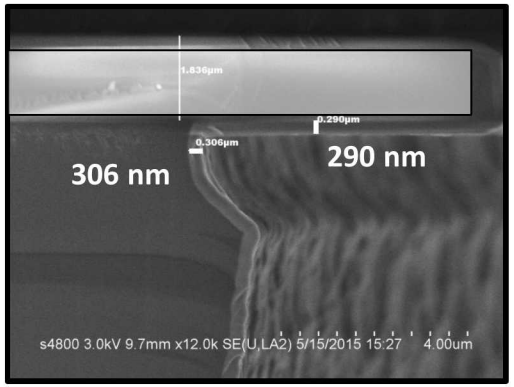
- Must be conformal
- Temperature can't exceed 450C
- Sufficient breakdown voltage

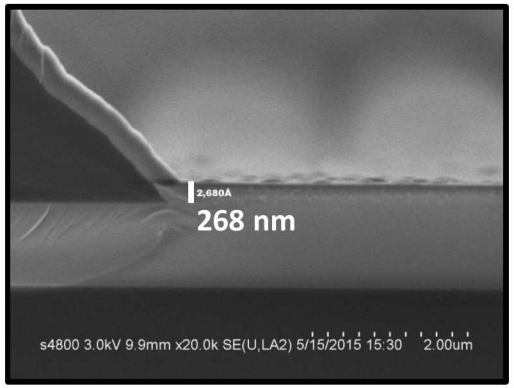
Liner Options

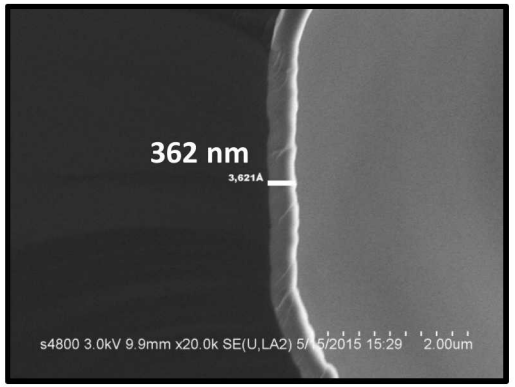
- ~~Sputter deposited insulator (SiO_2, Al_2O_3, etc.)~~
- ~~Low Temp Oxide (LTO)~~
- ALD Al_2O_3



Atomic Layer Deposition Al_2O_3 Cross Section



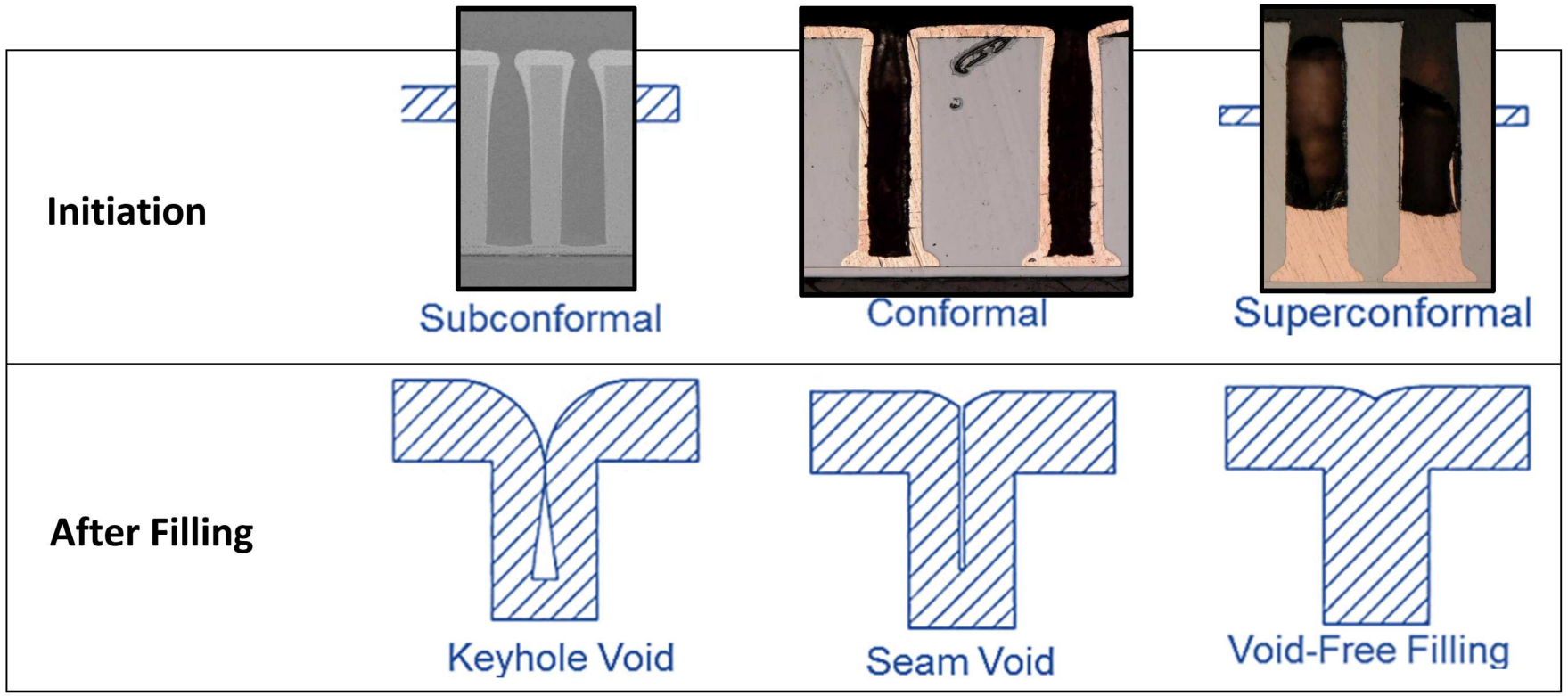




- ALD Al_2O_3 conforms around hardmask undercut and is extremely uniform between the top and bottom of the TSV

Electroplating Fill Profiles

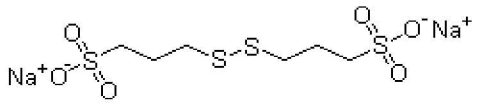
- **Additive free ECD leads to subconformal fill**
- **Pulsed plating regime can establish a conformal fill profile**
- **Additives enable superconformal void-free filling**



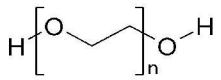
Acid Sulfate Electrodeposition Additives

Common Additives Used In Printed Circuit Board Plating

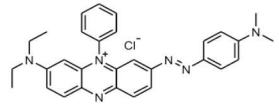
Accelerator
bis-(sodium sulfopropyl)-disulfide
(SPS)



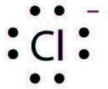
Suppressor
Polyethylene
Glycol (PEG)



Leveler
Janus Green B
(JGB)



HCl, KCl
Or
NaCl



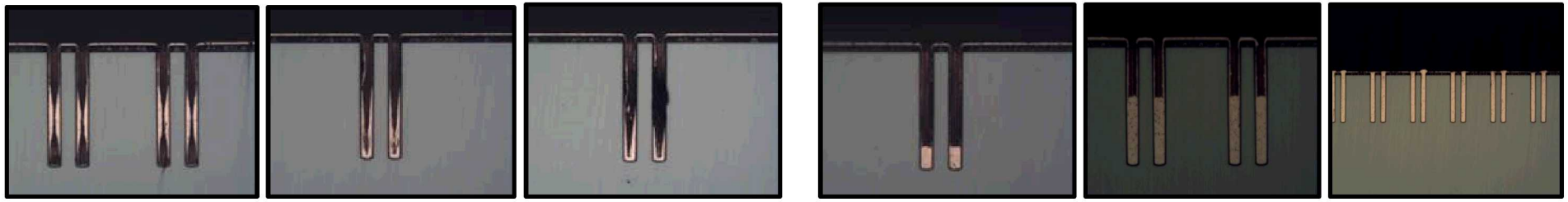
- **<u>Accelerator</u> – Surfactant molecule that adsorbs on the surface and, by coverage increase with area loss, preferentially increases plating rate in concave regions**
- **<u>Leveler</u> - Disables accelerator to reduce overburden thickness; grain refiner**
- **<u>Suppressor</u> - Large chain polymer, typically PEG, (1k-20k mW) whose gradient of concentration yields an associated gradient in deposition rate (slower higher in via)**

1. All 3 additives carried over from PCB plating development
2. **Only the suppressor is needed to achieve void free TSV filling**

S-NDR Electrolyte for Void Free Superfilling

NIST Bottom up filling in IBM 56 µm deep TSVs[1,2]

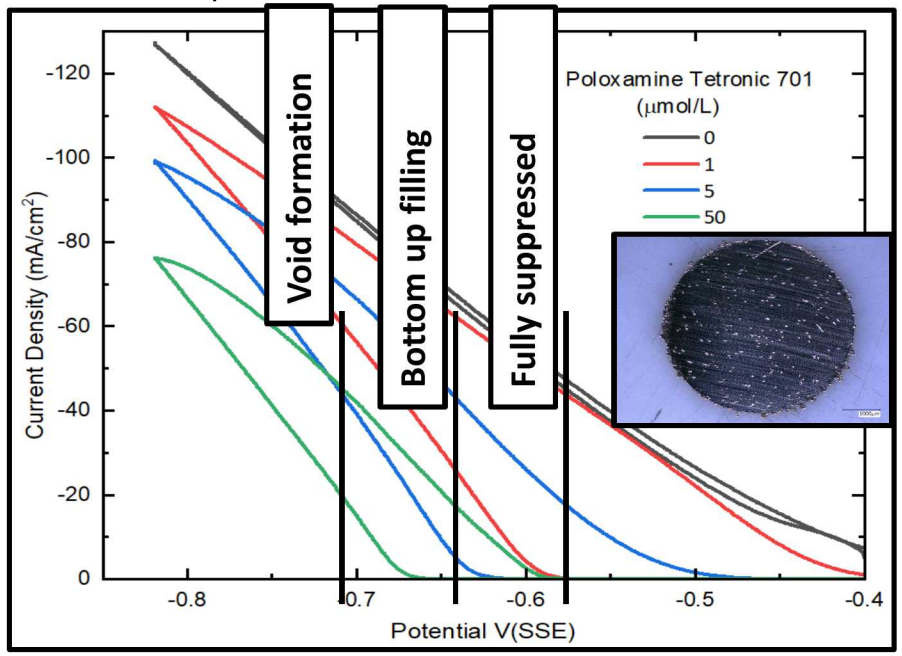
At a given suppressor concentration increasing applied potential pushes deposition down the TSV



1. Journal of the Electrochemical Society, 159 (4) D208-D216 (2012)
2. Journal of the Electrochemical Society, 159 (10) D570-D576 (2012)

Suppressor Breakdown in MSA Electrolyte

1.25 M $CuSO_4$, 0.25 M MSA, 1mM KCl



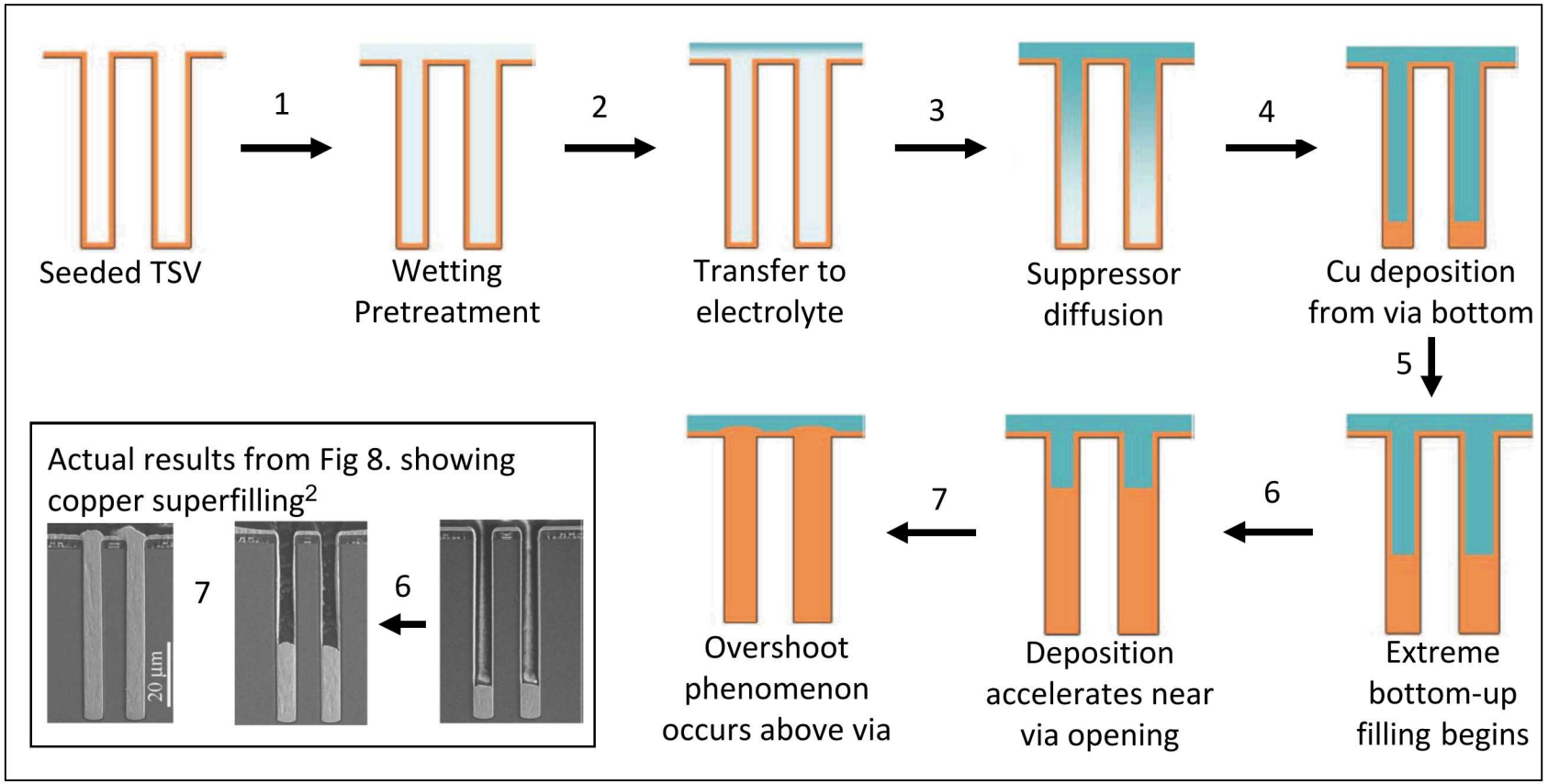
Superfilled Bottom Up Plating

- Void free filling
- Reasonable deposition times
- Complex balance b/t applied bias and electrolyte composition
- Geometry dependent plating conditions

Theory: Bottom Up Fill

S-Shaped Negative Differential Resistance (S-NDR) Approach[10]

- Single suppressor additive system
- Bottom-up growth mode even with conformal seed metal

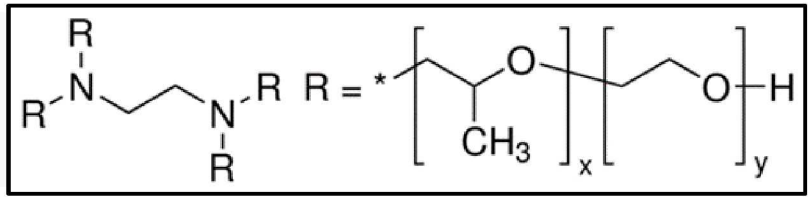


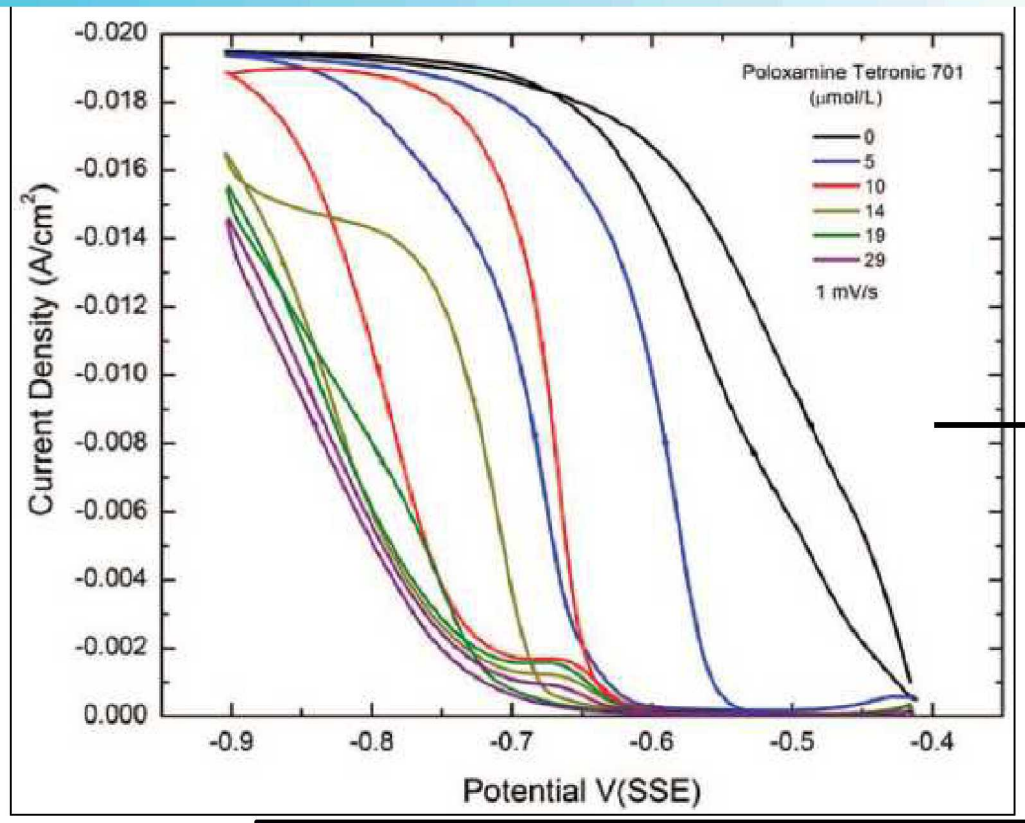
[10] Moffat, T. P., and D. Josell. "Extreme bottom-up superfilling of through-silicon-vias by damascene processing: suppressor disruption, positive feedback and turing patterns." *Journal of The Electrochemical Society* 159.4 (2012): D208-D216.

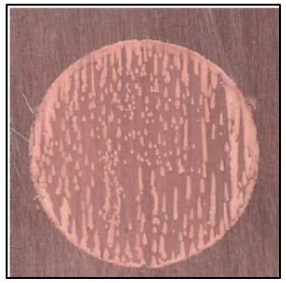
Characteristics of an Electrolyte Capable of Achieving a Bottom-Up Void Free Fill

- **Suppressor organics lead to hysteresis in CV curve**
- **Chemistries that exhibit this hysteresis cause 'Turing Patterns' on planar electrodes**

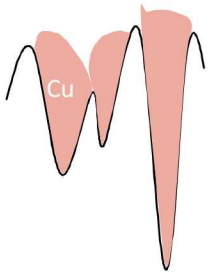
Tetronic 701



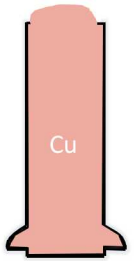


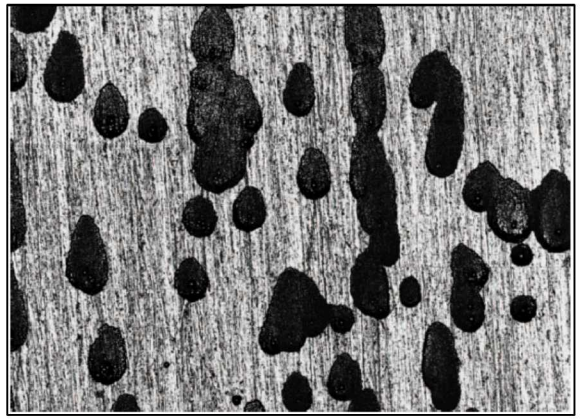


Abrasions



TSVs



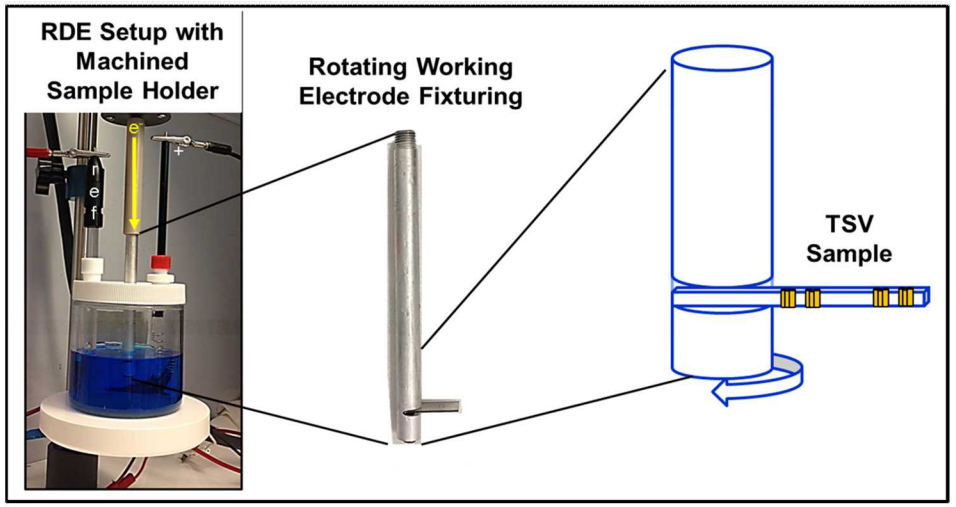


Presence of hysteresis and turing patterns is indicative of a chemistry capable of achieving a bottom up filled void free TSV

[10] Moffat, T. P., and D. Josell. *Journal of The Electrochemical Society* 159.4 (2012): D208-D216.
[11] Josell, D., D. Wheeler, and T. P. Moffat. *Journal of The Electrochemical Society* 159.10 (2012): D570-D576.
[12] Wheeler, D., T. P. Moffat, and D. Josell. *Journal of The Electrochemical Society* 160.12 (2013): D3260-D3265.

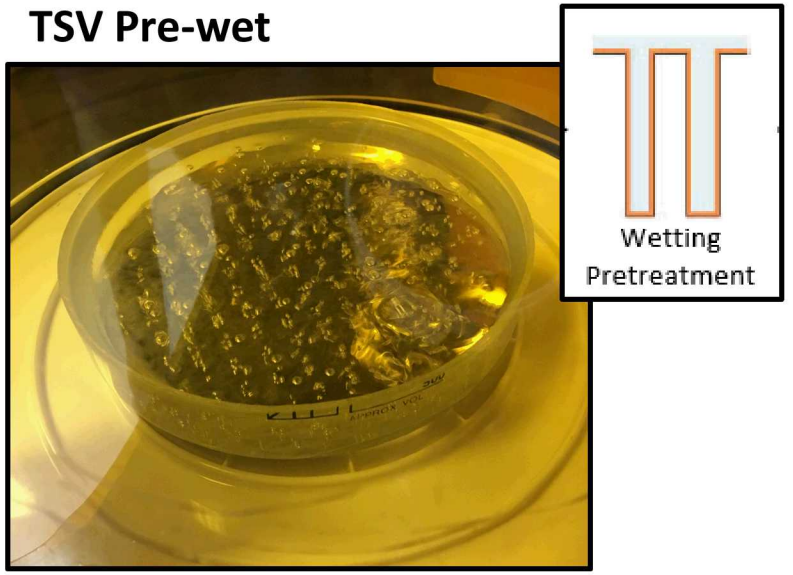
TSV Filling Experiments

Experimental Apparatus



- Hg/Hg_2SO_4 reference electrode
- Pt anode
- Al sample holder with rotating disk electrode (RDE) to control rpm
- Sample RPM can be correlated to fluid flow and solution replenishment within the TSVs

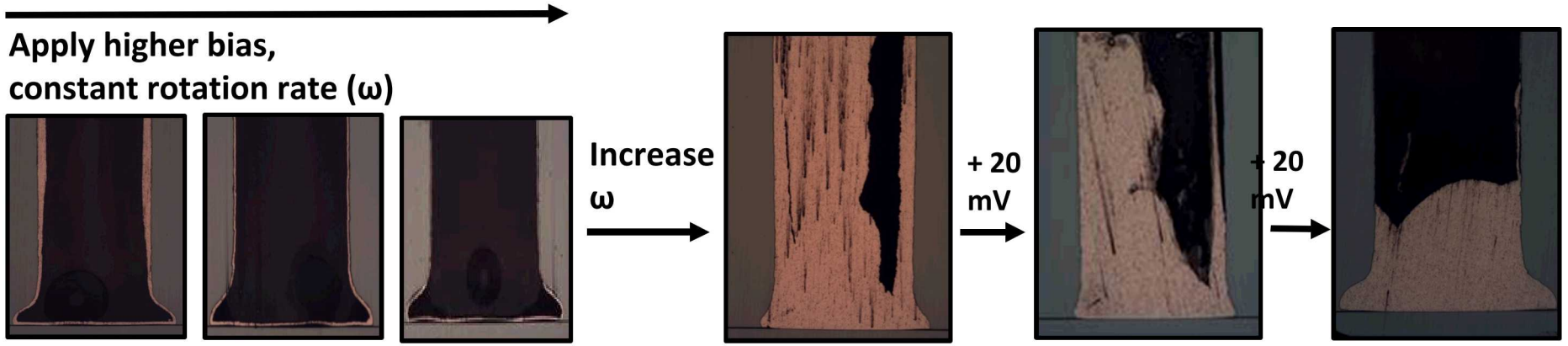
TSV Pre-wet



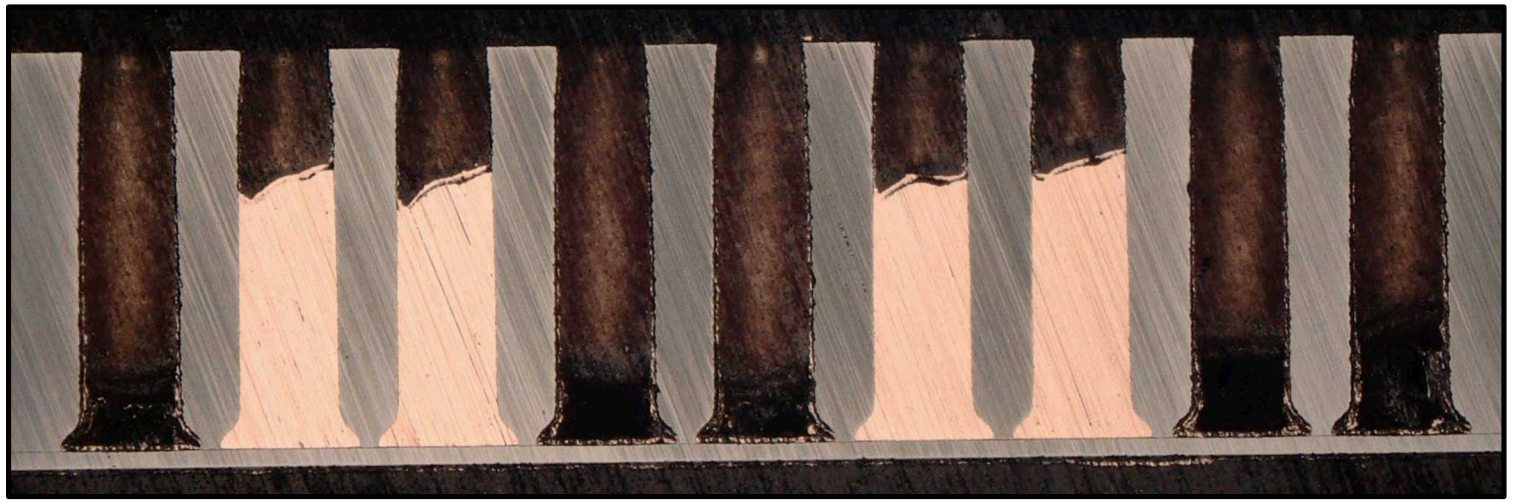
- TSV samples submersed in cooled IPA
- Rough pump vacuum chamber to evacuate all air from the TSVs
- TSV sample remains submersed in IPA until transferred directly to the plating electrolyte

Adapting Plating Conditions for Mesoscale TSVs

Applied potential, electrolyte fluid flow, and suppressor concentration effect filling

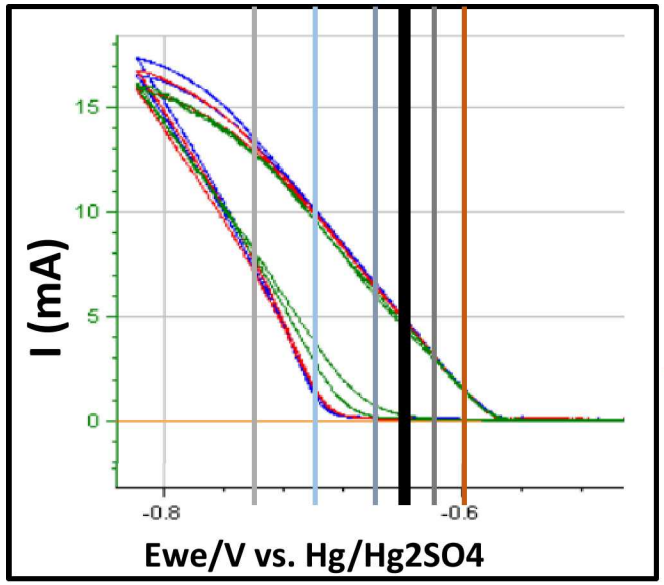


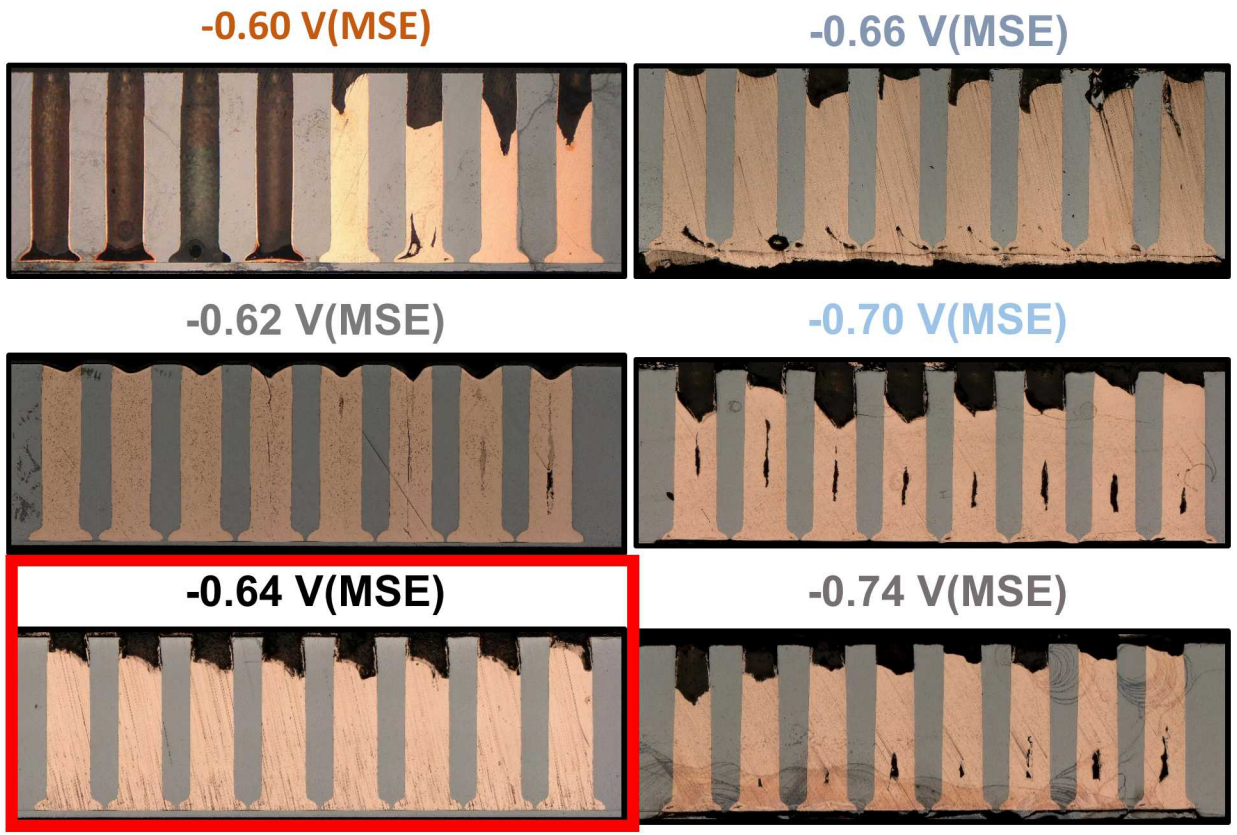
400 rpm, -0.6 V vs RE, 50 µM Suppressor, 1.25 M $CuSO_4$, 0.25 M MSA



Phase 1: Potentiostatic TSV Filling

- **Reference electrode use to finely tune applied potential**
- **Filling results are highly sensitive to applied voltage**
- **~20mV window to obtain void free filling**

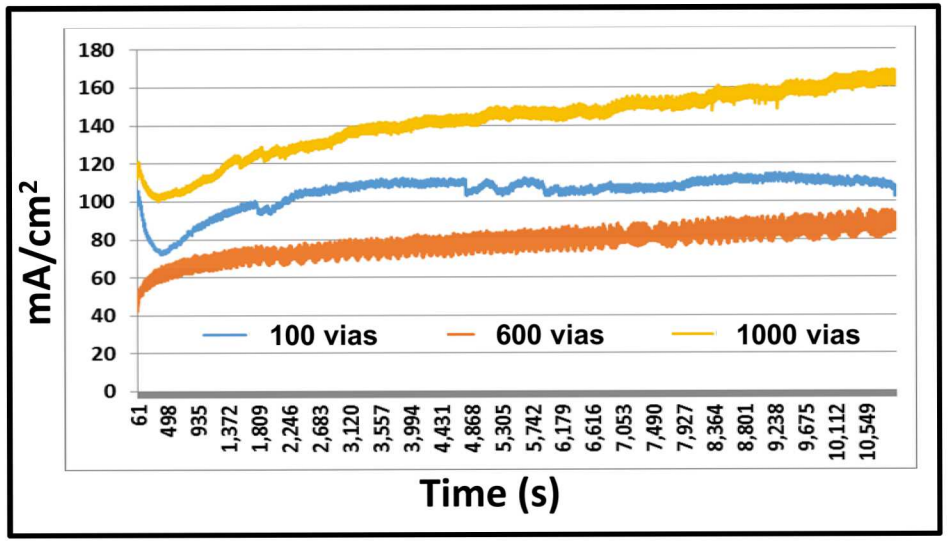




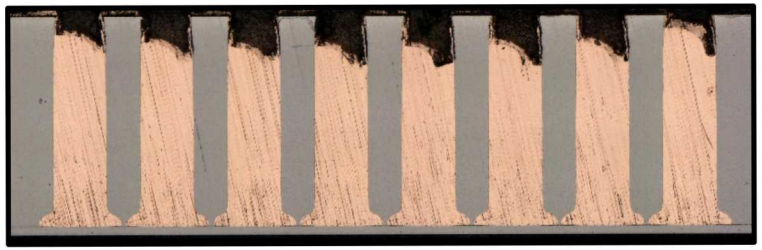
Determining a Range of Current Densities to Investigate

-0.64 V(SSE), 400 rpm, 50 µM TET701

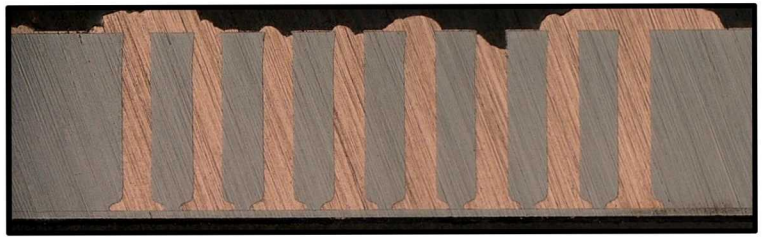
Chronoamperometry on TSV samples with Varying Area



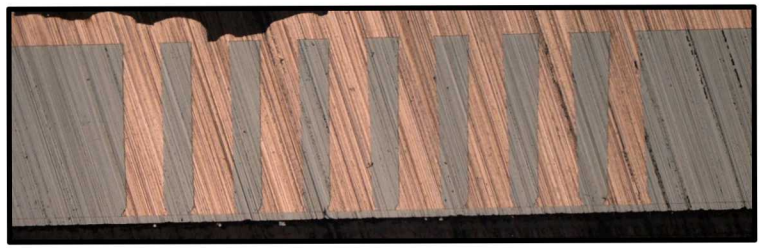
100 vias



600 vias

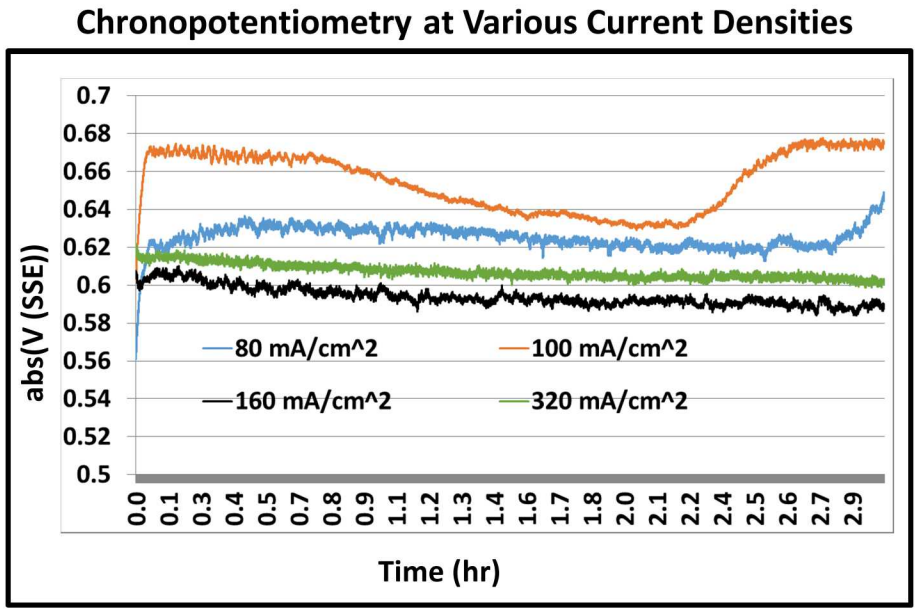


1000 vias



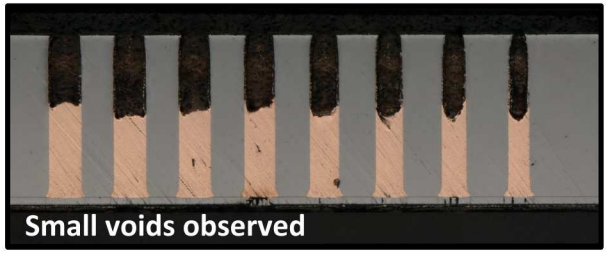
- **Resultant current does not scale consistently with increasing area**
- **Data used to establish a range of current densities to investigate**

Galvanostatic TSV Filling

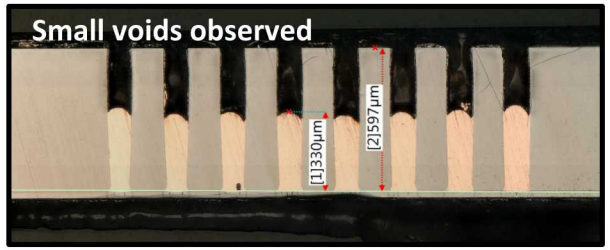


- Potential varies to accommodate applied current
- Electroactive vs total conducting surface
- Voltage does not scale consistently with increased current
- Galvanostatic plating dynamically adjusts for changes in suppressor breakdown

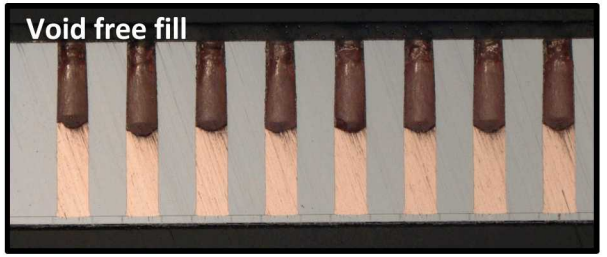
80 mA/cm^2 (TSV area)
0.55 mA/cm^2 (tot. conducting surface)



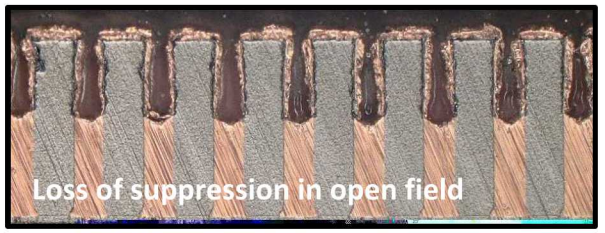
100 mA/cm^2 (TSV area)
1.38 mA/cm2 (tot. conducting surface)



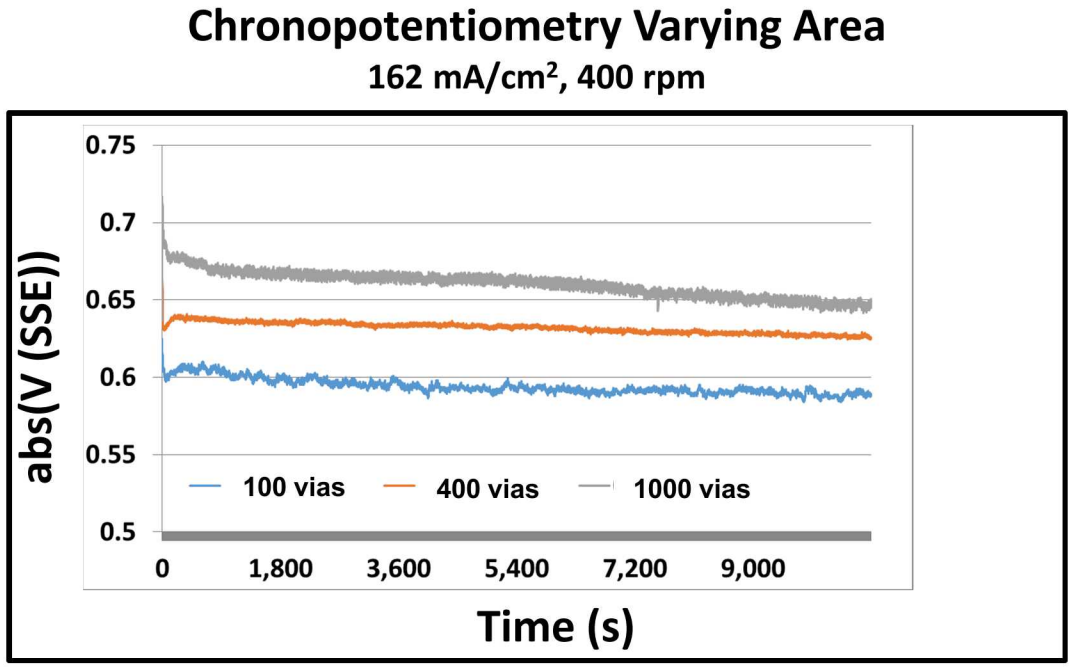
160 mA/cm^2 (TSV area)
2.22 mA/cm2 (tot. conducting surface)



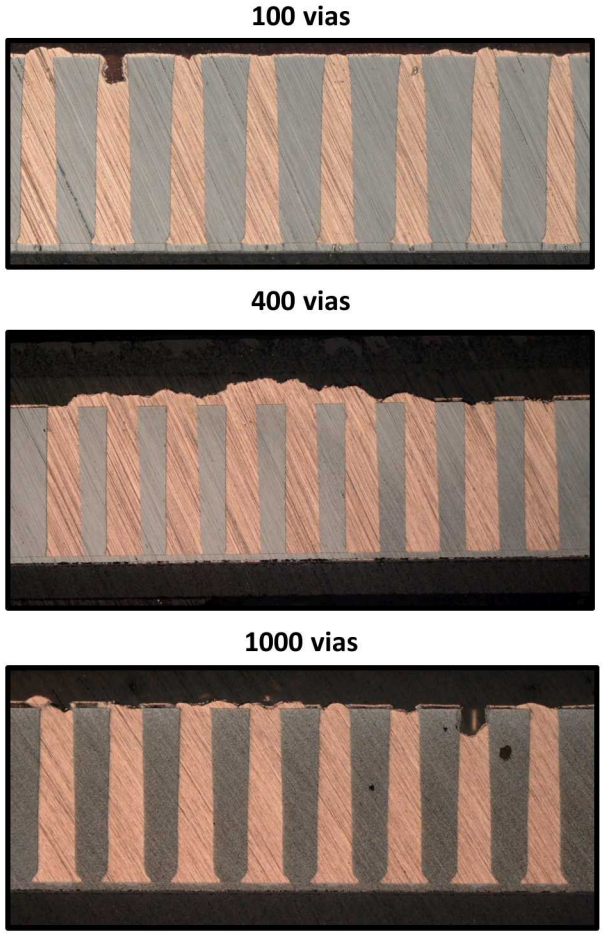
320 mA/cm^2 (TSV area)
4.44 mA/cm^2 (tot. conducting surface)



Scaling Current Controlled Deposition

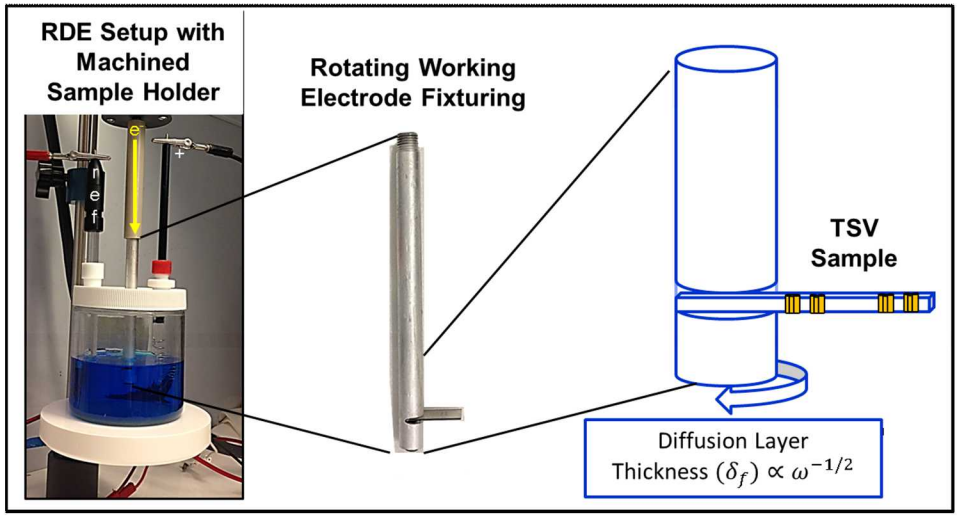


- Void free galvanostatic filling in a variety of sample sizes demonstrated
- Ongoing work focused on scaling this from die level filling to full wafer TSV filling



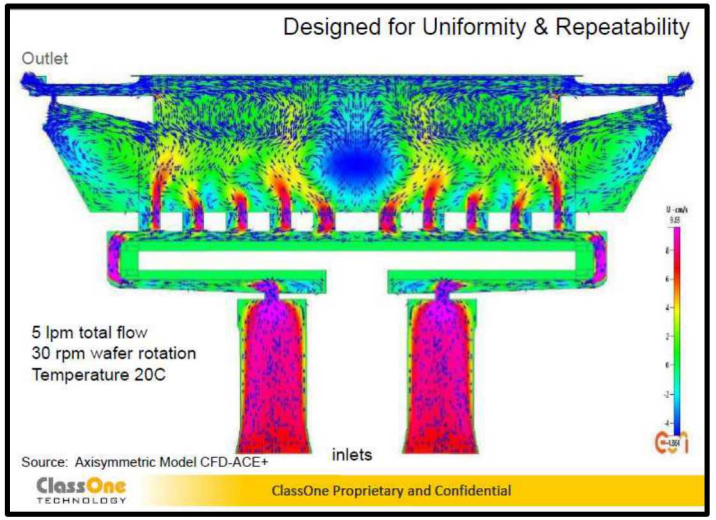
Full Wafer TSV Filling

Die Level Fluid Dynamics Control



- **Sample rotated in stagnant solution**
- **Change in RPM changes fluid replenishment in the TSVs**

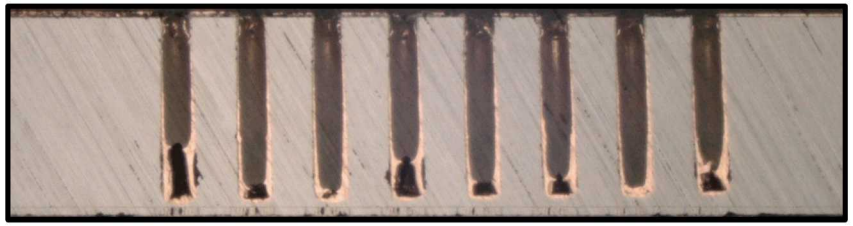
Production Tool Fluid Dynamics Control



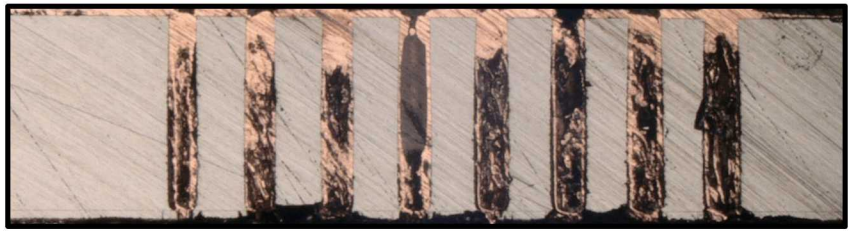
- **Full wafer rotation**
- **Fountain style solution replenishment**
- **Baffled showerhead for controlling uniformity**

Solution Replenishment Modeling

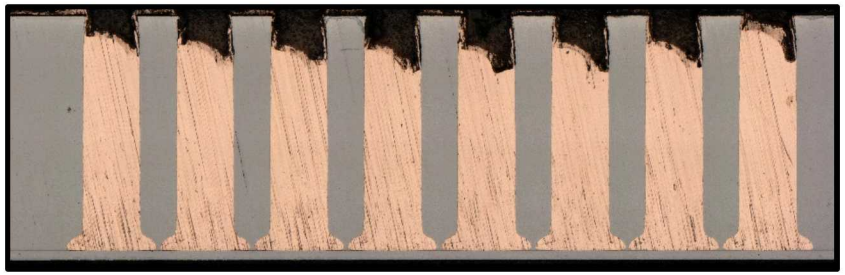
50 RPM



200 RPM

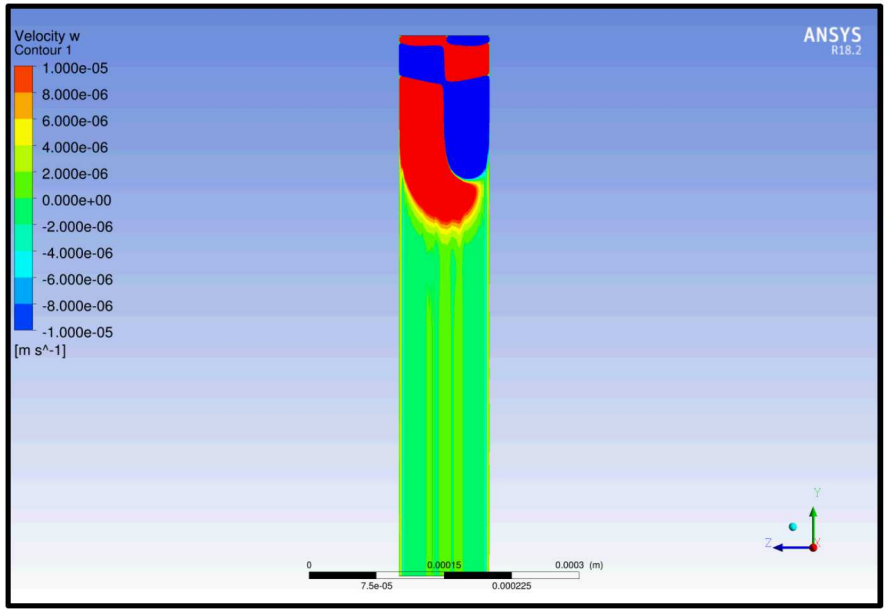


400 RPM



Solution replenishment across a 150 mm is radially dependent on the position of the vias

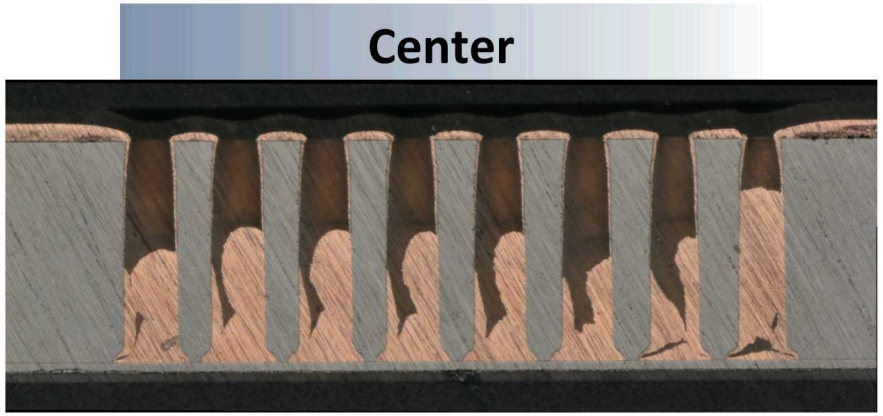
400 RPM CFD Model

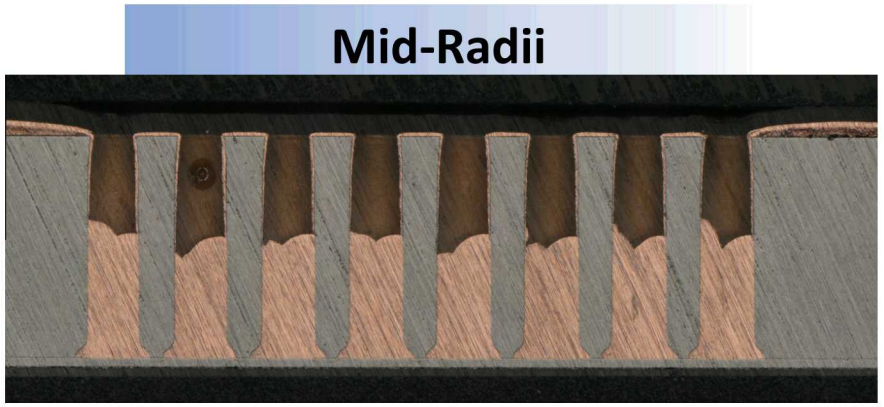


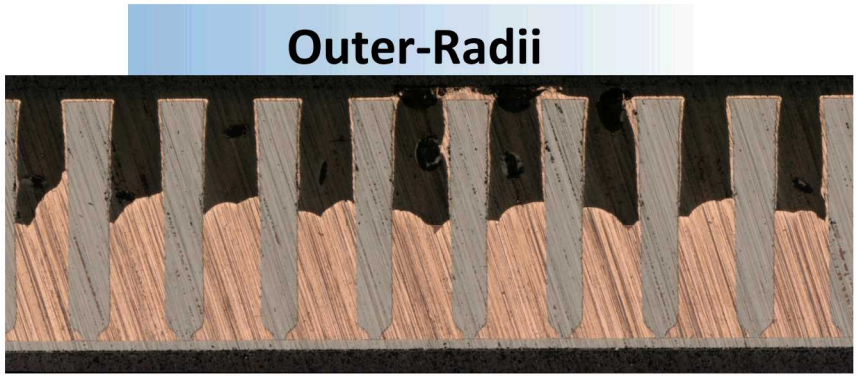
- **Ansys fluid dynamics modelling**
- **There is almost no flow about halfway down the channel.**
- **Asymmetry noticed during filling experiments**

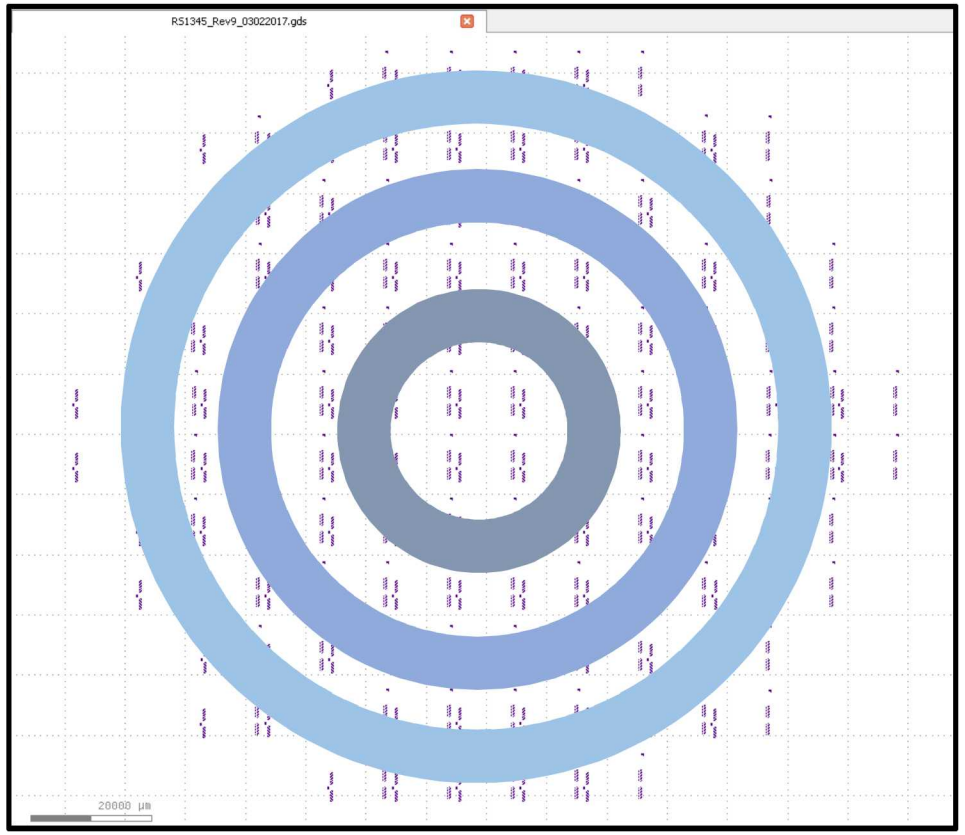
Filling result are highly dependent on fluid dynamics and solution replensihment

Increased Current Density: Void free filling







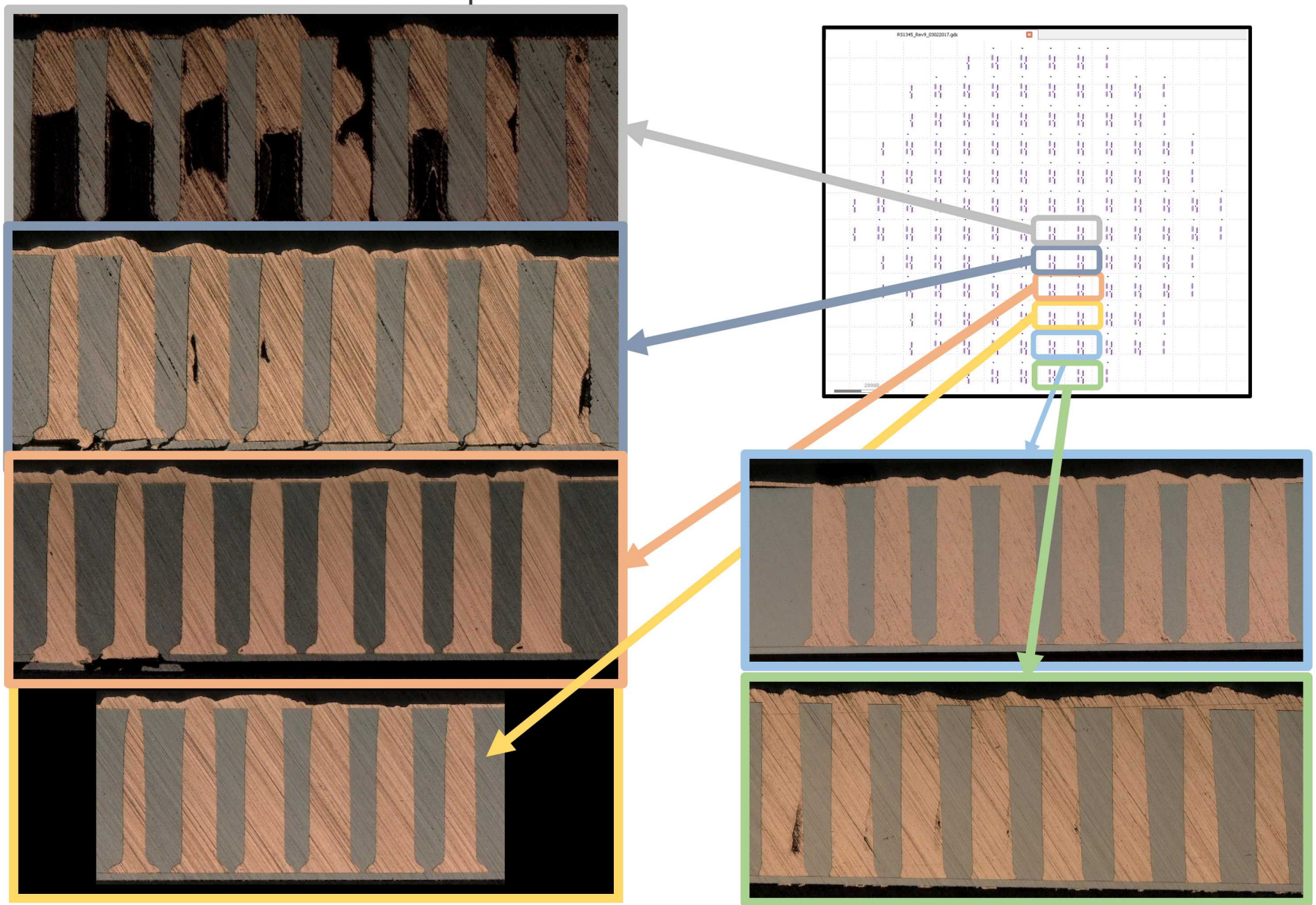


Void free filling except center wafer

Investigating :

- **Fluid flow**
- **Center current density**

Full Thickness Deposition Across150 mm Wafer

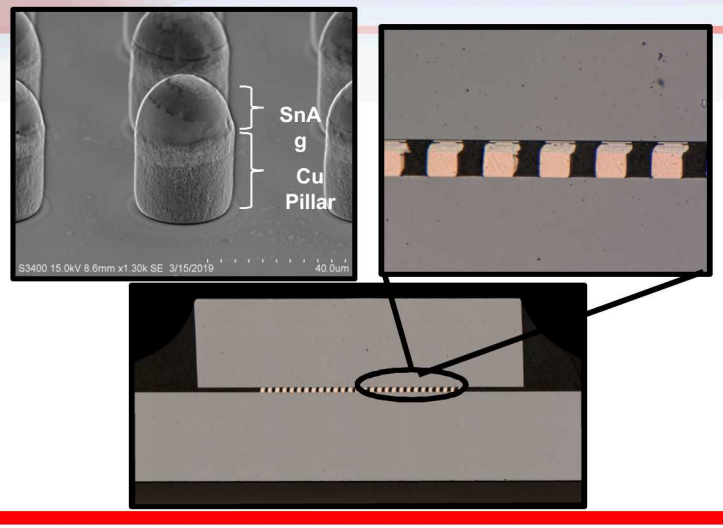


Ongoing and Future Work

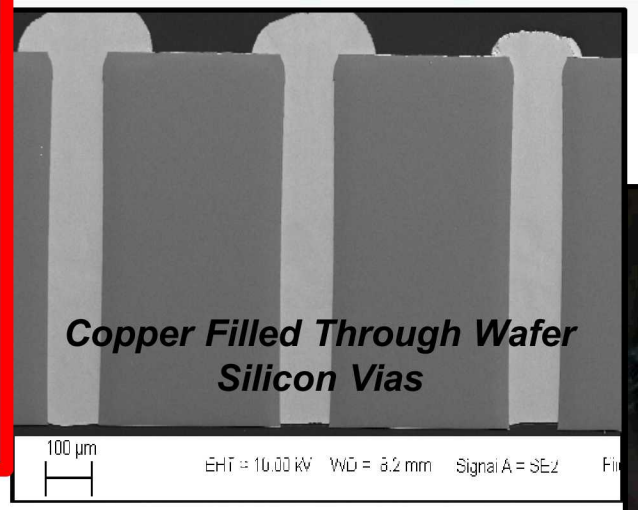
1. **Derive current controlled plating regime**
2. **Perform scaling experiments towards full wafer plating**
3. **Investigate different diameter TSVs**
4. **Post plating integration**
   - **CMP development**
   - **Cu Pumping**
   - **Flip chip bonding**
5. **Chemistry lifetime experiments**
   - **Suppressor precipitation onto Cu anode**
   - **Suppressor depletion vs A-min**

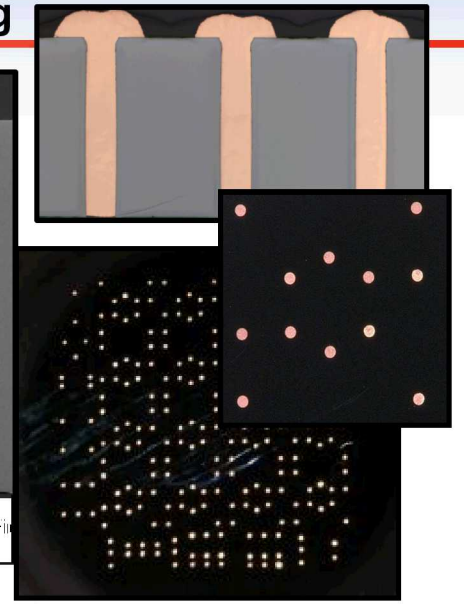
Mesoscale Fabrication
Filling, Forming, and Coating

Cu Pillar µ-Bumps

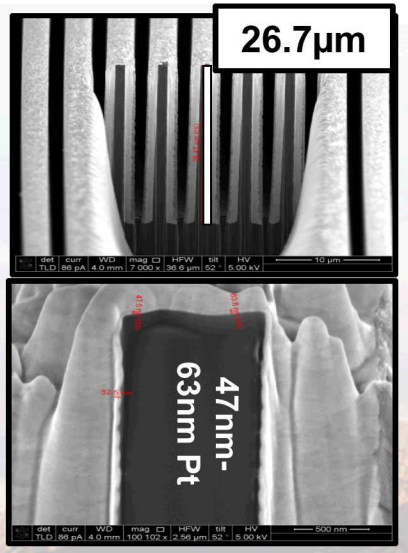


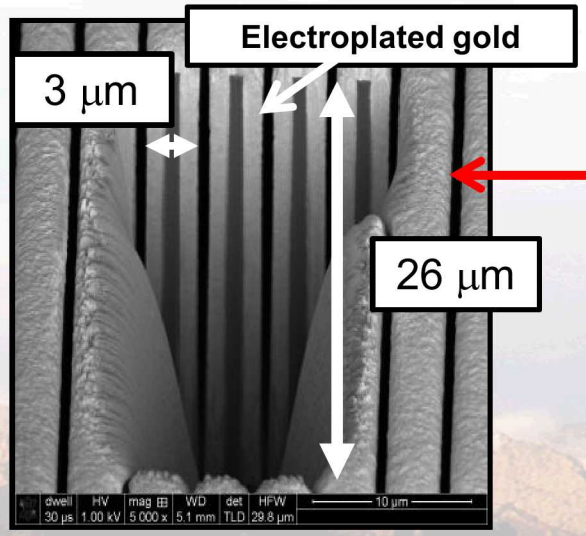
Through Full Substrate Via Filling



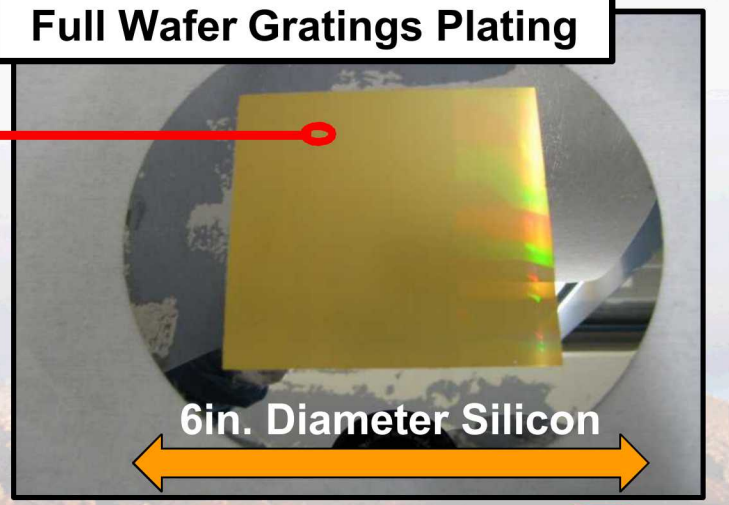


Precision Electro-coating





Full Wafer Gratings Plating

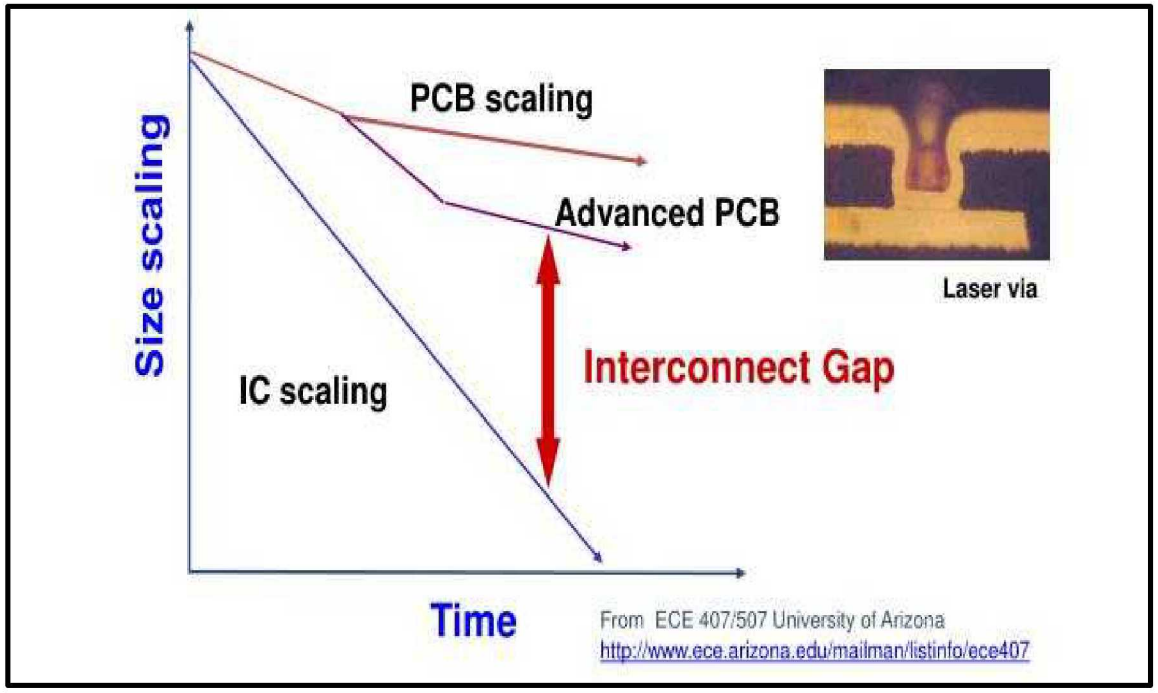


Sandia National Laboratories

More than Moore Advanced Integration Needed

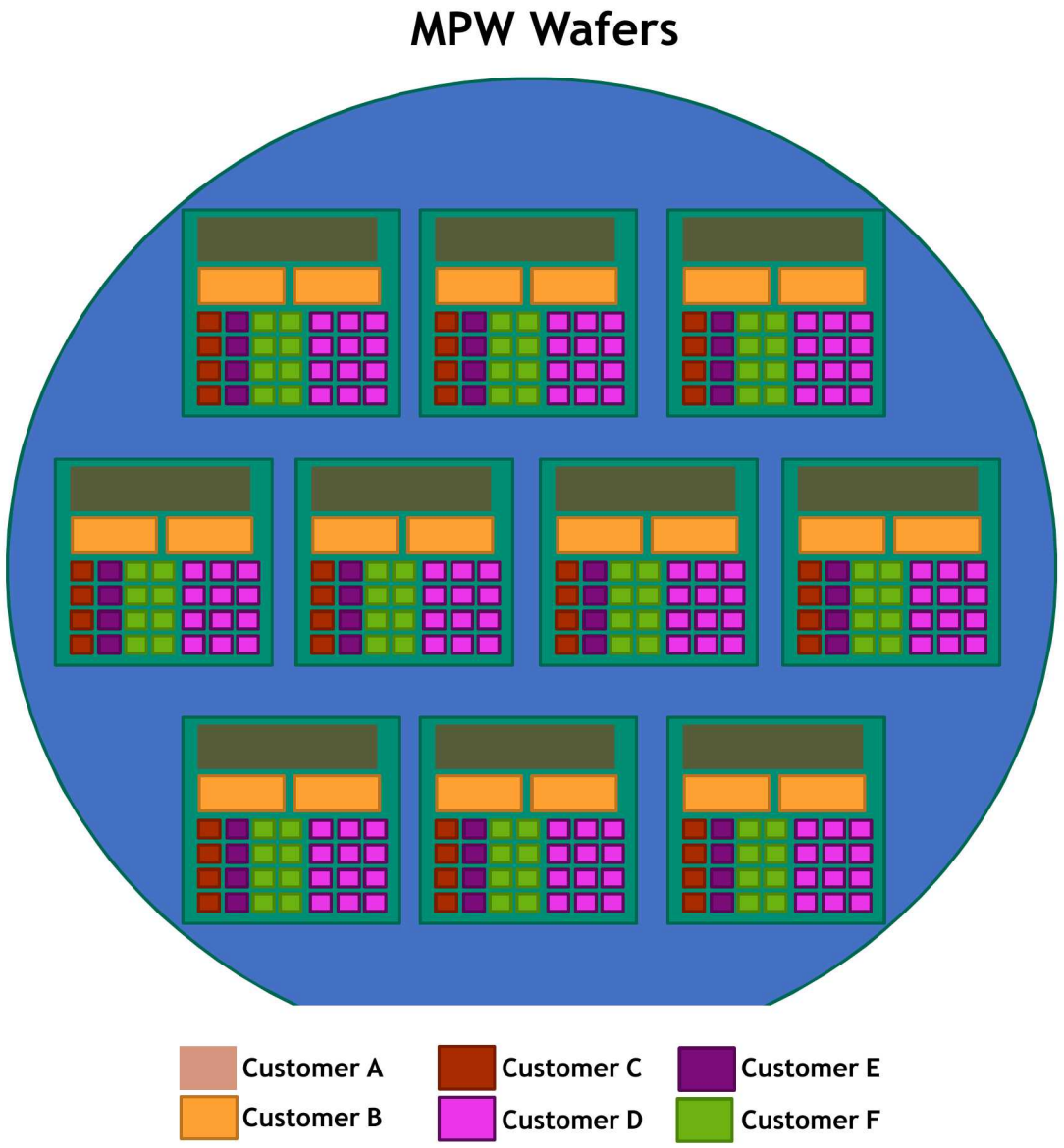
The Interconnection Gap

Improvement in density of standard interconnects and packaging technologies is much slower than IC Trends

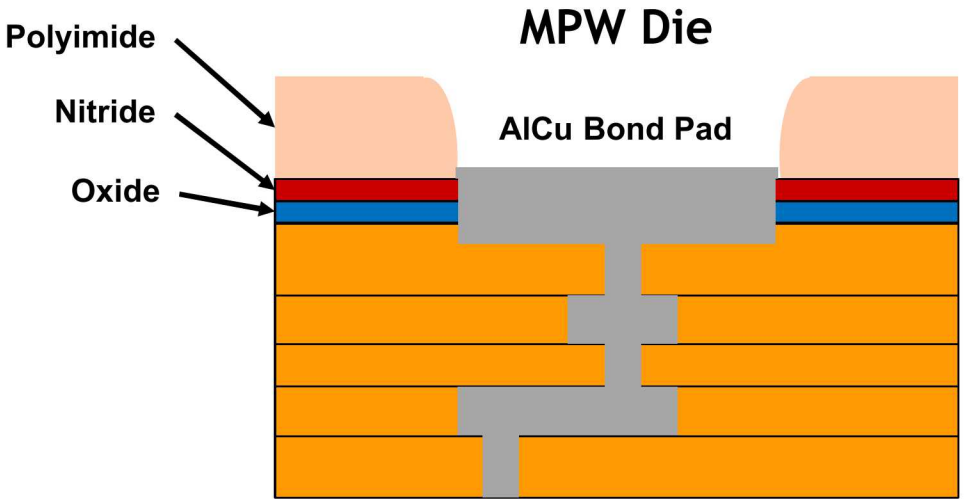


- **Need fine pitch bumping**
  - Increase I/O per chip
  - Reduce parasitics for RF applications
  - Pseudo-lithic integration (e.g. CHIPS)
- **Particularly challenging for USGov applications**
  - Smaller part counts (Foundries and OSATs un-interested)
- **Each new program initiates its own integration development**
  - R&D and rapid prototyping
  - Heterogeneous integration of boutique technologies
- **Need an integration platform with flexible post-fab processing steps for fine pitch interconnects with MPW die**

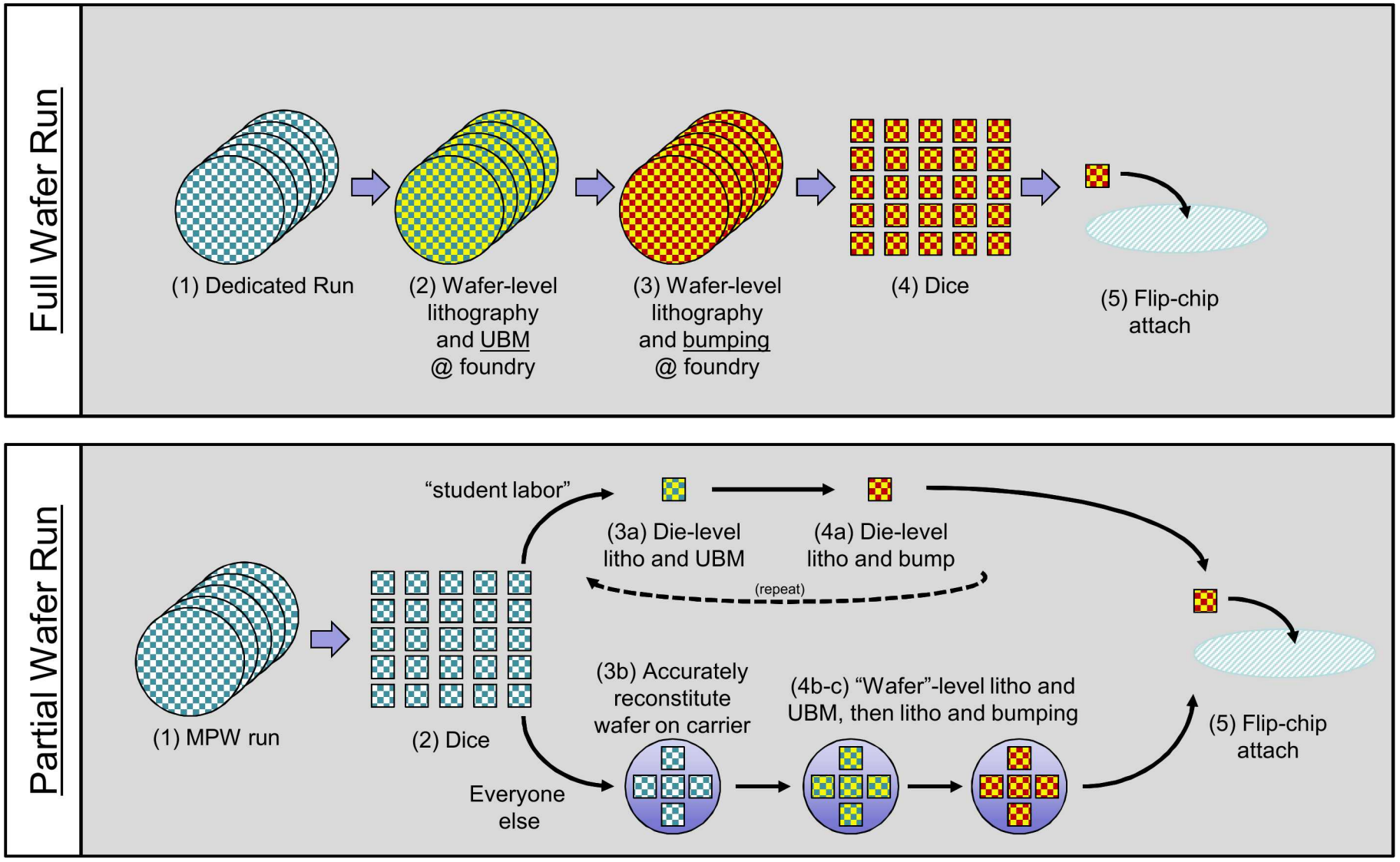
Multi-Project Wafers: a "Solution" to Low Volume



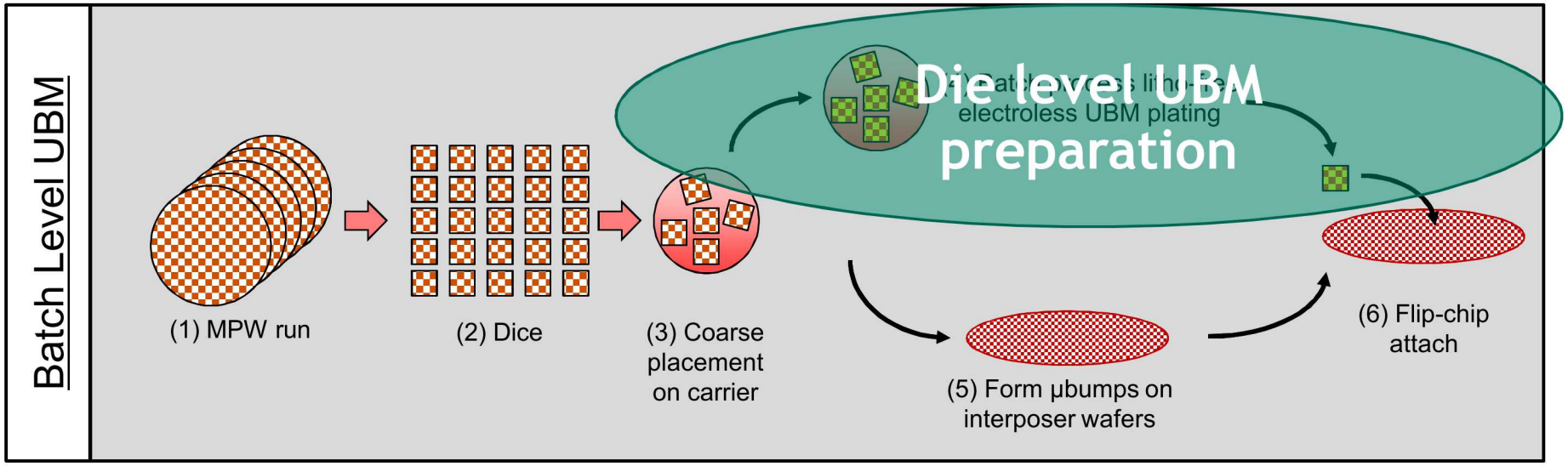
- Costs of a run are distributed across many different customers (10s-100s k$)
- Access to high performance technology nodes
- Must follow strict process flow and design rules making flip chip bonding challenging



Challenges with MPW Die: Foundry CMOS + Advanced 2.5D



Proposed Solution: Lithography Free Batch Level Processing



Benefits:

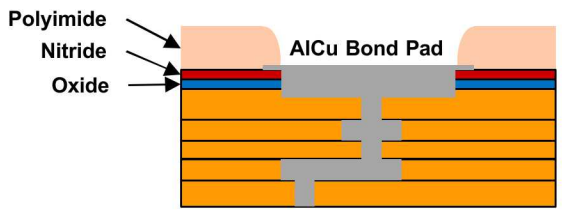
- Massive cost savings through MPW runs
- Lithography "free"
- Batch process with no fine alignment
- Wafer-level interposer bumping at legacy fab

What you'll see today:

- Proposed process
- Batch-level UBM preparation for singulated die
- Two flip chip approaches and µ-bump development

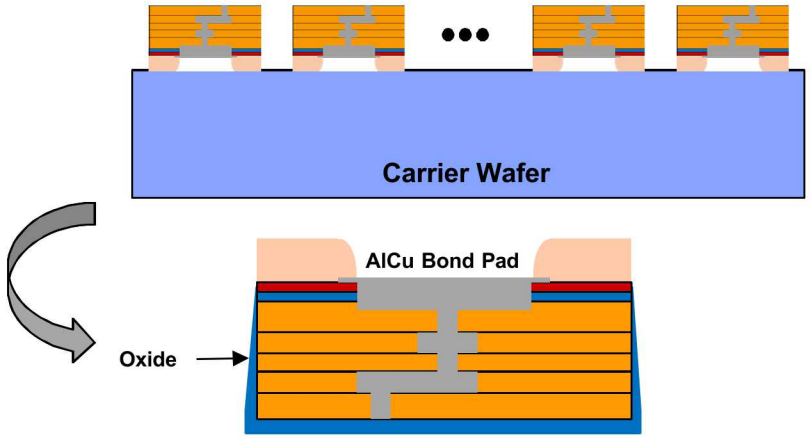
Batched ENIG/ENEPIG Deposition on Singulated Die

1. As received MPW die with AlCu bond pads



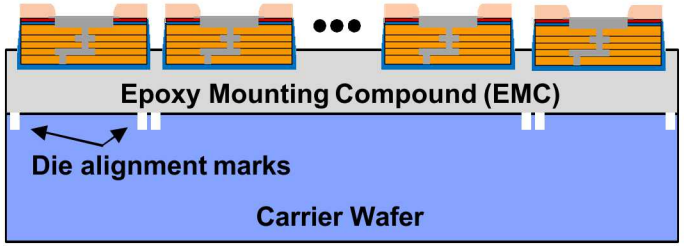
Exposed Si disrupts ENIG/ENEPIG electroless deposition and must be passivated

2. Flip die upside down onto carrier wafer and deposit 1 µm CVD TEOS to passivate exposed Si

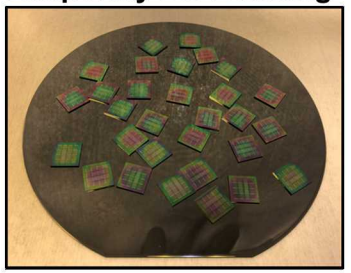


- 10% thickness coverage on sidewall
- No temporary bonding media necessary
- Potentially compatible with non-Si technologies (e.g. AlGaN, GaN, GaAs)

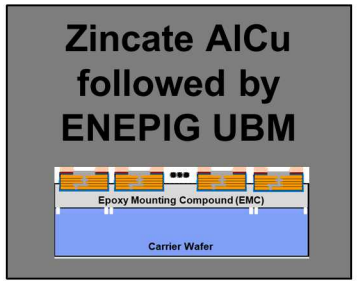
3. A temporary epoxy mounting compound (EMC) used for batch level under bump metallurgy (UBM) deposition



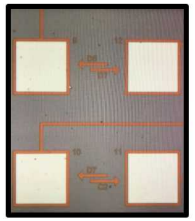
Temporary Die Bonding



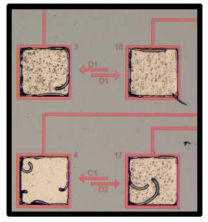
4. Electroless UBM deposition.
ENEPIG = electroless Ni, electroless Pd, immersion Au.



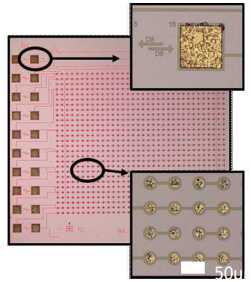
AlCu Pads



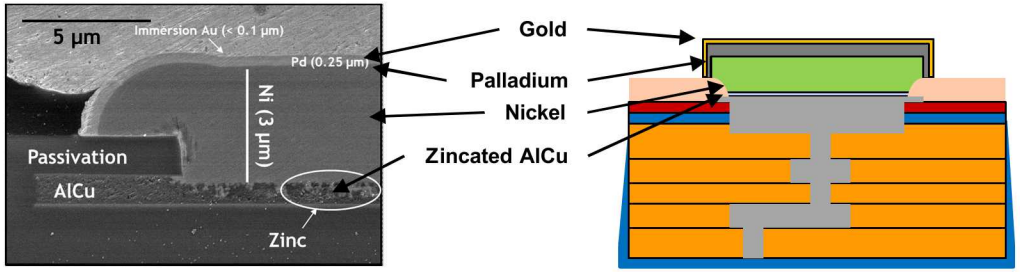
Zn + Ni



ENEPIG

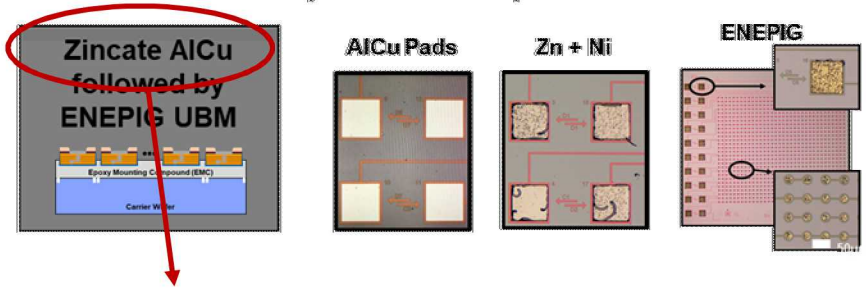


5. Solvent release die from EMC and die are ready for flip chip bonding

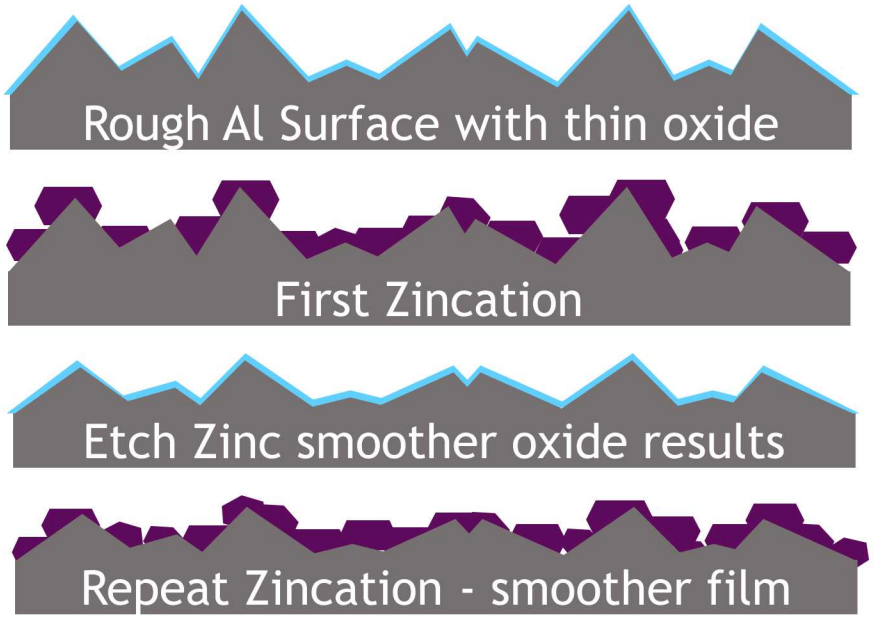


Zincation Process

4. Batch electroless UBM deposition.
ENEPIG = electroless Ni, electroless Pd, immersion Au.



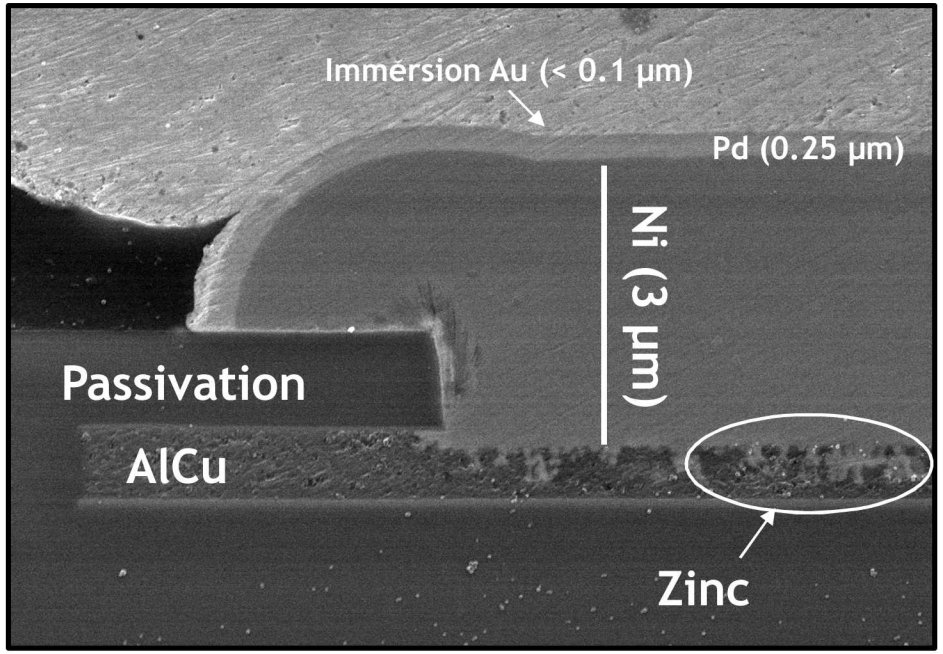
Enables adhesion of Ni (diffusion barrier) to AlCu



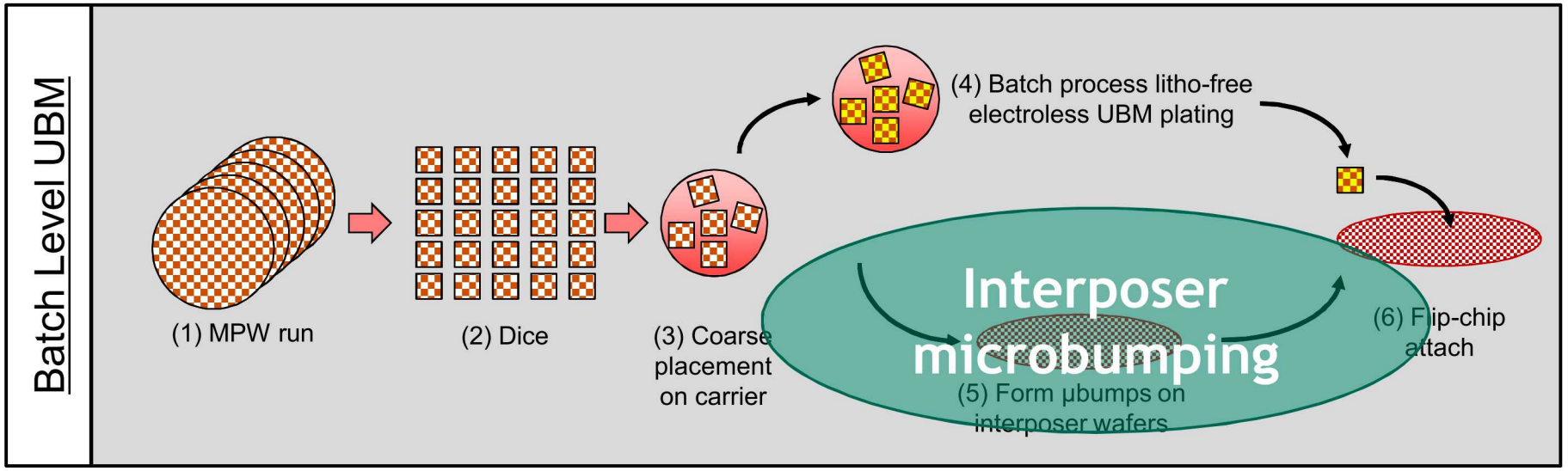
Process

- Zinc complexes exchange in solution with Aluminum resulting in Zn deposition and Al etching
- Grow zinc crystallites for 30-60 seconds
- Quickly dissolve zinc in HNO_3 and repeat

ENEPIG UBM



Proposed Solution: Lithography Free Batch Level Processing



Benefits:

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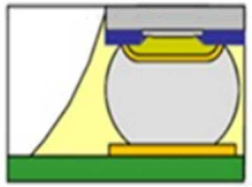
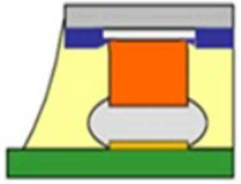
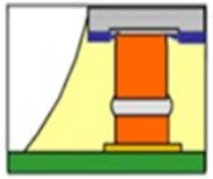
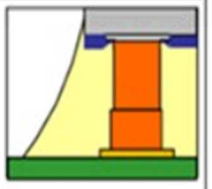
- Lithography "free"
- Batch process with no fine alignment
- Wafer-level interposer bumping @ legacy fab

What you'll see today:

- Proposed process
- Batch-level UBM preparation for singulated die
- Two flip chip approaches and µ-bump development

Micro-bumped Interposer Options

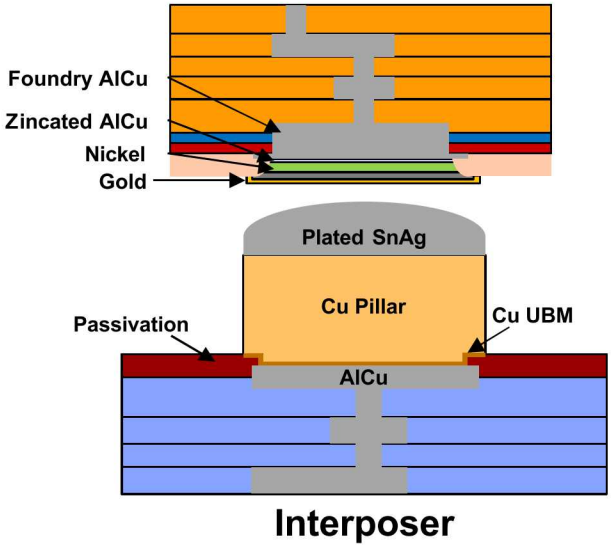
Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um

http://electroiq.com/insights-from-leading-edge/2014/09/iftle-208-ectc-part-3-thermal-compression-bonding-stats-toray-qualcomm/.
ECTC 2014

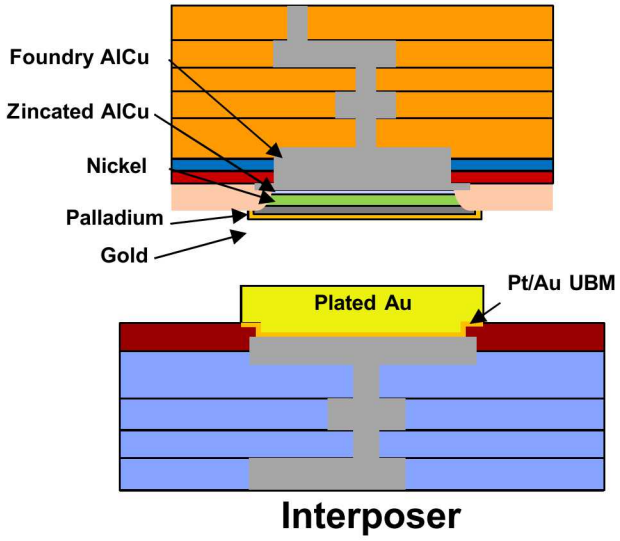
Microbump needs

- 55 - 10 µm targeted pitch
- Compatibility with single sided, asymmetric bumping approach

1. Cu Pillar Reflow Attachment



2. Au Thermocompression Bonding



1. Cu Pillar Reflow Attachment

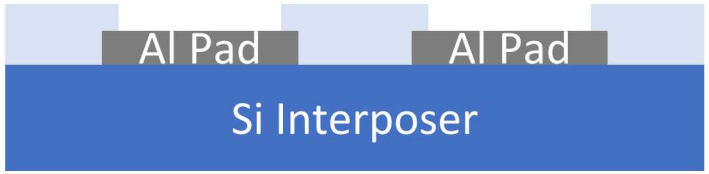
- Wide-spread industry adoption
- Bondline thickness determined by Cu Pillar
- SnAg T_{mp} = 220 C → temperature constraints (challenging integration with TSV processes)

2. Au Thermocompression Bonding (TCB)

- Non-reactive noble metal (long term reliability)
- High ductility (potential cryo/space compatibility)
- Au to ENEPIG TCB needs evaluation
- Potentially compatible with TSV thinning and TSV pad formation processes (high temp processes)

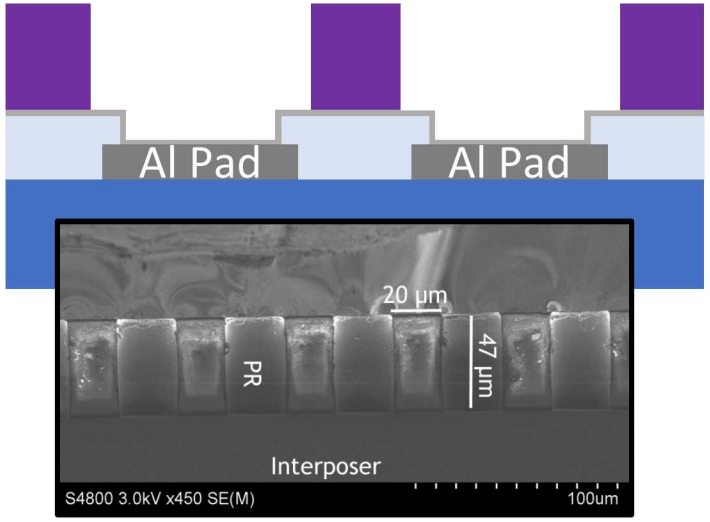
Interposer Microbump Fabrication

1. Multi-layer interposer fabricated in legacy fab

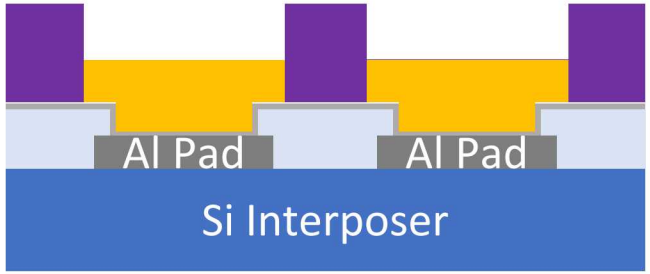


2. UBM and seed metal deposition

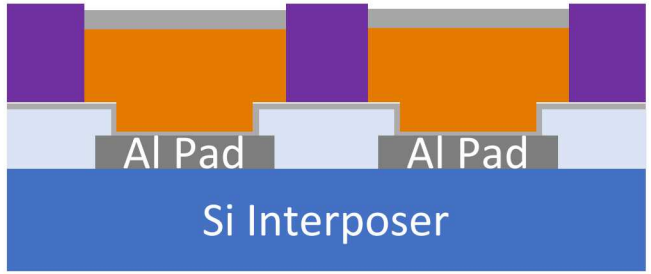
3. Bump lithography



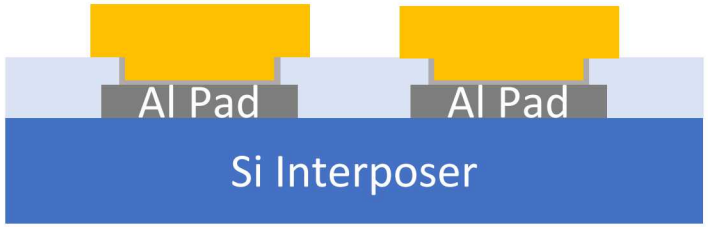
3a. Au Electrodeposition 10 µm height



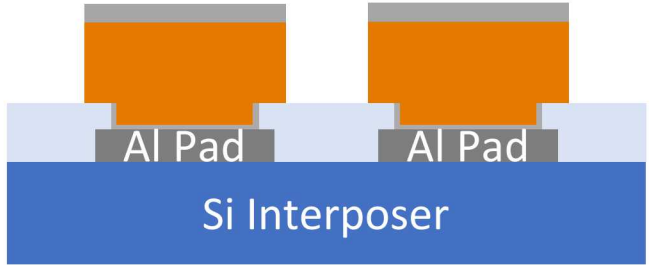
3b. Cu and SnAg plating, 40 µm height



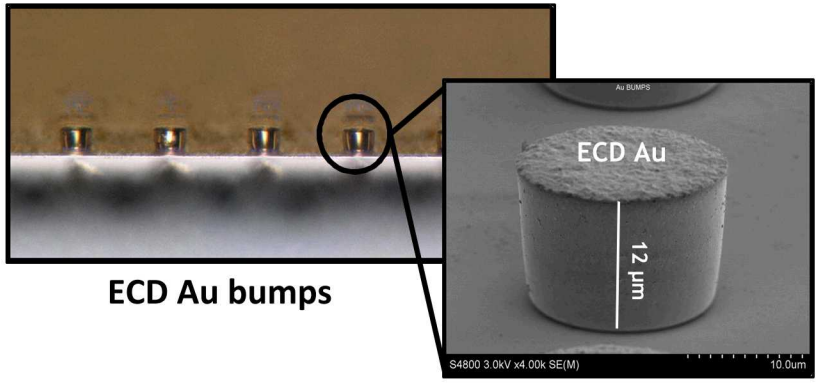
4. PR strip and seed metal etch



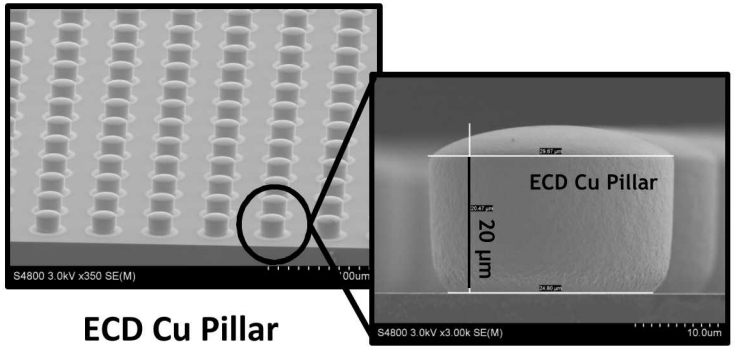
IBE seed metal etch of Ti/Au/Ti



Wet etch of Ti/Cu/Ti

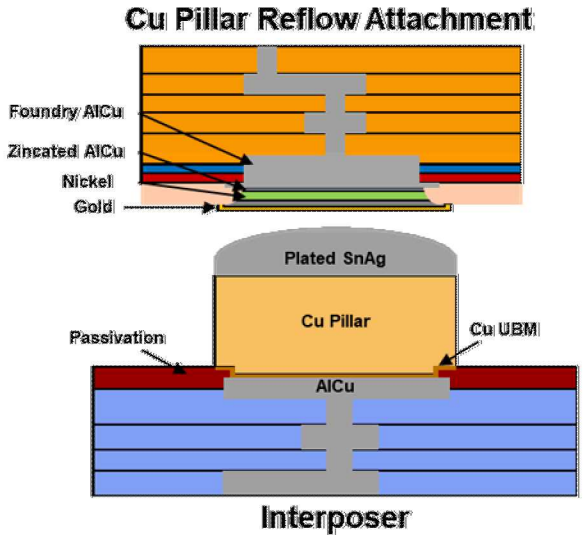


ECD Au bumps

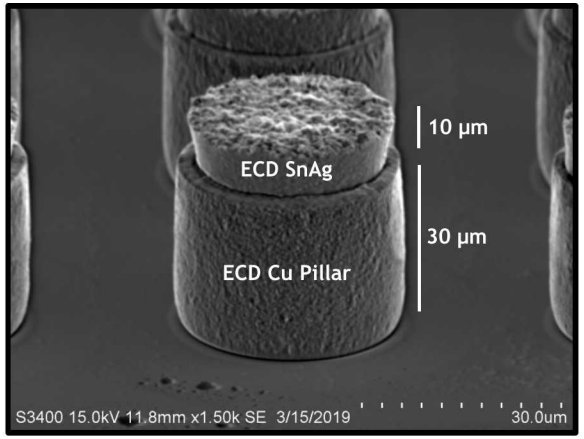


ECD Cu Pillar

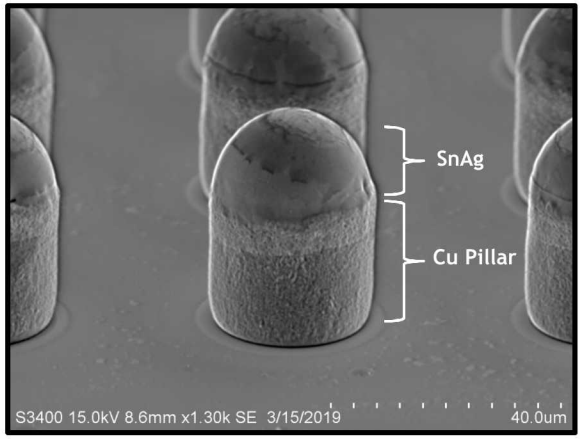
Cu Pillar Solder Reflow Bonding



SnAg Capped Cu Pillar

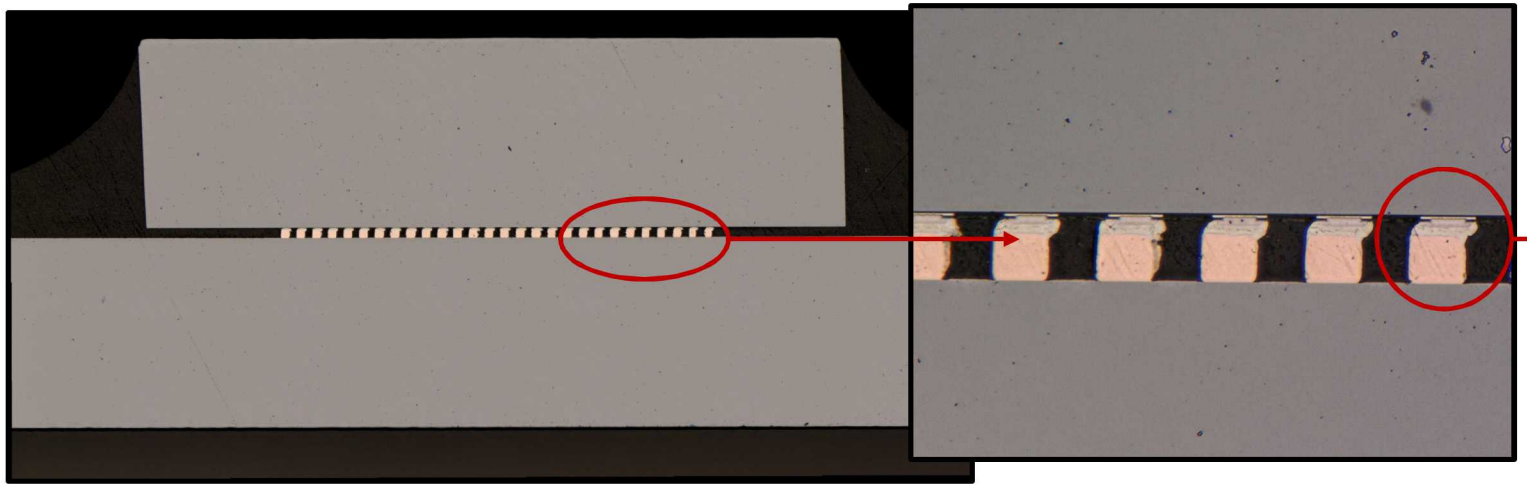


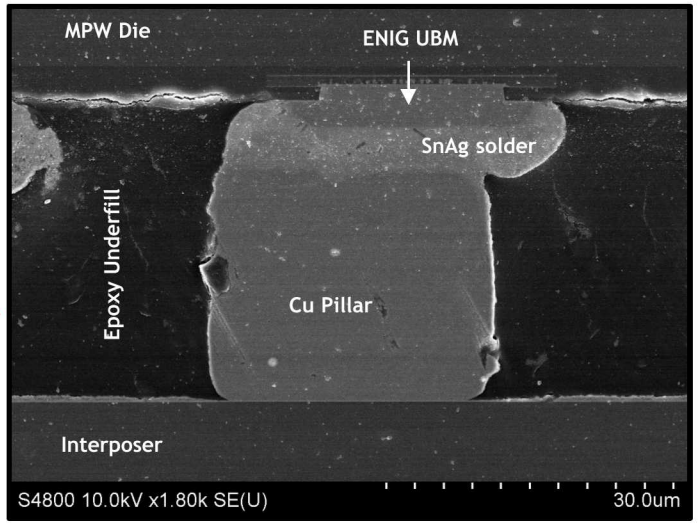
SnAg Reflow



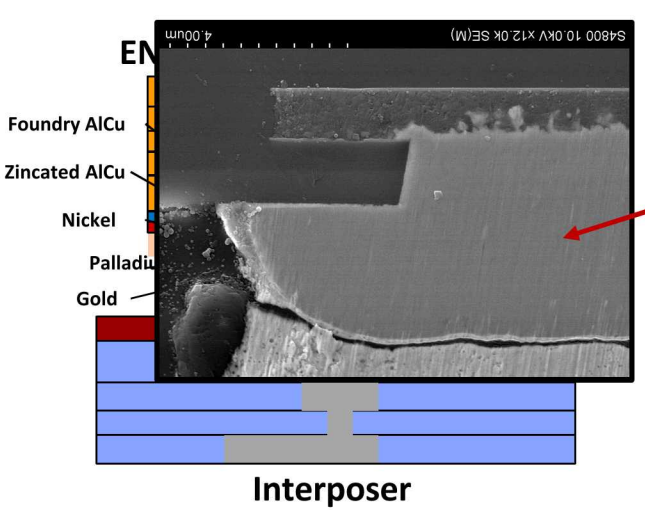
Bonded Pair: ENIG Coated Die to SnAg Capped Cu Pillar

Reflowed flip chip bond, 240C

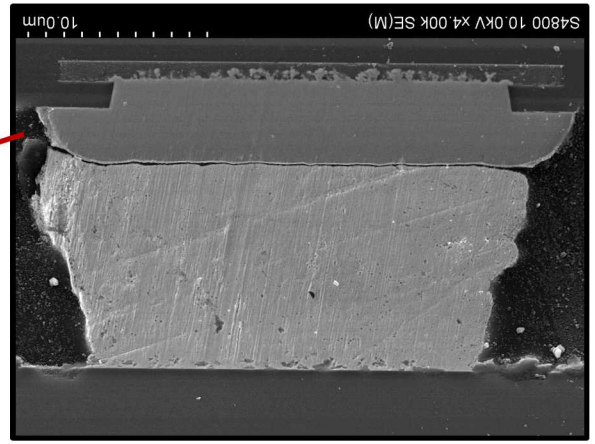




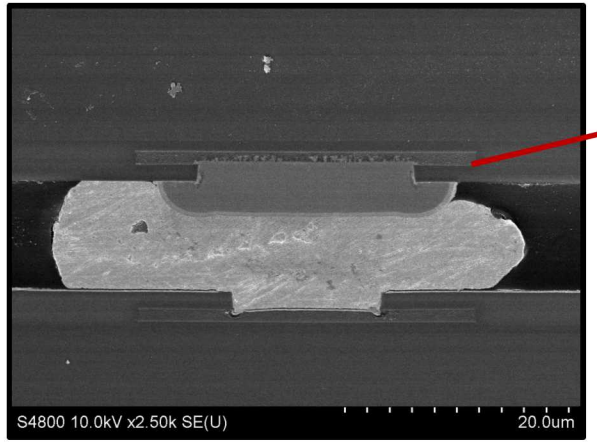
Au Thermocompression Bonding

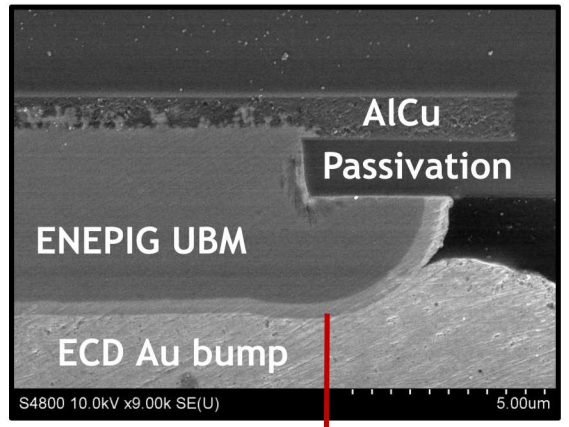


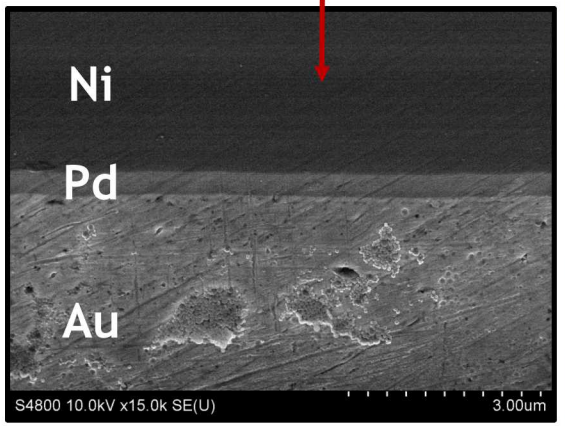
Au to ENIG -> Poor Bond



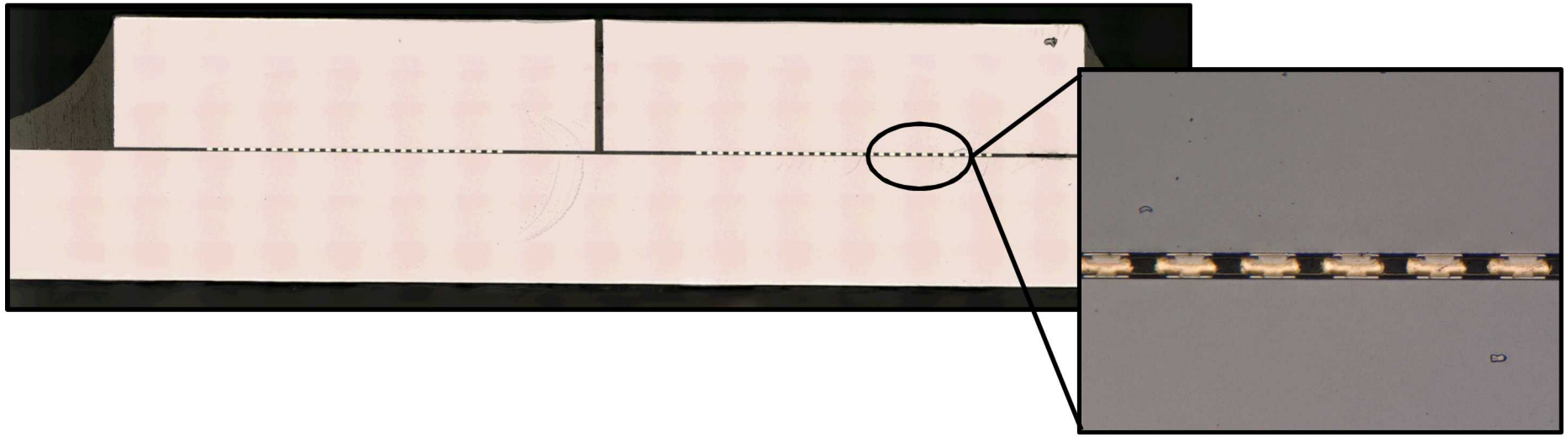
Au to ENEPIG -> Good Bond







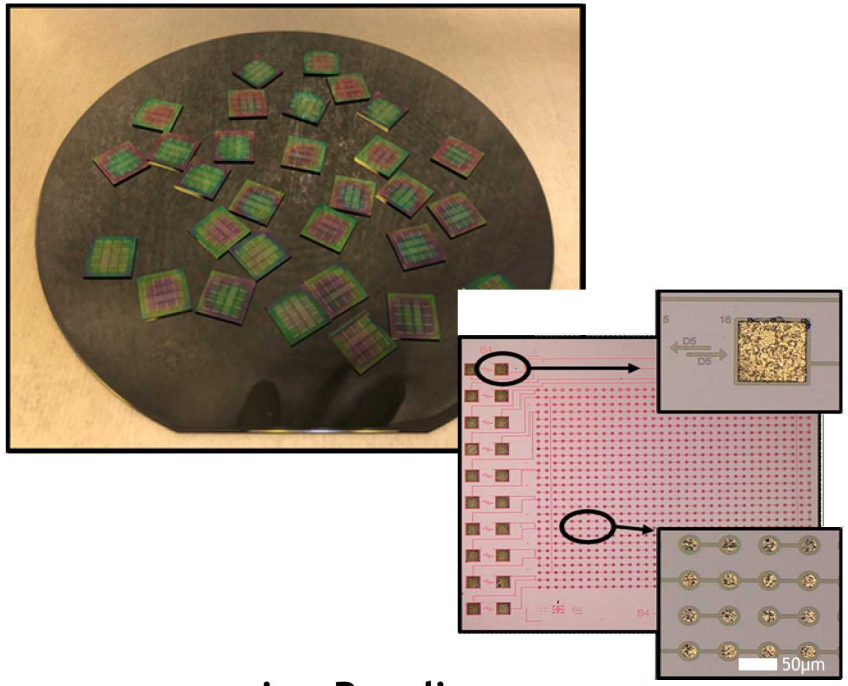
Multiple Chiplet Bonding (T = 250 C, F = 4 mg/μm², t = 20 minutes)



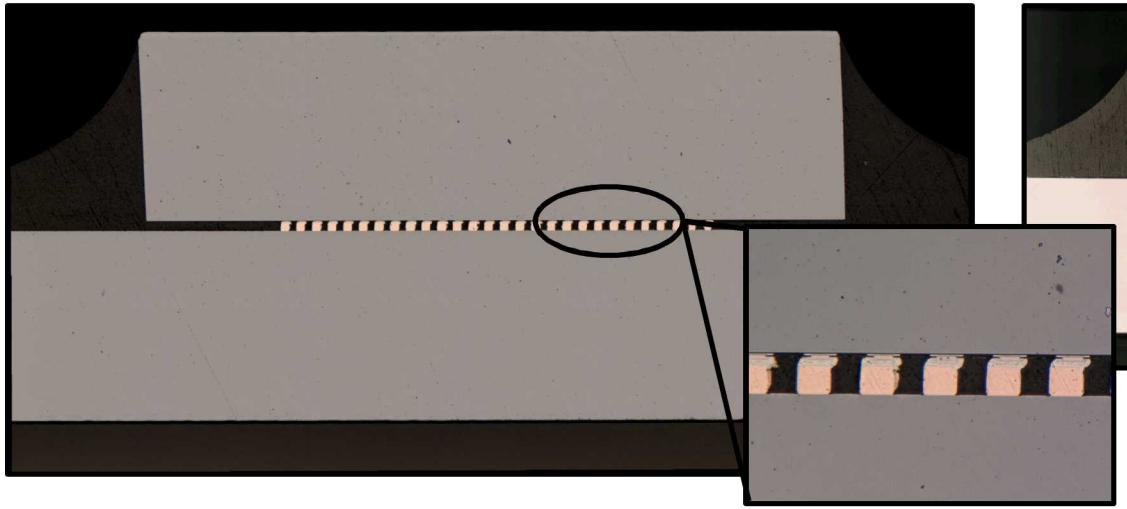
Summary

- Demonstrated proof of concept batch level UBM deposition on singulated die
- Microbump bonding approaches evaluated for 55 µm pitch flip chip bonding
  - Au thermocompression bonding
  - Cu pillar reflow solder attach
- Reliability tests in progress (IMC formation, cryo compatibility, resistivity and mechanical aging studies)

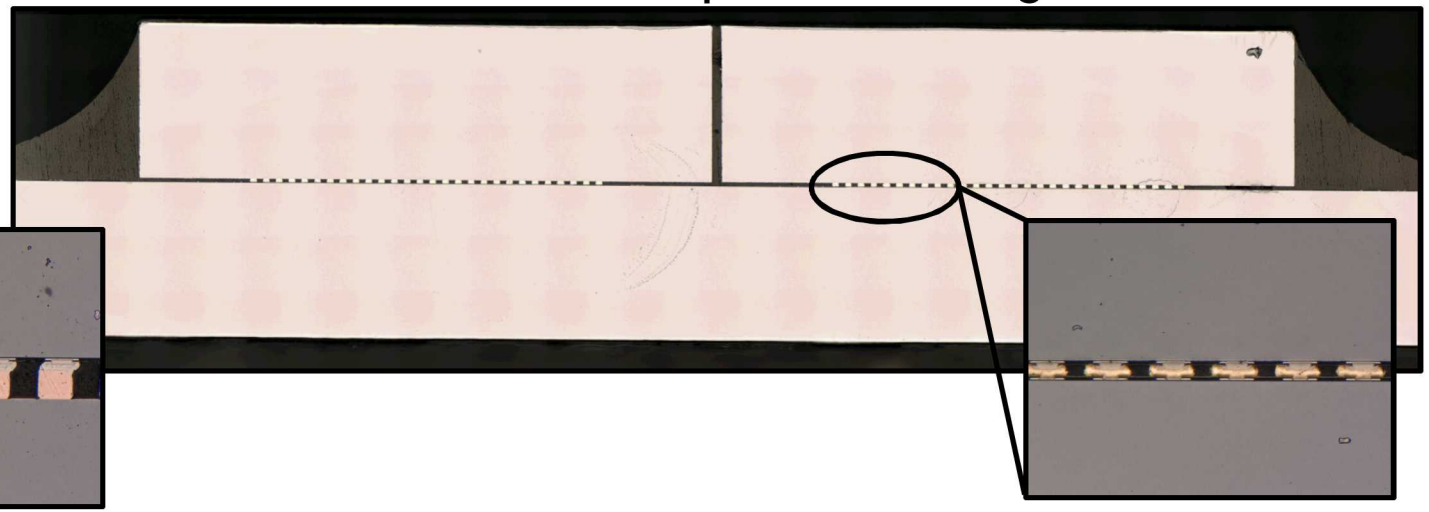
Batch level UBM deposition of singulated die



Cu Pillar Reflow Attachment



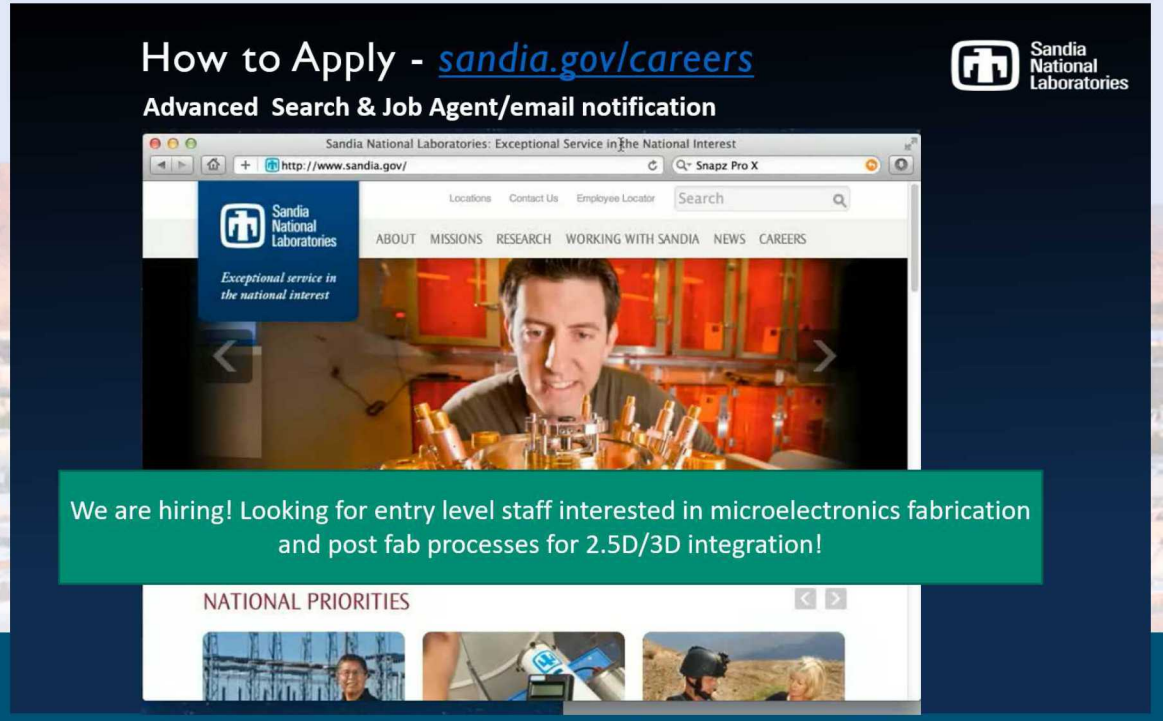
Au Thermocompression Bonding



Acknowledgements

- **TSVs** – Christian Arrington, Todd Bauer, Matthew Blain, Jason Dominguez, Ron Goeke, Edwin Heller, Robert Jarecki, Becky Loviza, Jaime McClain, Lyle Menk, Anathea Ortega, Jamin Pillars, Paul Resnick, Robert Timon

- **Micro bumping** – Christopher Michael, Todd Bauer, Christopher Nordquist, Matthew Jordan, Jaime McClain, Kate Musick, Christian Arrington, Jamin Pillars



Thank you – Questions?

Andrew E. Hollowell - aehollo@sandia.gov - 505.844.8301

Supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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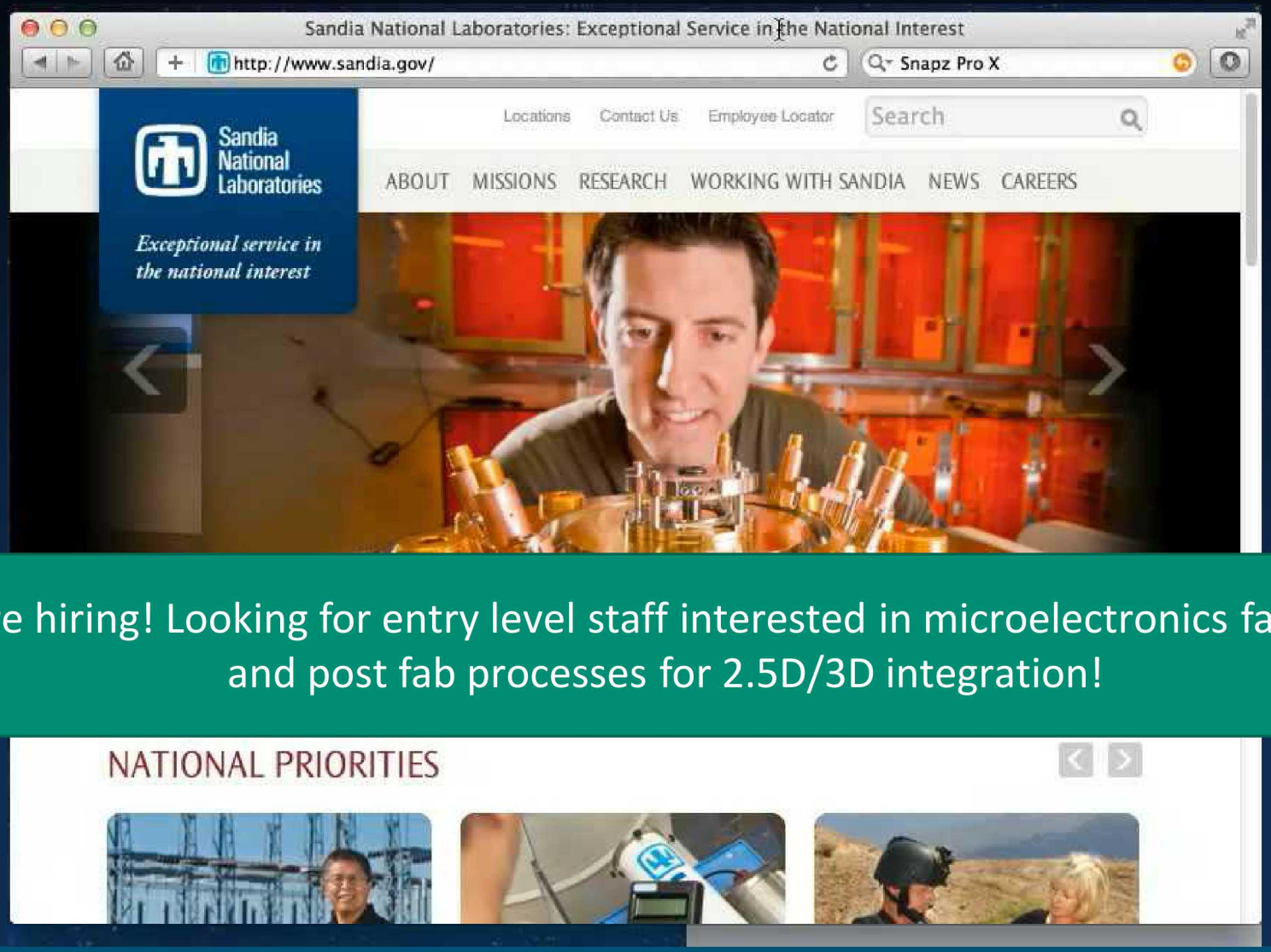
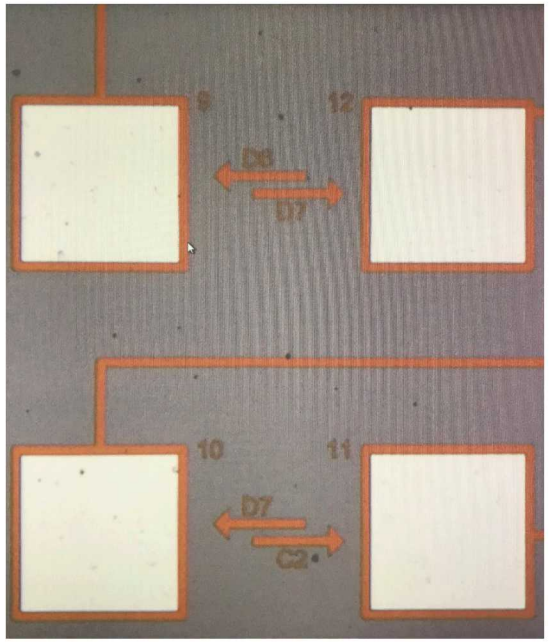
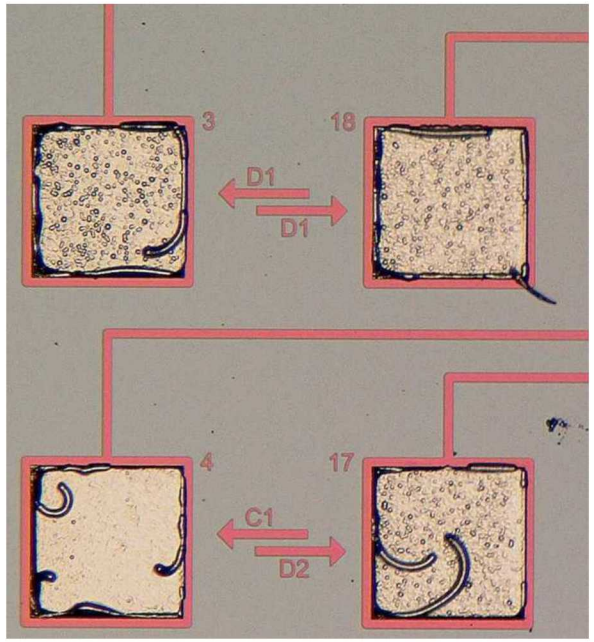


We are hiring! Looking for entry level staff interested in microelectronics fabrication and post fab processes for 2.5D/3D integration!

Zincation Results

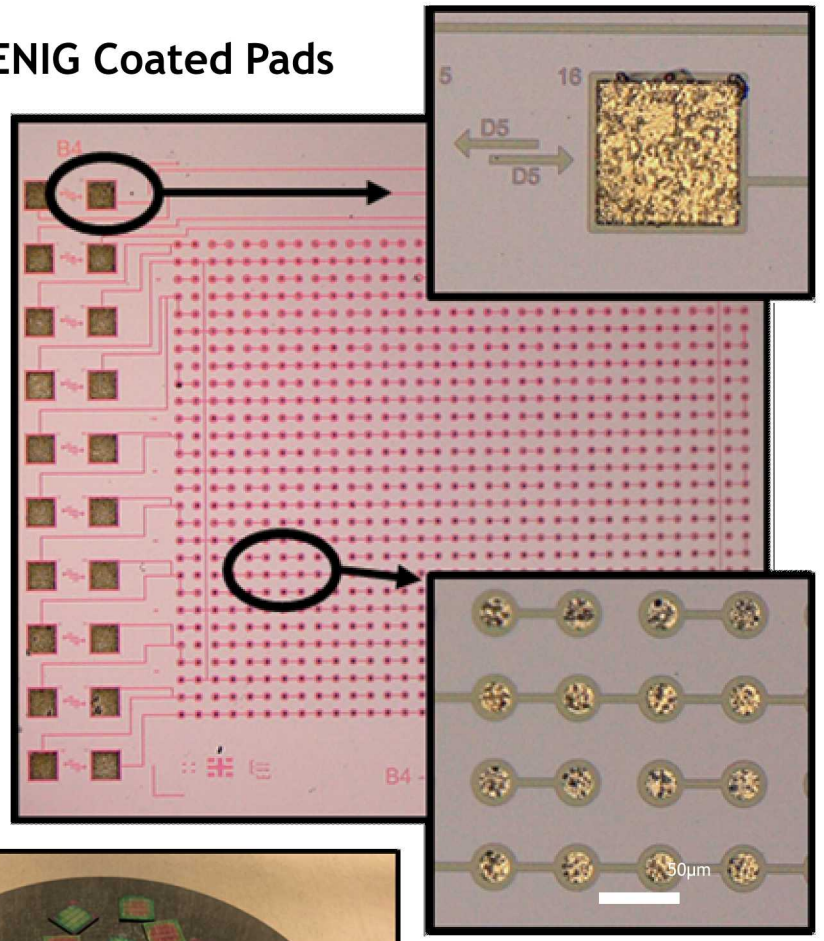


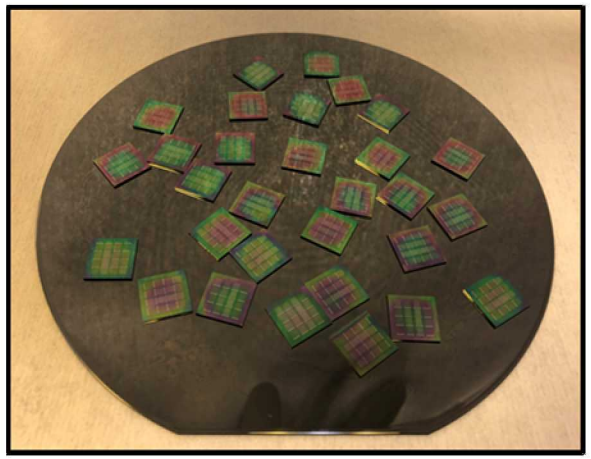
Al bond pads



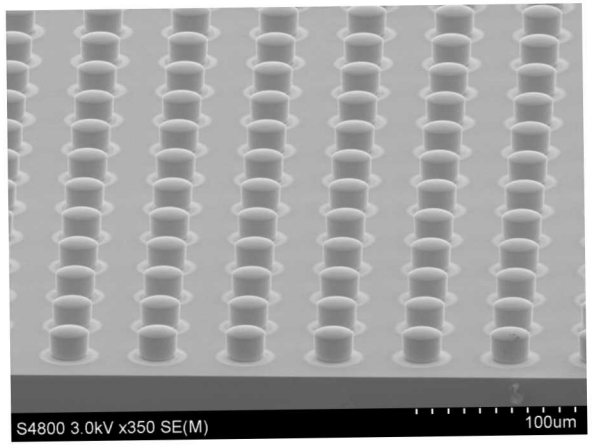
After Zincation
and Electroless Ni

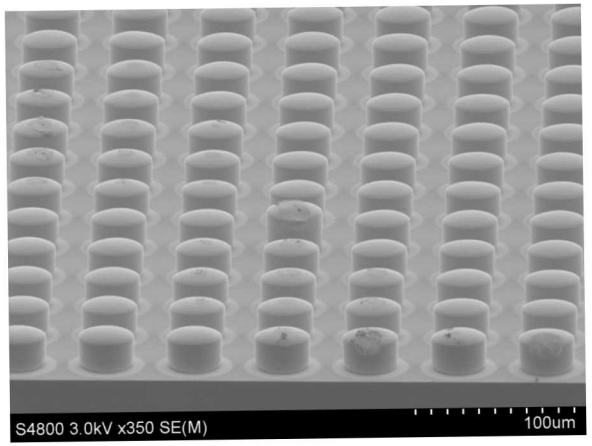
ENIG Coated Pads

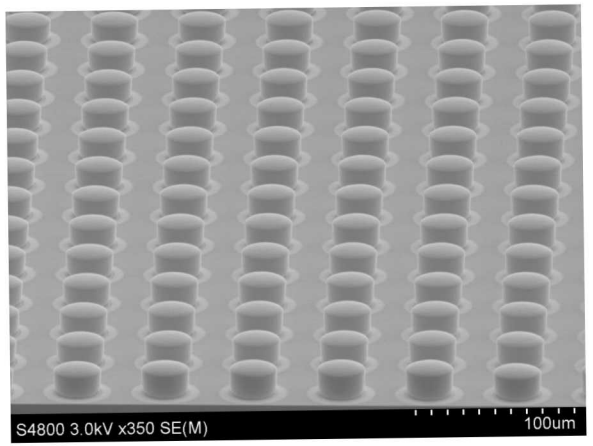


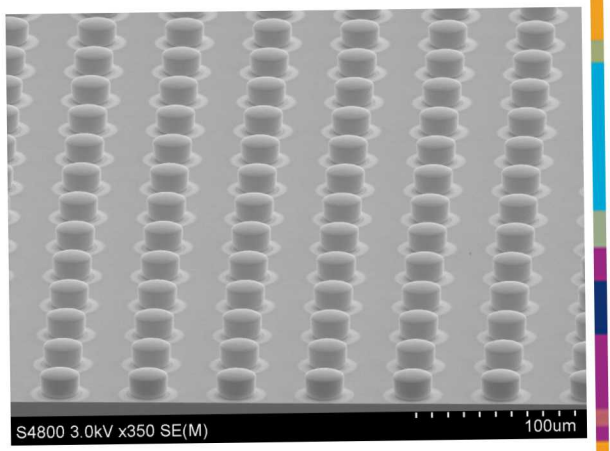


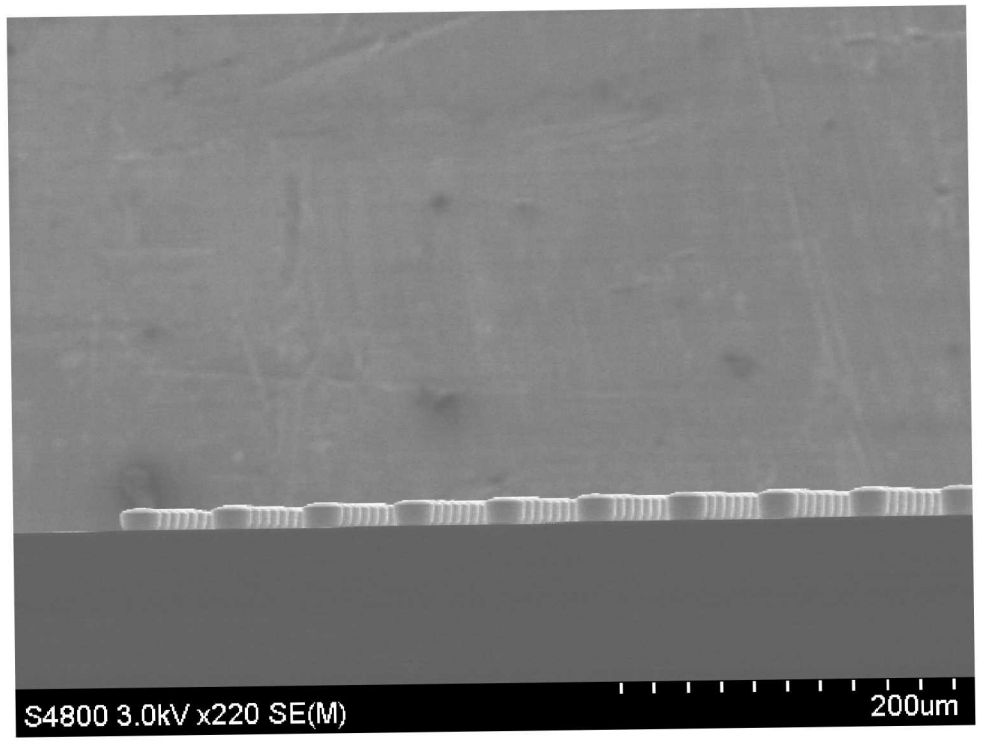
Copper Bump Development – Tune Additives and Current Density

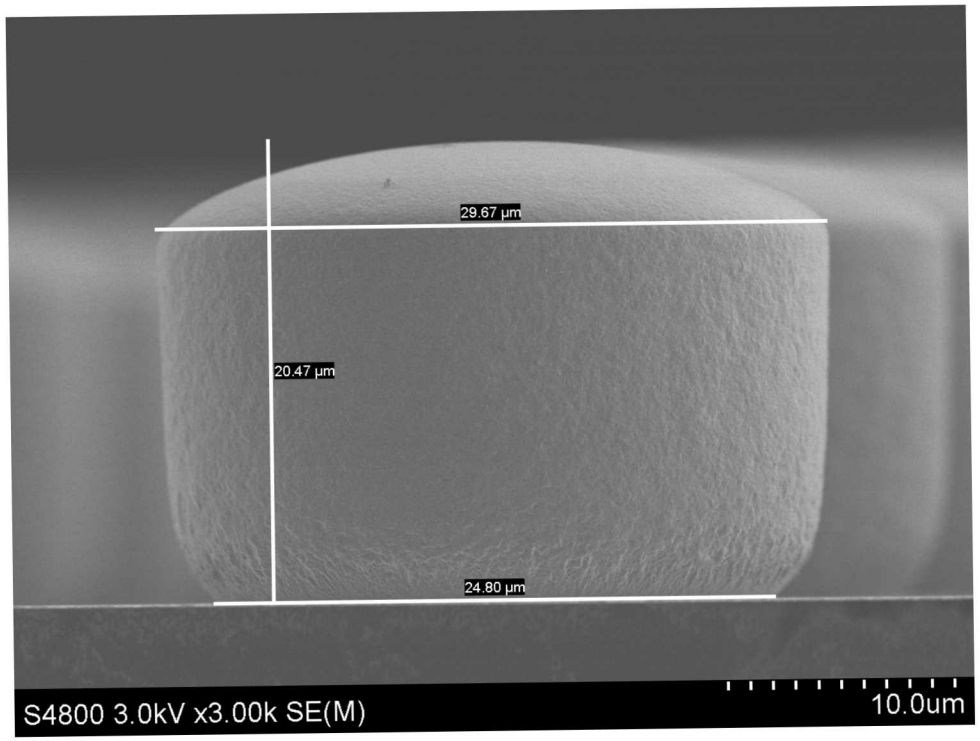




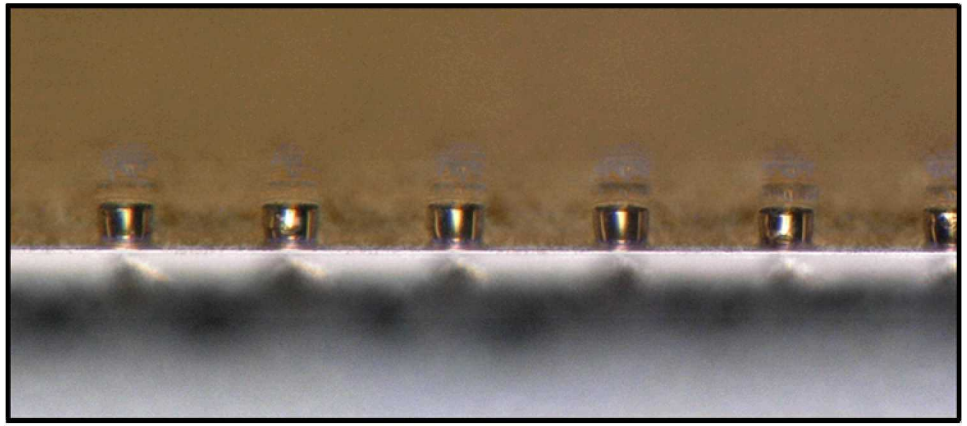


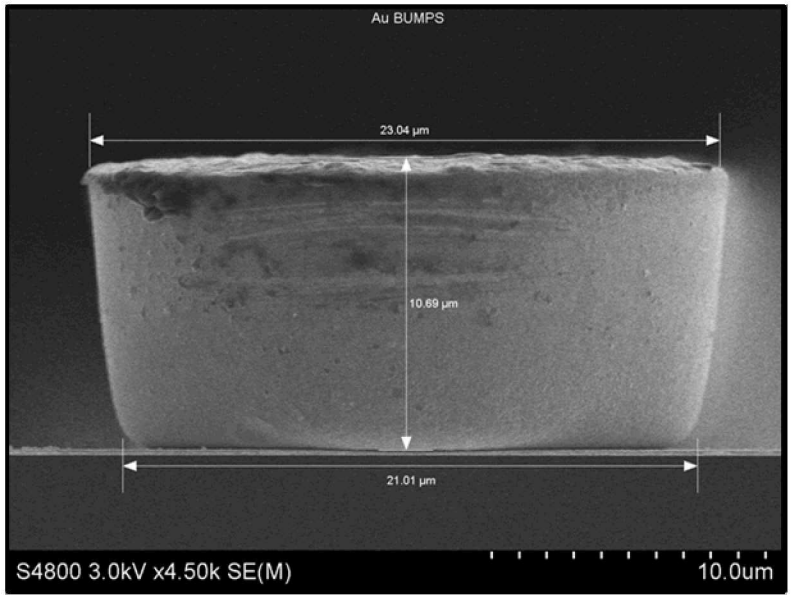


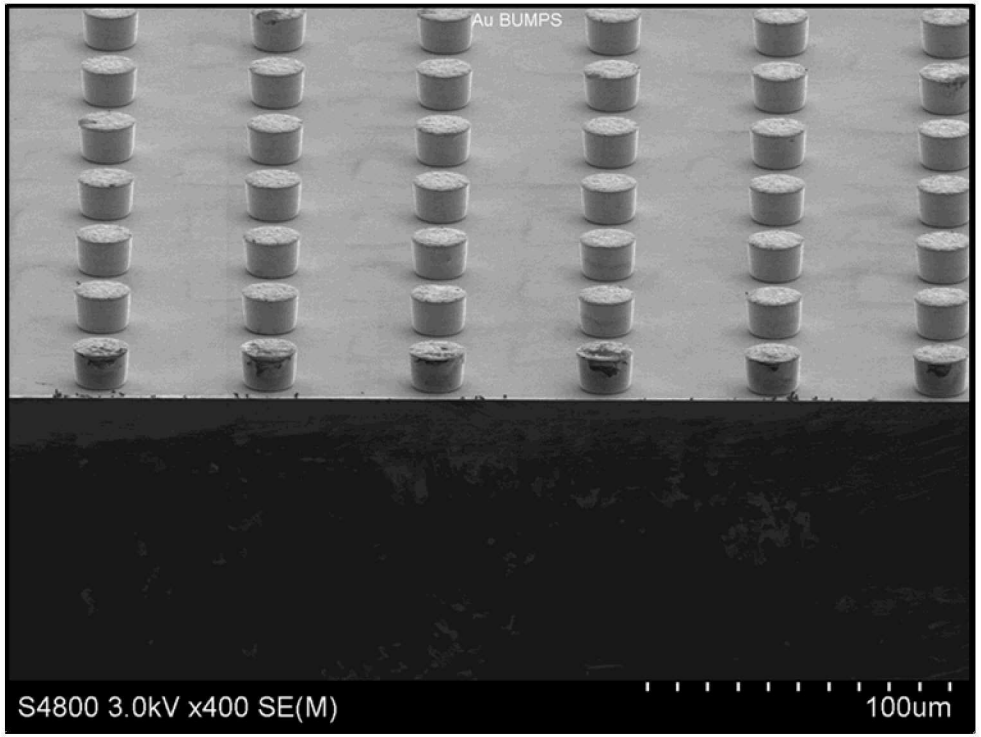


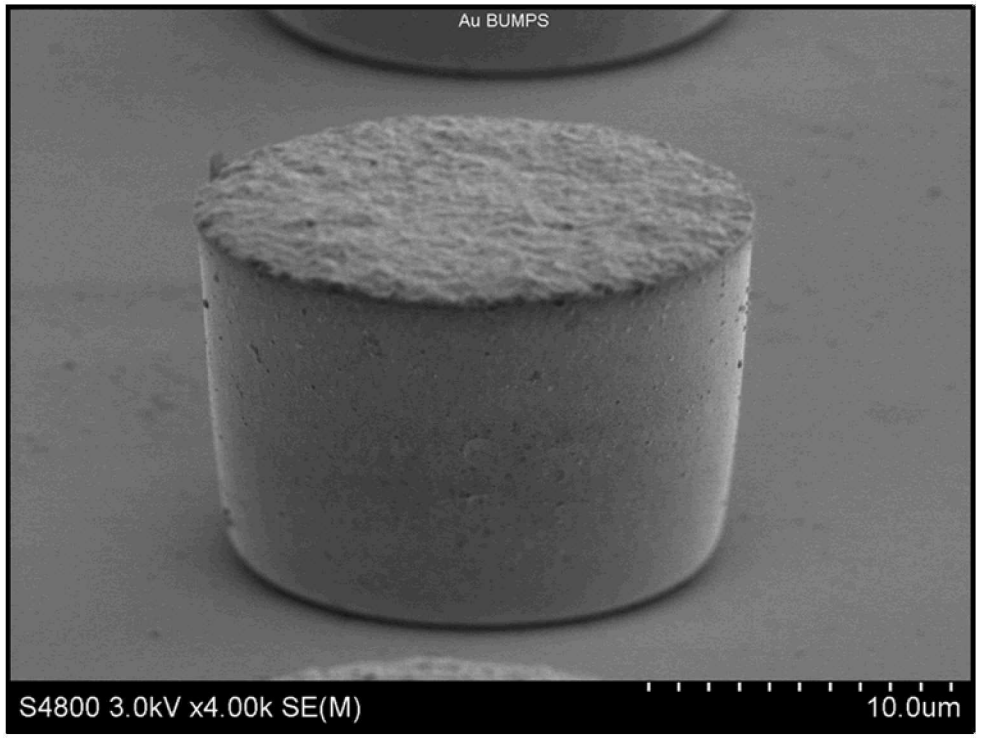


Gold Bump Development



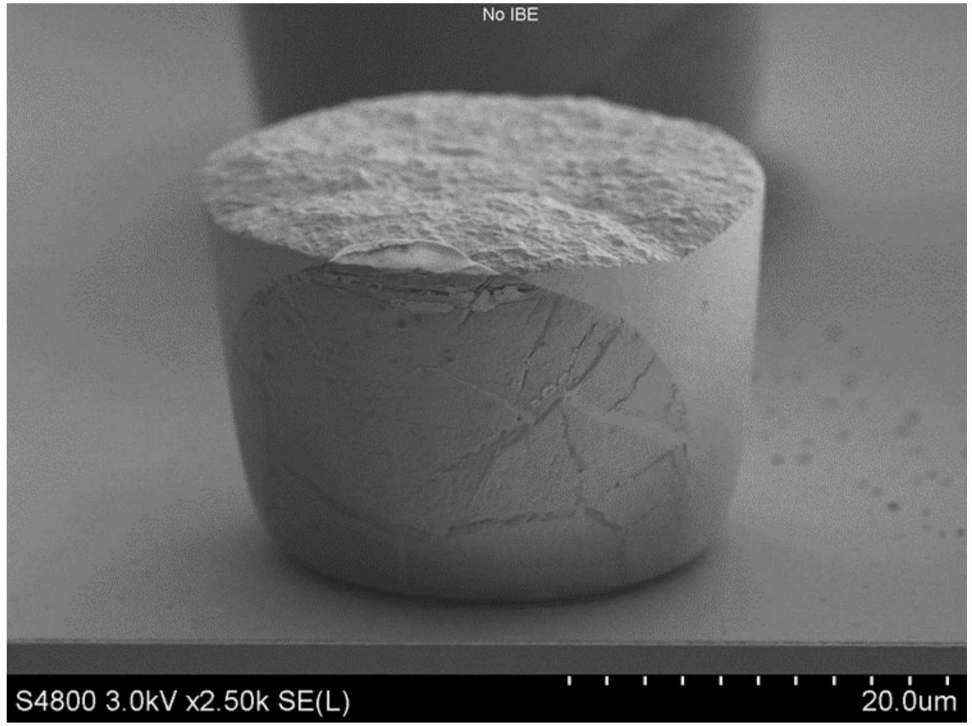




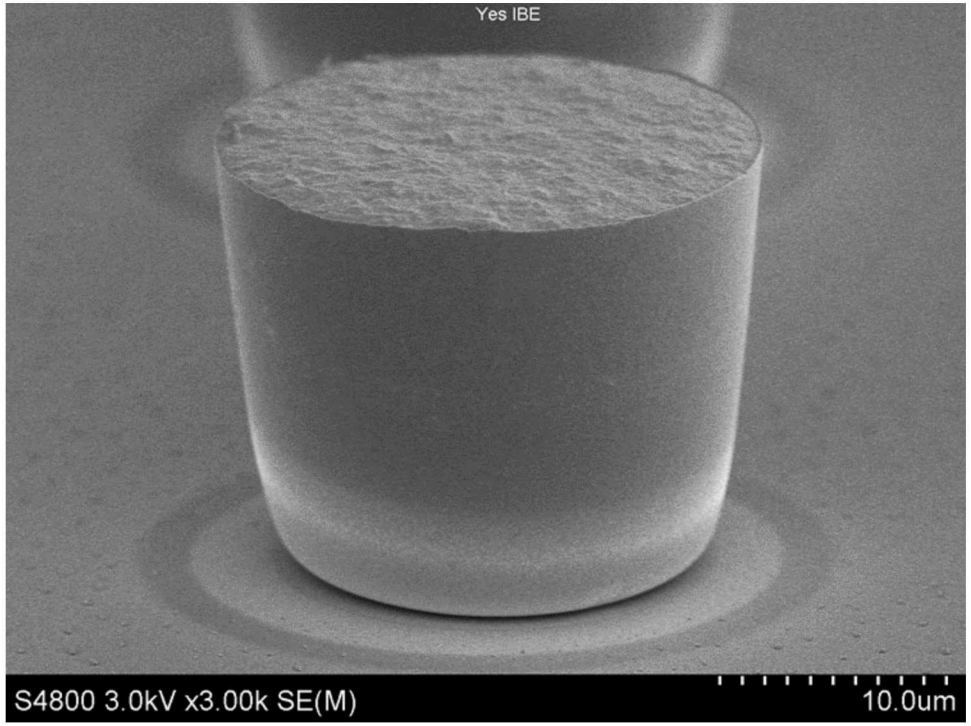


Gold Bump Development – Seed and UBM Removal

Pre seed removal

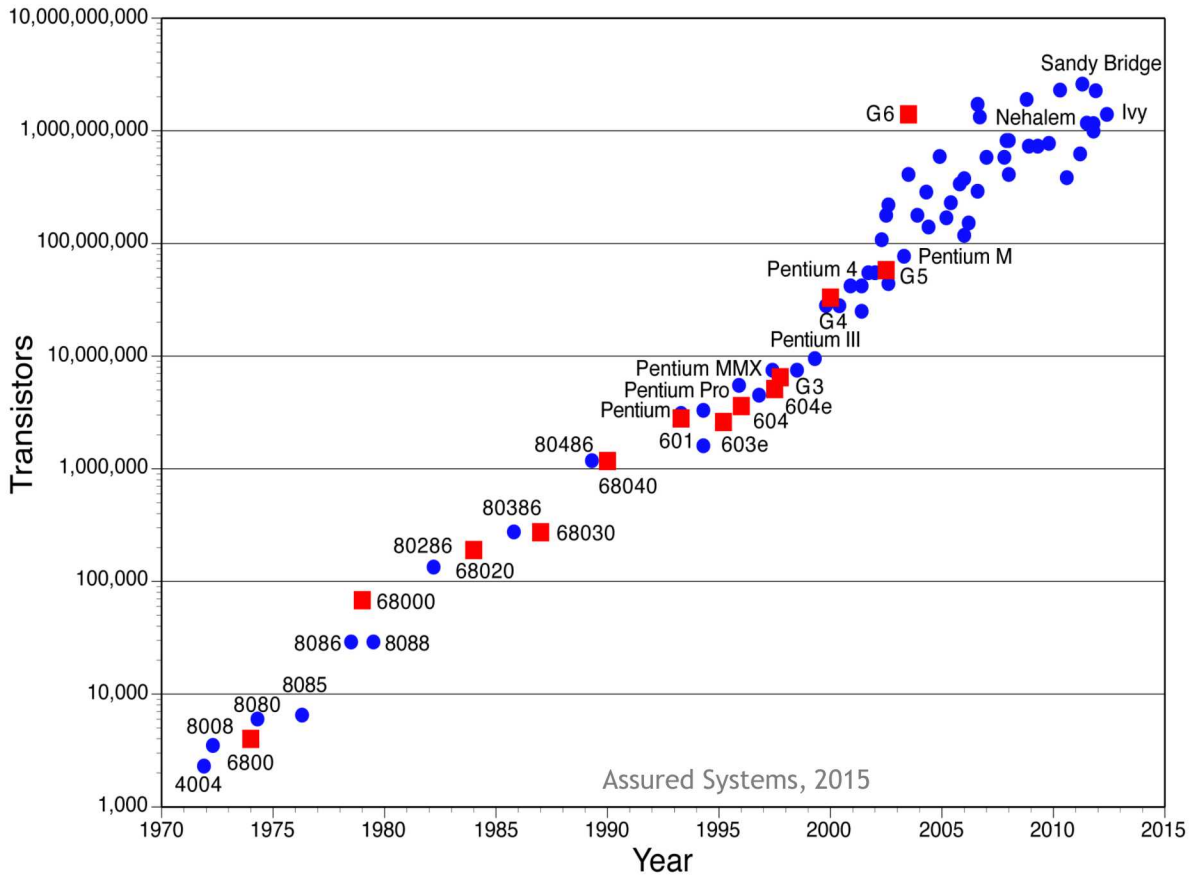


Post seed removal

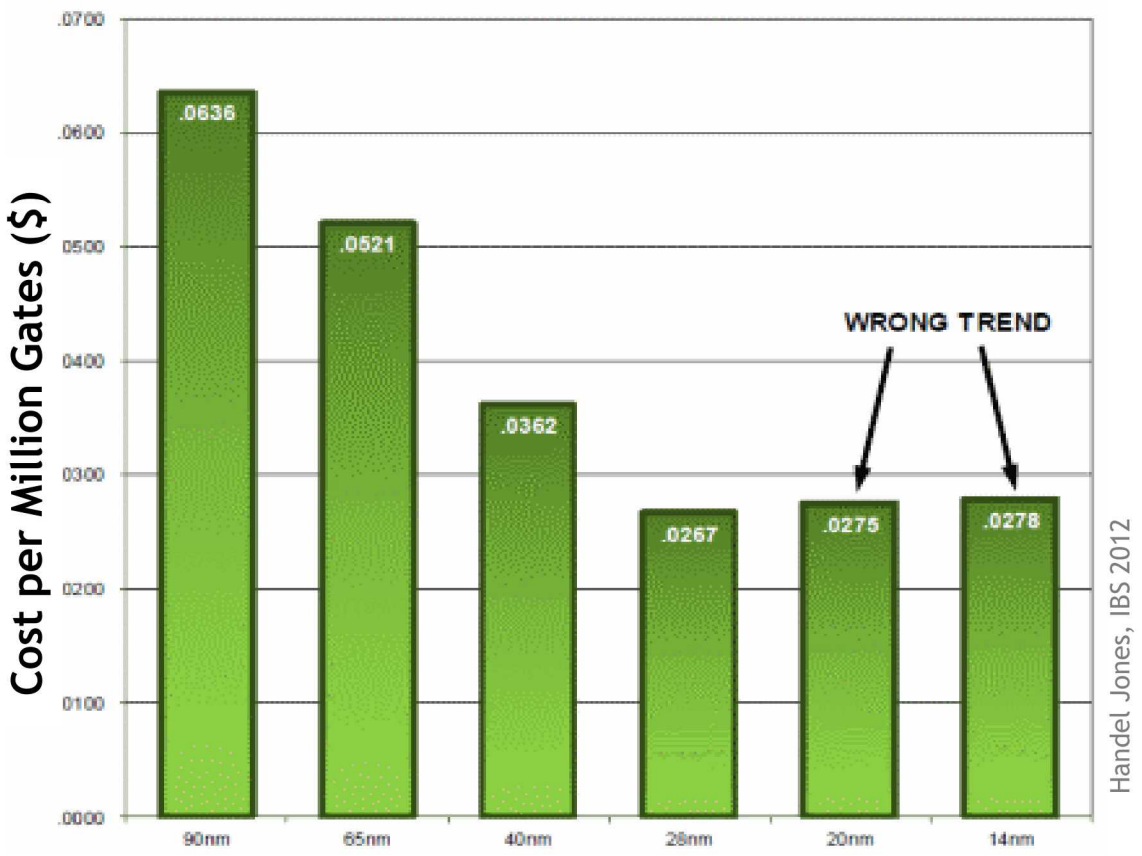


Moore's Law - Continued Scaling

Transistor density continues to increase



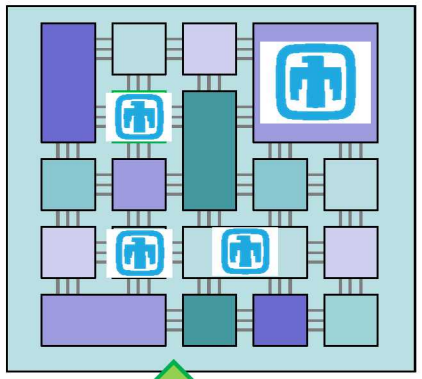
Cost per transistor is increasing

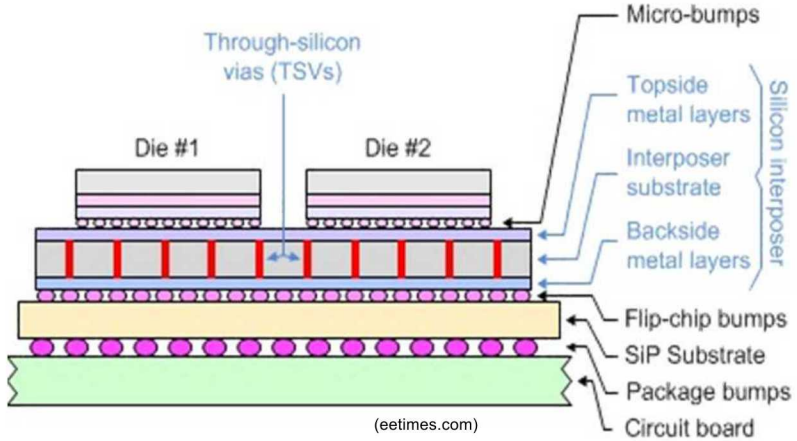


2.5D/3D Heterogeneously Integrated Microsystems

Path for Continued Scaling

2.5D "System in Package"





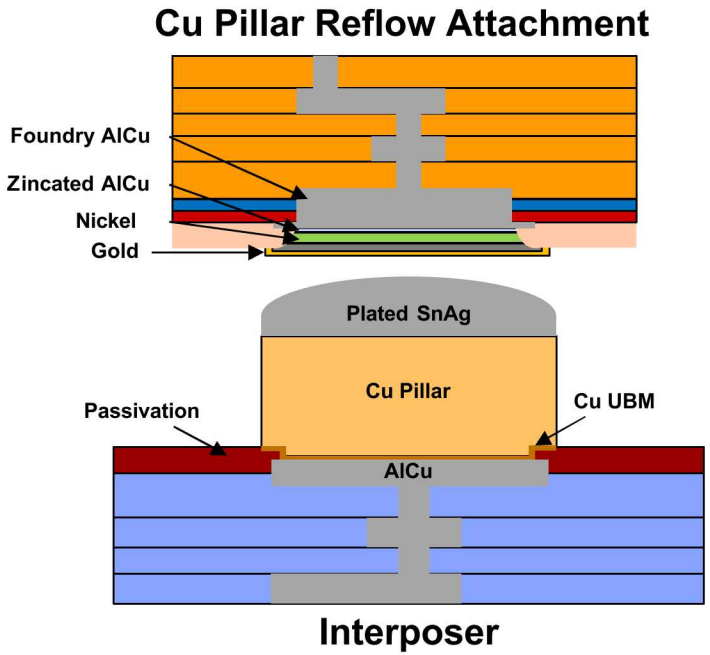
Flexible Interconnect Fabric

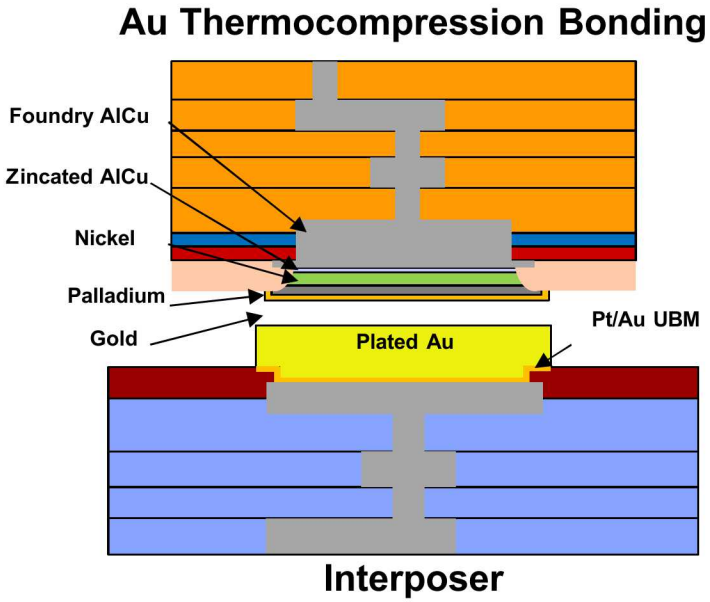
→ Multi layer high density routing
→ Leverage DARPA CHIPS standard
→ Massively parallel I/O for future functions (performance, rad-hard/trust functions)
→ Low latency, low packaging parasitics

- 2.5D Integration on Interposer
  - Use Sandia tech, COTS, MPW die, partner die, etc. in low volumes
  - Partially disentangle issues of performance, radiation hardness, etc.
  - Standardized digital/analog/power
  - Pre-build passive components and active device blocks
- Heterogeneous Integration
  - High-value functions in custom technologies
  - Unlock performance of disparate technologies
  - Internal and external tech: III/Vs, MEMS, photonics, etc.

Challenge: Microbumping for low-volume USG applications (DOE, DOD, etc.)
Current options: High Labor Cost - or - High Fab Cost

Micro-bumped Interposer Options





- Wide-spread industry adoption
- Height determined by Cu pillar
- Pd not necessary
- Reactivity has potential reliability concerns
- Rigidity has potential mechanical reliability concerns (cryo)
- SnAg T_{mp} = 220C -> temperature constraints (challenging integration with TSV thinning)

- Au is less reactive, more ductile than Cu
- Potentially compatible with TSV thinning and TSV pad formation processes
- ECD Au vs stud bumping -> full wafer bumping
- TCB usually has thick Au on both sides
- Au to ENEPIG bonding needs to be evaluated
- Small gap between bonded pair
- TCB force may damage low-k dielectrics

Challenges with Low Volume, High Value 2.5D Integration

Very Low Volume ≈ 1 - 100 die

Use interns/students/postdocs

Feasible for demonstrations and development

Low Volume ≈ 100 - 1000s of die

Utilize interns, students, postdocs… (but they hate you)

Make a wafer-like substitute at OSAT $$$

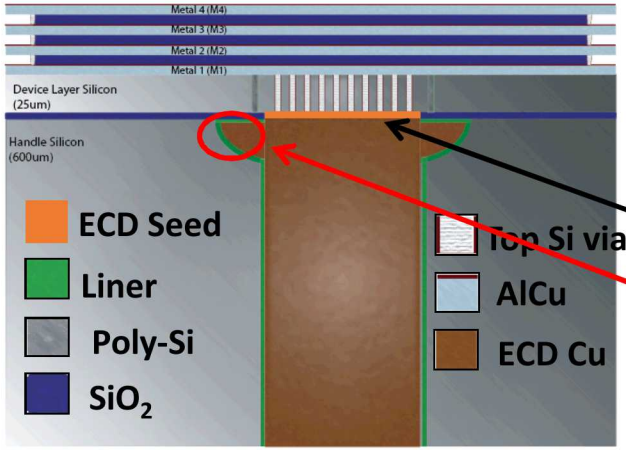
Spend lots of $$$ and purchase full wafers from a foundry

Mid-high volume ≈ > 1000s die

Buy a dedicated run at an advanced foundry

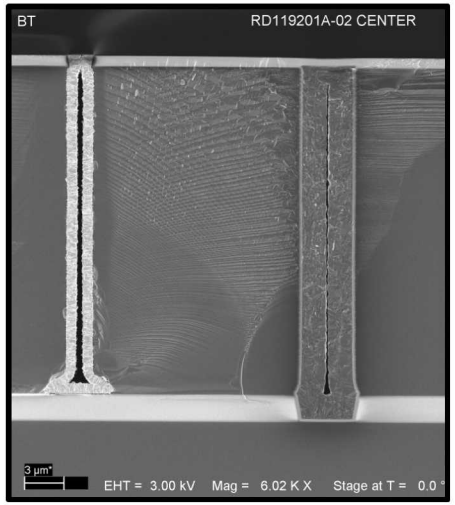
TSV Integration - Hybrid W via first, Cu via last Approach

A. E. Hollowell, et. al. "A Unique 3D Integration Approach for SOI Substrates – Mating CVD W Filled TSVs with ECD Cu Filled TSVs." ECS PRiME October 2016

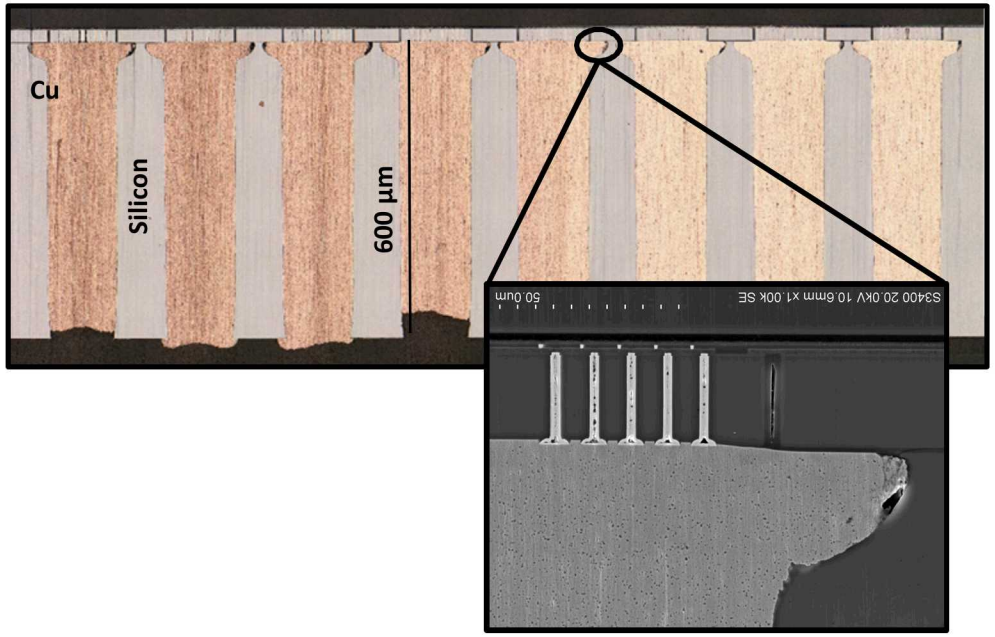


Through mask Cu filling from a discontinuous evaporated seed

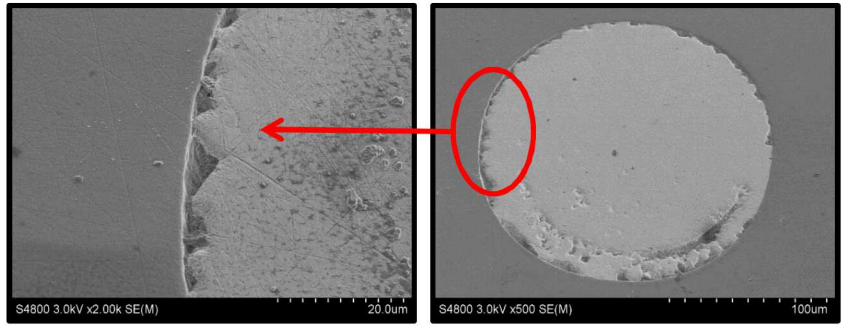
- Top Si vias to connect Cu TSV through BOX to M1
- Isolation trench to electrically isolate the vias from the device Si layer
- ECD seed deposited only at the bottom of the TSV
- A void free fill of the notch is impossible to achieve
- Less than 10 mΩ per TSV



Through Mask Plating Cross Section

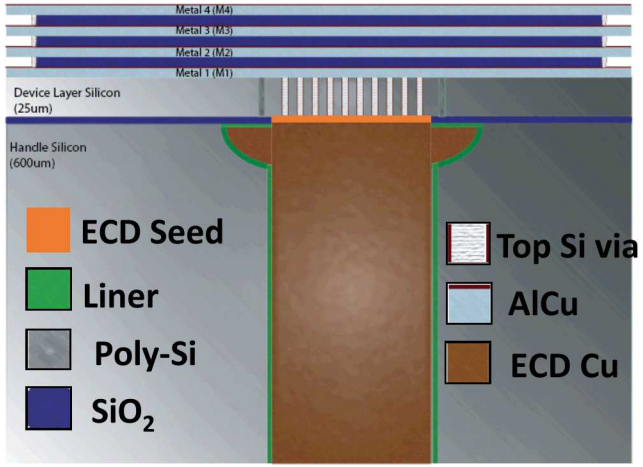


SEM after Parallel Delayering

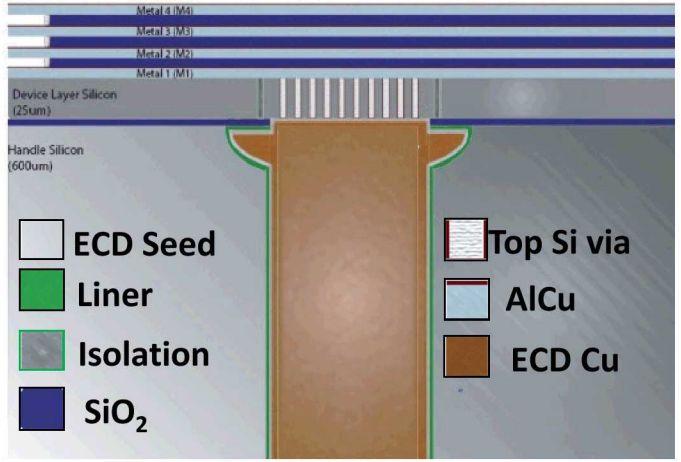


Bottom Up Filling from an ALD Pt Seed

Through Mask Plating



Bottom Up Plating From Continuous Pt Seed Metal



Superfilled Bottom Up Plating

- Adapted from research by Josell and Moffat at NIST-Gaithersburg
- Void free filling
- Reasonable deposition times
- Complex balance between applied bias and electrolyte composition
- Plating conditions for void free filling is dependent on TSV geometry

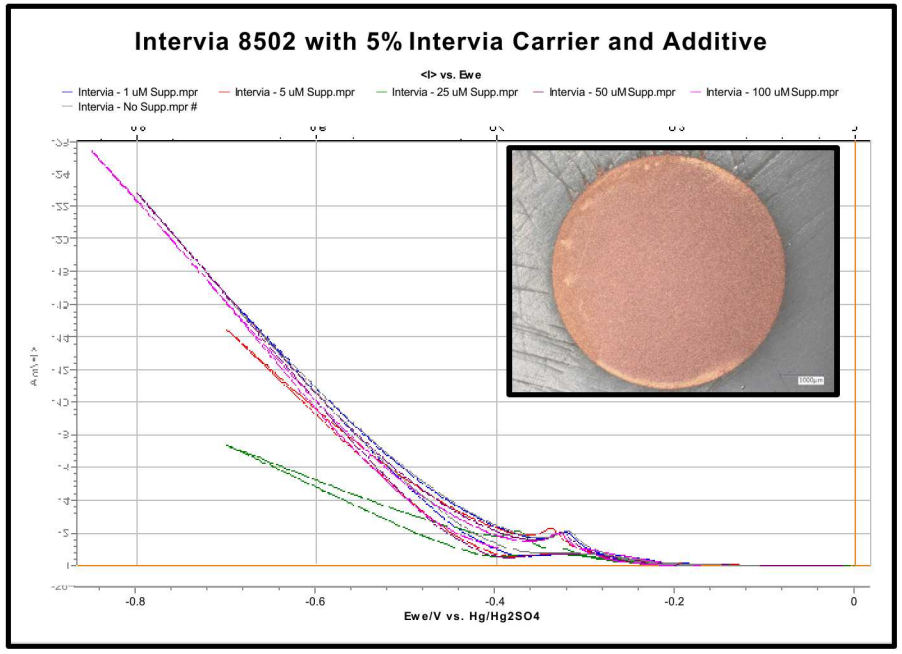
Full Wafer Production Scale Filling

1. Production plating tools do not have reference electrodes
2. Establish voltage controlled super filling
3. Derive current controlled void free filling from potentiostatic filling results

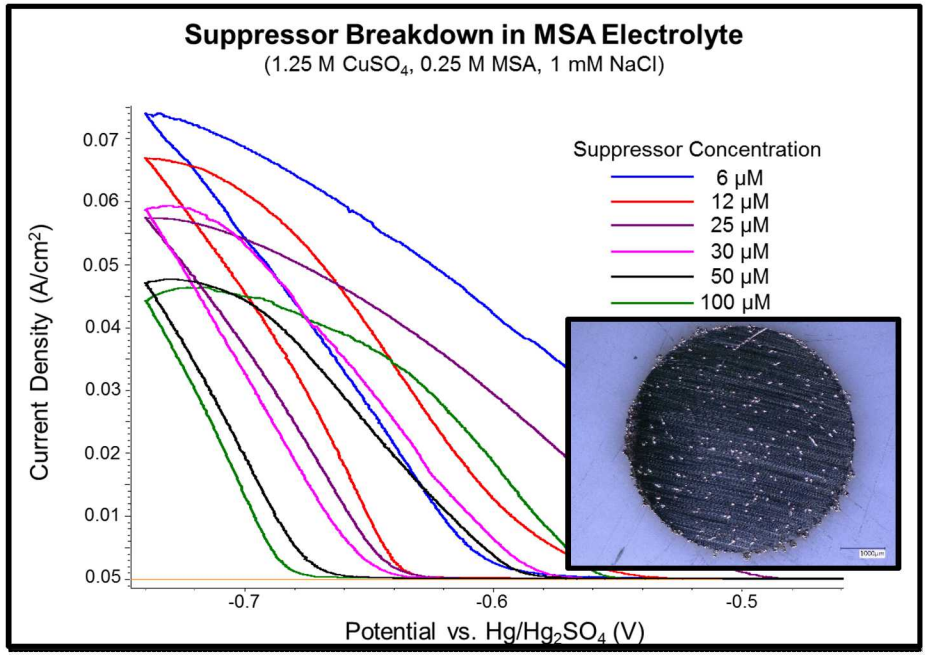
3-Additive Commercial Chemistry vs MSA Electrolyte with Tetronic 701 Suppressor

- **Commercial plating chemistry does not exhibit S-NDR characteristic**
- **Methane Sulfonic Acid (MSA) has a higher solubility limit**
- **MSA + Tetronic 701 exhibits CV hysteresis and S-NDR mechanism**

Commercial H_2SO_4 Plating Chemistry

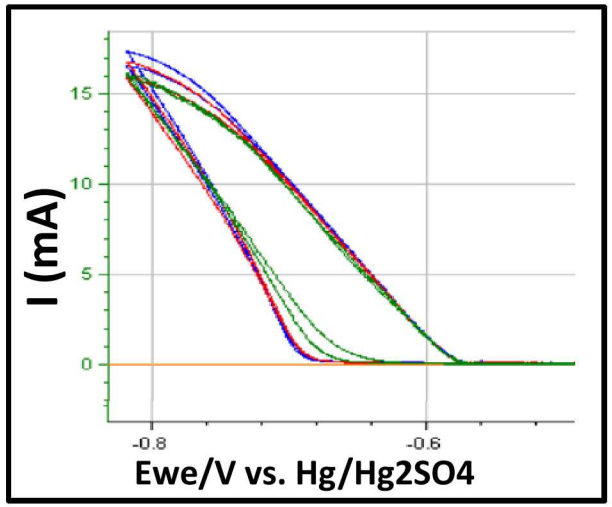


MSA Electrolyte w/ Tetronic 701 Suppressor

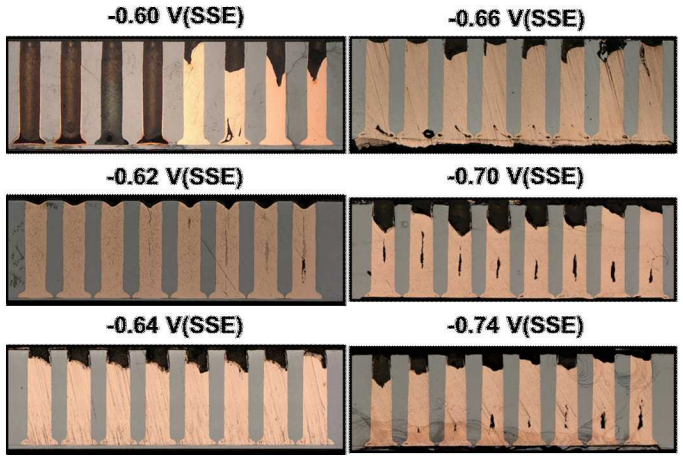


Investigating the Effect of Suppressor Organics on Galvanostatic Deposition

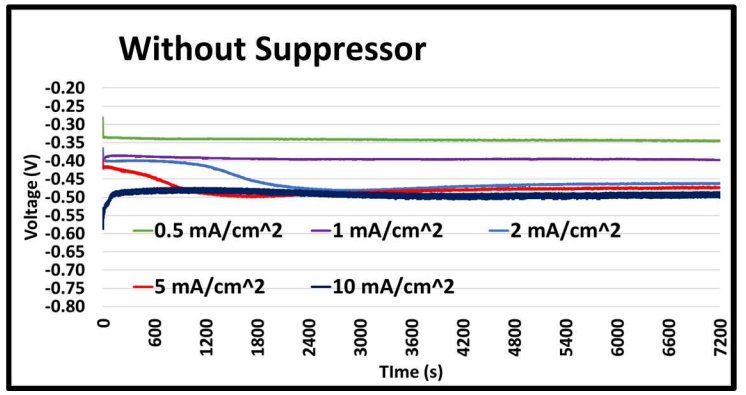
Plating Electrolyte CV Curve

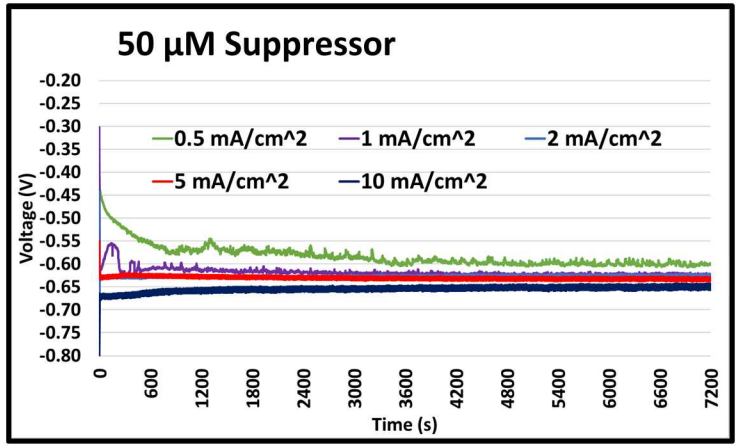


Potentiostatic plating is very sensitive to applied voltage



Chronopotentiometry on Unpatterned Sample Coupons





- **Larger voltage window w/o suppressor**
- **Suppressor pins voltage to > -0.55 V(SSE)**