

Metal Micromachining Team

SAND2019-3583PE



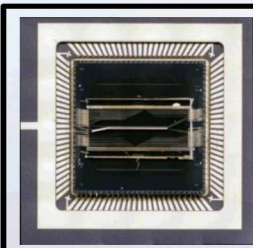
EPICs

clarrin@sandia.gov

Metal Micromachining Team

MMT - MESA Light Labs

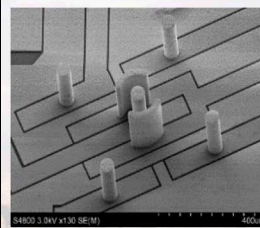
Lab #1 – Lithography



Lithography

- EPICs Ion Trap (Lithography on optical coatings)
- mm thickness range
- Can be electrofilled
- Micromolding or cast w/ PDMS
- Accommodates topography
- Polymer or glass

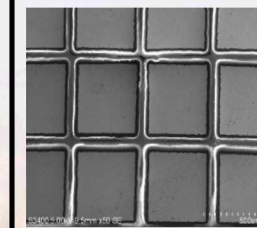
Lab #2 – Electroplating



Electroplating

- LIGA Stylus Ion Trap
- 2.5D structures
- Precision coatings
- Magnetic materials
- Insulating materials
- Conductive polymers
- >10:1 aspect ratio
- Multi-layer

Lab #Planarization



Planarization

- Improved R_a 1.46 $\rightarrow$ 0.07 μm
- R_a as low as 50nm
- Wafer/die thinning
- Provide flat/parallel surface for processing
- Beveled edges
- Vacuum, pad, wax mount



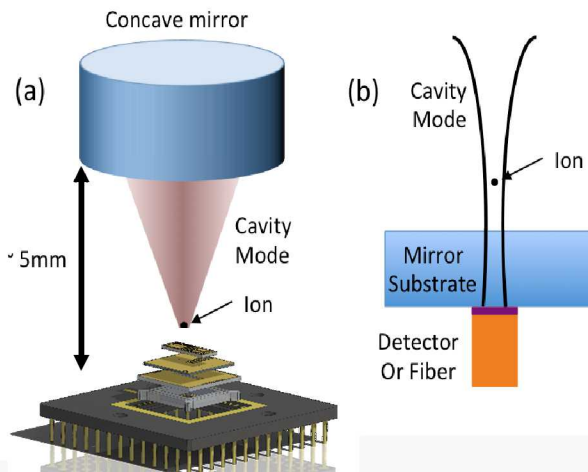
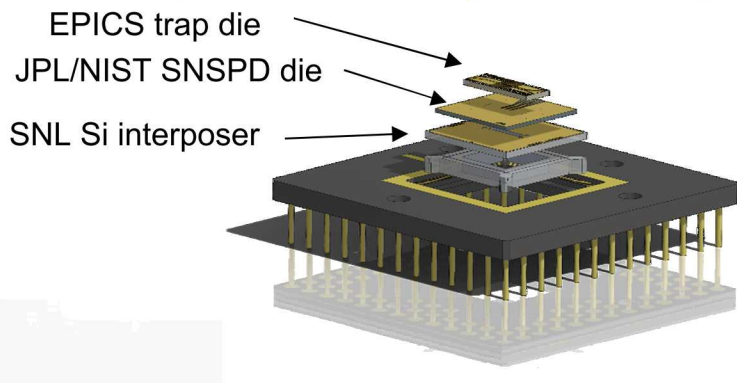
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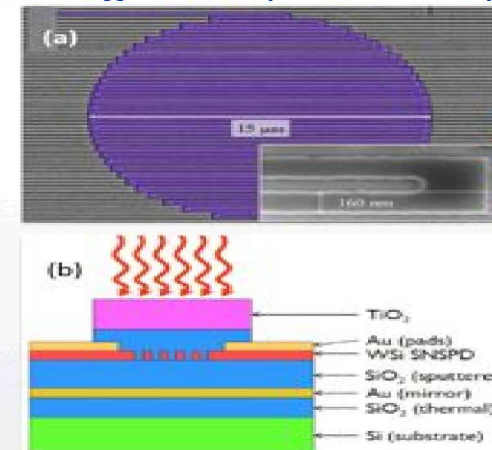
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Generation 3 integration

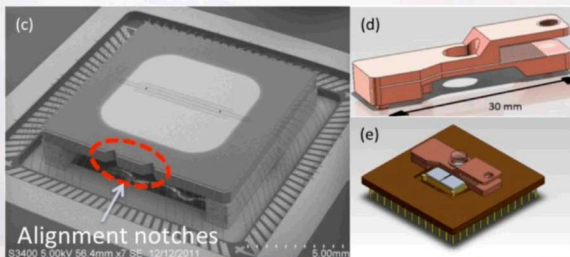
Ion Trap Fabrication (Duke/SNL)



SNSPD Detector Development & Integration (NIST/JPL)



Optomechanical Integration (Duke/SNL)



EPICS goal for generation 3 fabrication

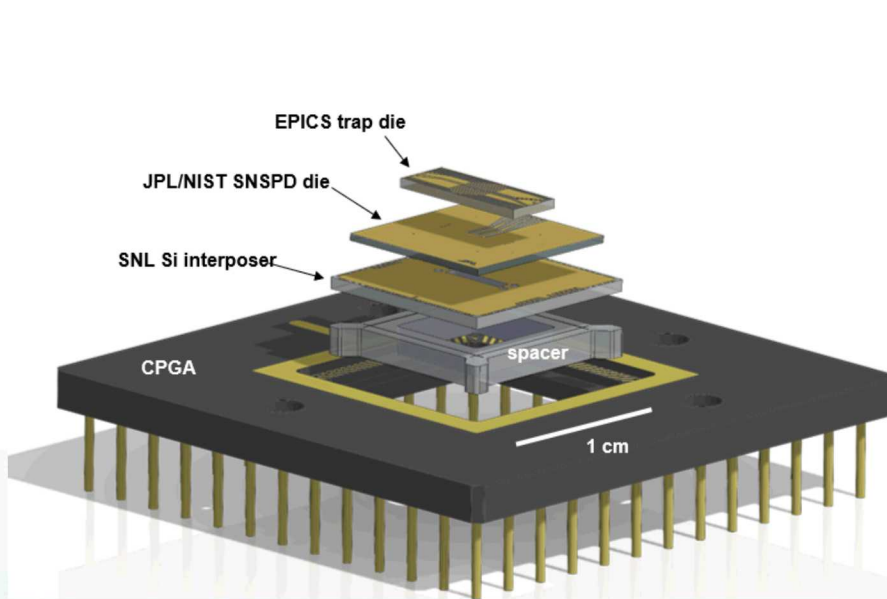


Figure 3: EPICs Ion trap integration model showing EPICs ion trap die, SNSPD detector, interposer, spacer, and CPGA.

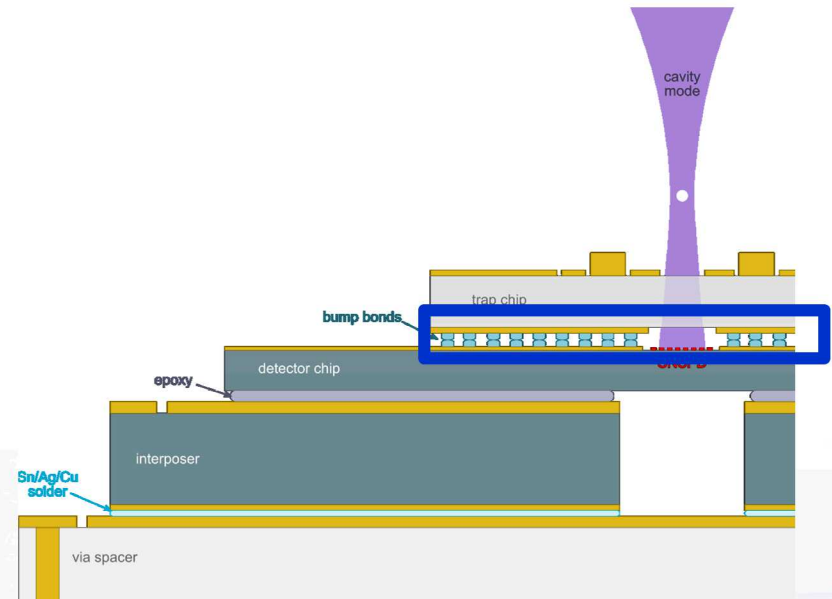
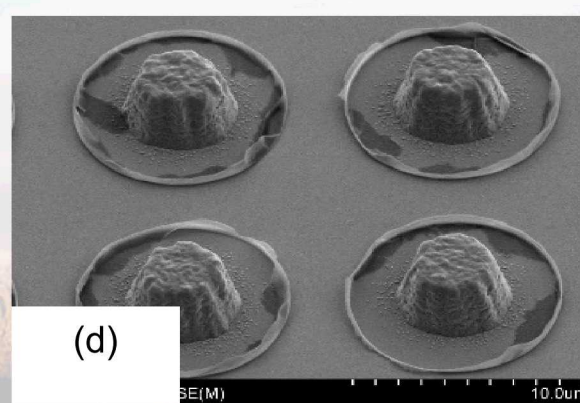
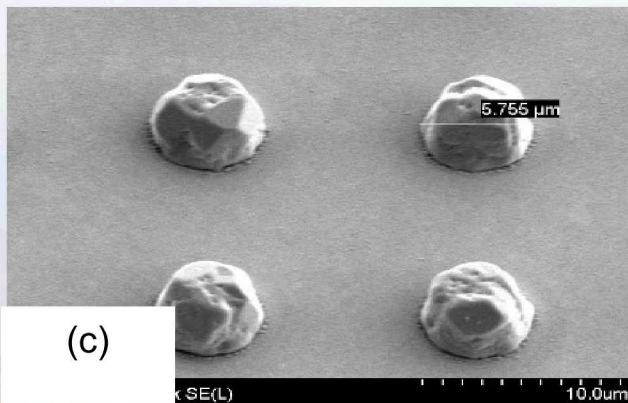
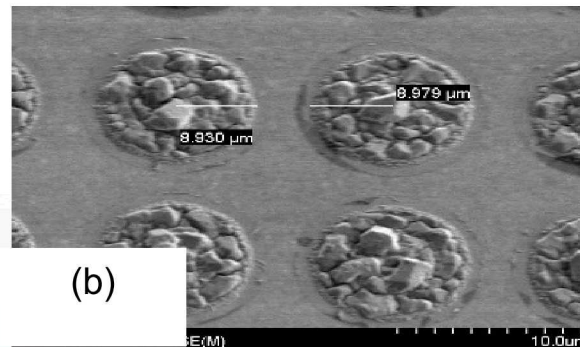
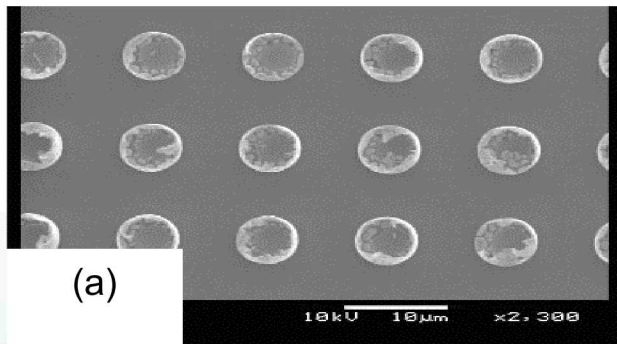


Figure 4: Generation 3 EPICs cross section view showing full integration of cavity mode, ion trap location, Sandia Trap chip, JPL/NIST SNSPD, interposer, and spacer.

Indium bump progression

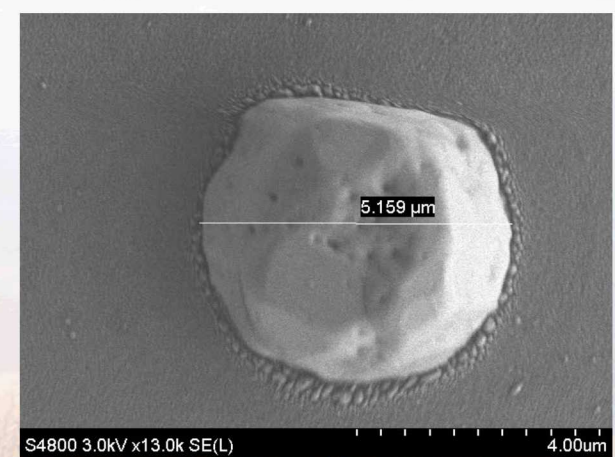
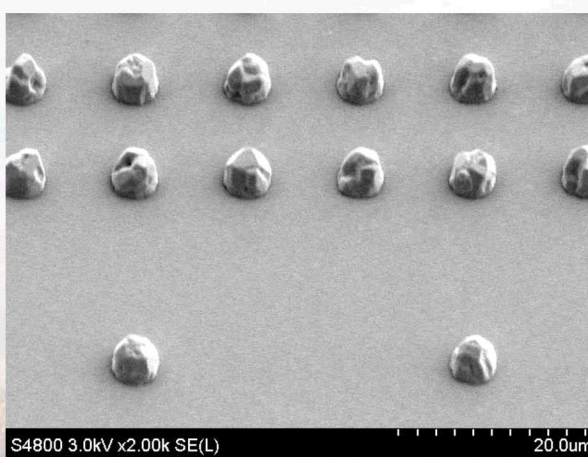
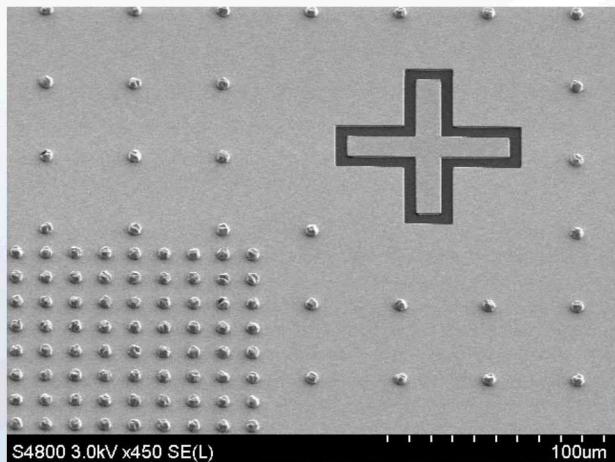
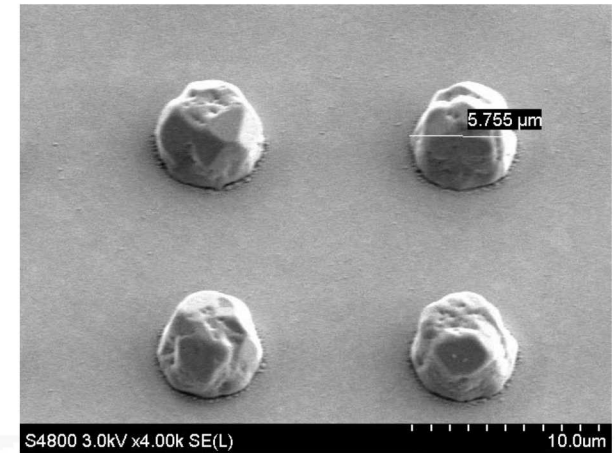
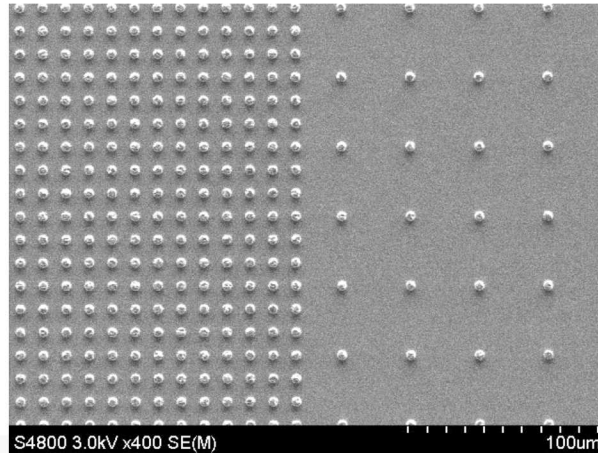
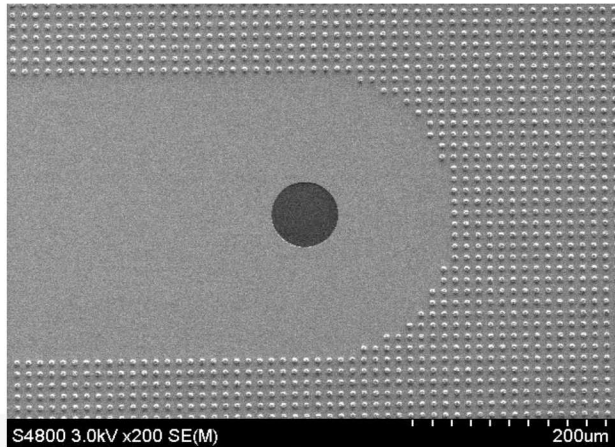
- (a) Poor lithography
- (b) Thin indium
- (c) Sandia Indium in CHA tool
- (d) Jet processing indium



SNL CHA Indium bump deposition

✓ CHA tool in Microfab

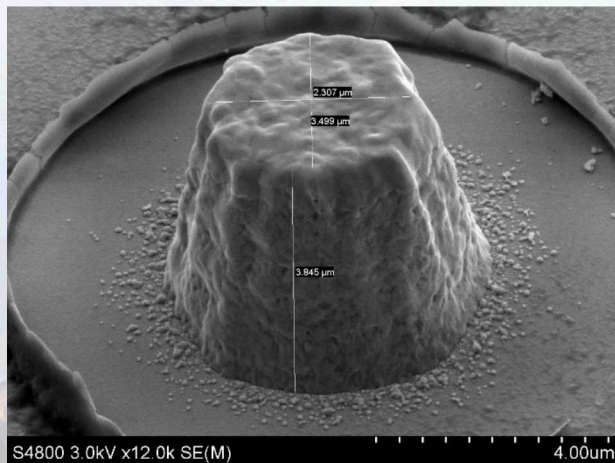
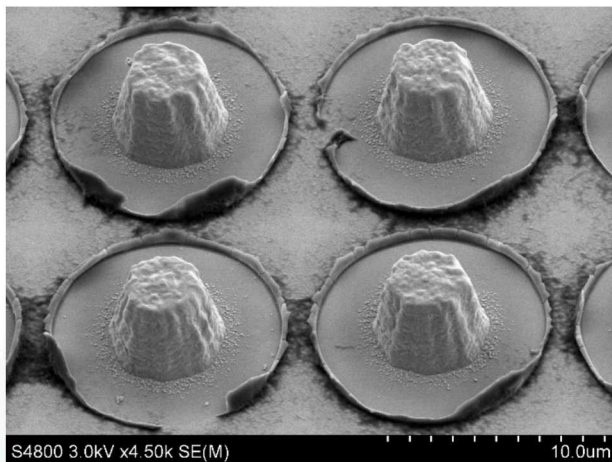
✓ Processed only backside: layer 1 Ti/Au (100/5000 $\text{\AA}^\circ$), layer 2 Ti/Ni/In (100/100/30,500 $\text{\AA}^\circ$)



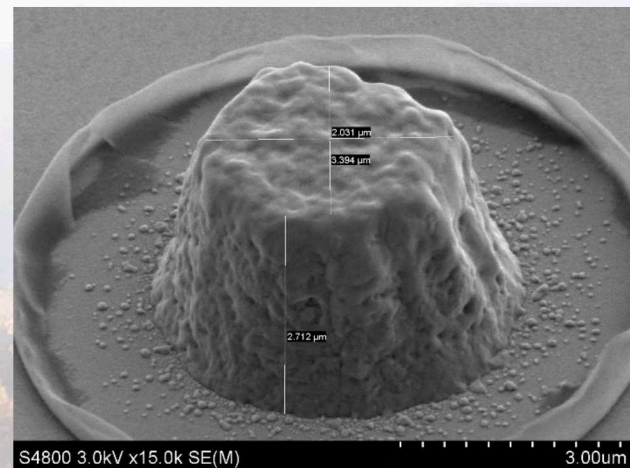
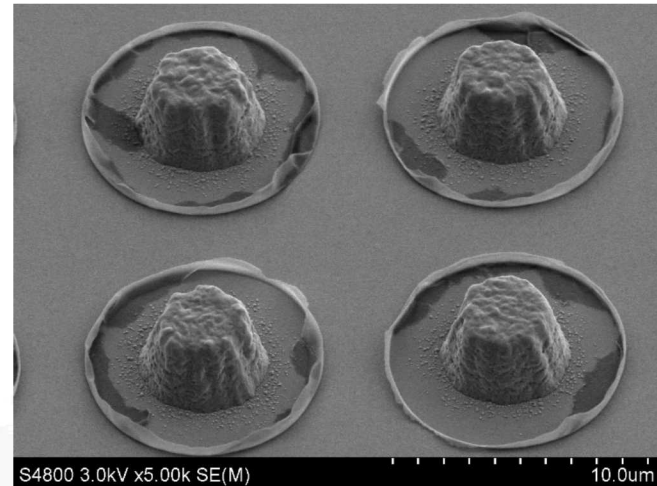
★ Jet Processing Indium in 2035 & 2070

- 2035 and 2070 lift off requesting Ti/Ni/In 200/1000/30,000 Å°

nLOF 2035

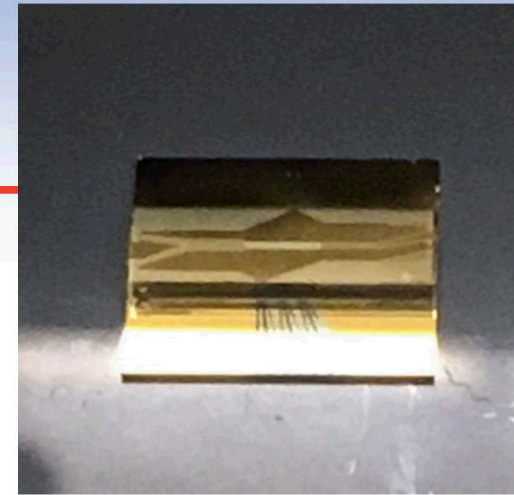
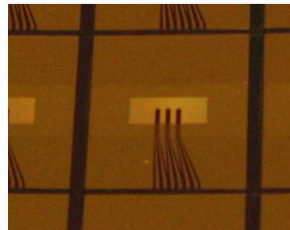
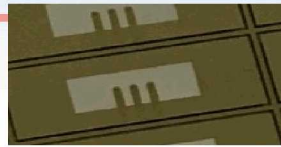


nLOF 2070

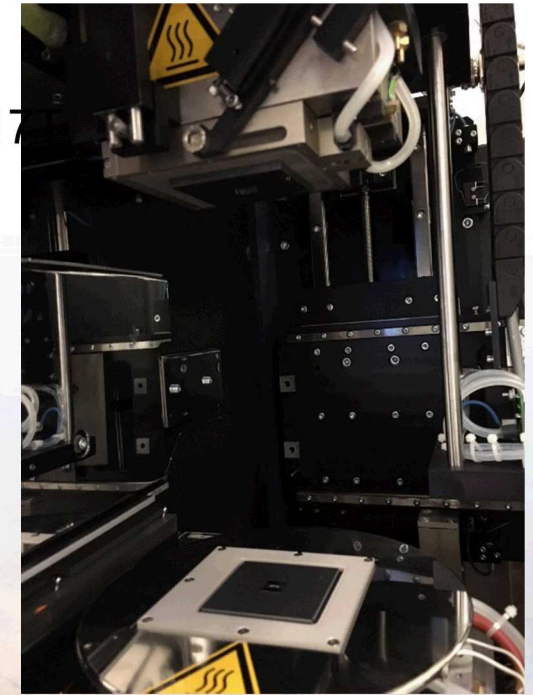
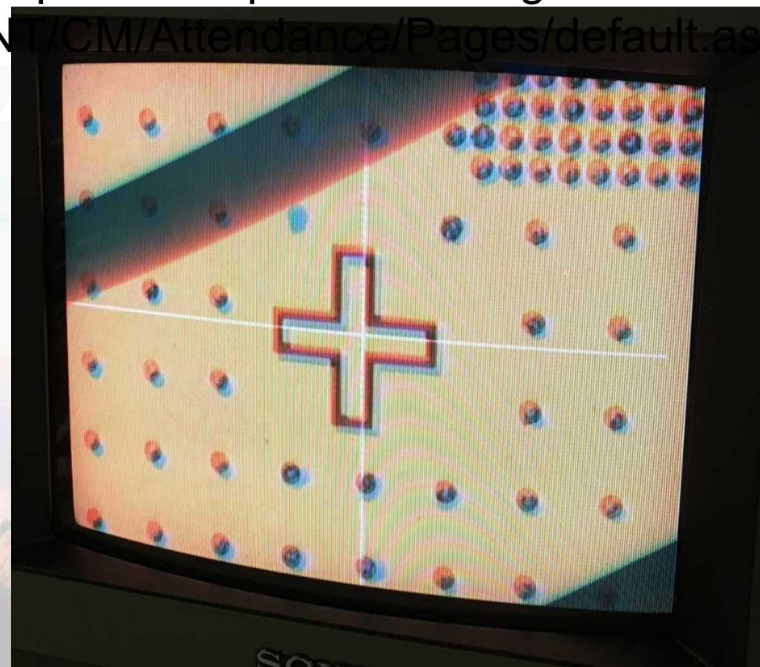


★ Indium bond testing

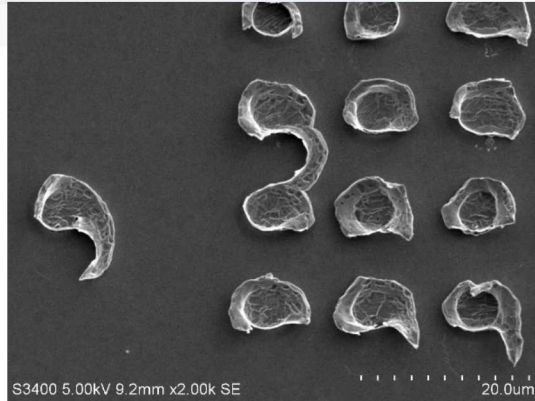
- Acetone, isopropanol clean
- Formic acid clean at Bond 135°C
- Bond 100°C and 10 kg force



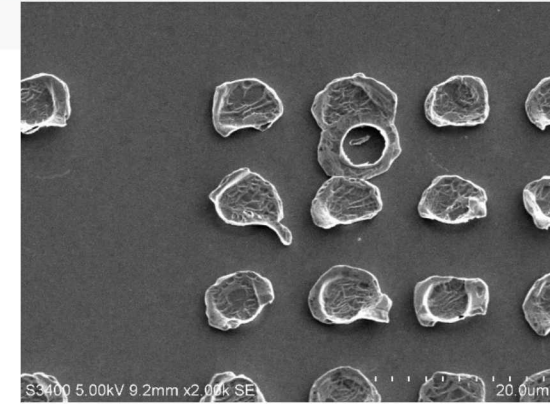
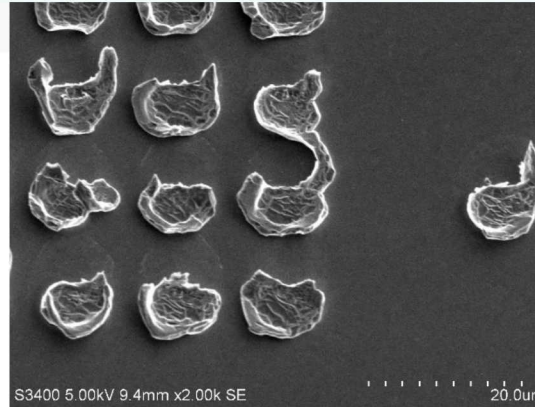
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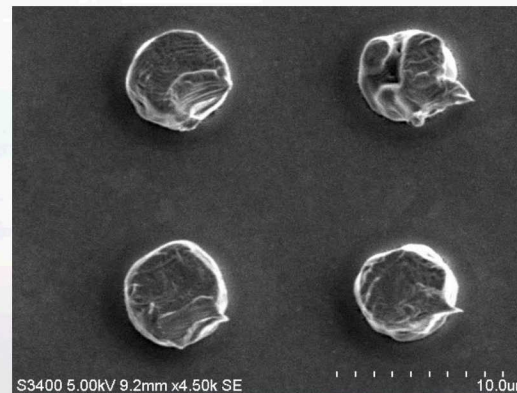
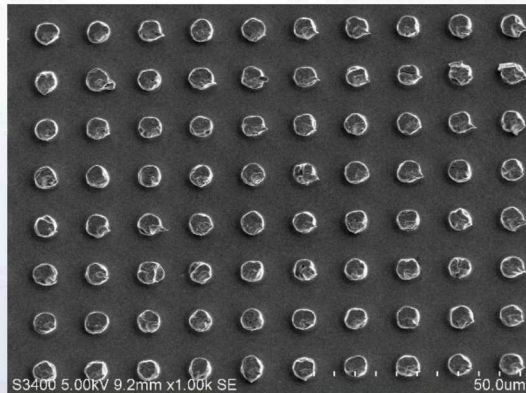
Indium bump bonding



Corresponding sites of bonded die



Corresponding sites



Uniform deformation observed on all or the majority of indium bumps

- Uniform bumping observed
- Further uniformity and bump evaluation in progress
- Taffy pull characteristic observed during debonding the two pieces



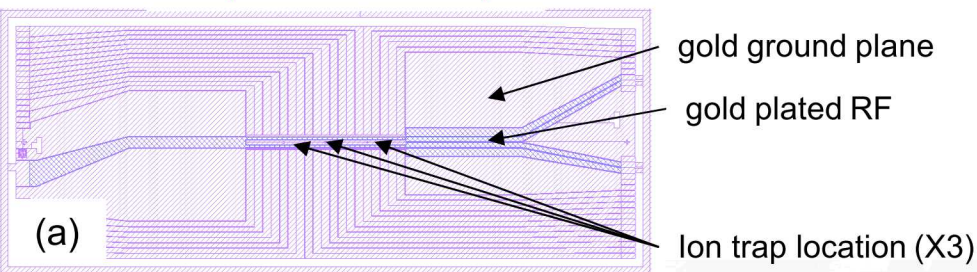
* SNL die 6 bonded to 9 at 100C and 10kg-force after a formic acid reflow at 130C

Generation 3 EPICs fabrication

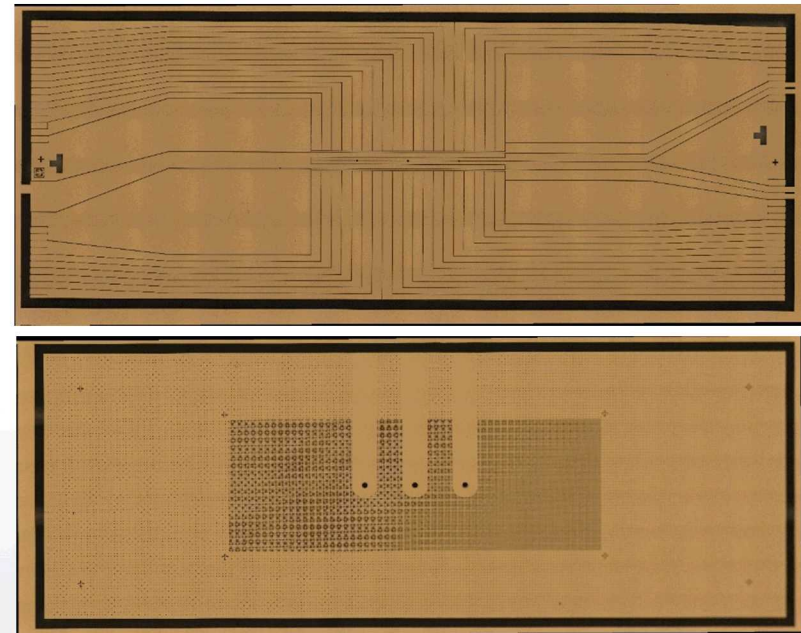
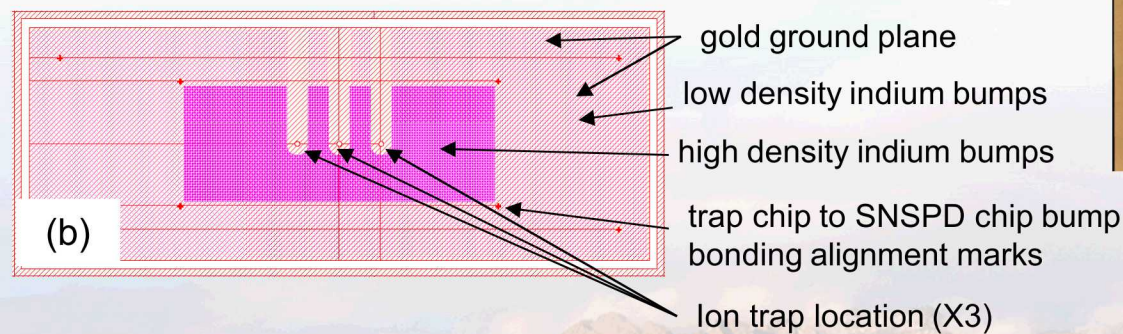
CAD Layout

Microscopy image

Top of Sandia Trap

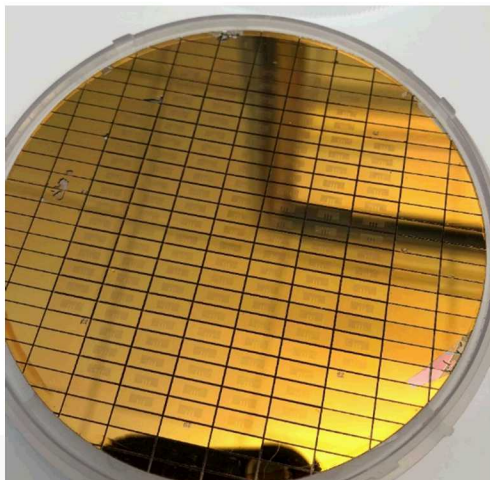


Bottom of Sandia Trap

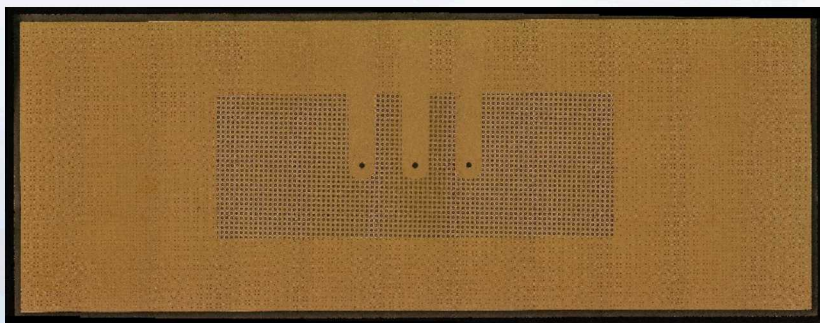


7000 ppm wafer and SNSPD JPL/SNL indium 1/2 wafer

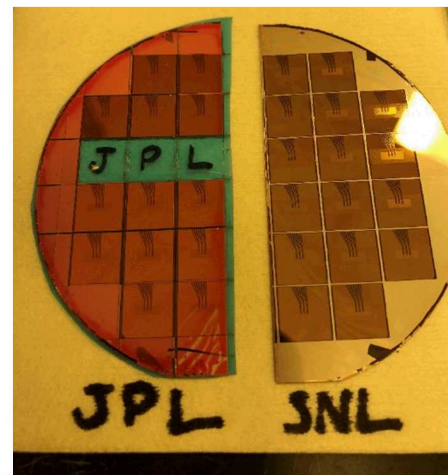
Front side SNL trap fabrication



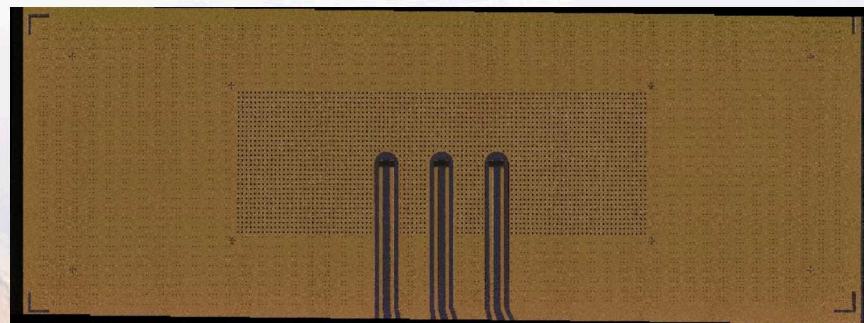
SNL device die



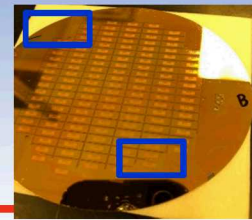
SNSPD JPL & SNL Indium



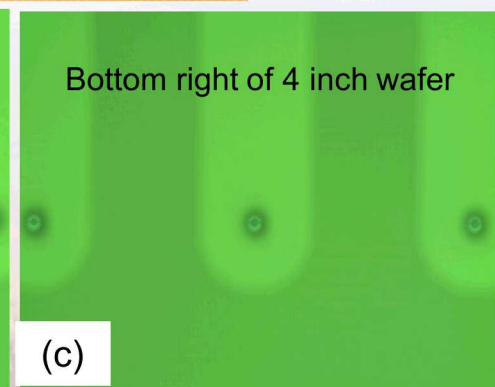
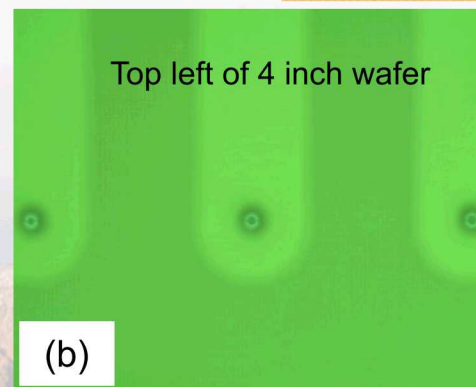
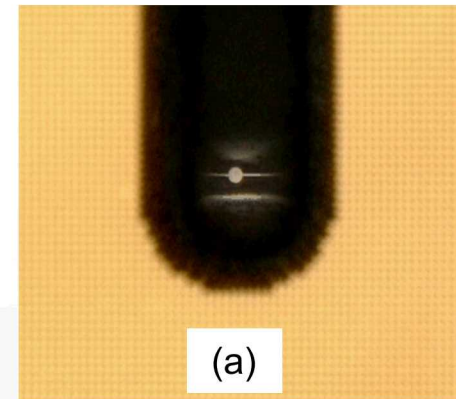
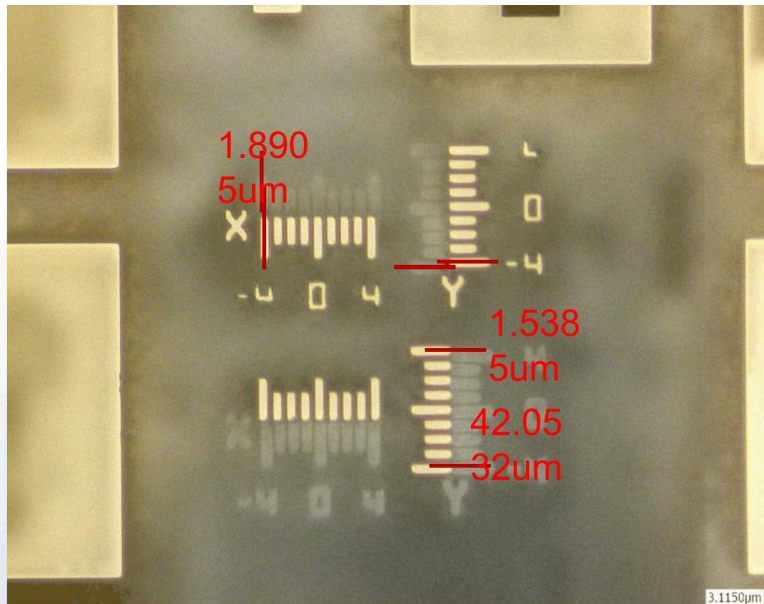
JPL device die



Alignment



- Tested alignment on test substrates
- Confirmed ability to align ± 2 micron
- 7000 ppm device substrate after full fabrication





SEM Images SNL trap chip



SNL Deliveries

- Delivered 4 detector die packaged without trap for testing
- Delivered 4 generation 2 devices fully packaged

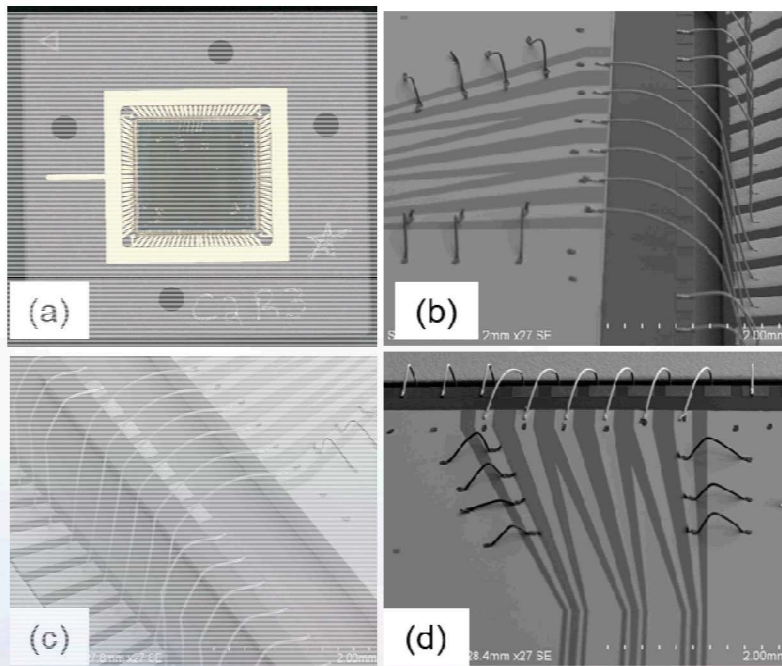


Figure 1: (a) top view of a packaged SNSPD delivery to Duke (b,c,d) SEM side profile view showing wire bonding done to CPGA and to ground plan of chip

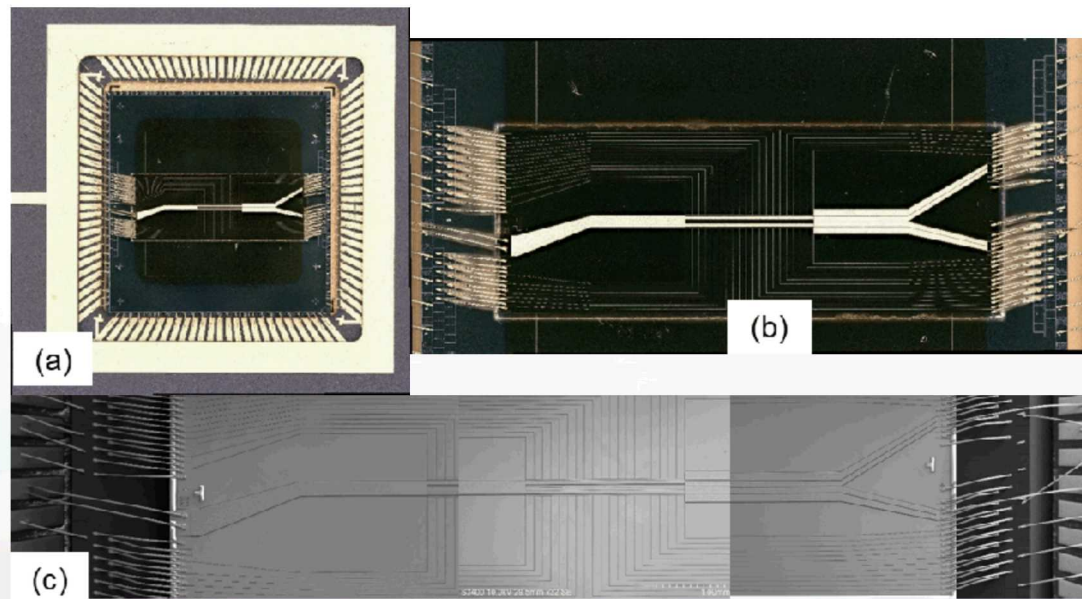


Figure 2: (a) top view of gen 2 packaged trap (b) magnified view of trap die (c) top SEM view of gen 2 trap