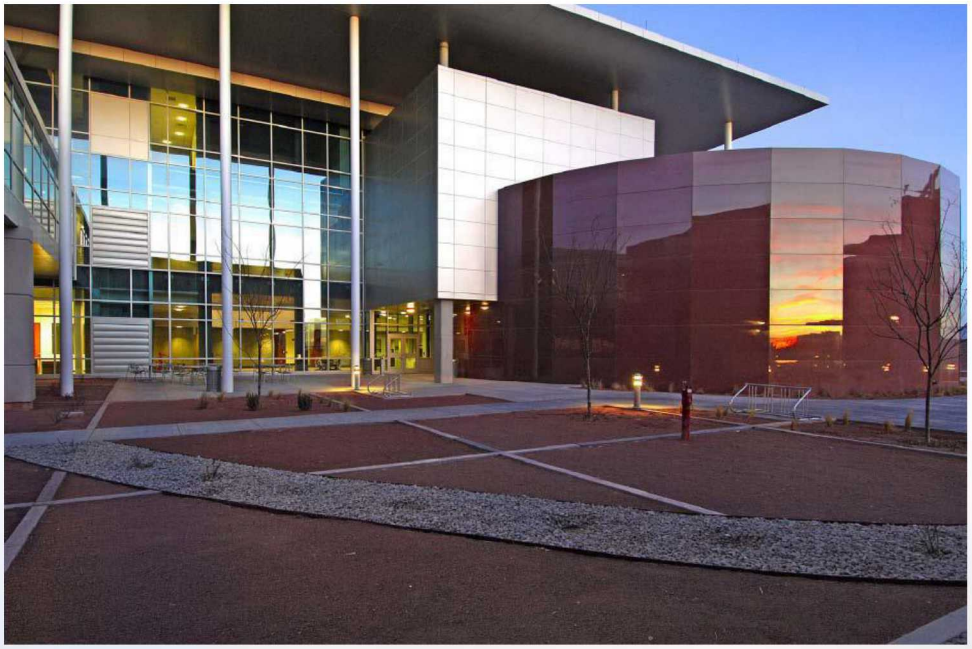
Metal Micromachining Team

SAND2019-3579PE

CAMD user's meeting April 29, 2016



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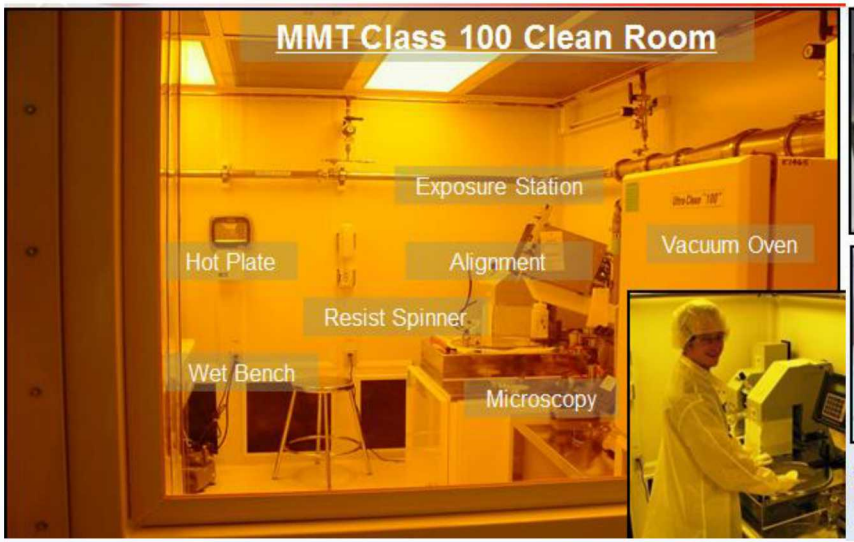
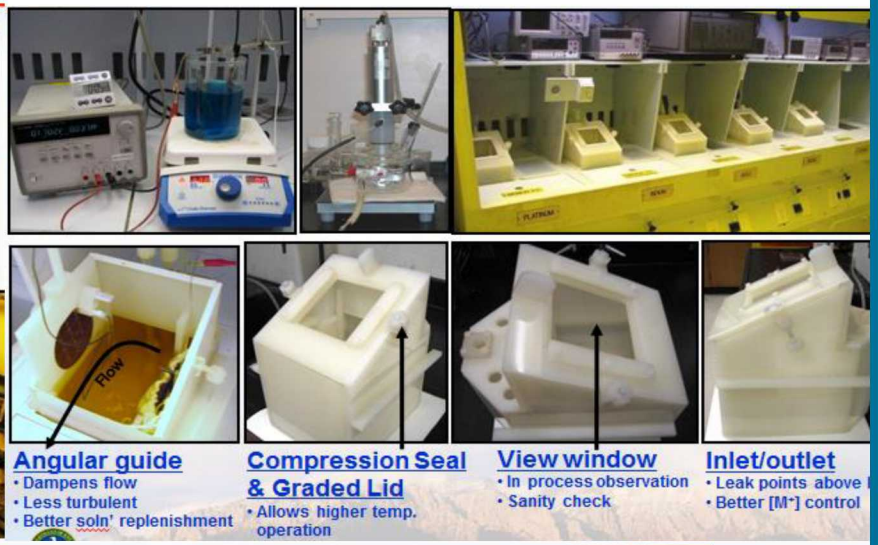
Lithography



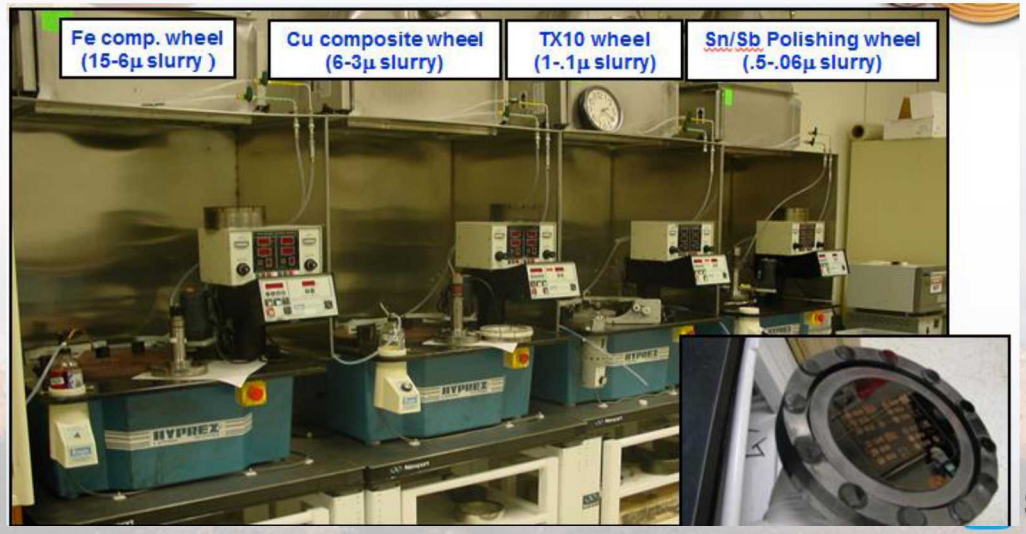
Electroplating



Chemistries

1. Hard Gold
2. Soft Gold
3. Copper
4. Nickel
5. Indium
6. Platinum
7. Monel
8. Kovar
9. Permalloy
10. NiW
11. BiTe
12. SbTe
13. PbTe
14. Te
15. PbS
16. PbSe
17. CoFe

Chemical Mechanical Polishing (CMP)



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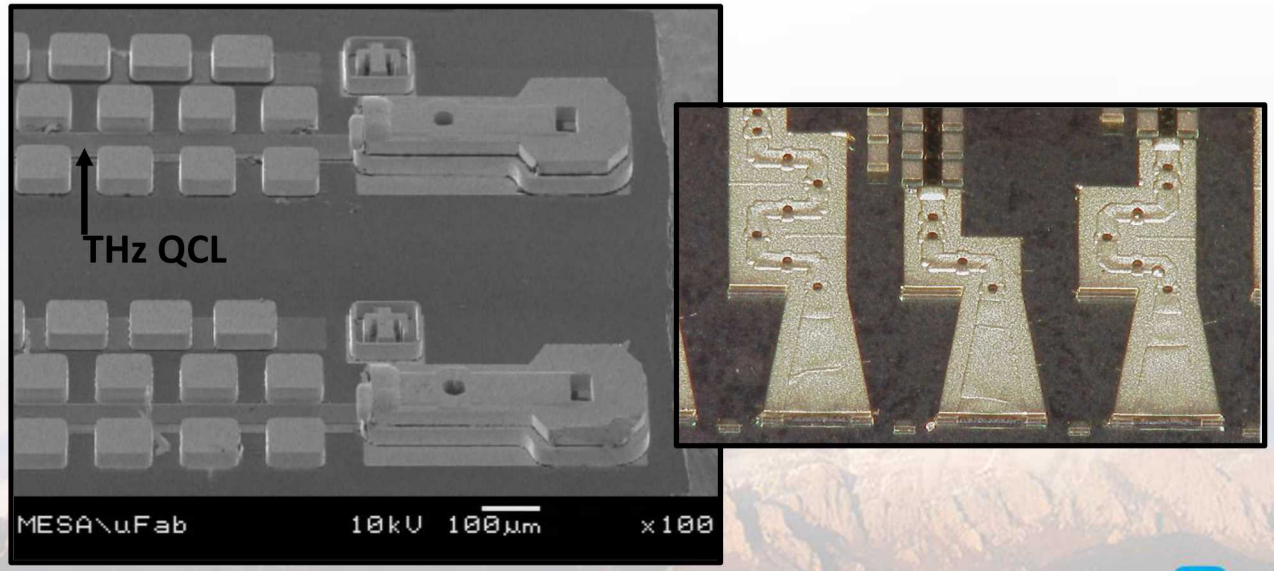
Plating Applications

Masking achieved through unique fixturing and controlled polymer deposition

3-D Integrated Gold THz Waveguides



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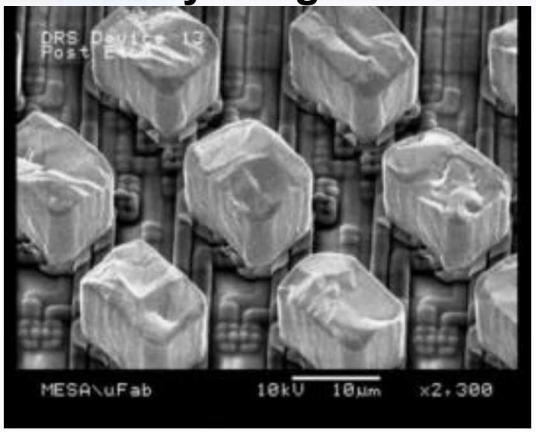
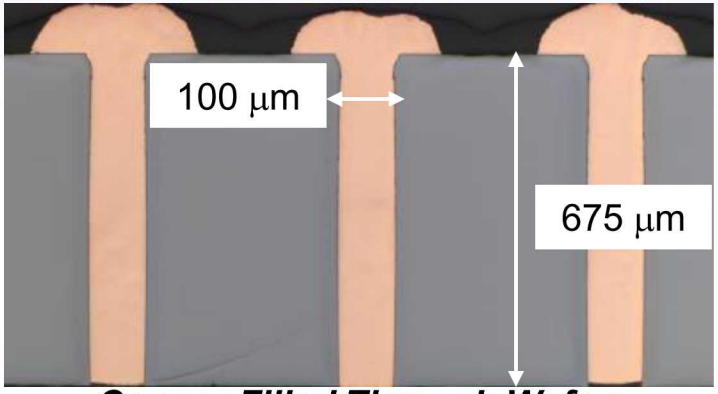
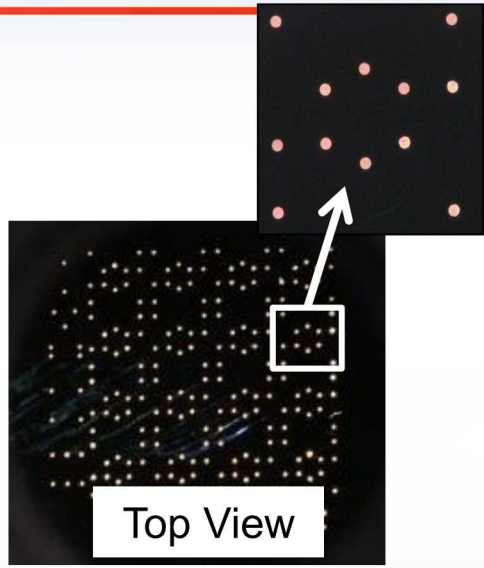
Indium Bumps for Focal Plane Array Integration



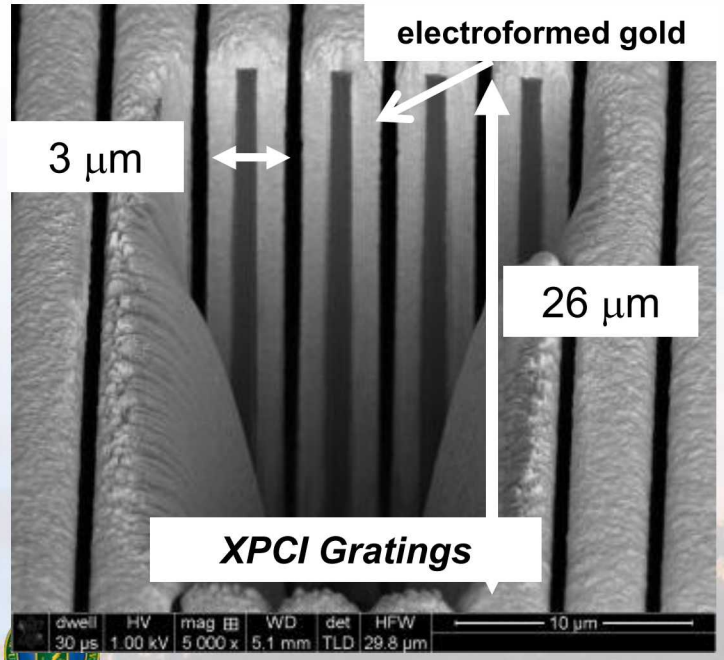
Copper TSV's

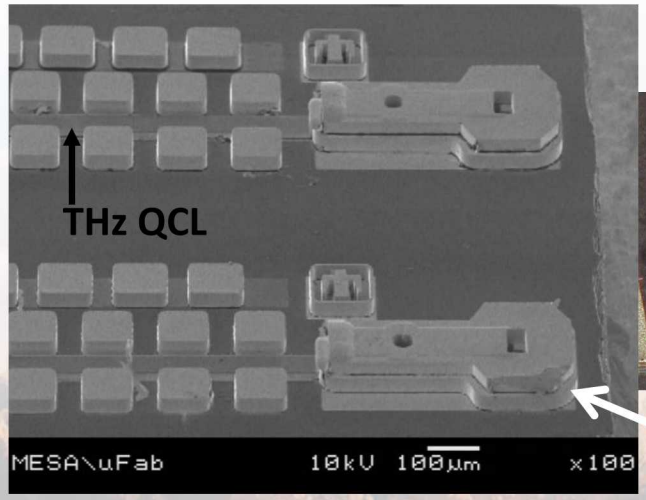


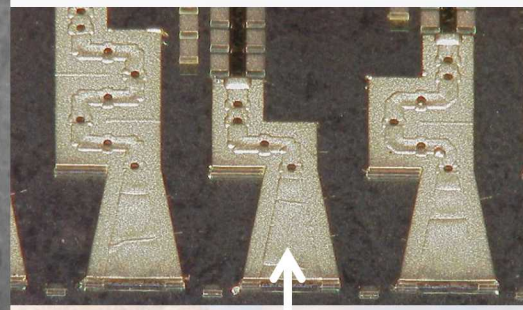
Copper Filled Through Wafer Silicon Vias



3-D Integrated Gold THz Waveguides







2 layer electroformed Gold

Trapped ions as a quantum computing platform

Classical computer

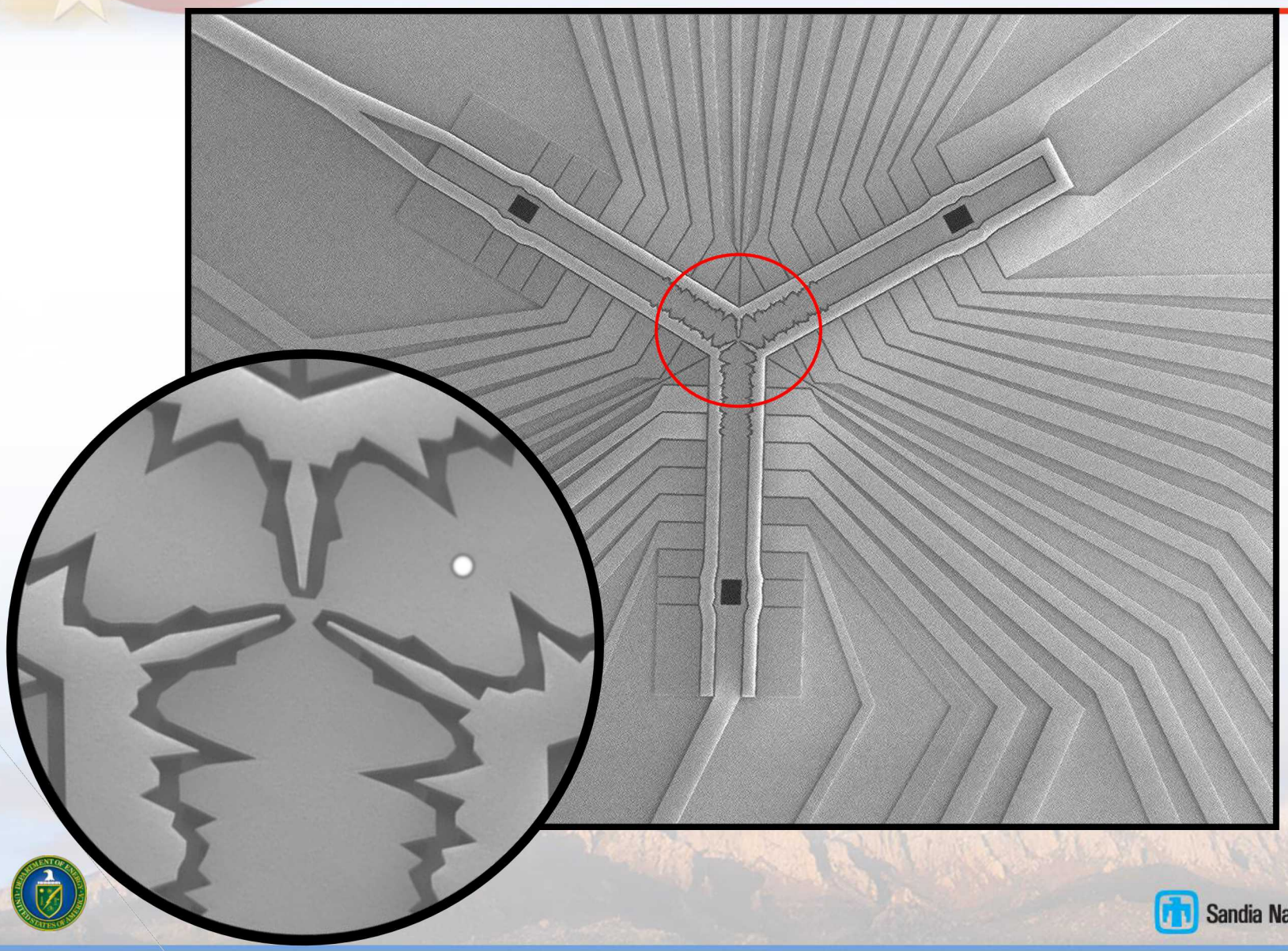
- Single states:
  - 0_a0_b or 0_a1_b or 1_a0_b or 1_a1_b
- Only local operations

Quantum computer

- **Superposition states:**
  - $0_a0_b+0_a1_b+1_a0_b+1_a1_b$
- **Entanglement (non-classical states)**

Exponential speedup for ***particular*** algorithms
(most notably Shor's factoring algorithm)

Y-Junction Trap shuttling through the junction



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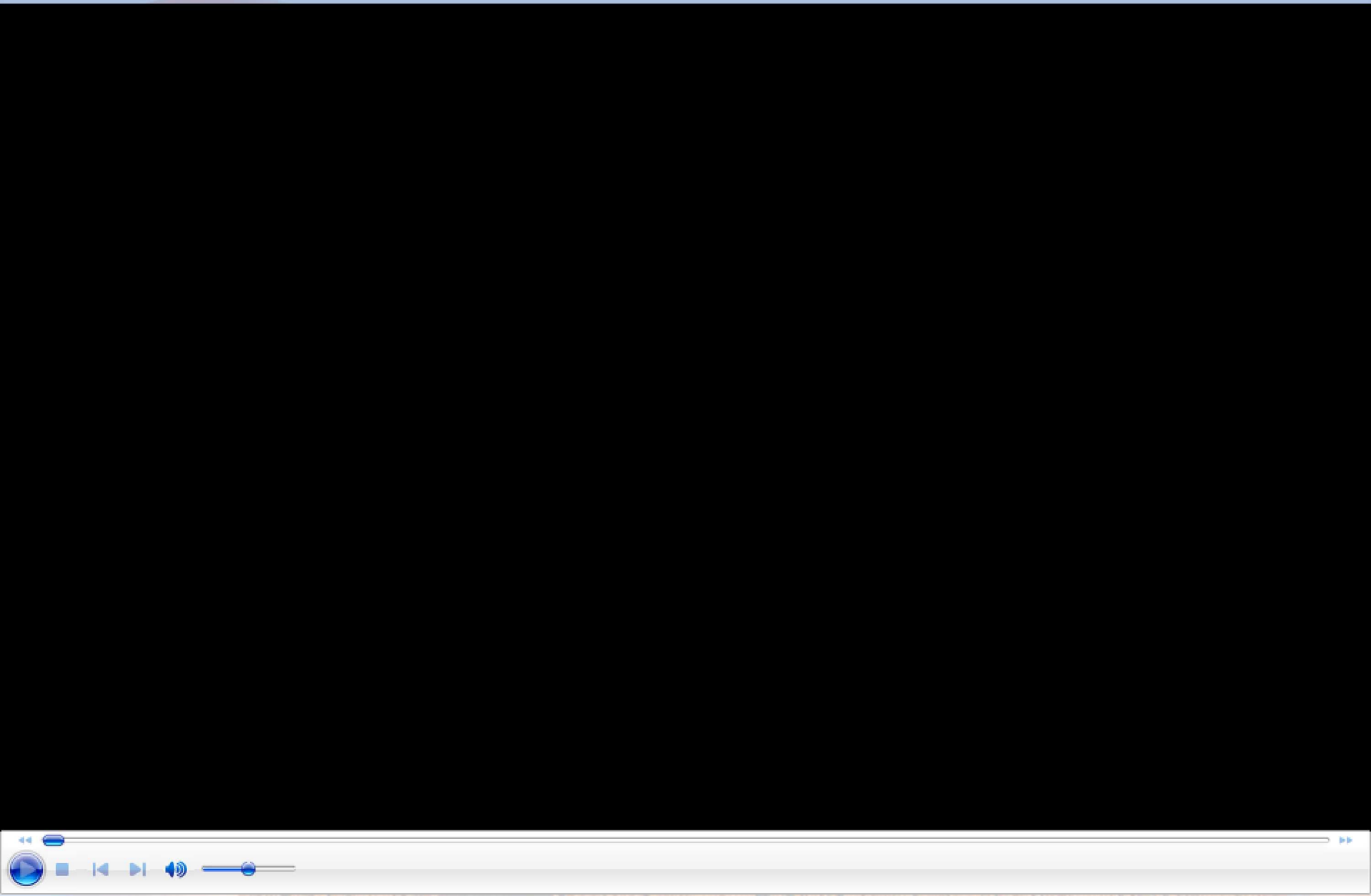

Animation courtesy of Dan Stick

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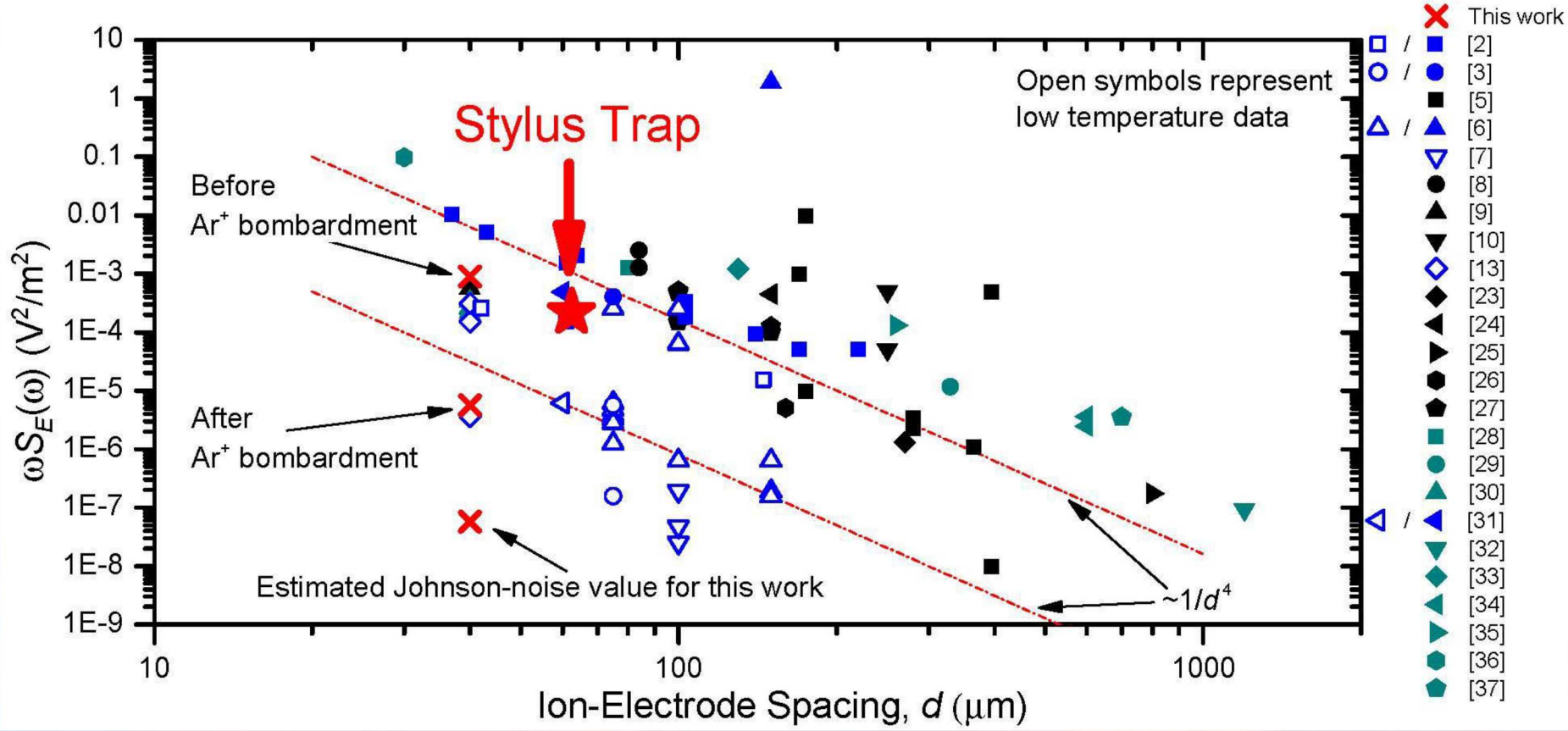
Anomalous Heating Rate Experiments



National Institute of Standards and Technology, Boulder, CO 80305, USA David P. Pappas and David J. Wineland

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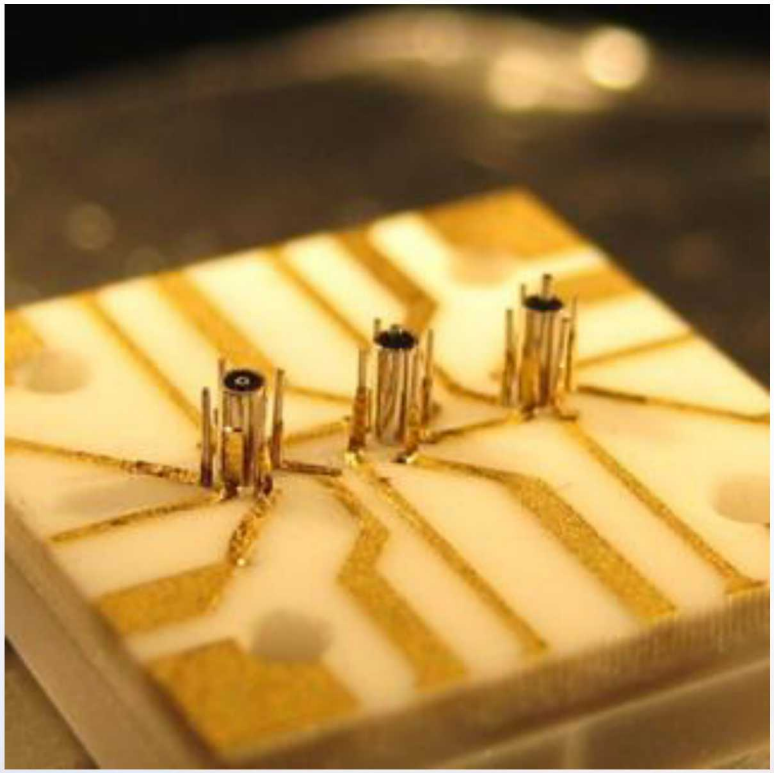
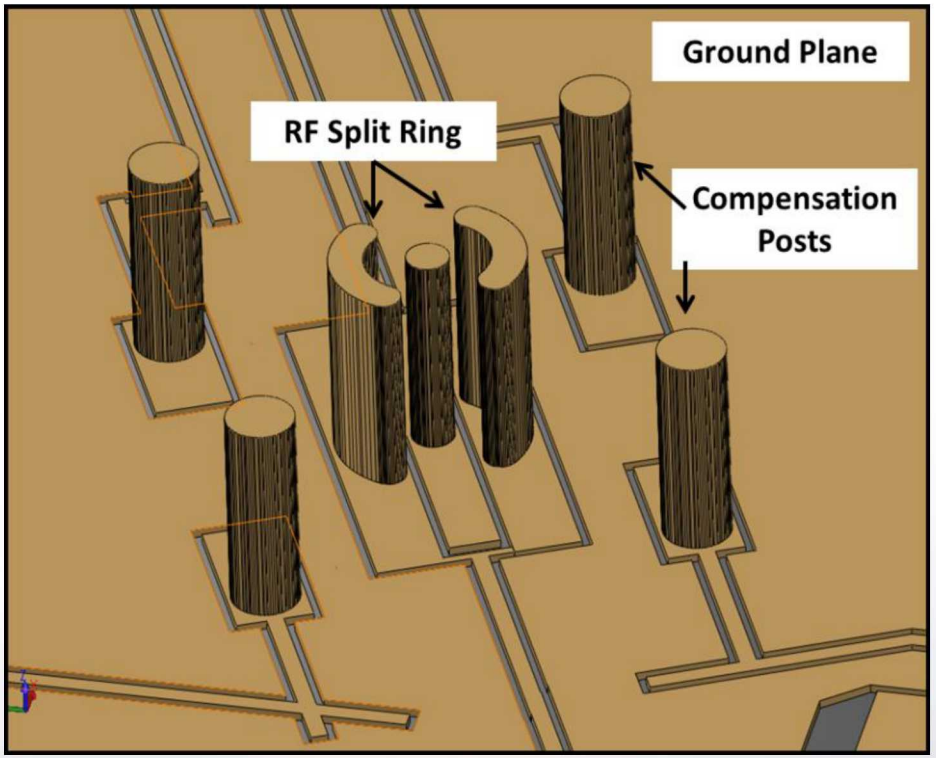
Stylus Ion Trap Background

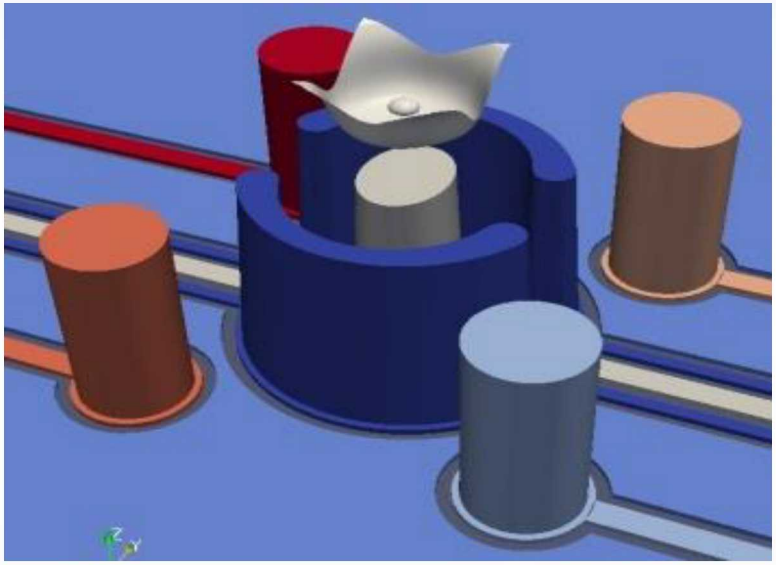


R. Maiwald, D. Leibfried, J. Britton, J. C. Bergquist, G. Leuchs, and D. J. Wineland, Nature Physics **5**, 551 (2009).



Model of Microfabricated Sylus Ion Trap

Microfabricated Stylus Ion Trap



BEM simulation results showing center ground post, RF biased ring, and four compensation posts. The two surfaces show example equipotentials for a 25Mg+.

	Measured values Nominal U_{trap}=100 V	BEM modeling results Fit U_{trap} = 85 V	
		Symmetric center electrode $A_{electrode}$=0	Asymmetric center electrode $A_{electrode}$=0.11
Ion height (μm)	60(15)	64.2	62.2
Well depth (meV)	Not measured	86	95
x motional frequency (MHz) f_x	4.03(5)	3.35	4.09
y motional frequency (MHz) f_y	4.17(5)	4.078	4.34
z motional frequency (MHz) f_z	8.15(5)	7.58	8.63
x-y frequency asymmetry, A_f	0.017(9)	0.194	0.031

Micro-fabricated Stylus Ion Traps, 2013 AIP, Review of Scientific Inst.
C.L. Arrington, K.S. McKay, D.P. Pappas, D.J. Wineland,

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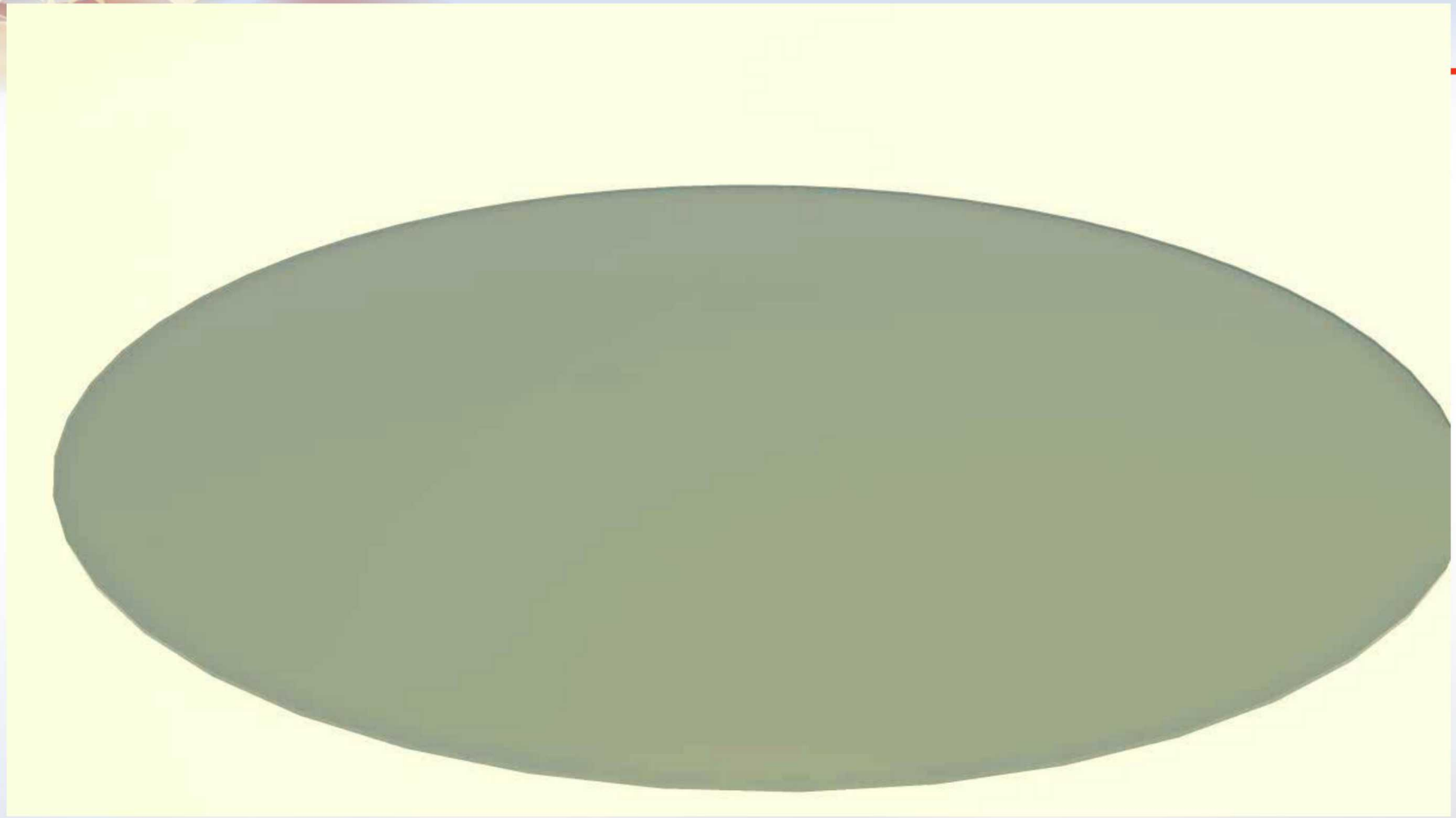
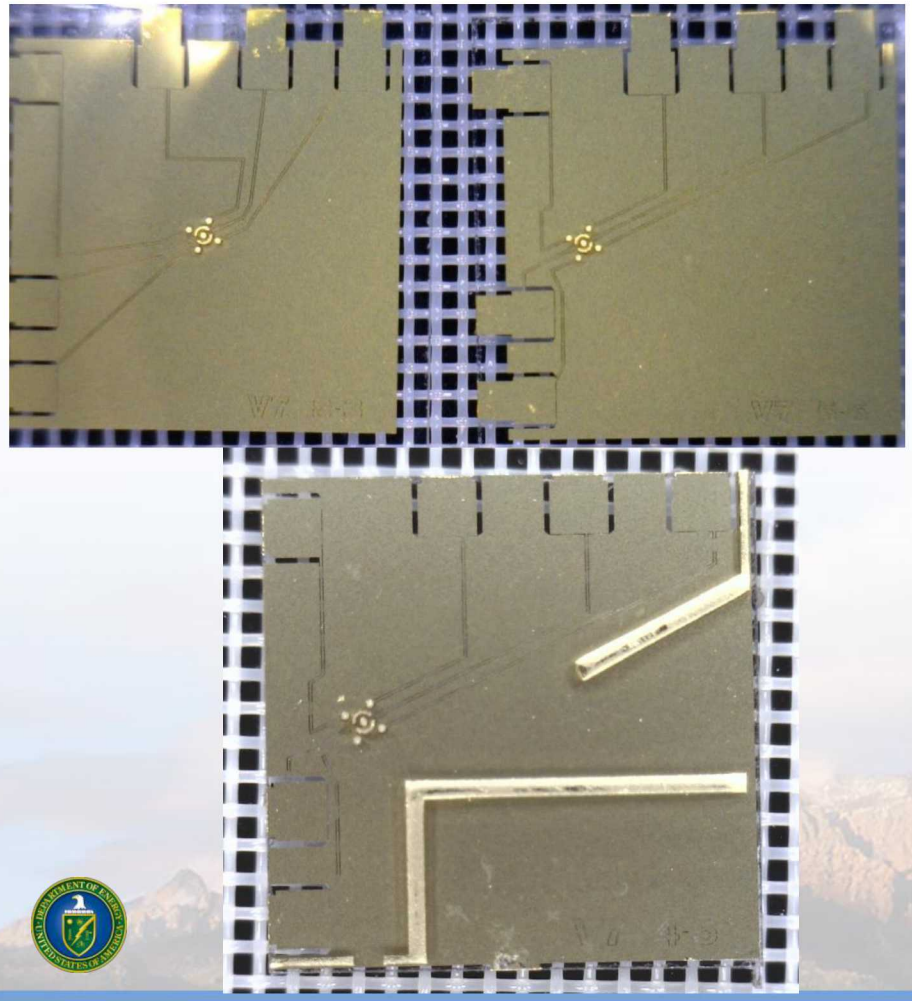


Animation courtesy of , Carol Alynn Payne, Lozanne M Chavez, & Johanna Hartenberger.

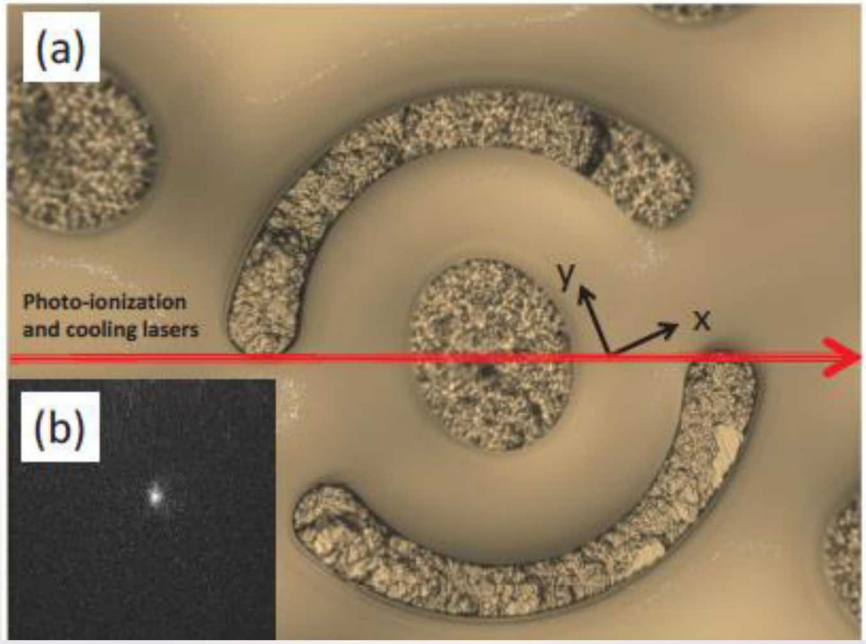
Generation 1 Stylus Traps

Delivery May 2012

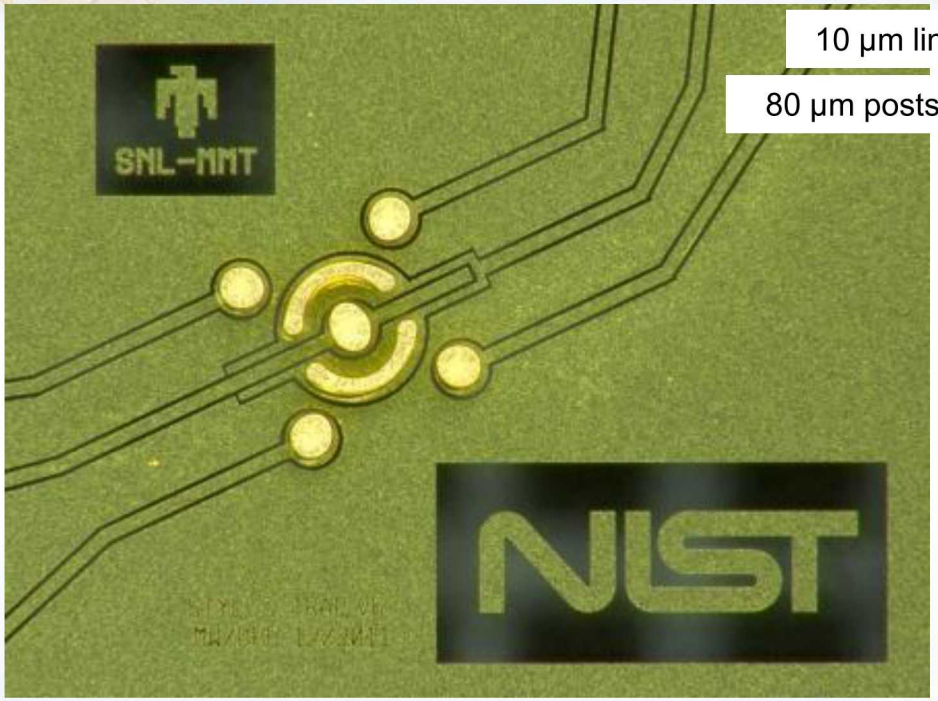
Asymmetrical and center located traps



Resist swelling causing deformed structures

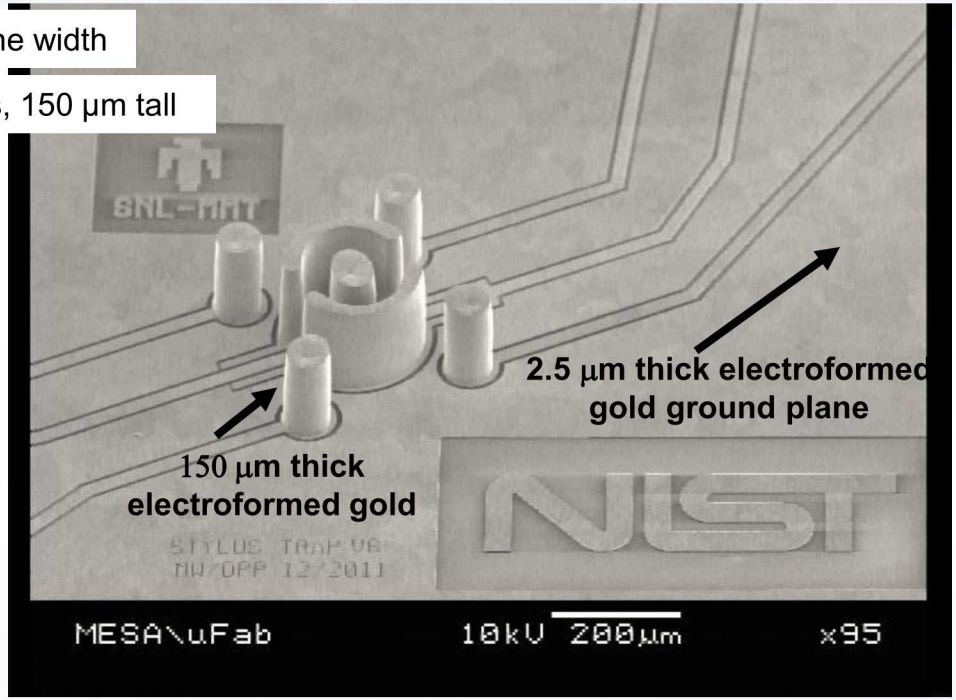


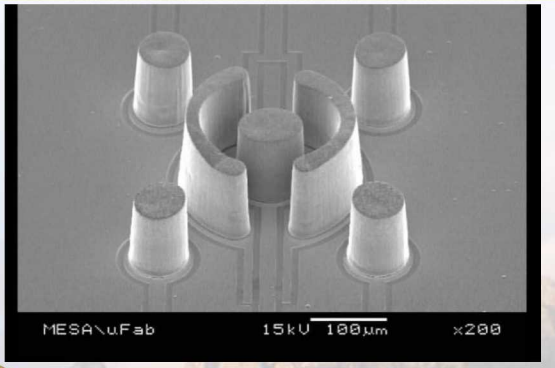
Generation 1

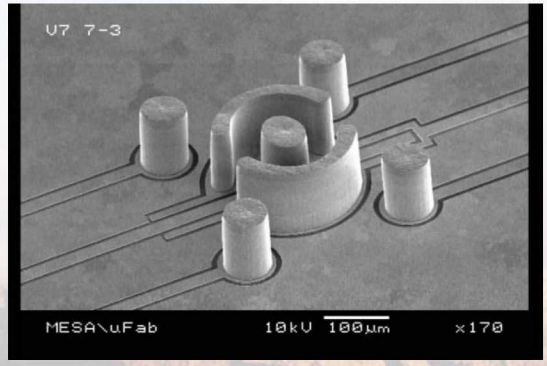


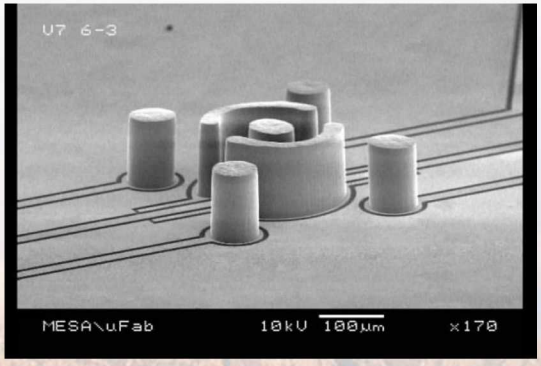
10 µm line width

80 µm posts, 150 µm tall

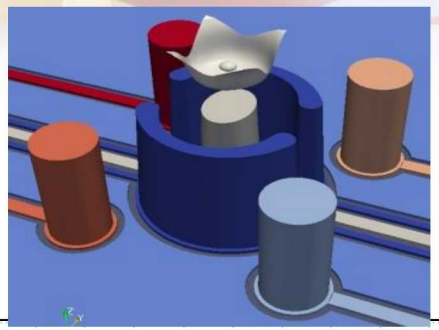




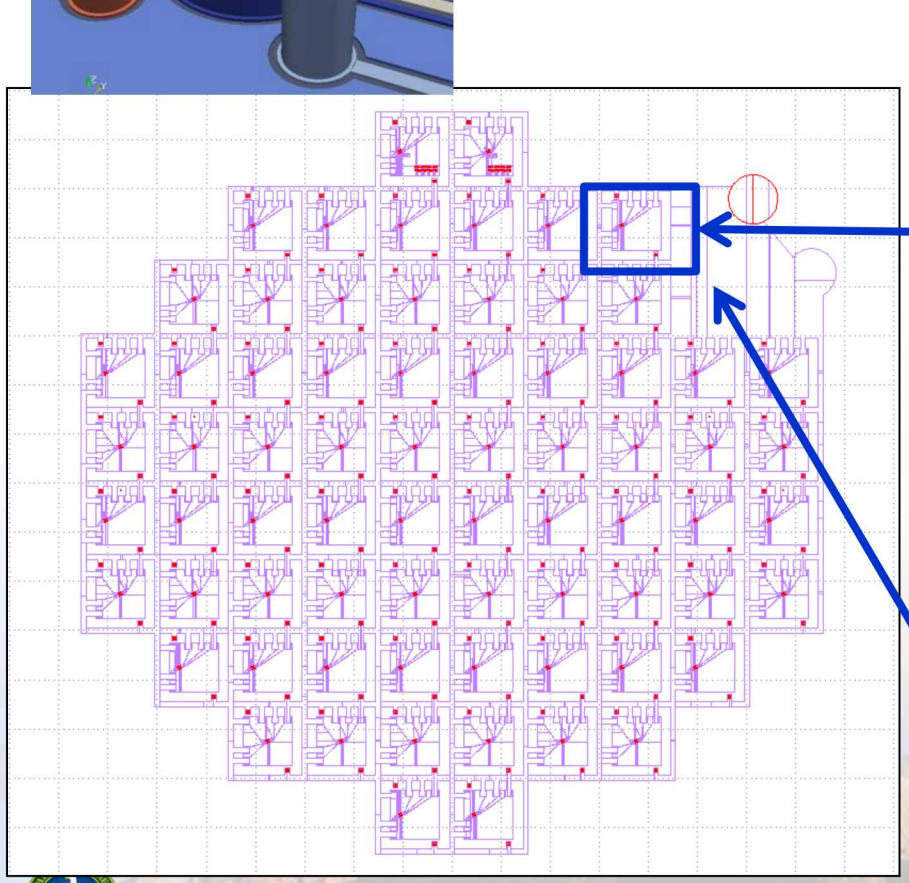


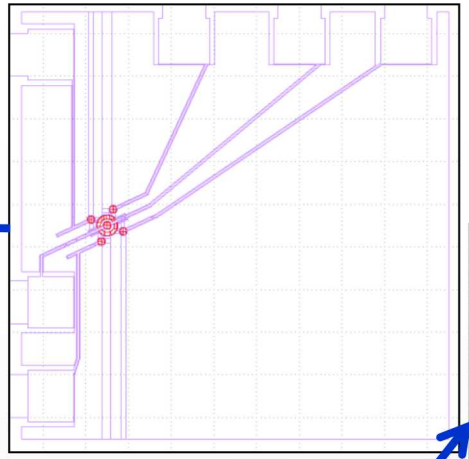


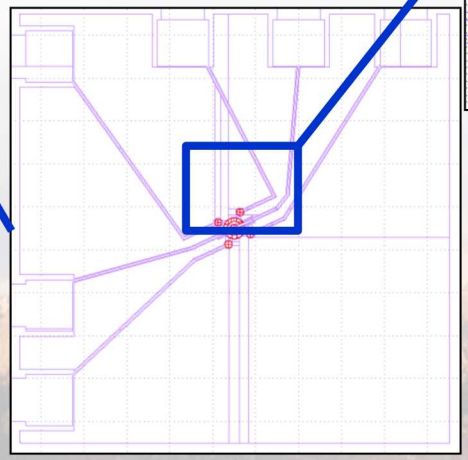
Generation 2 Mask Design

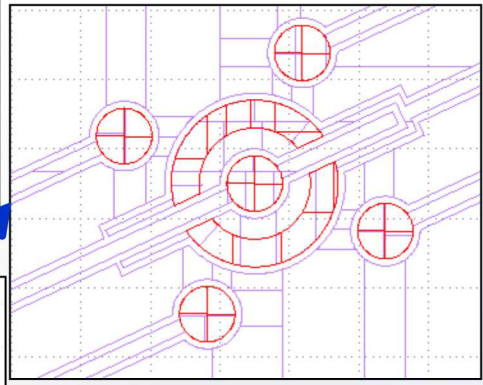


1. Layer 1 AZ 4330 postive resist
2. Layer 2 KMPR negative resist









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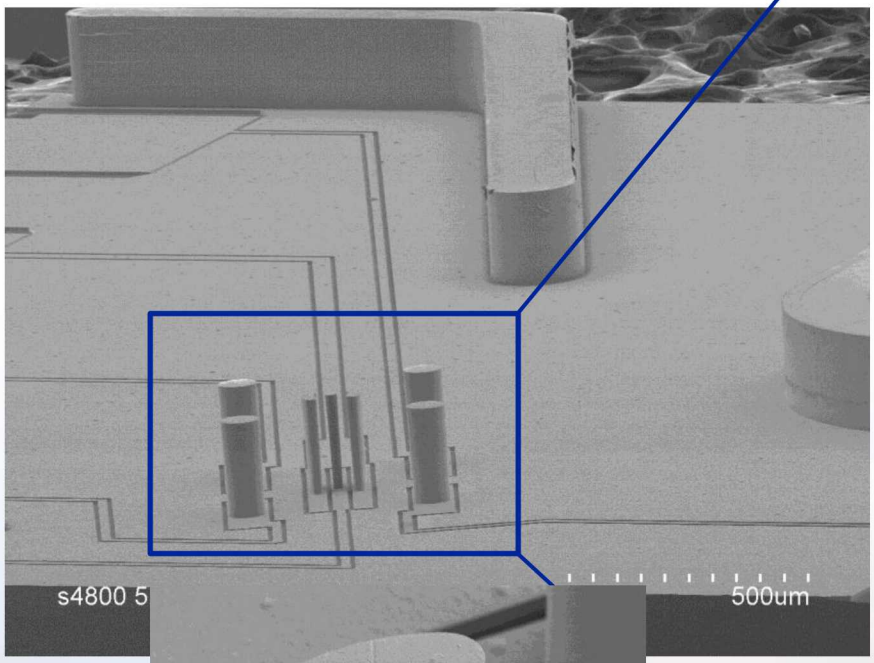
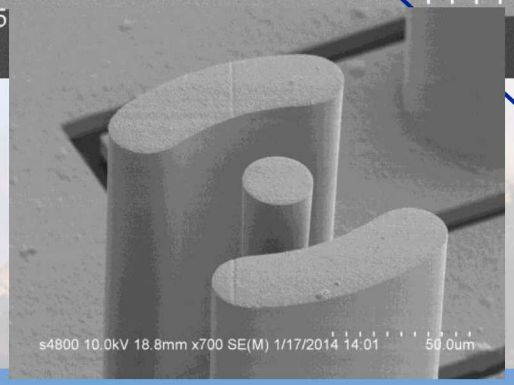
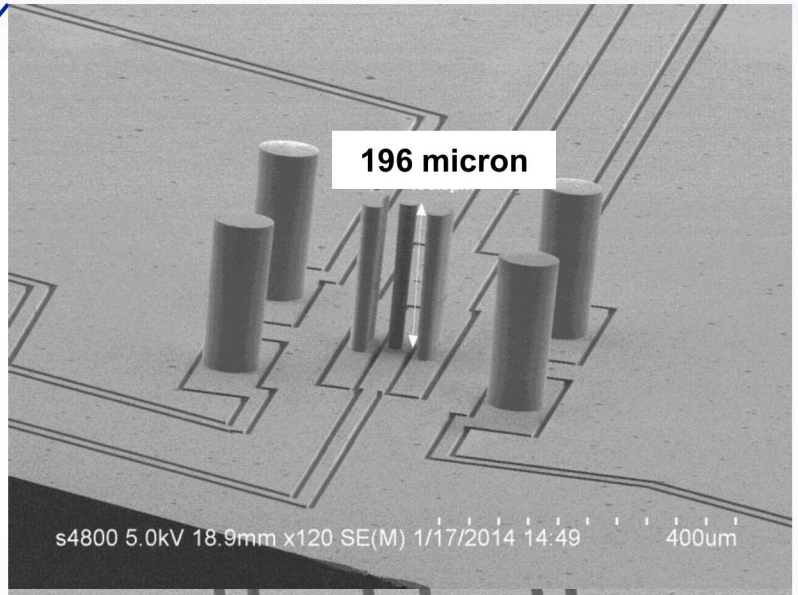
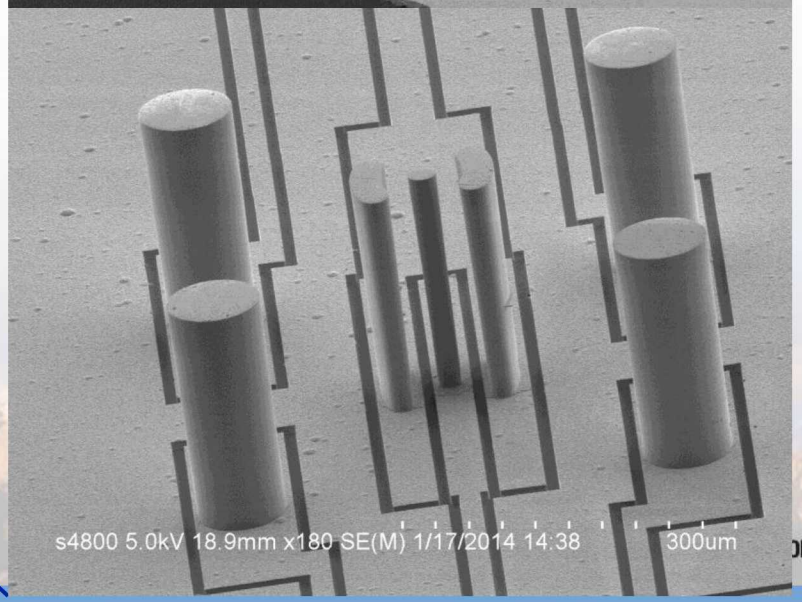
Generation 2 LIGA Traps

- 25-25-25 μm die
- 200 μm layer 2 feature height
- Improved sidewall profile
- Reduced PR swelling

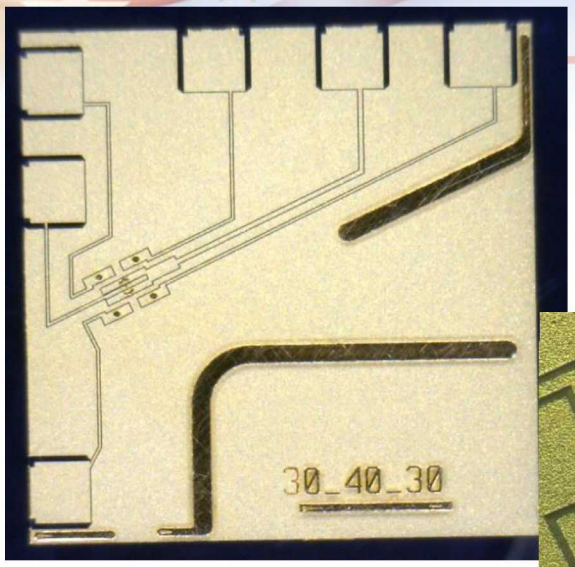


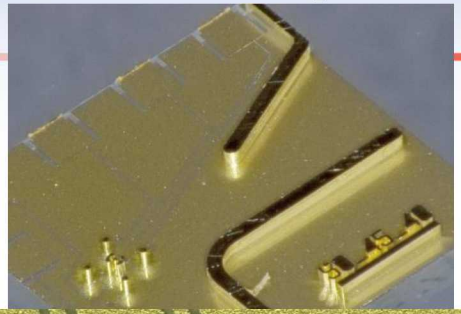


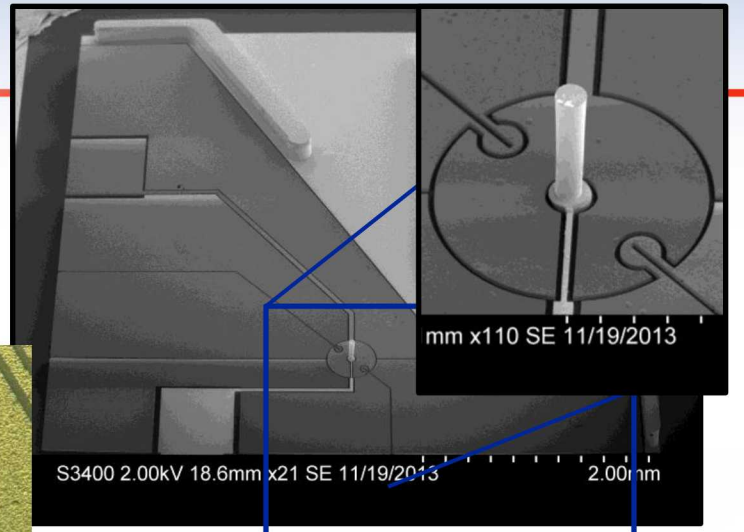


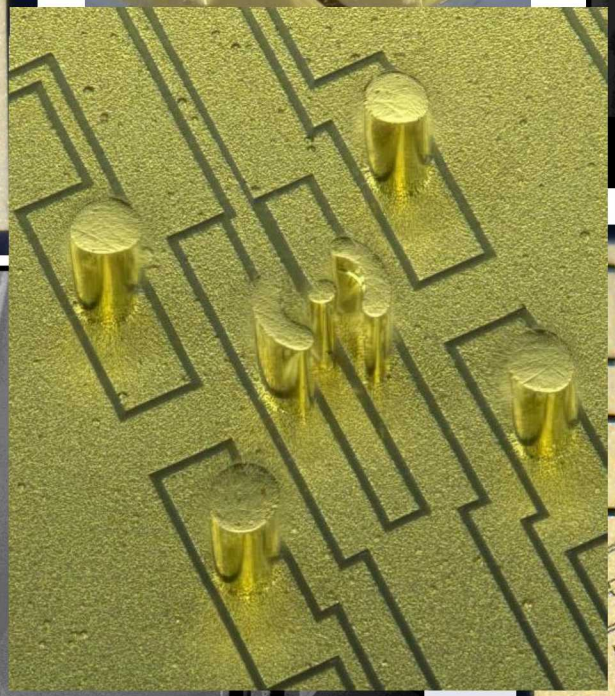


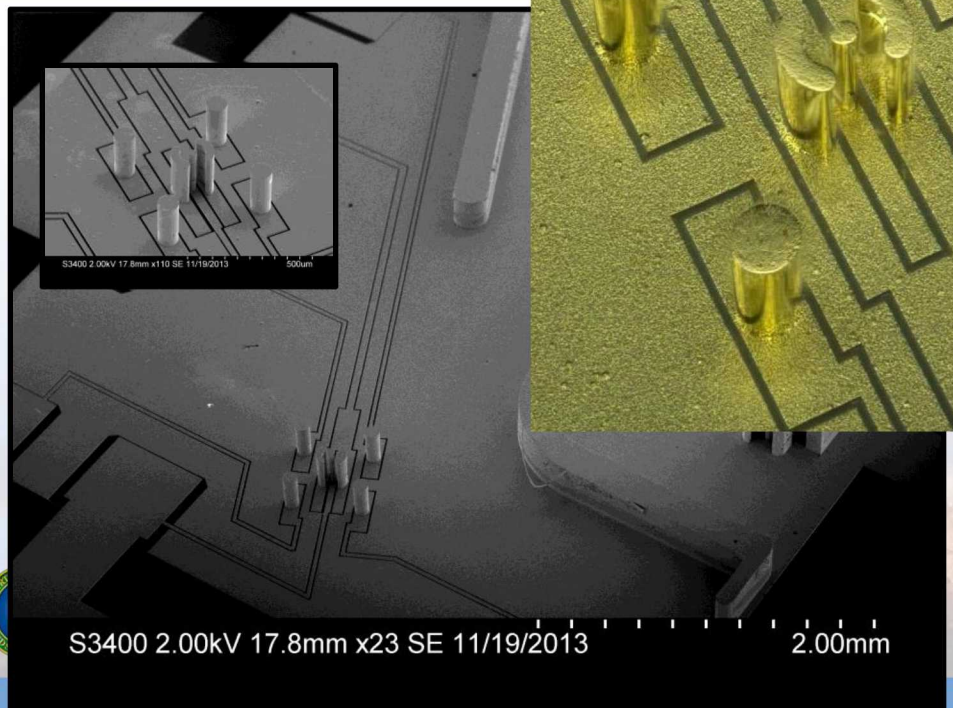
Generation 2 LIGA Traps

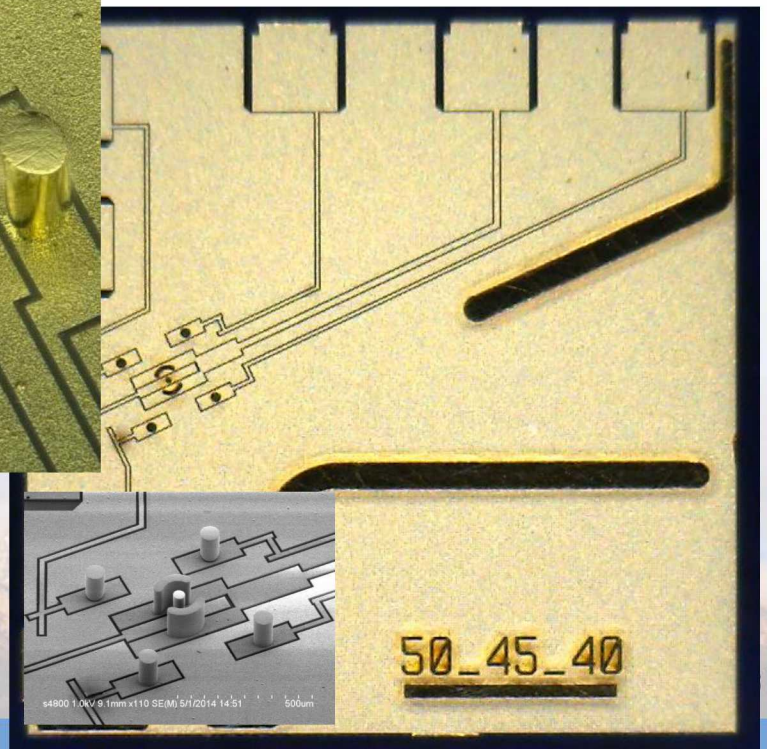






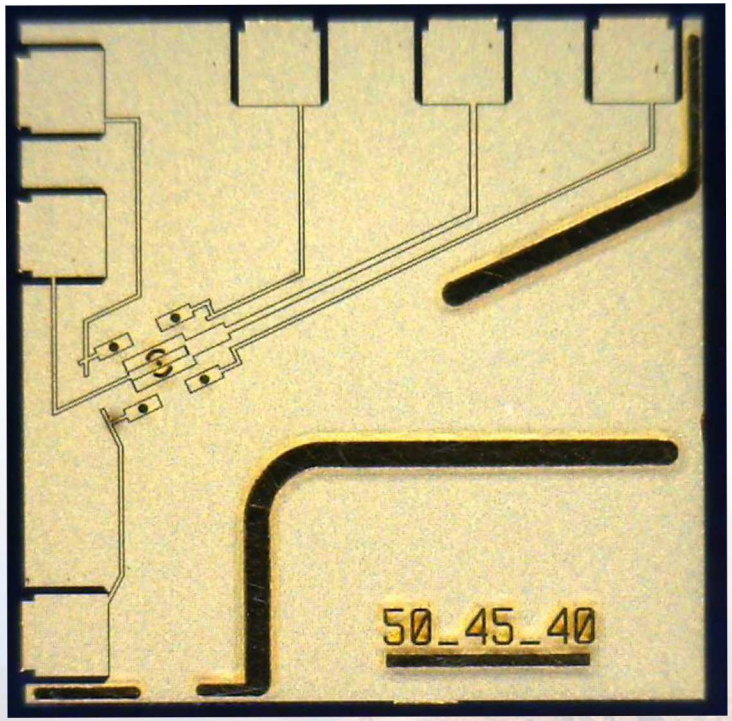


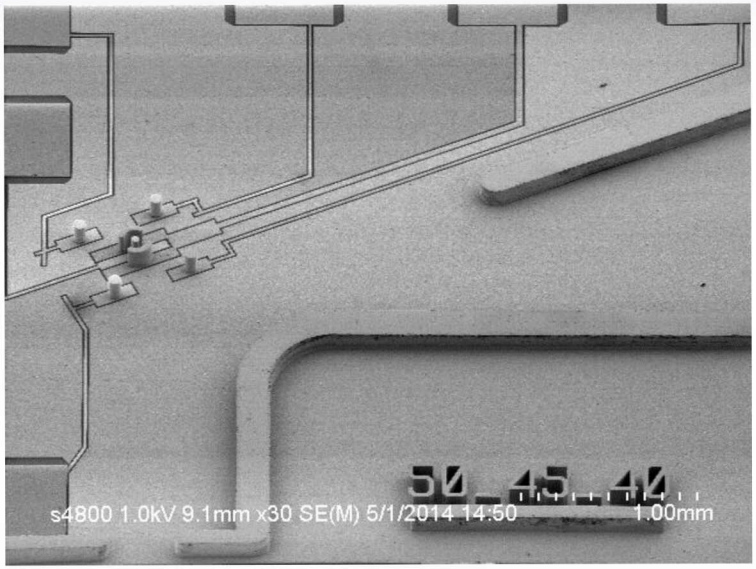


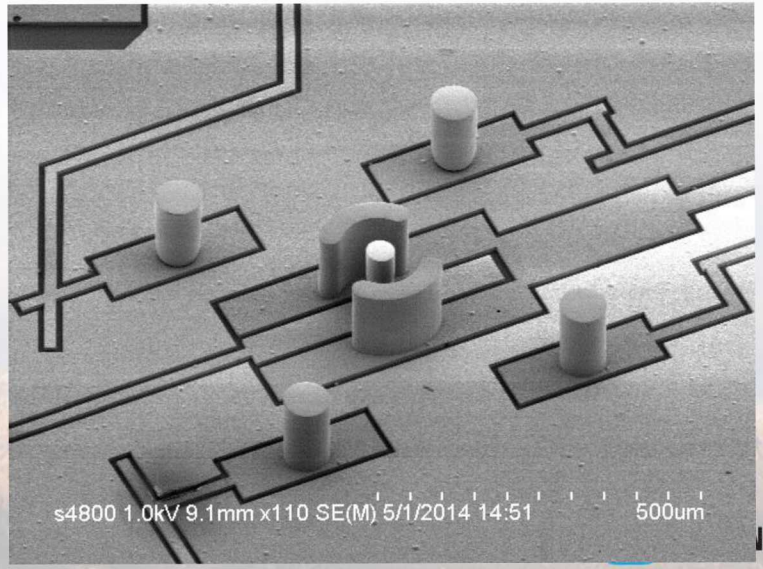


Generation 2 LIGA Traps

- M1- 10 μm
- M2- 150 μm
- 50-45-40 features

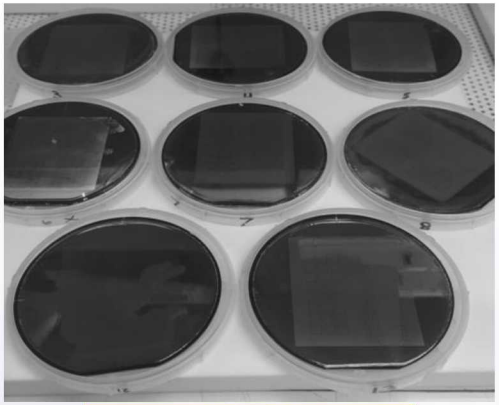


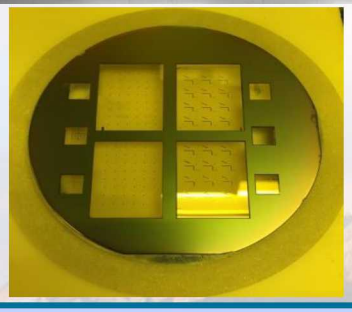




Generation 3 LIGA Traps

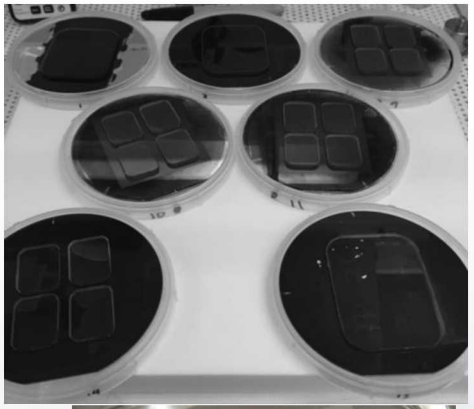
- **Recent key accomplishment(s):**
  - ✓ New Design
    - ✓ CAMD exposed and developed 2 of 7 total PMMA wafers, SNL gold plated, PMMA removed, SEM images taken (Slides 2-7)
    - ✓ SUEX wafers x-ray exposed, but delaminated from Titanium oxide
    - ✓ Striped all SUEX wafers, cleaned, laminated SUEX to bare gold, and sent to CAMD
    - ✓ Two non-Titanium oxide wafers were exposed, developed, and returned to Sandia. (Slide 8)
  - ✓ Old design
    - ✓ wafer found cracked, but with usable 60 micron die in one quadrant
    - ✓ gold plated the PMMA mold, polished, diced, and in cleaning process now to yield 3 (60 micron) die (Slide 9-12)

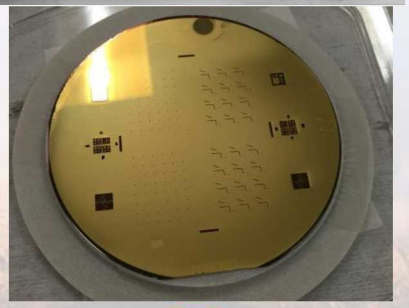




SUEX **X-ray mask**

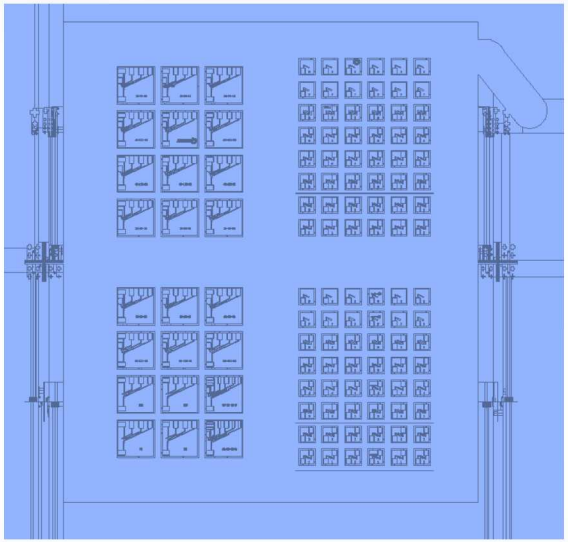
Layer 1 gold ~5 μm **height** with bonded **SUEX (on left) and PMMA (on right)**

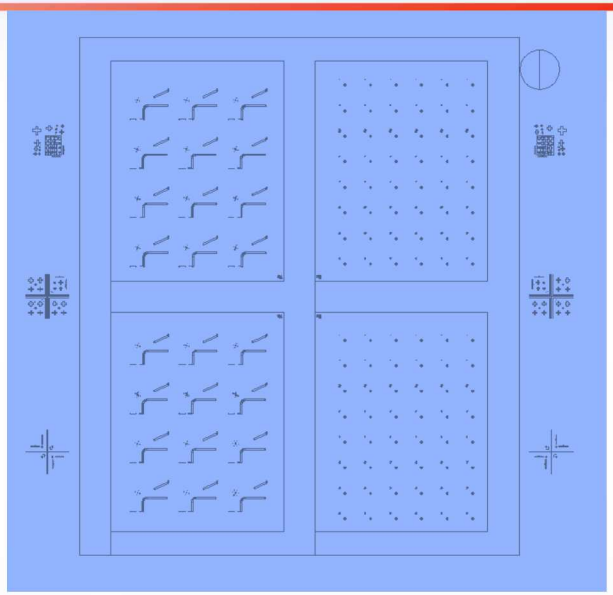


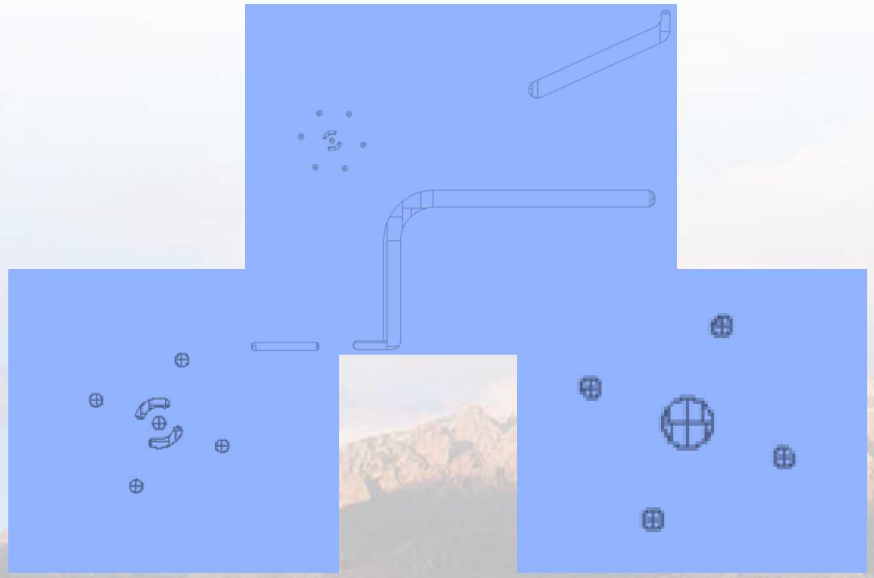


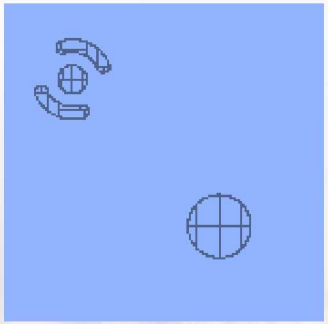
PMMA **X-ray mask**

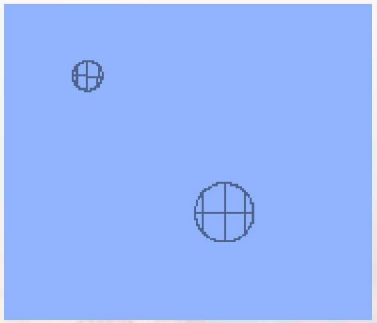
Mask Changes



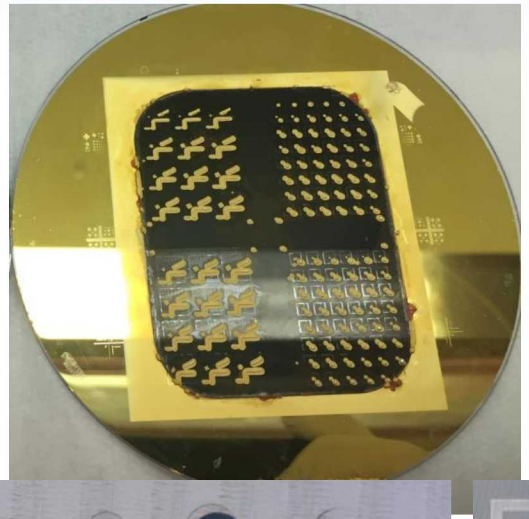






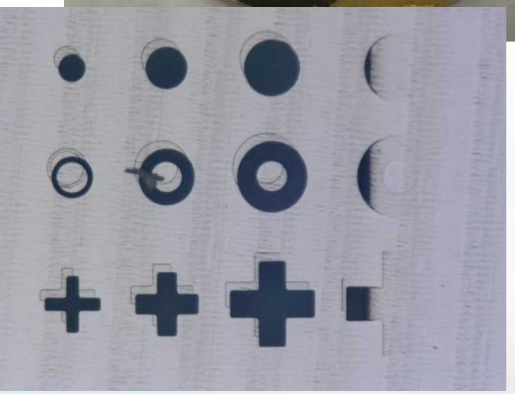


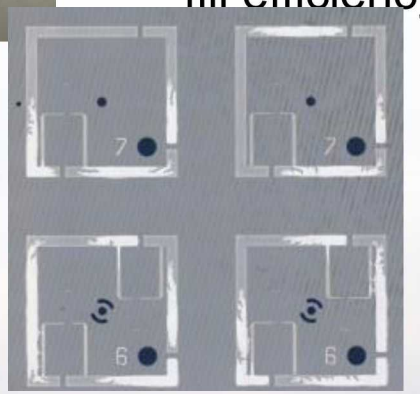
PMMA Wafer 1



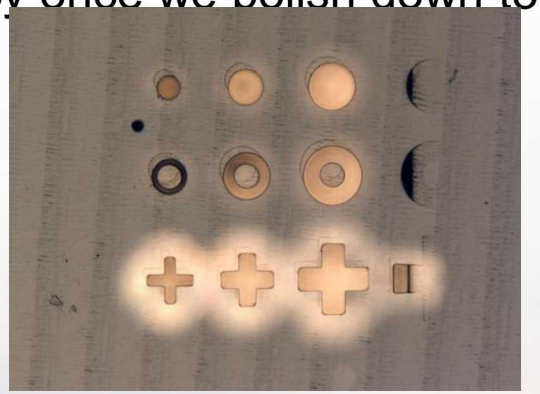
Wafer 1

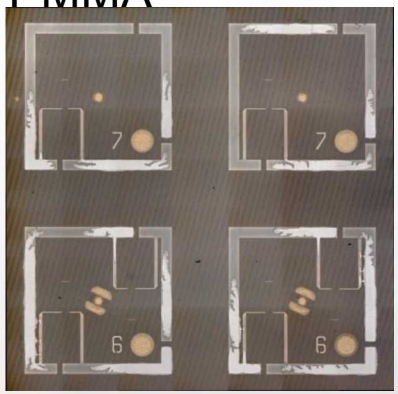
- Latent image exposure on top of PMMA
- 9 minute dip 100:1 HF to remove Ti oxide
- Ti oxide did not remove in small post regions
- SF6/O2 plasma ash, reason for exposed gold
- Gold plate
- Features look really good
- Polishing in process, still need to determine fill efficiency once we polish down to PMMA





Before Plasma clean

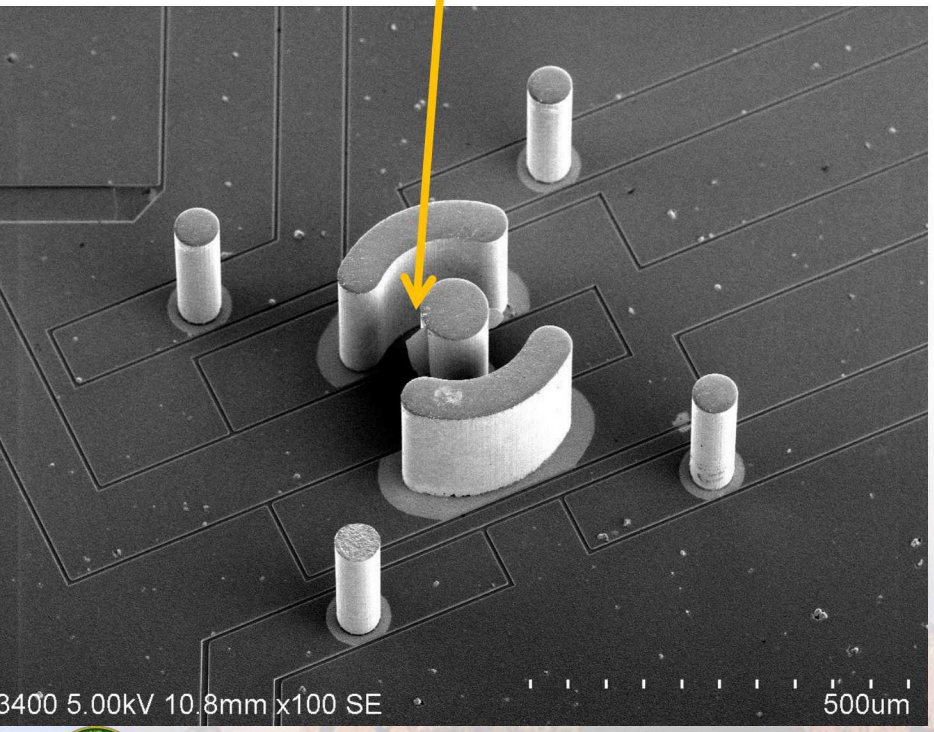




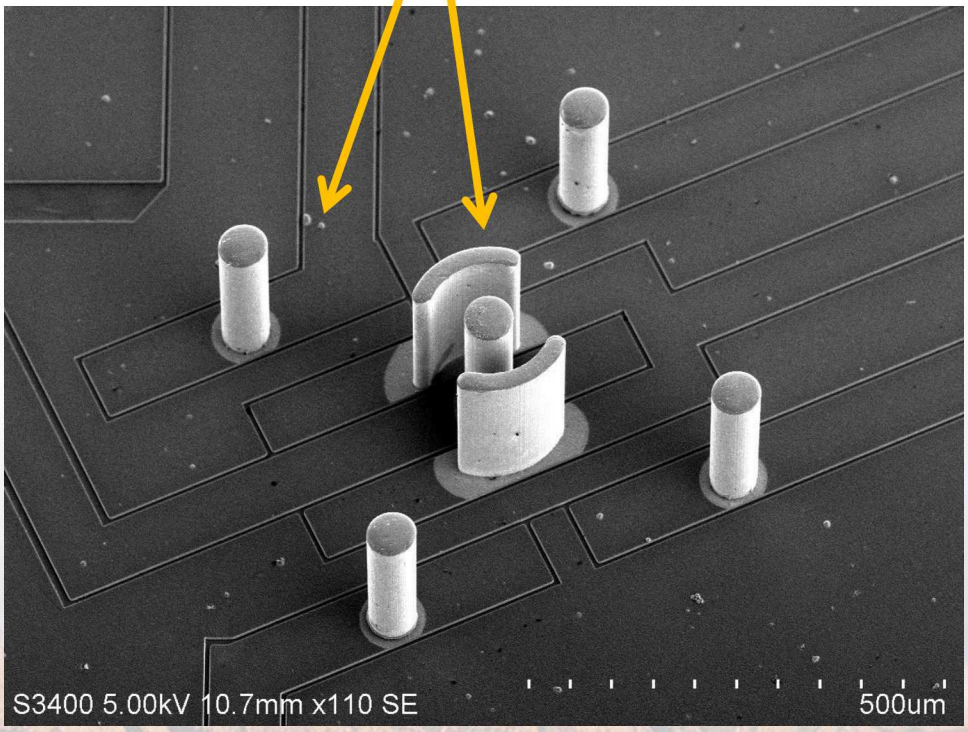
After Plasma clean

PMMA Wafer 1

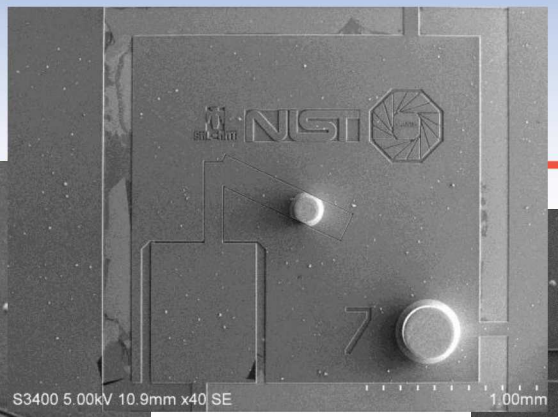
Crack in PMMA mold leading to gold plating sliver extruding from center post.

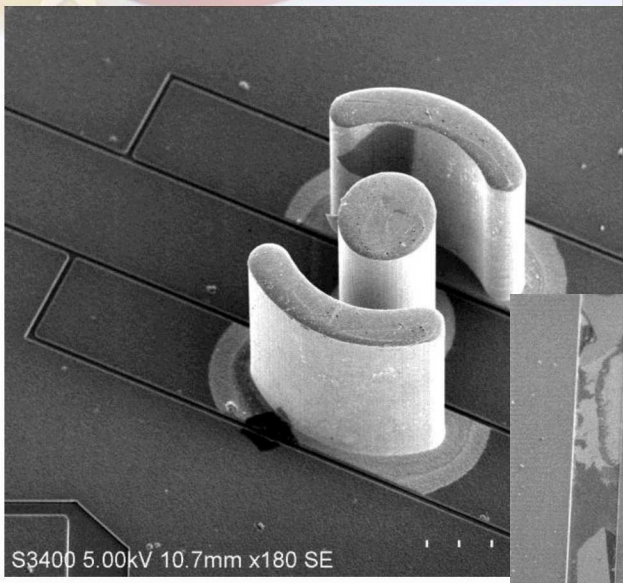


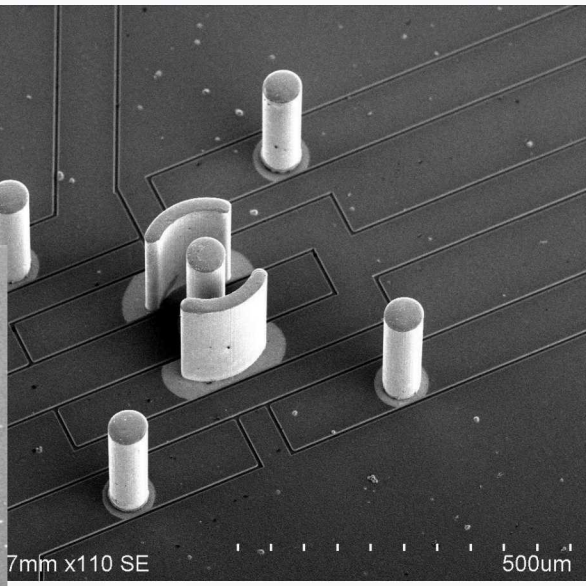
Perfect result in layer 2 features, no gold slivers, Layer 1 gold plating shows some nodules, not seen in later processed wafers.

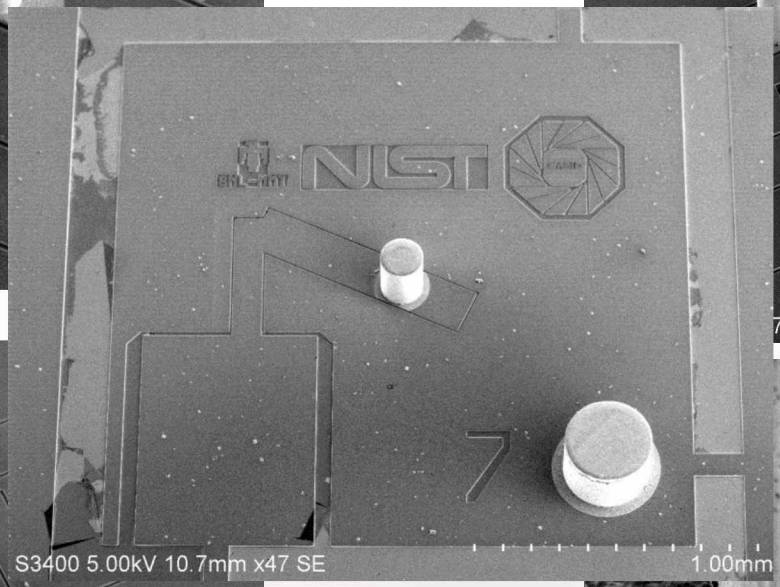


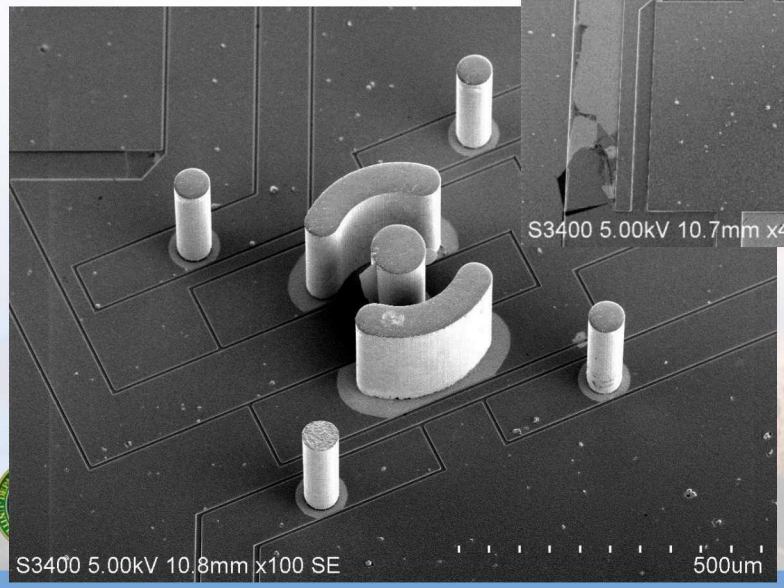
PMMA Wafer 1

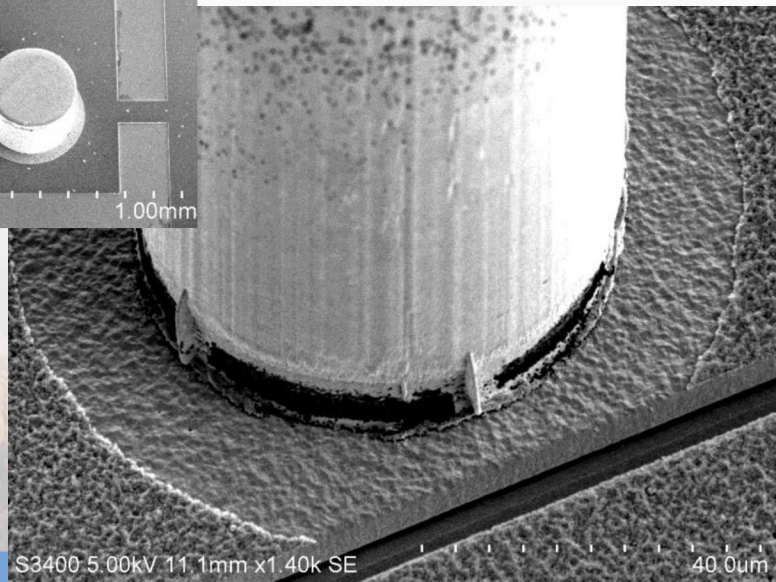

S3400 5.00kV 10.9mm x40 SE
1.00mm


S3400 5.00kV 10.7mm x180 SE

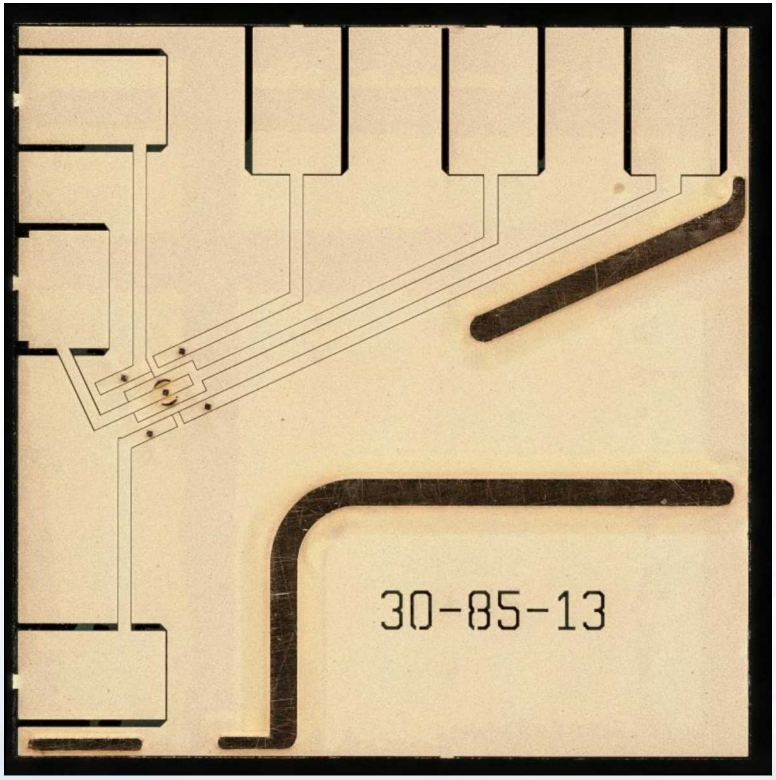

7mm x110 SE
500um

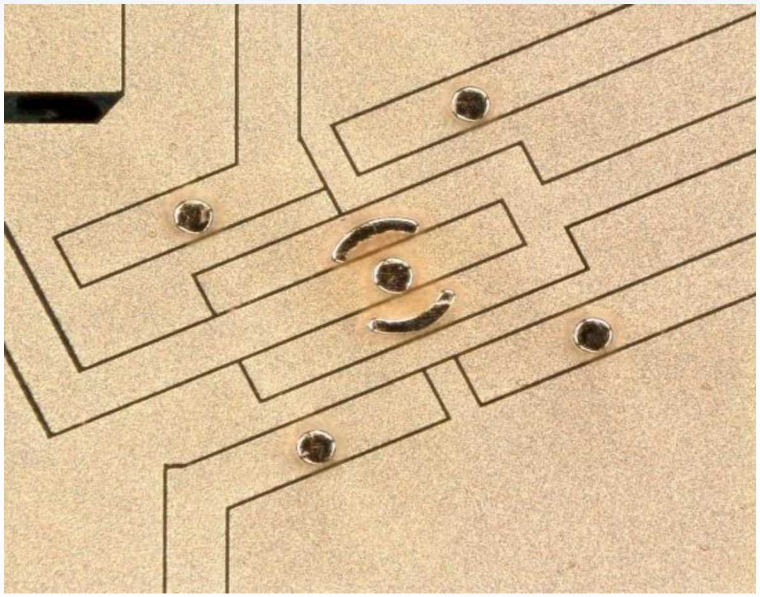

S3400 5.00kV 10.7mm x47 SE
1.00mm

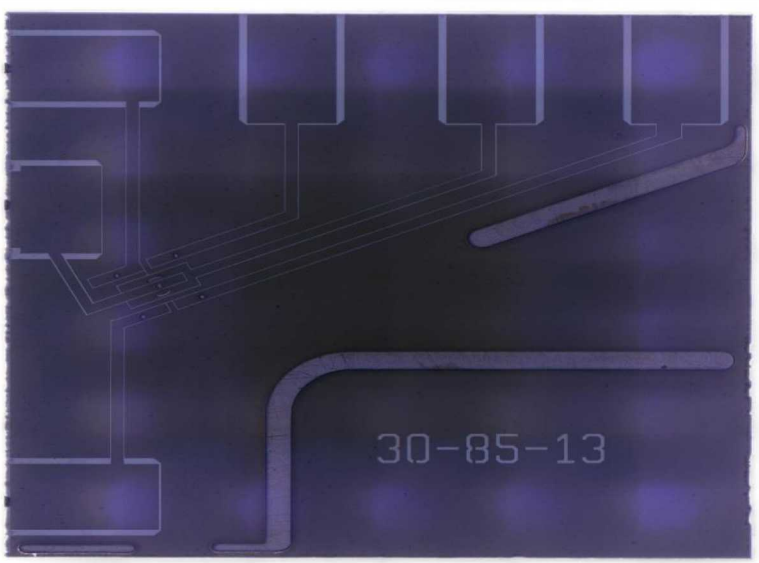

S3400 5.00kV 10.8mm x100 SE
500um


S3400 5.00kV 11.1mm x1.40k SE
40.0um

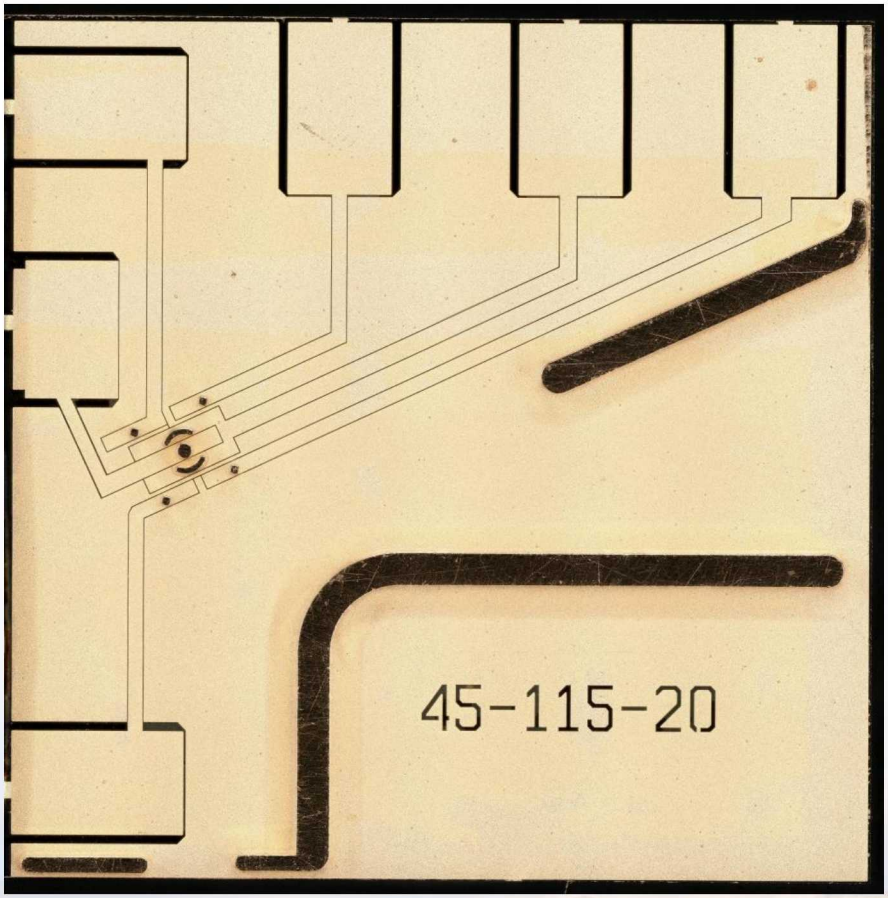
Gen 3 delivered Traps

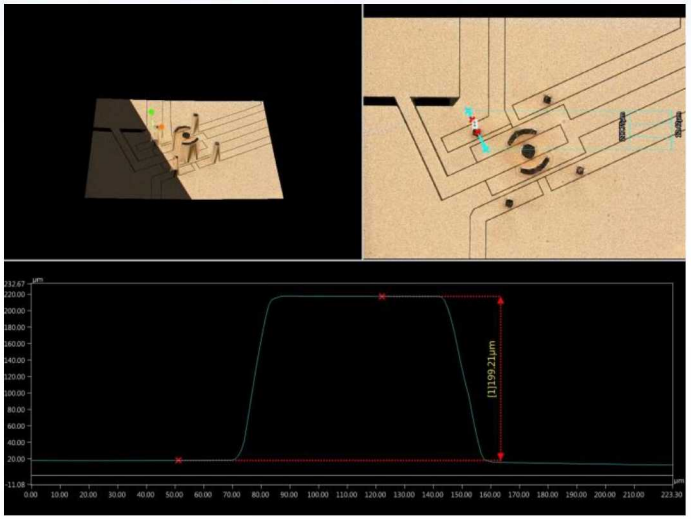


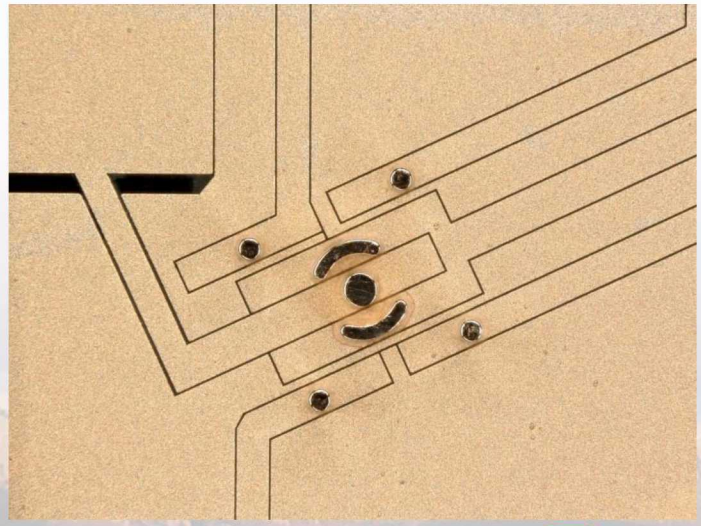




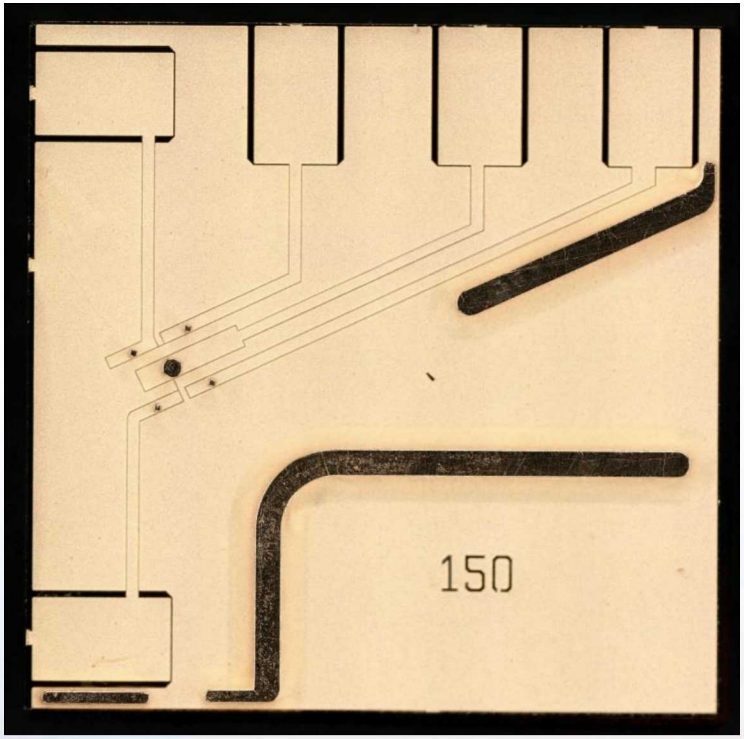
Gen 3 delivered Traps

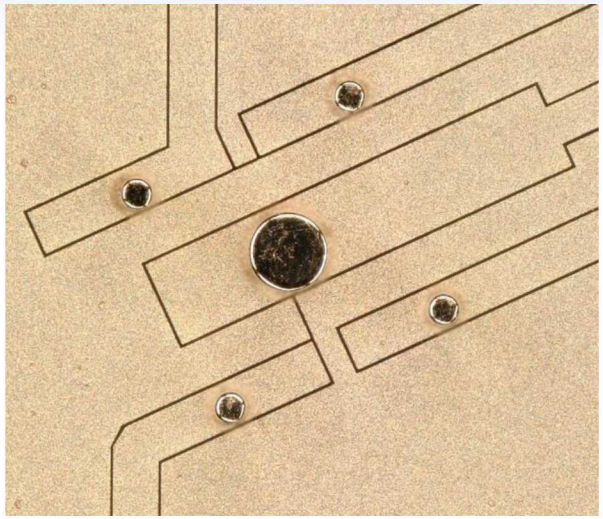


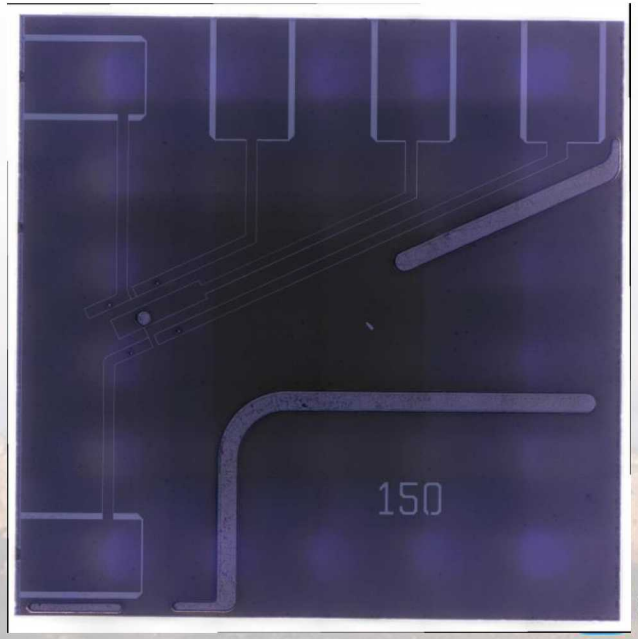




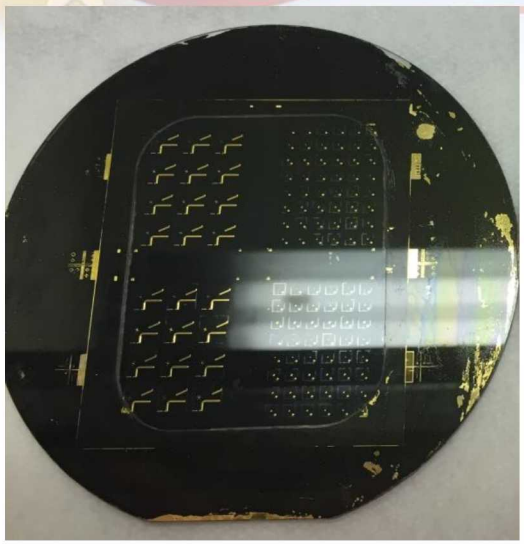
Gen 3 delivered Traps





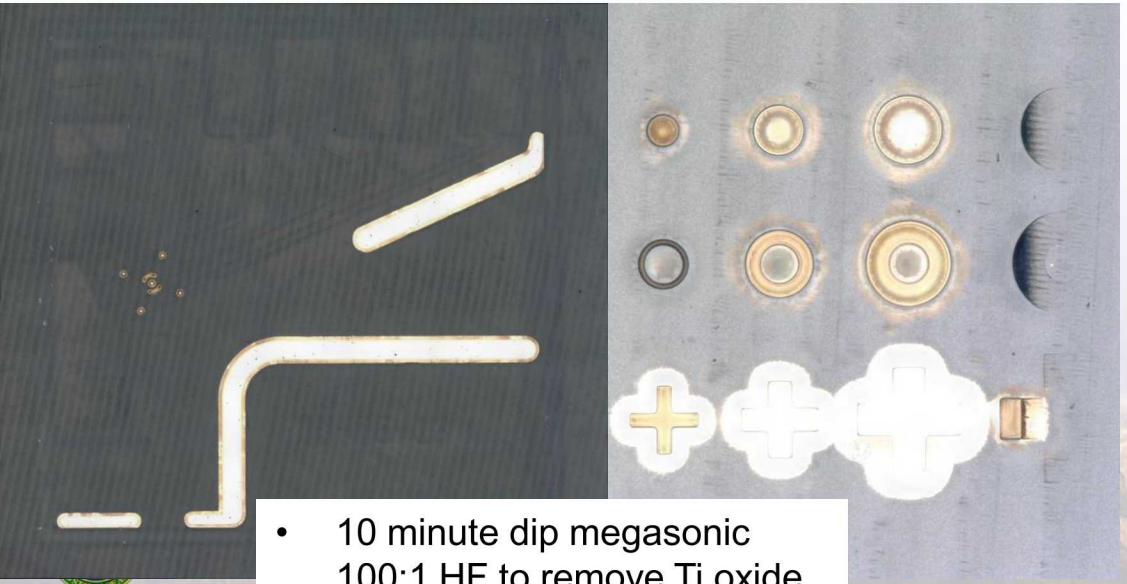


PMMA Wafer 2

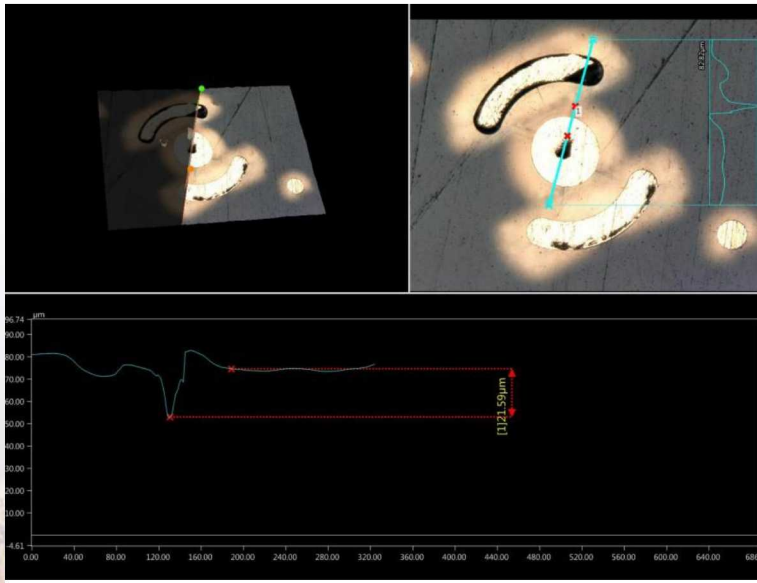


Wafer 2

- 10 minute dip megasonic 100:1 HF to remove Ti oxide
- Gold plate
- Polish
- All features plated, 80-90% of all features maintained uniform gold fill, 10-20% features saw evidence of gold plated defects where gold plating did not make it to the top of mold uniformly, bottom right image. Likely caused by not being completely developed out prior to gold plating



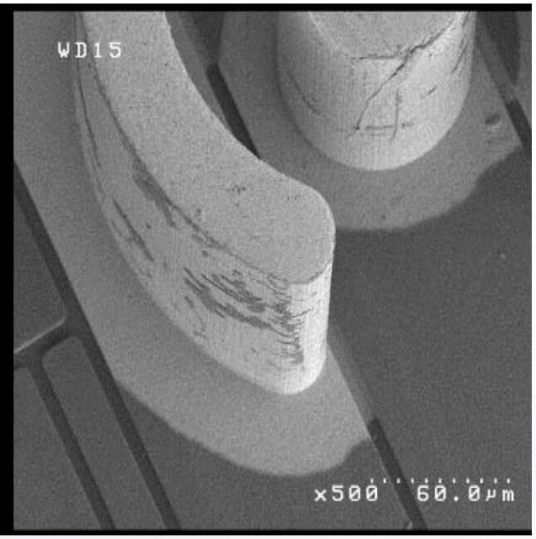
- 10 minute dip megasonic 100:1 HF to remove Ti oxide

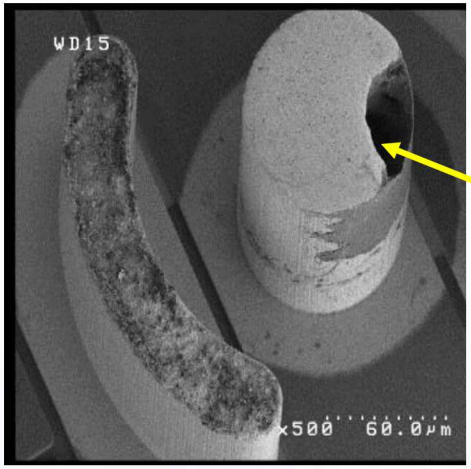


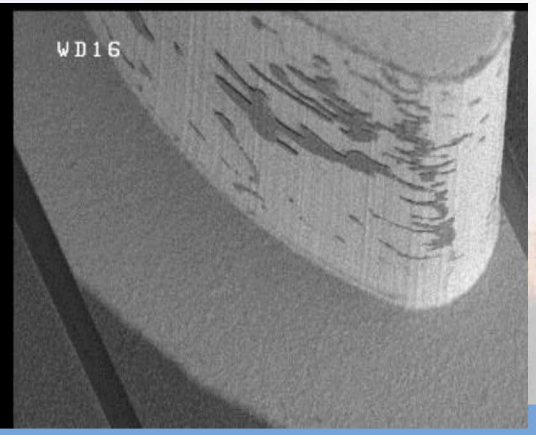
- Fill efficiency where some features are under filled after polishing down to PMMA

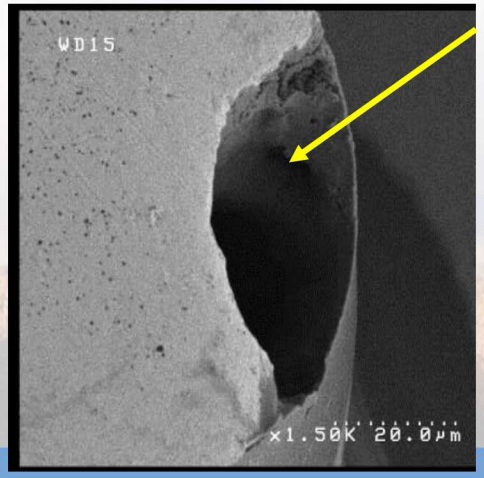
PMMA Wafer 2

- Undercut does not change feature geometry at the bottom of PMMA mold
- Plasma clean still useful to clean out bottom of features prior to plating

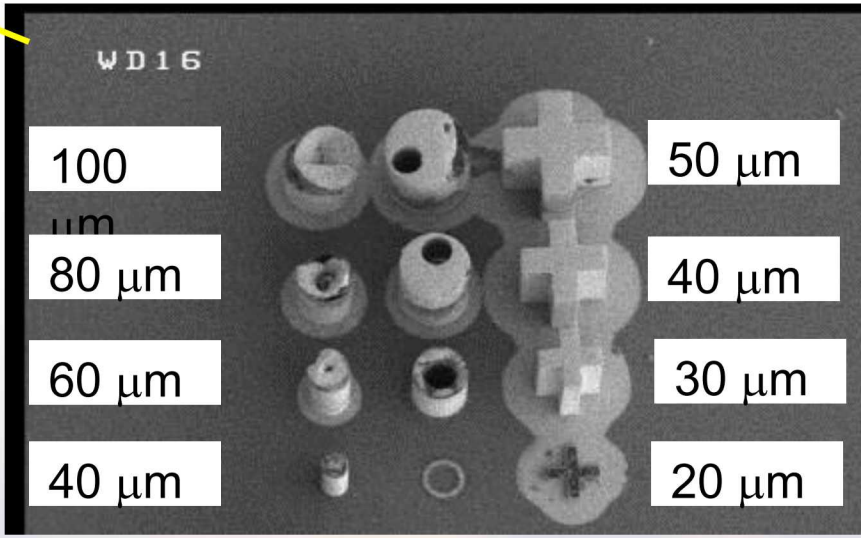






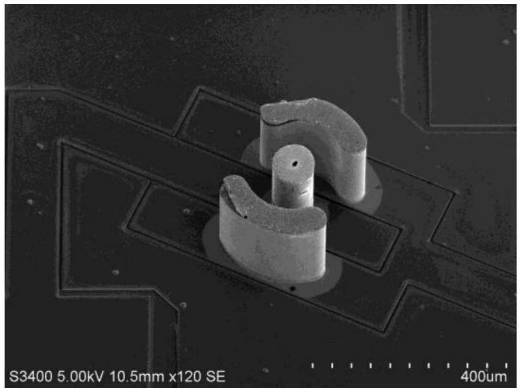


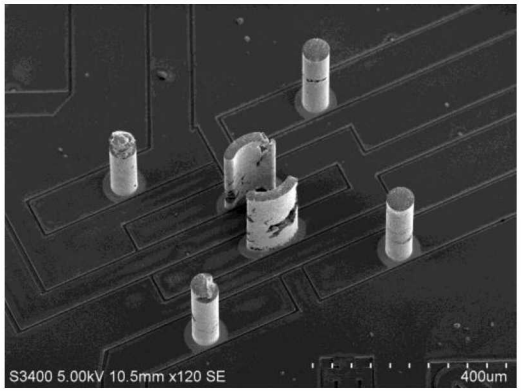
Defects & resolution

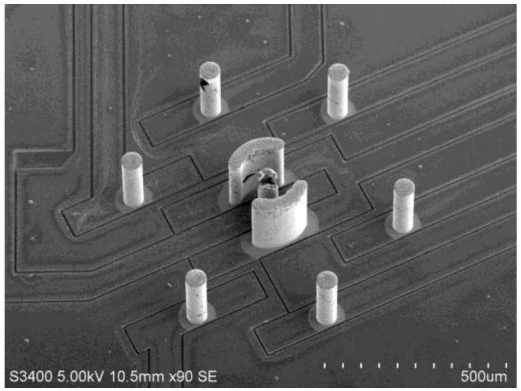


40 µm
30 µm
20 µm
10 µm

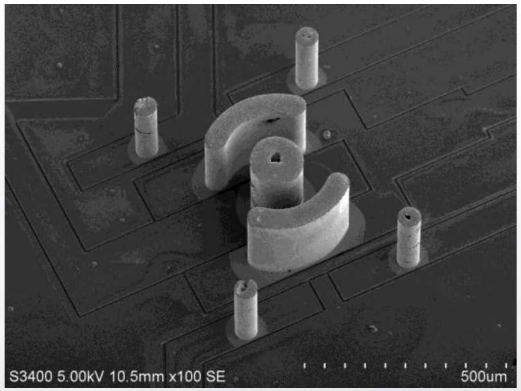
PMMA Wafer 2

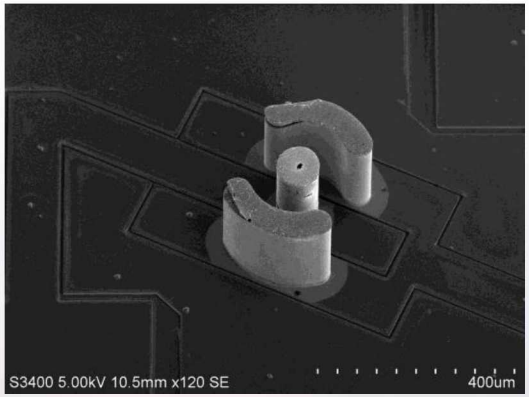

S3400 5.00kV 10.5mm x120 SE
400um


S3400 5.00kV 10.5mm x120 SE
400um


S3400 5.00kV 10.5mm x90 SE
500um

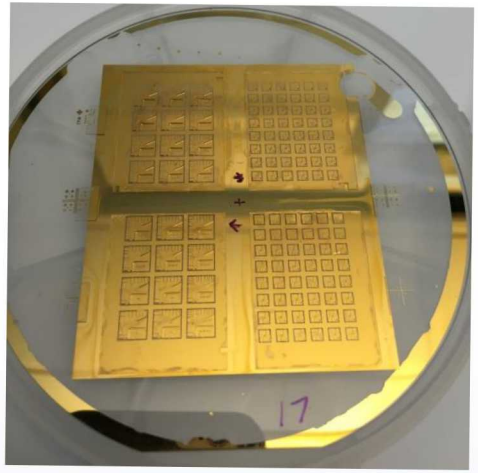

S3400 5.00kV 10.5mm x200 SE
200um

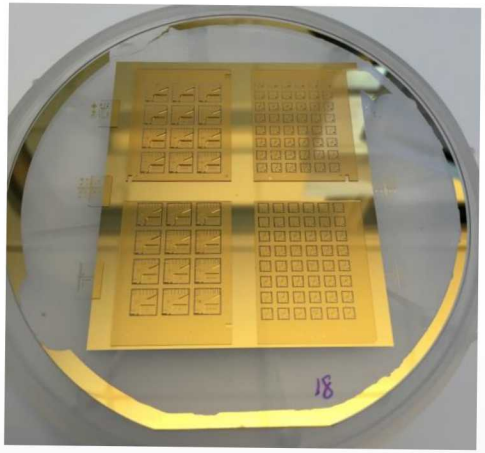

S3400 5.00kV 10.5mm x100 SE
500um

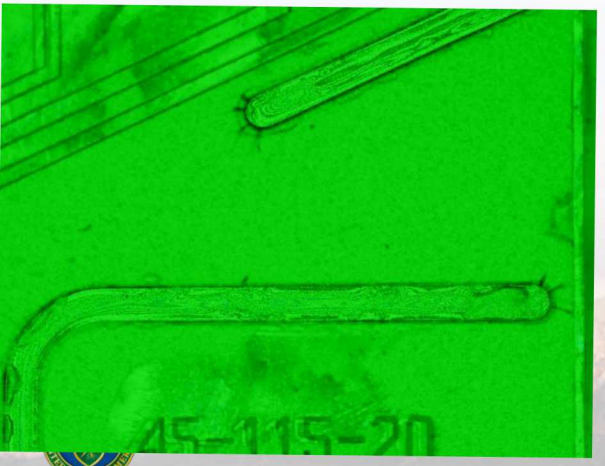

S3400 5.00kV 10.5mm x120 SE
400um

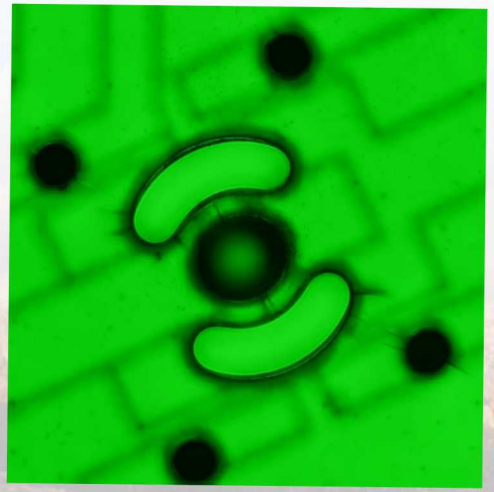
SUEX Wafer 17 & 18

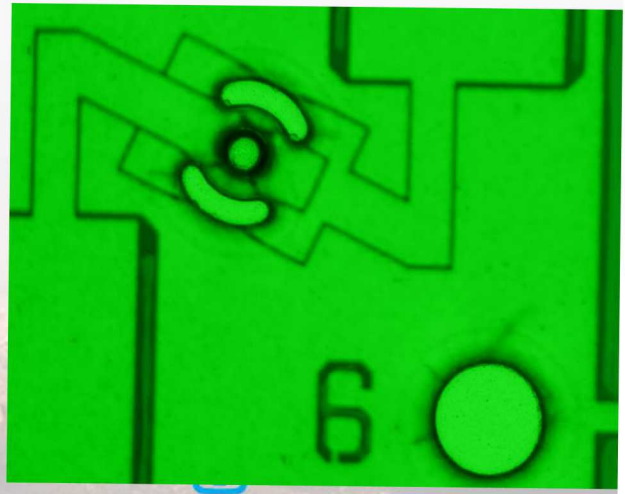
- Wafer 17 has residue
- Wafer 18, mixed result, some good/bad die
- More SUEX wafers coming





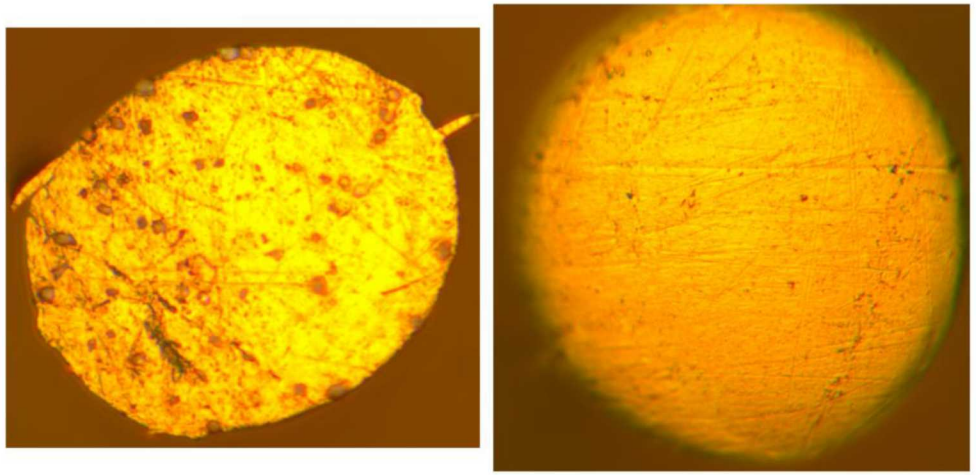






Polishing

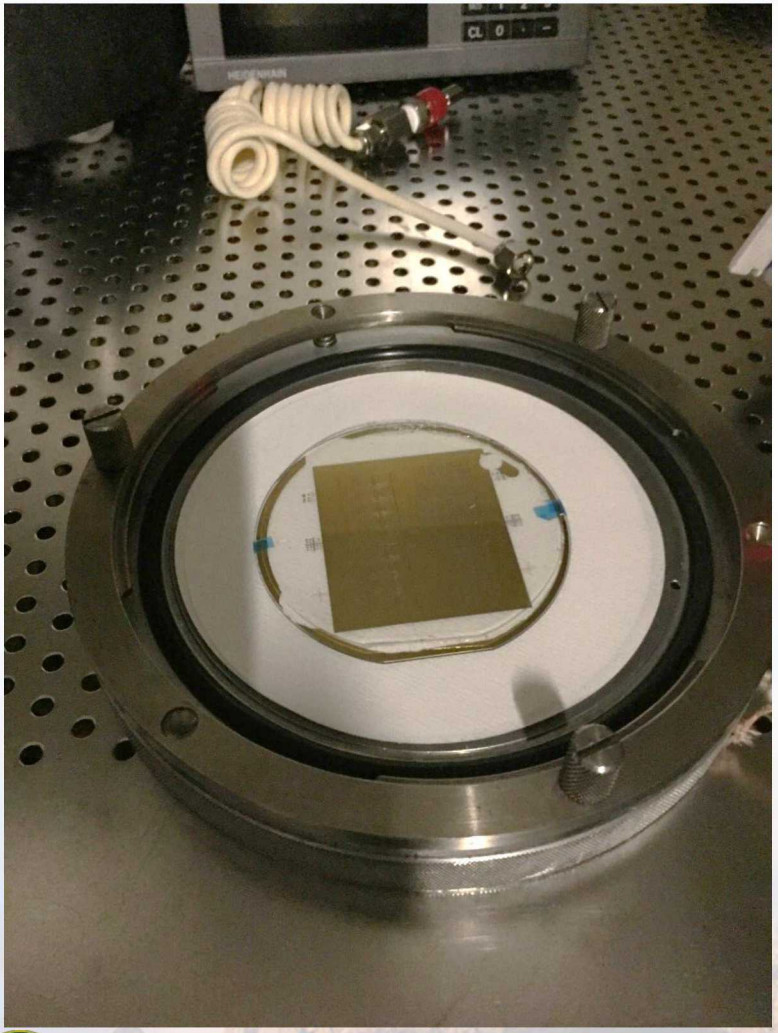
Gen 2 versus Gen 3 traps



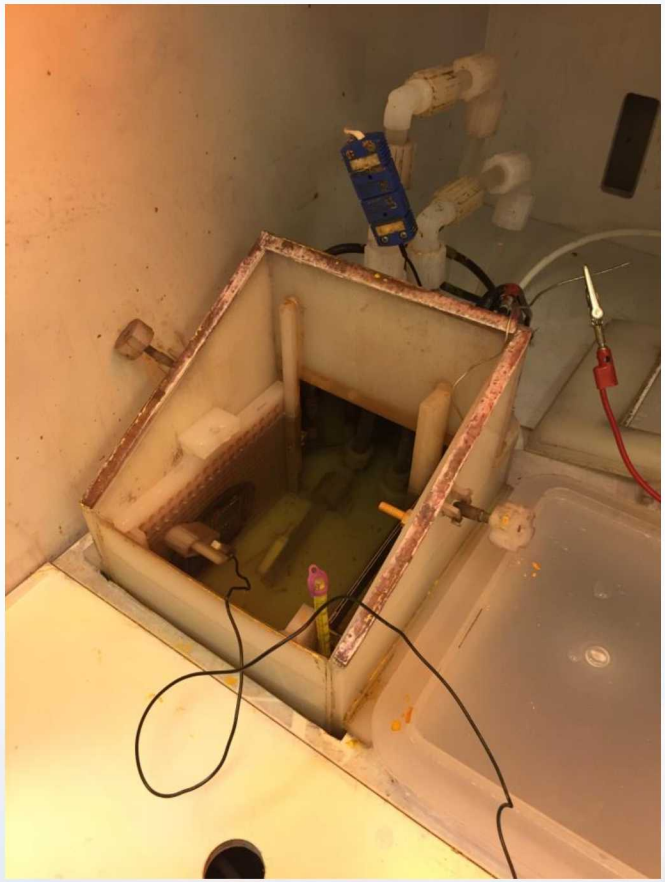
Etching the Titanium oxide

- 1% HF using Ultrasonic agitation

Bladder bonding SUEX



Gold plating wafer 10 & 11



Acknowledgments: A. E. Hollowell[1], P. Finnegan[1], Quoc Nguyen[2], Dawit G. Yemane[2], Varshni Singh[2]

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