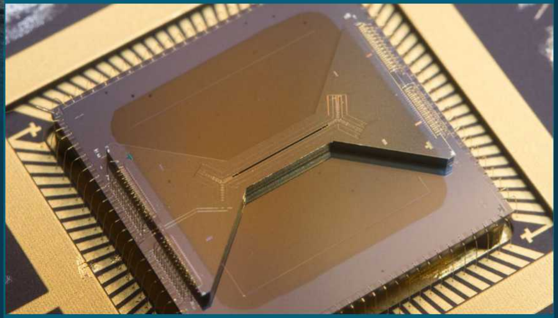
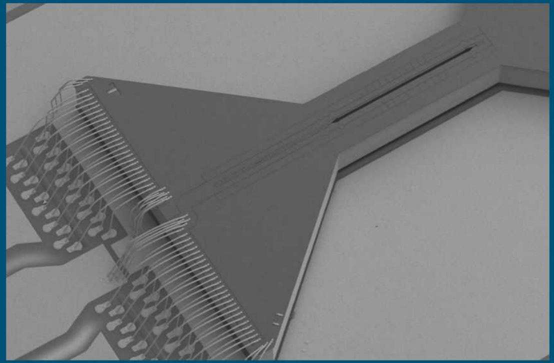
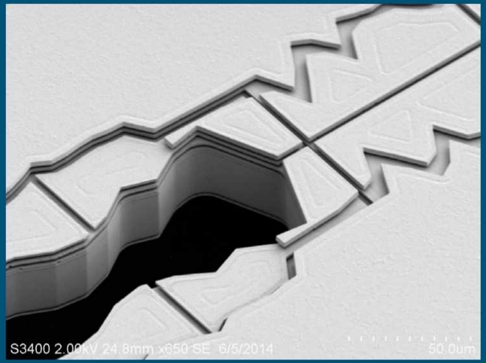
SAND2019-3443PE

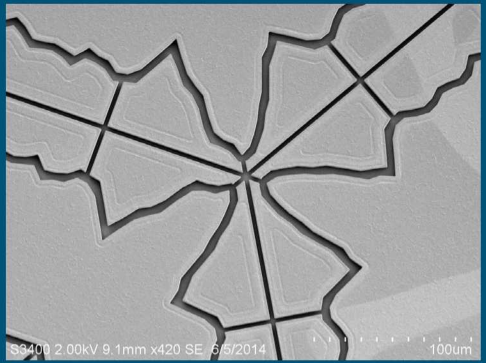
Sandia National Laboratories

Microfabricated ion traps for LogiQal Qubits









IARPA
BE THE FUTURE

PRESENTED BY

Peter Maunz

U.S. DEPARTMENT OF ENERGY NNSA

Current trap challenges

Challenges

- Cryogenic operation
  - Ion heating rates
  - Trap performance
  - Trap heating (rf dissipation)
- Trap charging
  - Exposed silicon in slot
  - Exposed oxide
- Degrees of freedom for long chains
- Trap stability
- What are we missing?

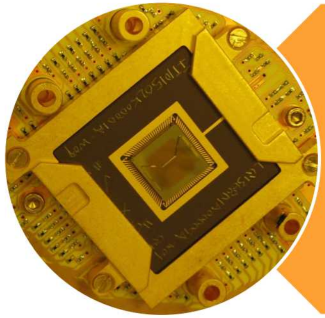
Approach

- Improve cryogenic operation
  - Identify origin of high heating rates at cryo
  - Operate trap at cryo at Sandia
  - Reduce capacitance of trap (Phoenix)
- Better charging mitigation
  - Avoid slot (Phoenix surface trap)
  - Thicker gold cover for sidewall
- Phoenix trap with segmented outer electrodes
- Reduce rf dissipation improve thermal anchoring (AlN Phoenix package)

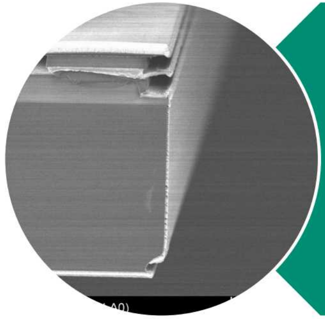
Timeline for trap deliveries

- Available now:
  - HOA-2.0, HOA-2.1
  - HOA-2.x with thicker gold coating in slot, (need your trap back to characterize)
- Expected to be available by end of 2019
  - Phoenix (slotted or surface versions)
- Possibly by end of 2020
  - LQ-2 trap
- What are your needs?

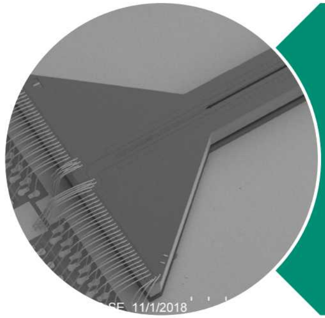
Outline



Cryogenic characterization

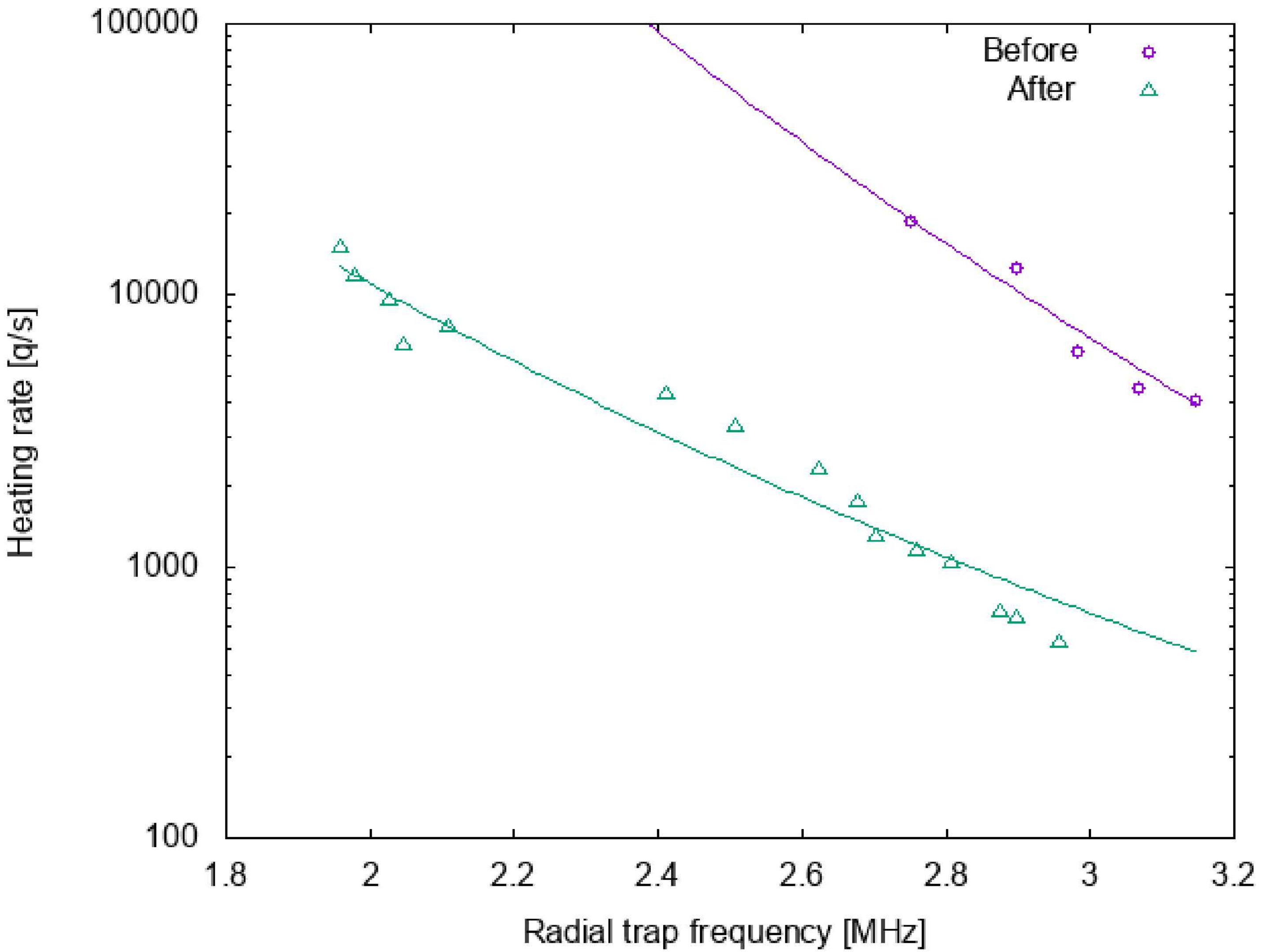


Trap charging and sidewall coverage



Phoenix trap

Heating rate dependency on radial trap frequency



Changes between 2/19 and 3/19

- Heating to 80K
- Reduced (room-temperature) pressure from 7×10^{-10} to 7×10^{-11}

Purple (before heating) shown with approximated power law

$$\dot{n} \propto f^{-11}$$

Green (after heating) shown with approximated power law

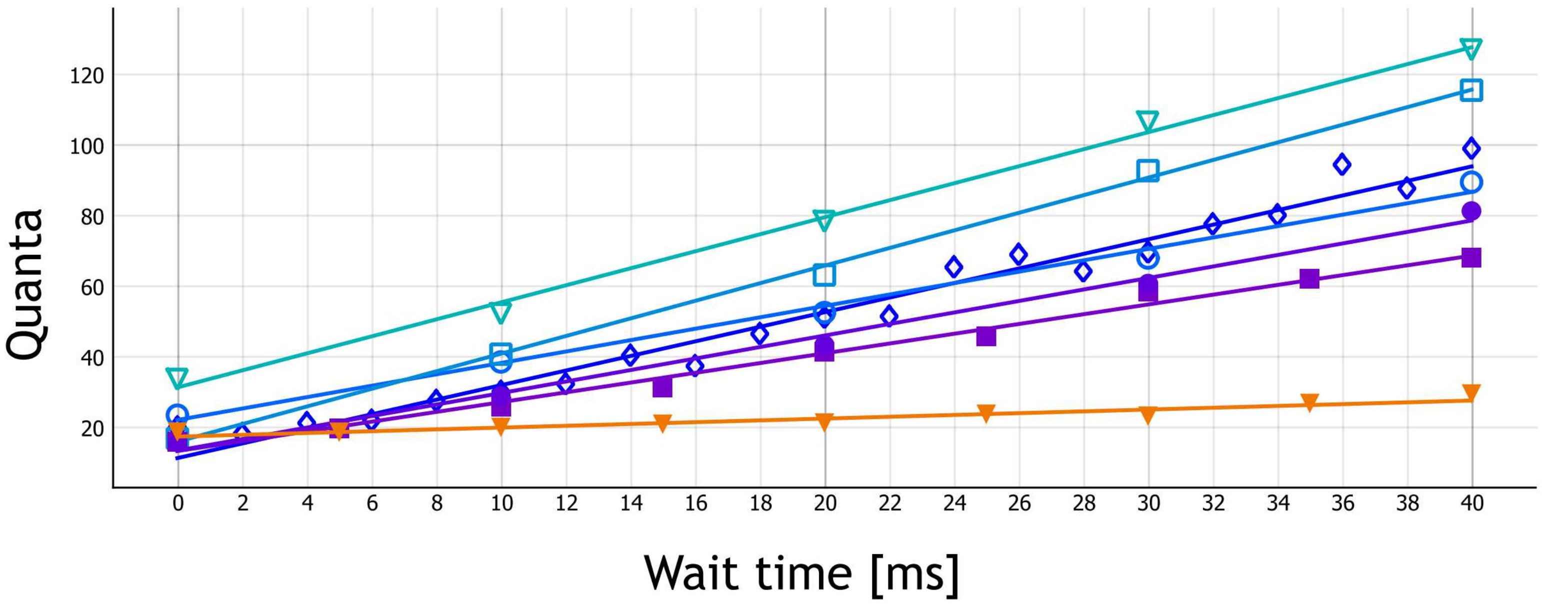
$$\dot{n} \propto f^{-7}$$

Cryogenic trap characterization
Ion heating rates

Measured heating rates in cryogenic trap
- 2000/s - 3000/s measured above slot
  - Higher than at room temperature
- 500/s measured after 80K "bake"
- 255/s measured above surface of trap next to junction

Currently used trap
- HOA-2 trap with 100µm backside slot
- No sidewall coverage (exposed silicon)

Possible causes for remaining heating above surface
- Trench capacitors
  - Rf testing shows no difference between room temp and cryo
- Vias
  - Tested independently resistance is reduced by going cold



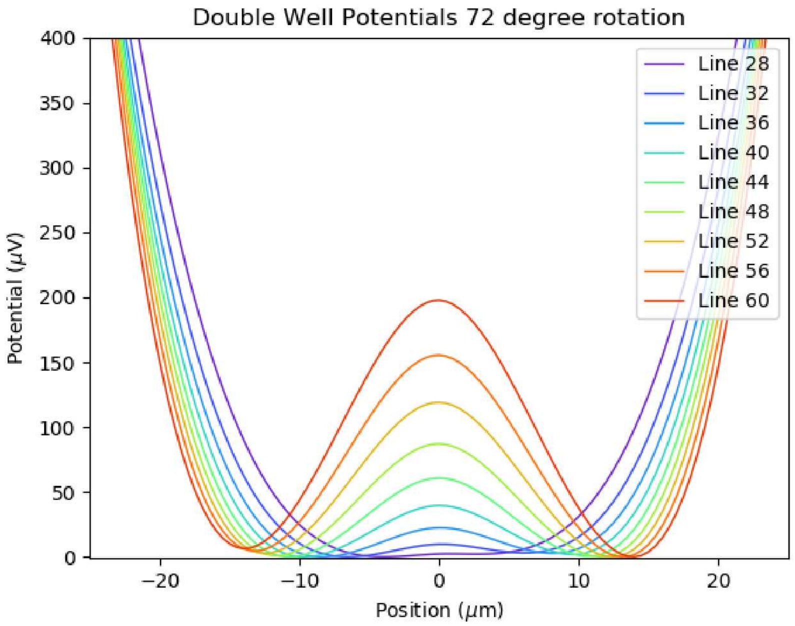
- Heating rates measured using Carrier Rabi oscillations
- ytterbium
- 435nm transitions to D state
- Radial modes
- 2.5MHz trap frequency
- 35Kelvin

Cryogenic trapping chamber
Residual pressure measurement

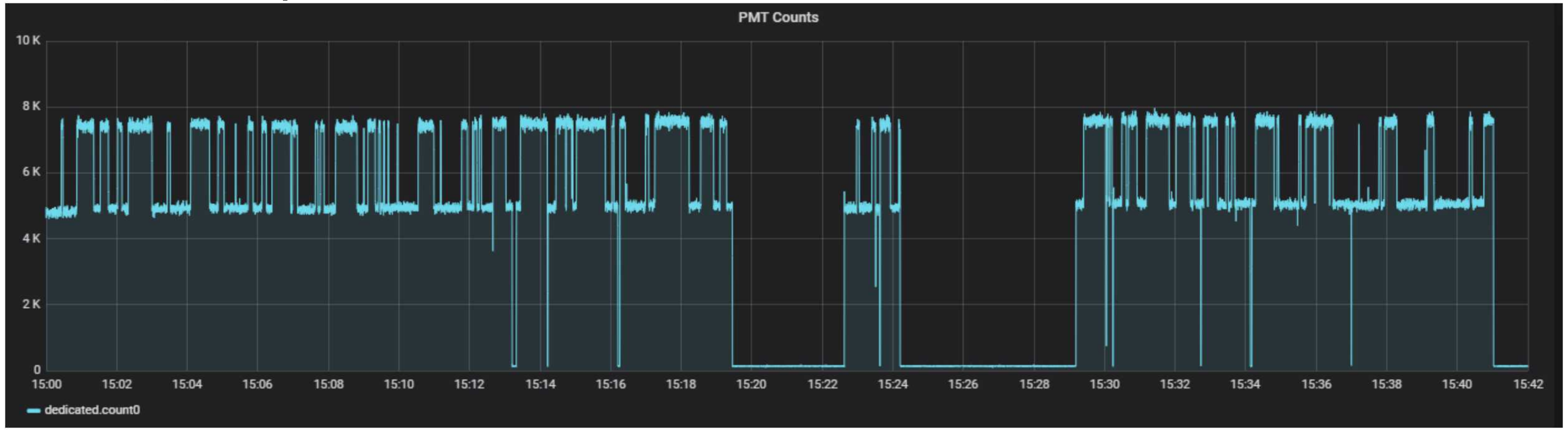
- Following method described by UMD team
- Prepare double well potential
- Count jumping between wells
- Maximum energy transfer ≈ 60μeV

- Langevin collision model:
- Trap temperature 35K, pill-box 8K
- Residual pressure: 2.5×10^{-10} Torr

- Will look as function of barrier height to see whether it is Hydrogen or Helium or ?



Line 32; ≈ 15μeV



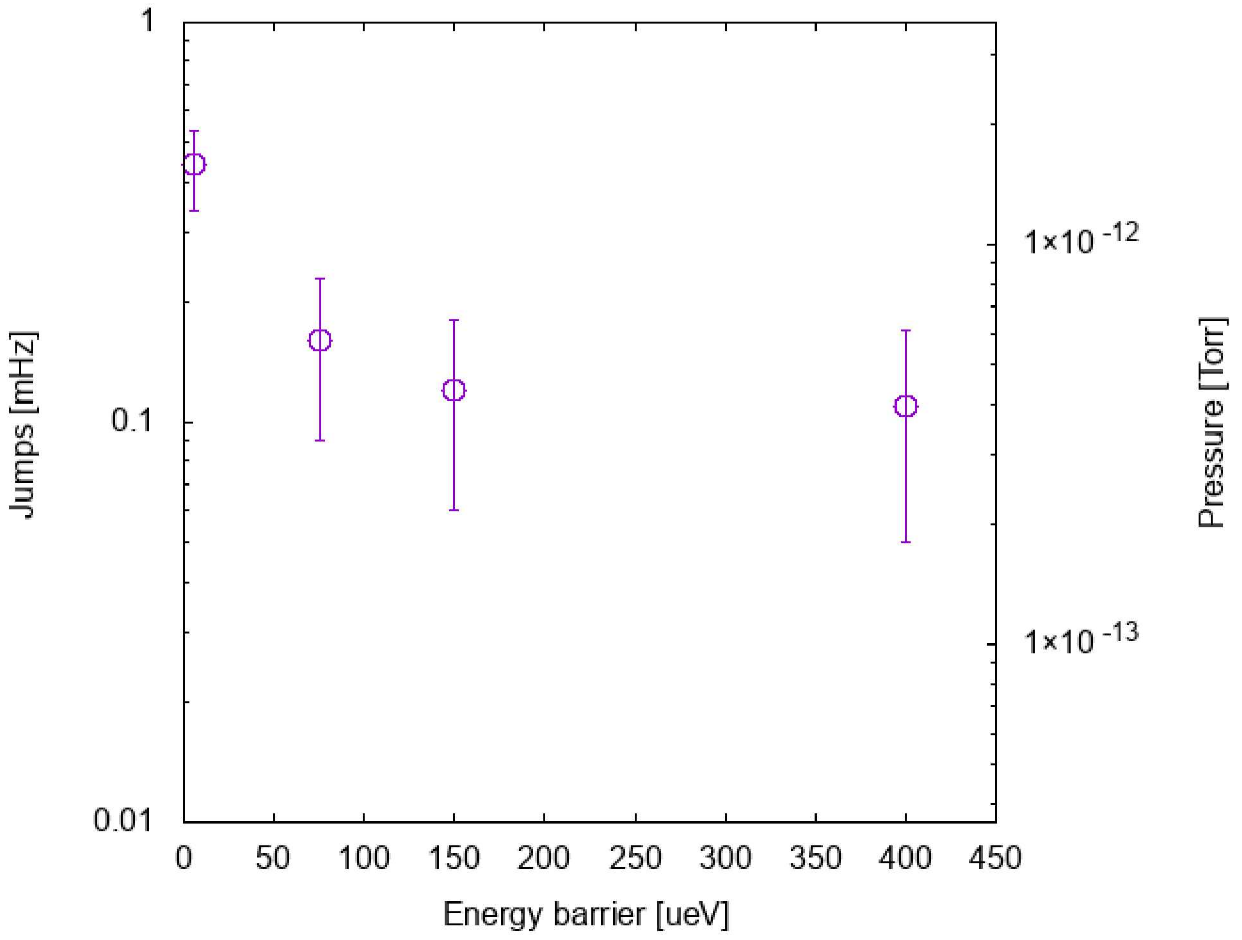
Site hopping: 68/ks F-state transistions: 4/ks

Cryogenic trapping chamber
Reduced background pressure

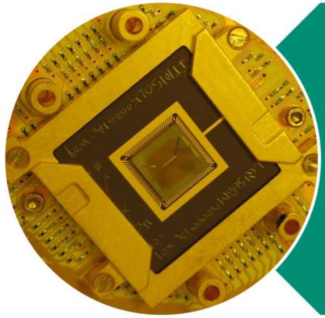
- Room temp pressure 1.1×10^{-9}
  Collisions 68/ks
  - Partial warm-up and cool-down
  - Ti-evaporation
- Room temperature pressure 1×10^{-10}
  Collisions 0.44/ks

Energy	Collision rate	Pressure	# Events
5μeV	0.44/ks	1.6×10^{-12}	12
75μeV	0.07/ks	8.4×10^{-13}	5
150μeV	0.06/ks	6.5×10^{-13}	5

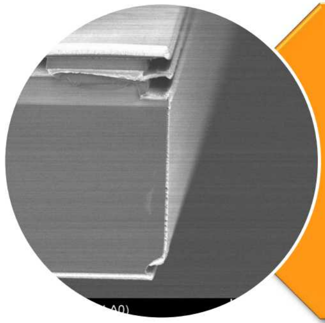
Collisions as function of barrier height



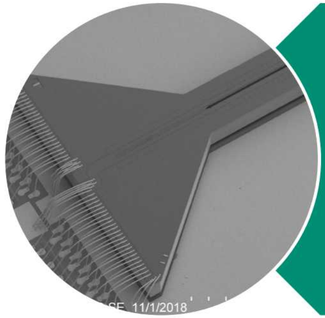
Outline



Cryogenic characterization

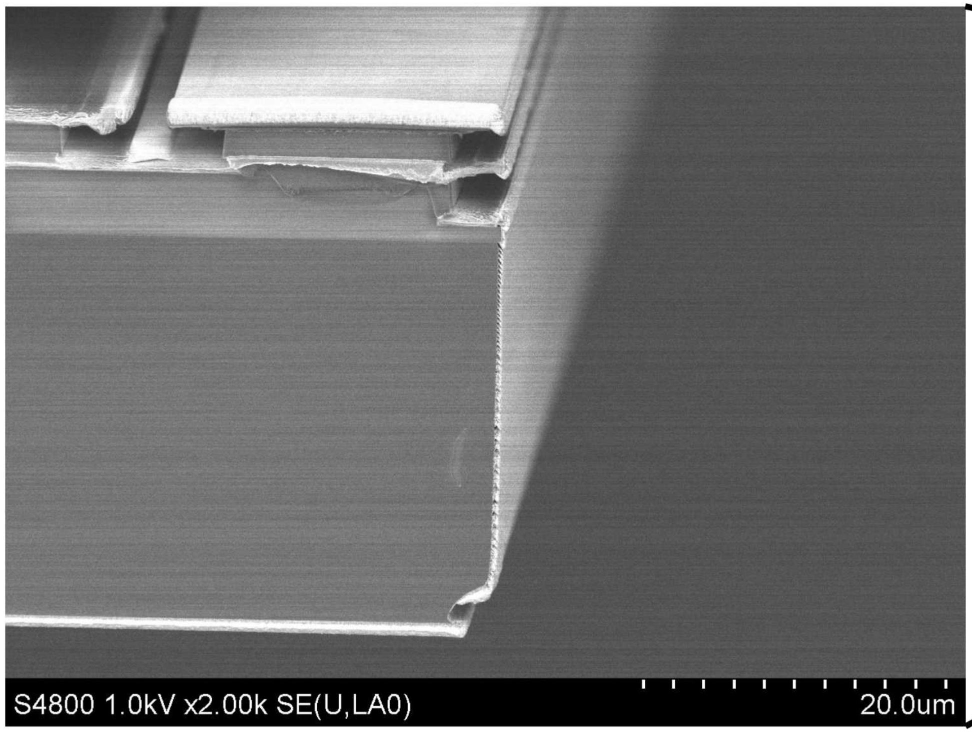


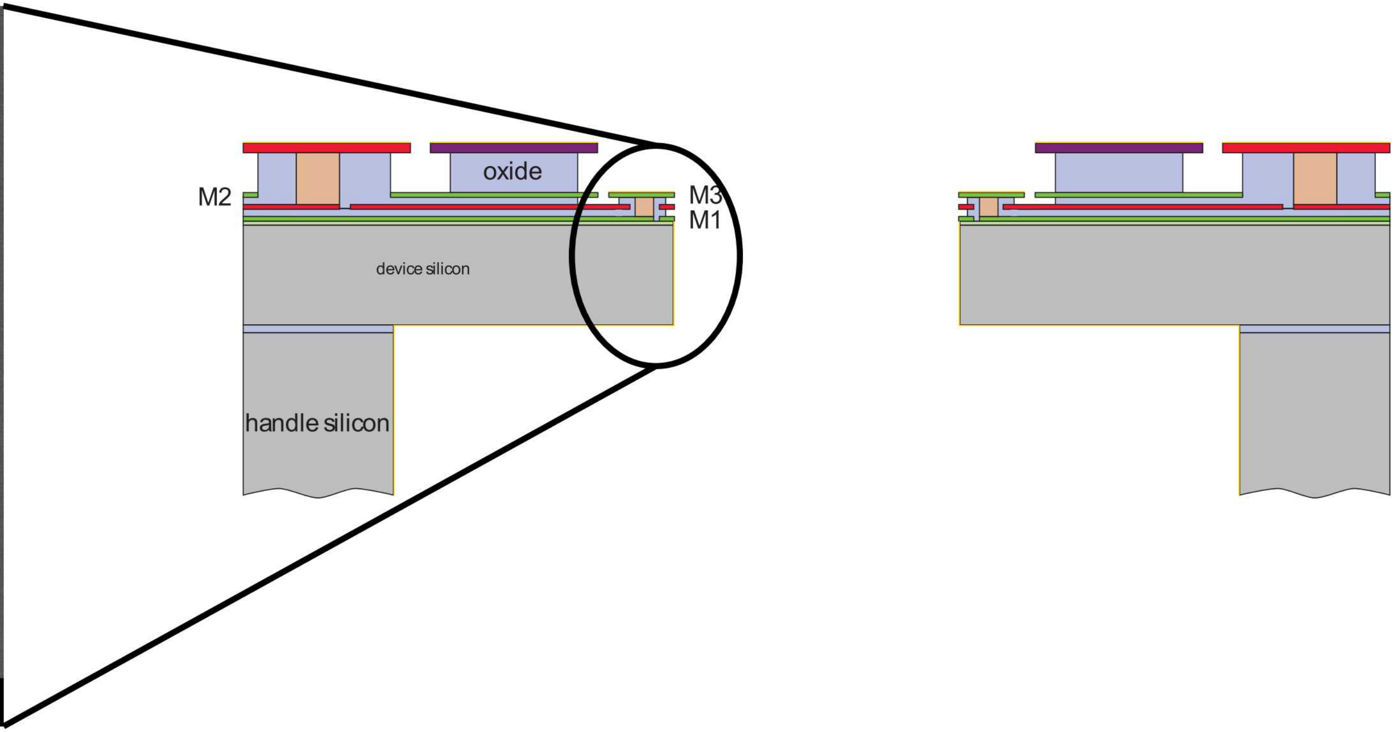
Trap charging and sidewall coverage



Phoenix trap

HOA-2 trap characterization
Covered sidewalls

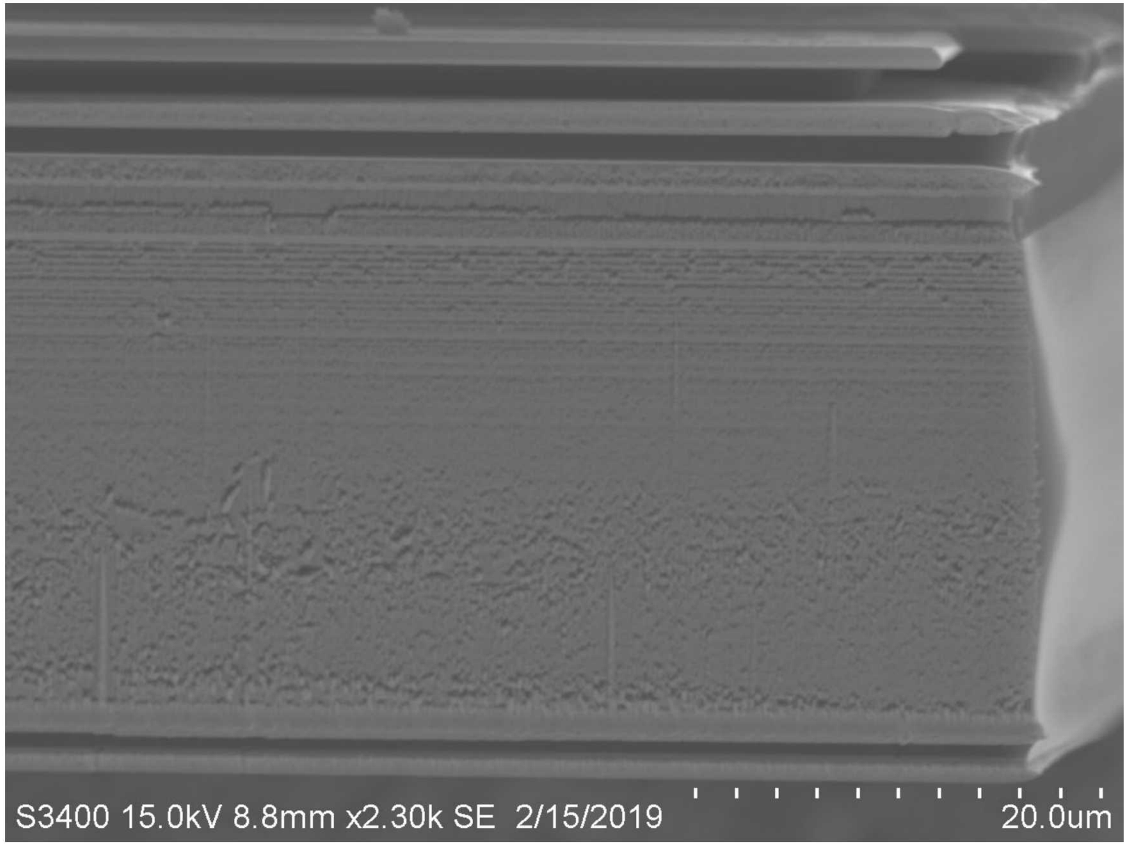


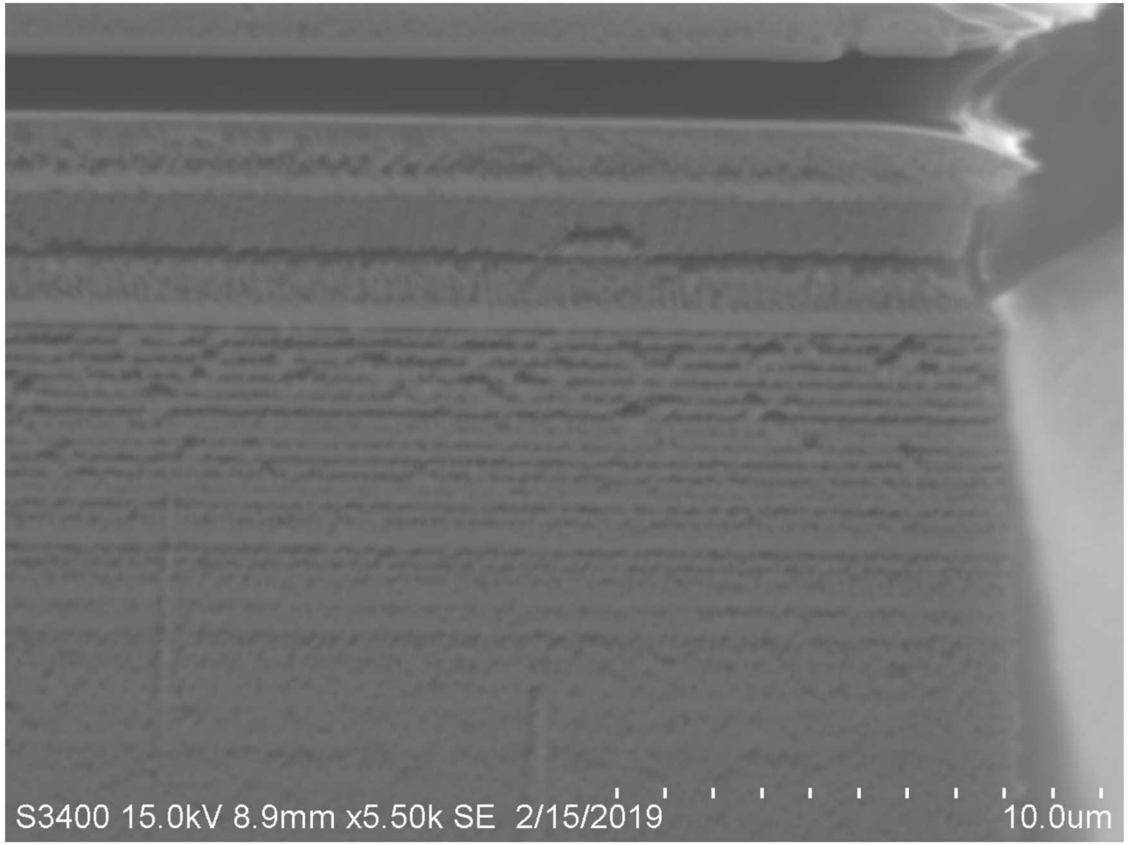


- Increased evaporated gold layer thickness on backside ten times
- Adjusted evaporation angle to optimize for sidewall coverage
- SEM shows gold layer on sidewall >100nm
- Fast-onset charging is suppressed by 5 orders of magnitude
- However, Innsbruck team, cryogenic operation, still observe charging

Second look at sidewall coverage

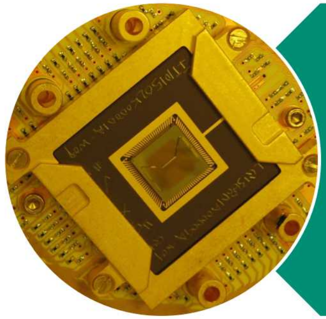
Some devices have scalloping sidewall



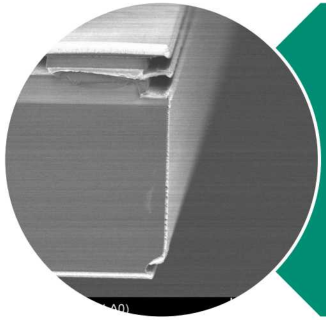


There might be exposed silicon that is susceptible to charging

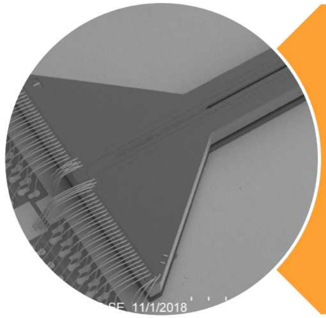
Outline



Cryogenic characterization



Trap charging and sidewall coverage

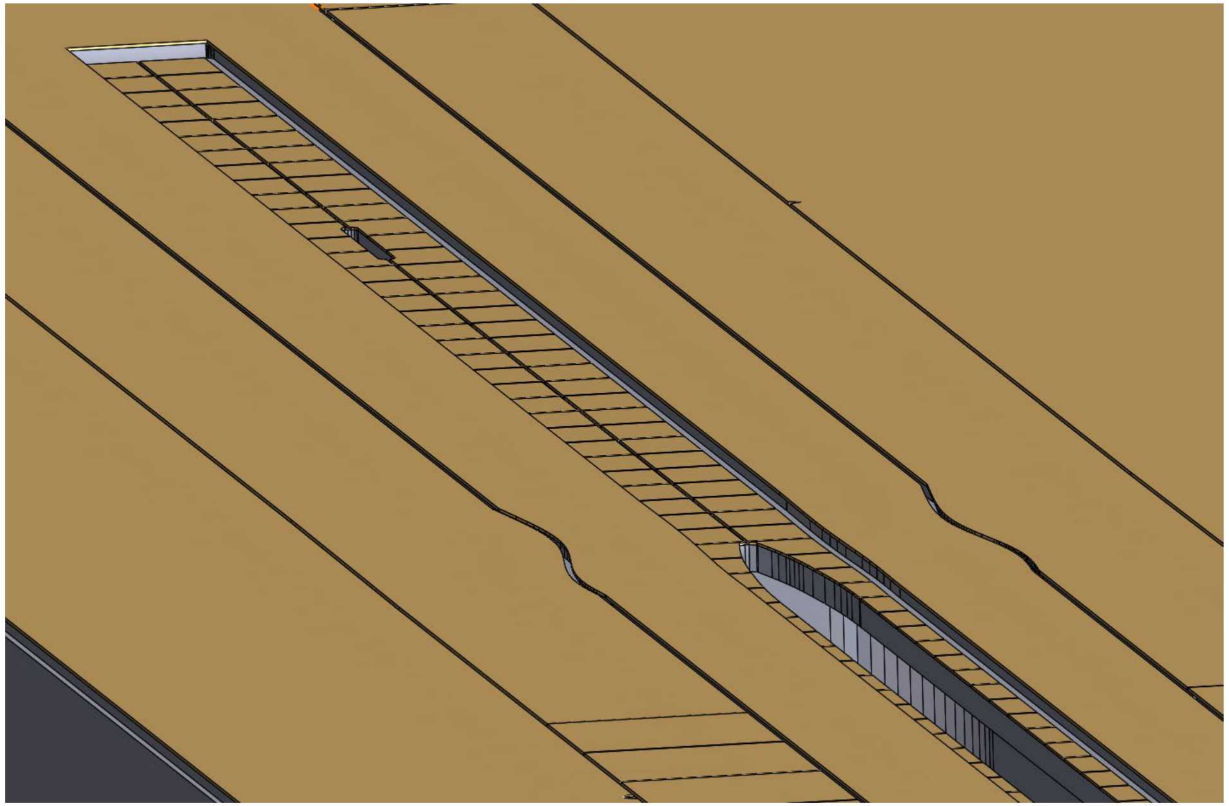


Phoenix trap

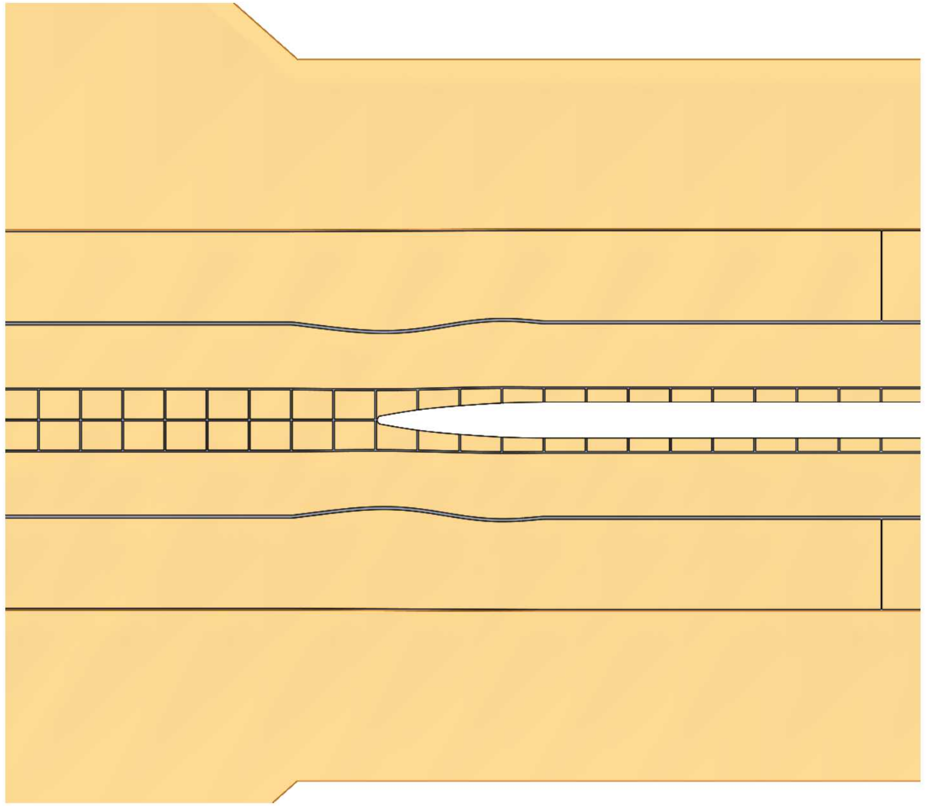
Phoenix trap revisions

- Use less risky but higher capacity internal structure
- Make design and routing more failure resilient
- Improve sidewall flatness

- Move all inner control electrodes to lower metal layer

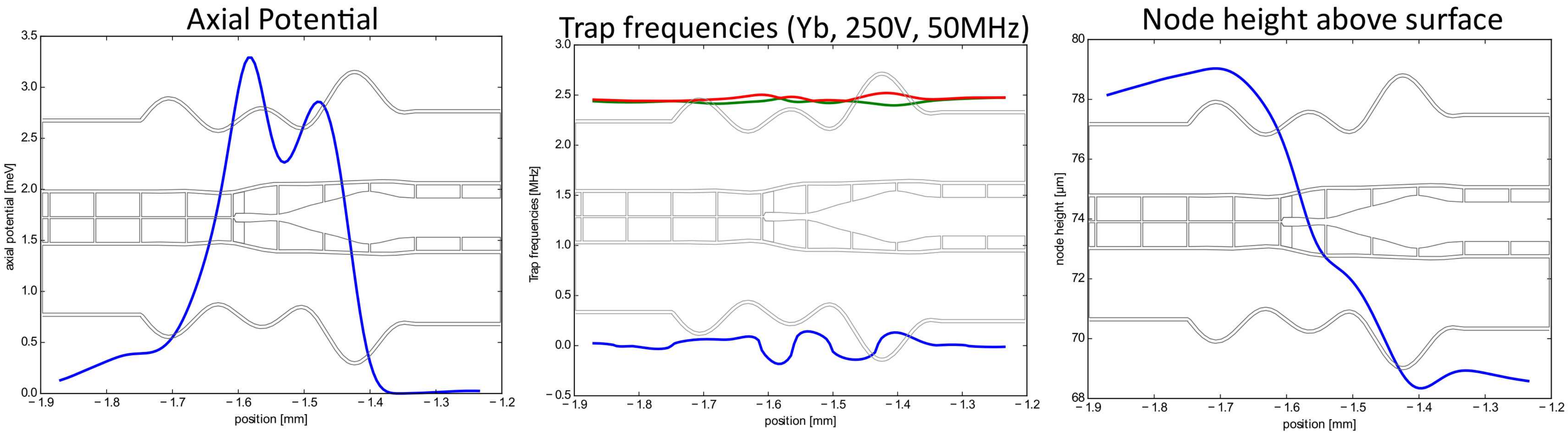


- Simplify junction

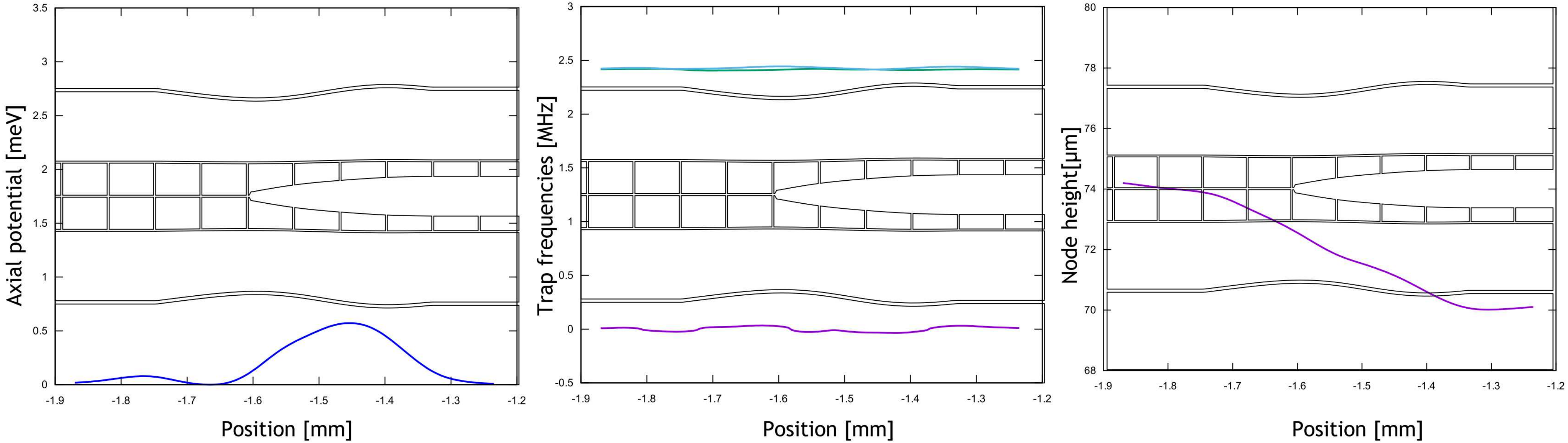


Raising the Phoenix
Design improvements

Inner elec on top metal



Inner elec on M3

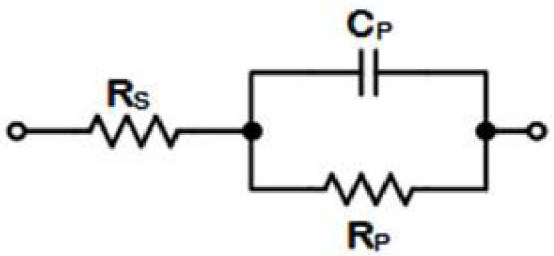


Estimated performance metrics of Phoenix traps

Capacitance as calculated from full device design data

Device version	M5	M3	M2 oxide	M2 vacuum	total
Phoenix (re-fabrication) above surface	1.02pF	0.10pF	2.9pF	-	4.0pF
Phoenix (re-fabrication) Slotted design	1.12pF	0.14pF	4.23pF		5.5pF
Phoenix (failed)		1.24pF	1.97pF		4.12pF
HOA-2.1		5.53pF	0.09pF	0.79pF	6.54pF

Rf-dissipation in traps
electrical characterization



R_s : Series resistance (lead resistance)

R_p : (rf) parallel resistance (dielectric absorption)

C_p : capacitance

For 100 V amplitude at 100 MHz:

Trap	Temp	C_p	R_s	R_p	P_s	P_p
Phoenix-0 (measurement)	300 K	4 pF	0.4 Ω		5 mW	
Phoneix-surface (calc.)	4 K		0.05 Ω		1 mW	
Phoenix-slotted (calc.)	300 K	5.5 pF	0.4 Ω		9.4 mW	
	4 K		0.05 Ω		1.4 mW	
HOA-2.1	300 K	7.6 pF	0.9 Ω	1.6 MΩ	100 mW	3.1 mW
	77 K		0.7 Ω		80 mW	
	4 K		0.5 Ω		60 mW	
Au/FS	300 K	1.93 pF	2.0 Ω	1.4 MΩ	15 mW	3.7 mW
	77 K		1.3 Ω		10 mW	
	4 K		0.8 Ω		5.9 mW	
Thunderbird	300 K	2.4 pF	0.6 Ω	1.5 MΩ	6.7 mW	3.3 mW

$$P_s \approx \frac{1}{2} R_s U^2 \omega^2 C_p^2$$

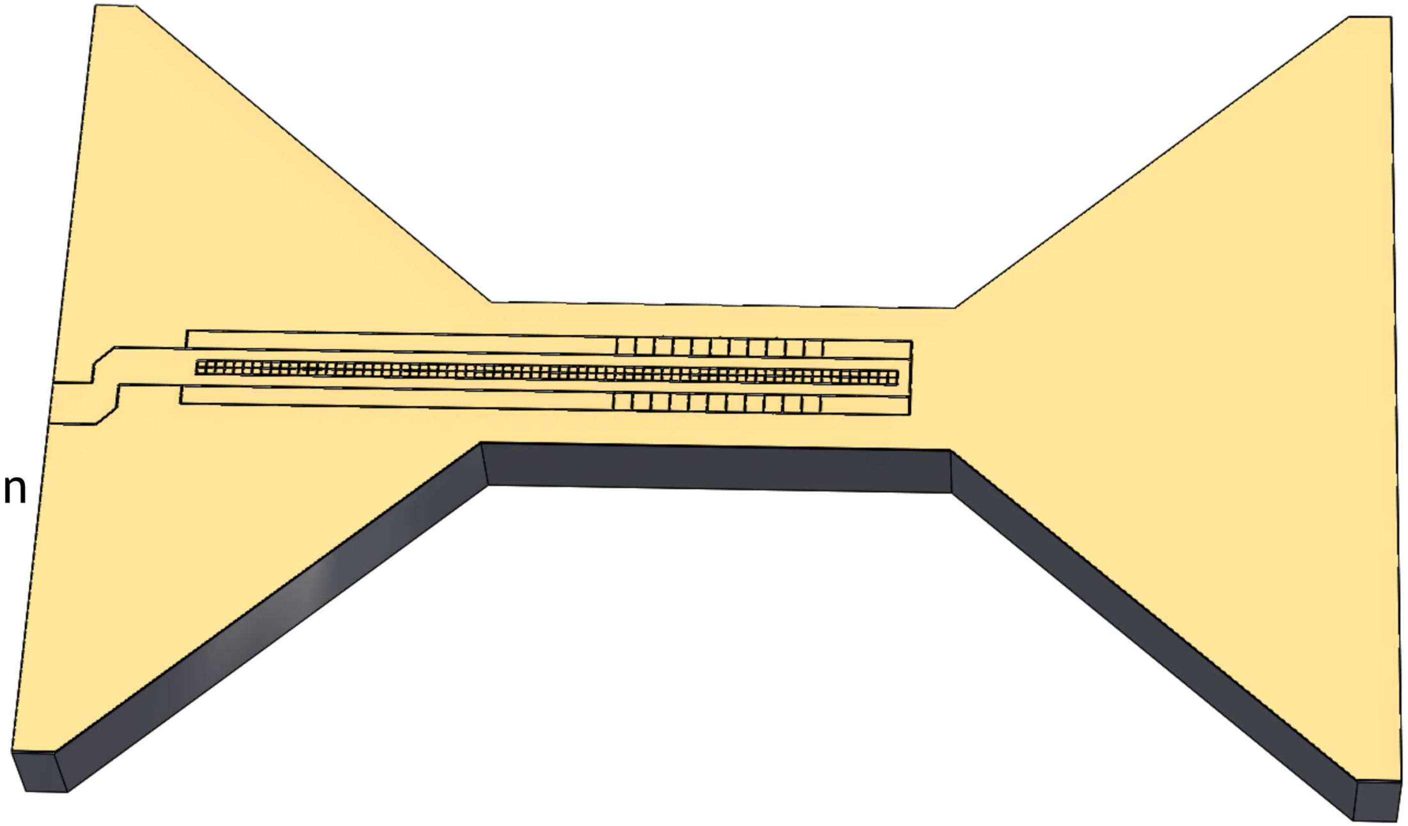
$$P_p = \frac{1}{2} \frac{\omega U^2}{R_p}$$

Raising the Phoenix
QSCOUT Phoenix surface trap

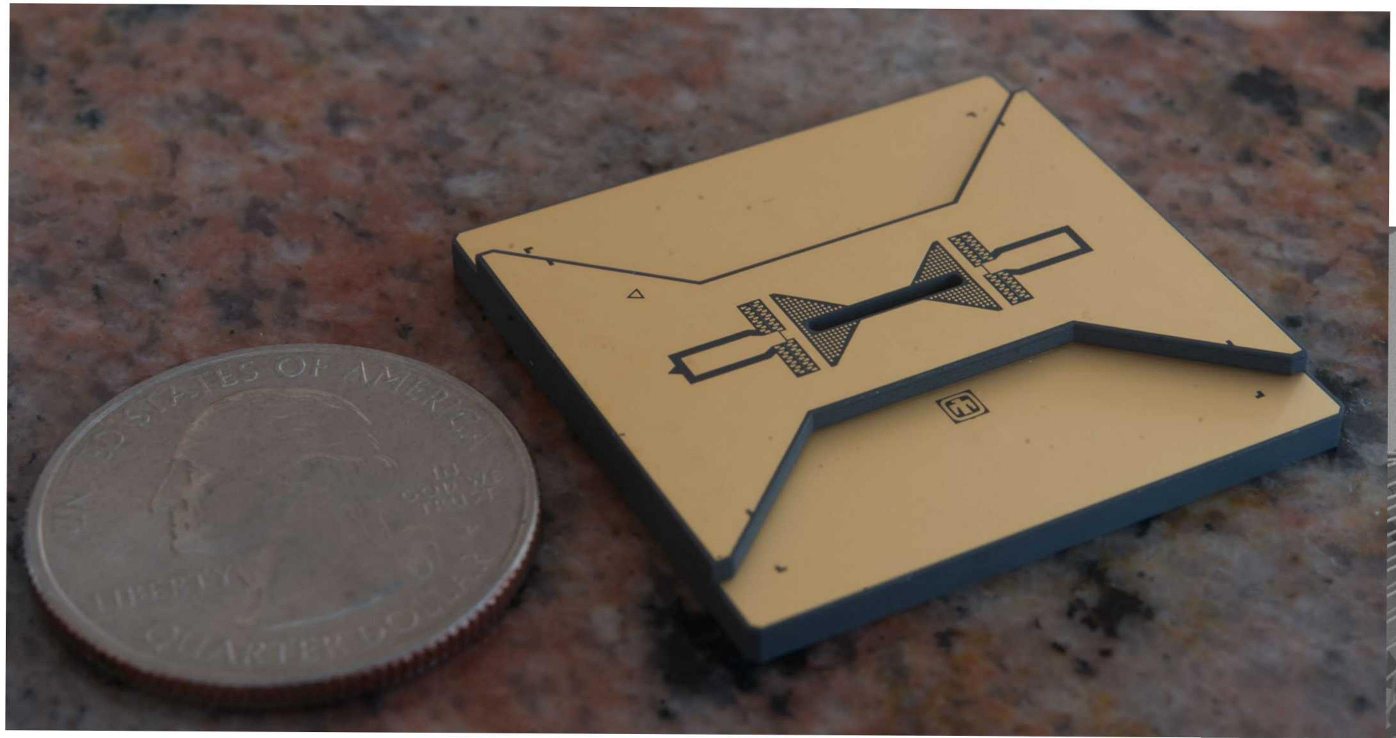
DOE Quantum testbed for Science project QSCOUT
Surface trap fabrication

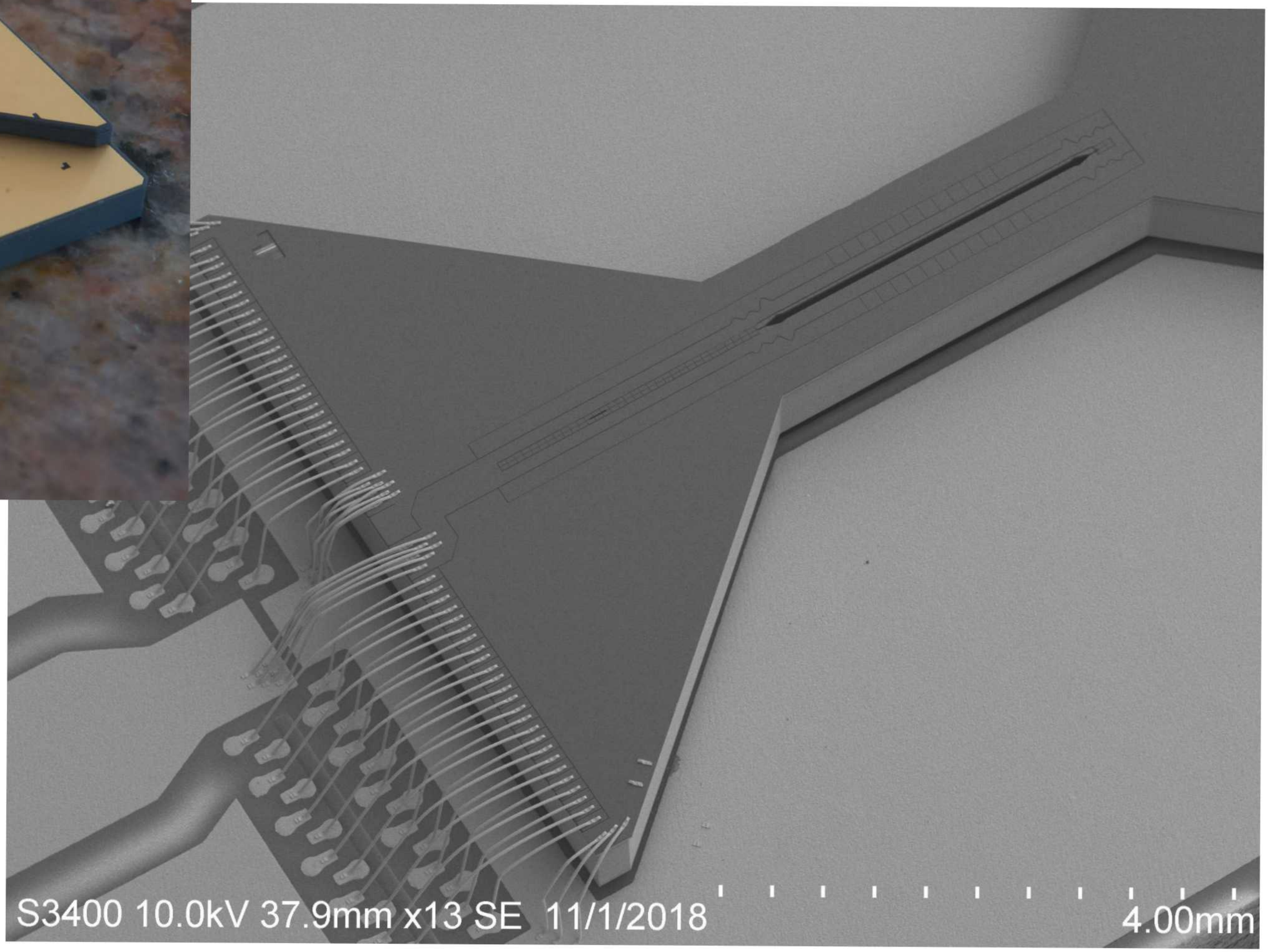
- Co-fabricated with LogiQ Phoenix trap
- Pure surface trap
  all electrodes on top metal layer
- Identical loading hole
- Identical electrode wiring

- Can be available to researchers interested in testing the trap and providing feedback



Custom trap package Is available





Thanks

Trap design and fabrication

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John Rembetski
Paul Resnick
SiFab team

Trap packaging

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Andrew Hollowell
Anathea Ortega
Tipp Jennings

Theory

Setso Metodi
Brandon Ruzic

Trap design and testing

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Craig Hogle
Daniel Lobser
Melissa Revelle
Dan Stick
Christopher Yale

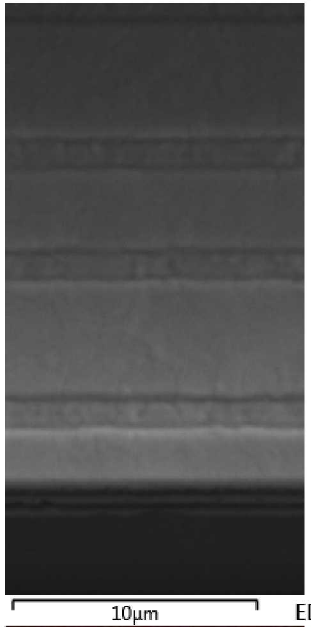
RF Engineering

Christopher Nordquist
Stefan Lepkowski

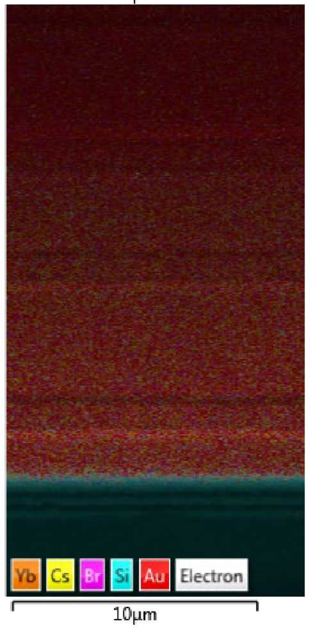
Backup slides

HOA-2 trap characterization
Fast onset charging

Electron Image 2



EDS Layered Image 1

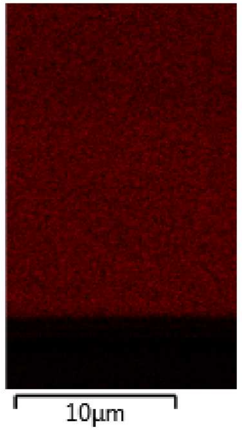


Origin of fast-onset charging

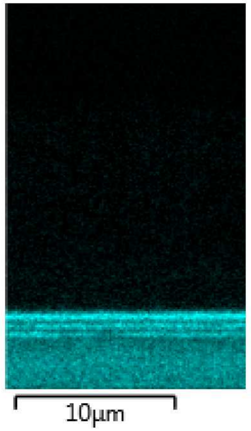
- Slot sidewalls were meant to be covered with evaporated gold
- Not covered due to narrow backside slot
- EDS cannot detect gold on sidewalls, sees silicon instead

- Elevated heating rates were observed above this electrode
- Found Yb particulate (introduced in trapping chamber)

Au L series

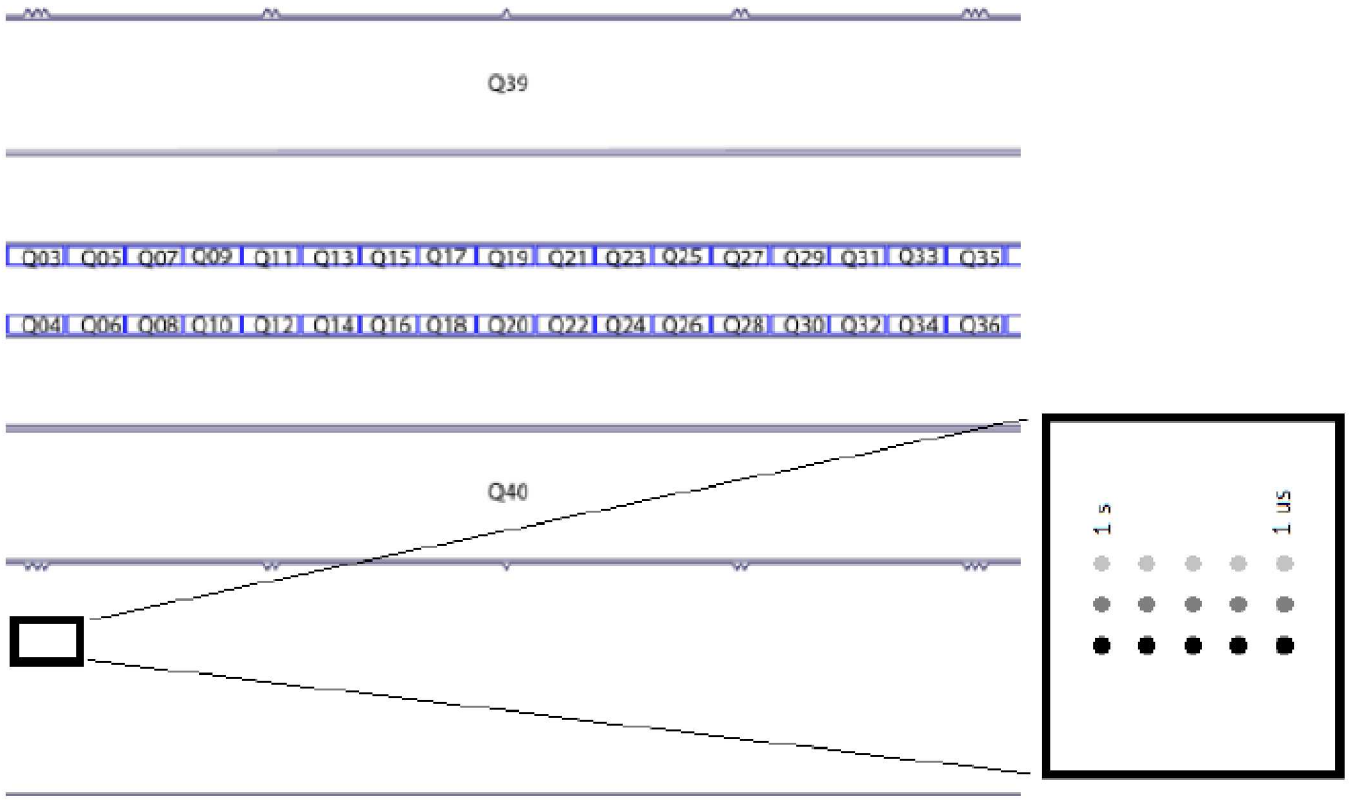


Si K series

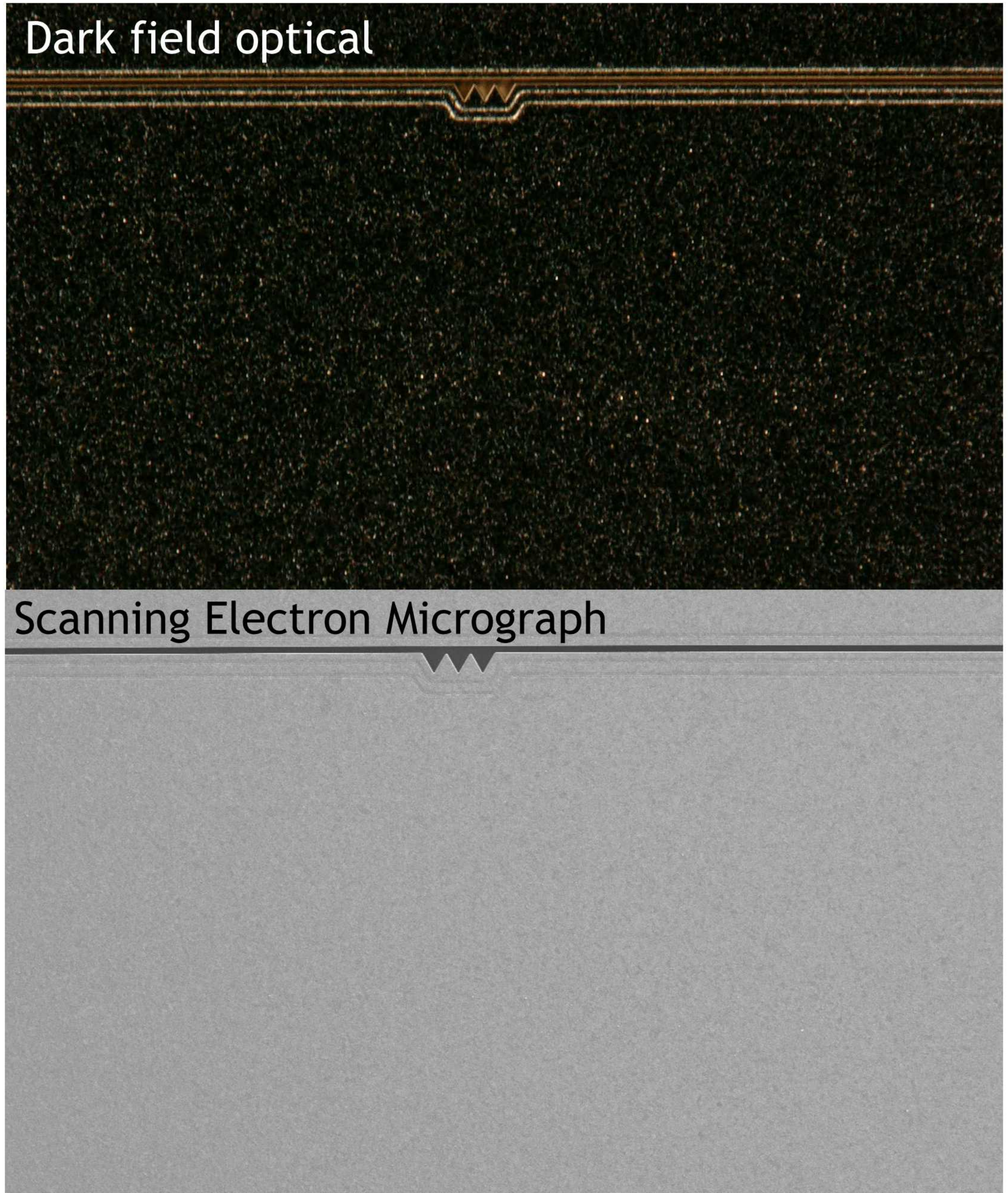


Yb L series

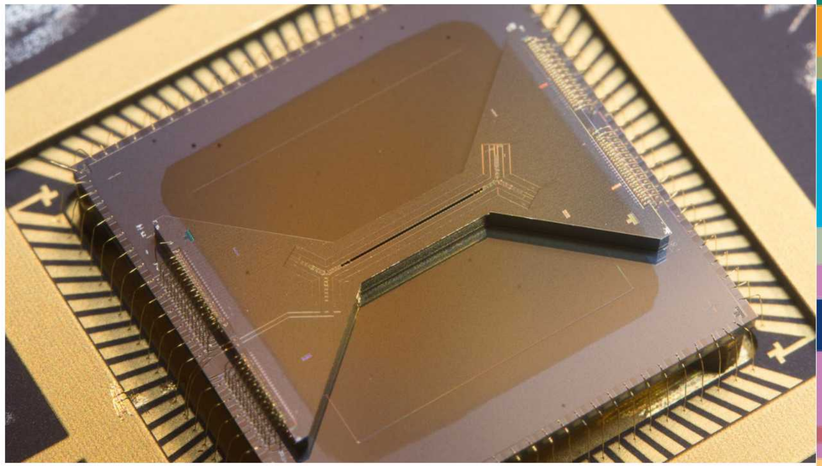
HOA-2 trap characterization
355nm picosecond pulsed power handling of trap surface



- Beam diameter 1.4µm
- 200µW, 450µW, 1mW
- 1µs to 1s exposure
- No damage visible in optical microscope, Electron microscope (SEM), and white light interferometry



HOA-2 trap characterization
Heating rates at room temperature



- HOA-2.0 at room temperature
  - 30/s (Yb, radial, 2.5MHz, parallel to surface, Sandia setup 1)
- HOA-2.1 narrow backside slot with exposed silicon in slot
  - 60/s – 120/s (Yb, radial, 2.5MHz, parallel to surface, Sandia setup 1)
- HOA-2.1 wide backside slot gold coated
  - 200/s (Yb, radial, 2.5MHz, 15º to surface, Sandia setup 2)

- HOA-2.1 wide backside slot gold coated
  - 135/s (Yb, radial, 3MHz, 45º to surface, UMD EURIQA setup
- HOA-2.1 wide backside slot gold coated
  - 220/s (Yb, radial, 2º to surface, Duke room temp system)

Charging

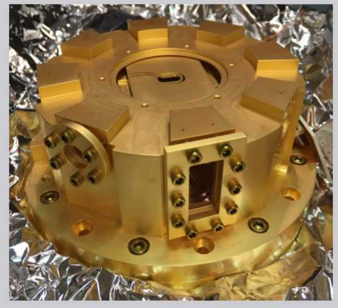
- Fast onset charging observed by Duke team
- On 355nm laser application trap charges in μs discharges in ms

Cryogenic testing system

Cryostat

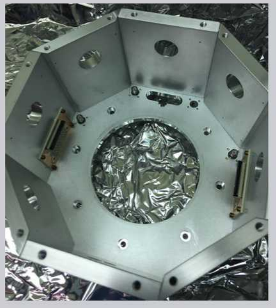
- 4K closed-cycle cryostat with Gifford-McMahn cold head
- He exchange gas to mediate cooling & reduce vibrations

4K Pillbox



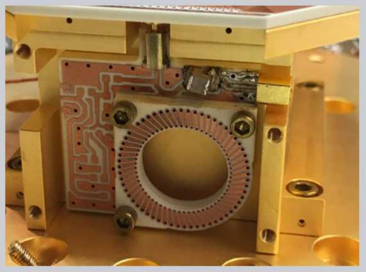
- Housing for trap, resonator, & filter board
- Gold-plated OFHC copper, secured w/ brass screws

40 K Shield



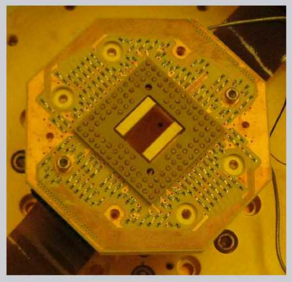
- Intermediate stage for RF & electrical thermal lagging
- Electropolished aluminum, secured w/ brass screws

Internal RF Resonator



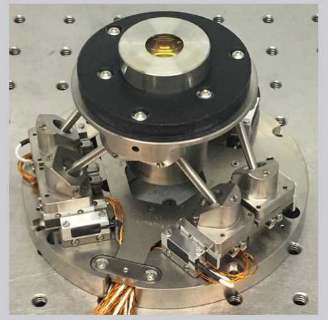
- PCB toroidal inductor in parallel w/ capacitive trap
- 637 nH + 15.6 pF → 47.4 MHz resonance

DC Voltage Delivery



- 300K → 40K: Micro-D cable w/ Kapton coated 32 AWG
- 40K → 4K: Kapton flex cables
- 4K: RC filter board (100 kHz)

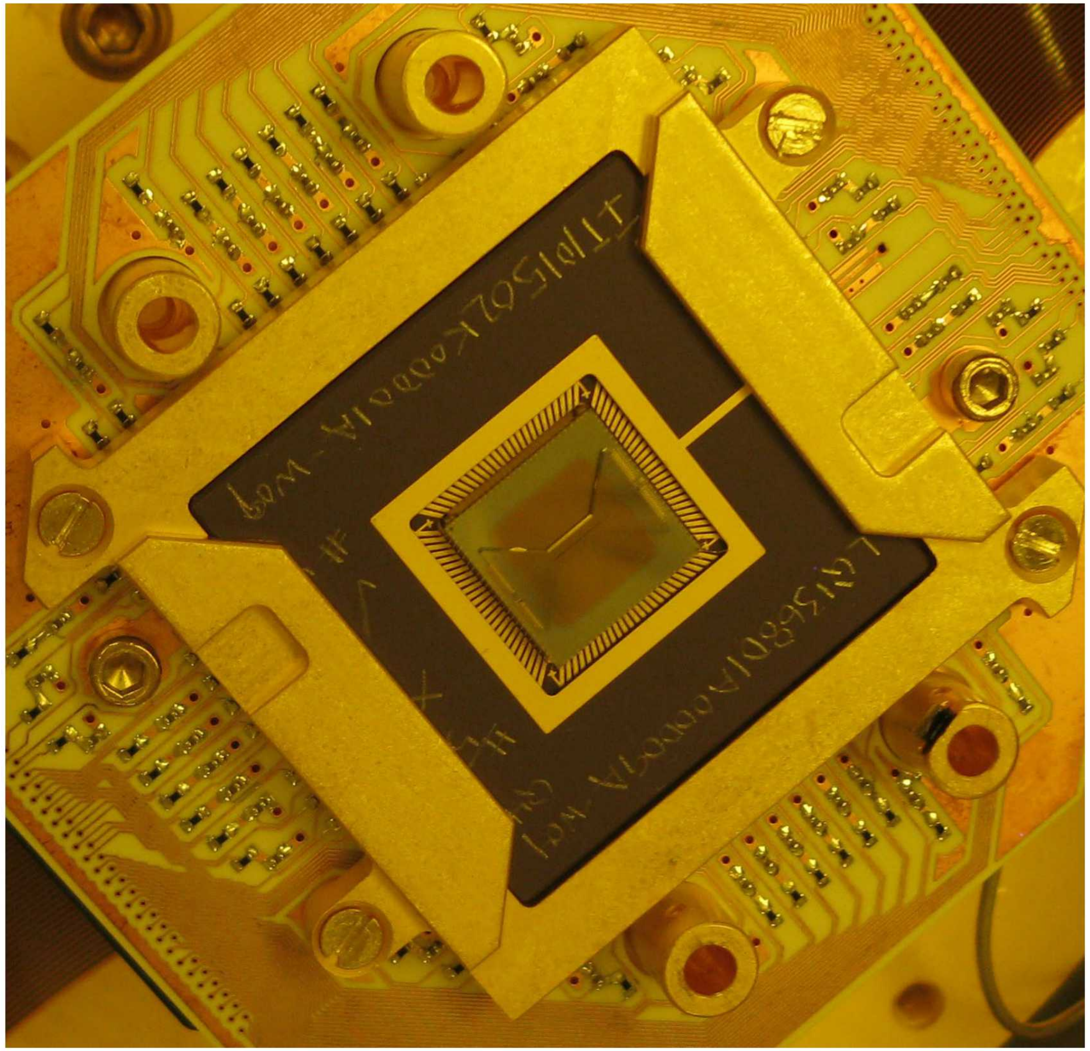
Internal Lens Hexapod



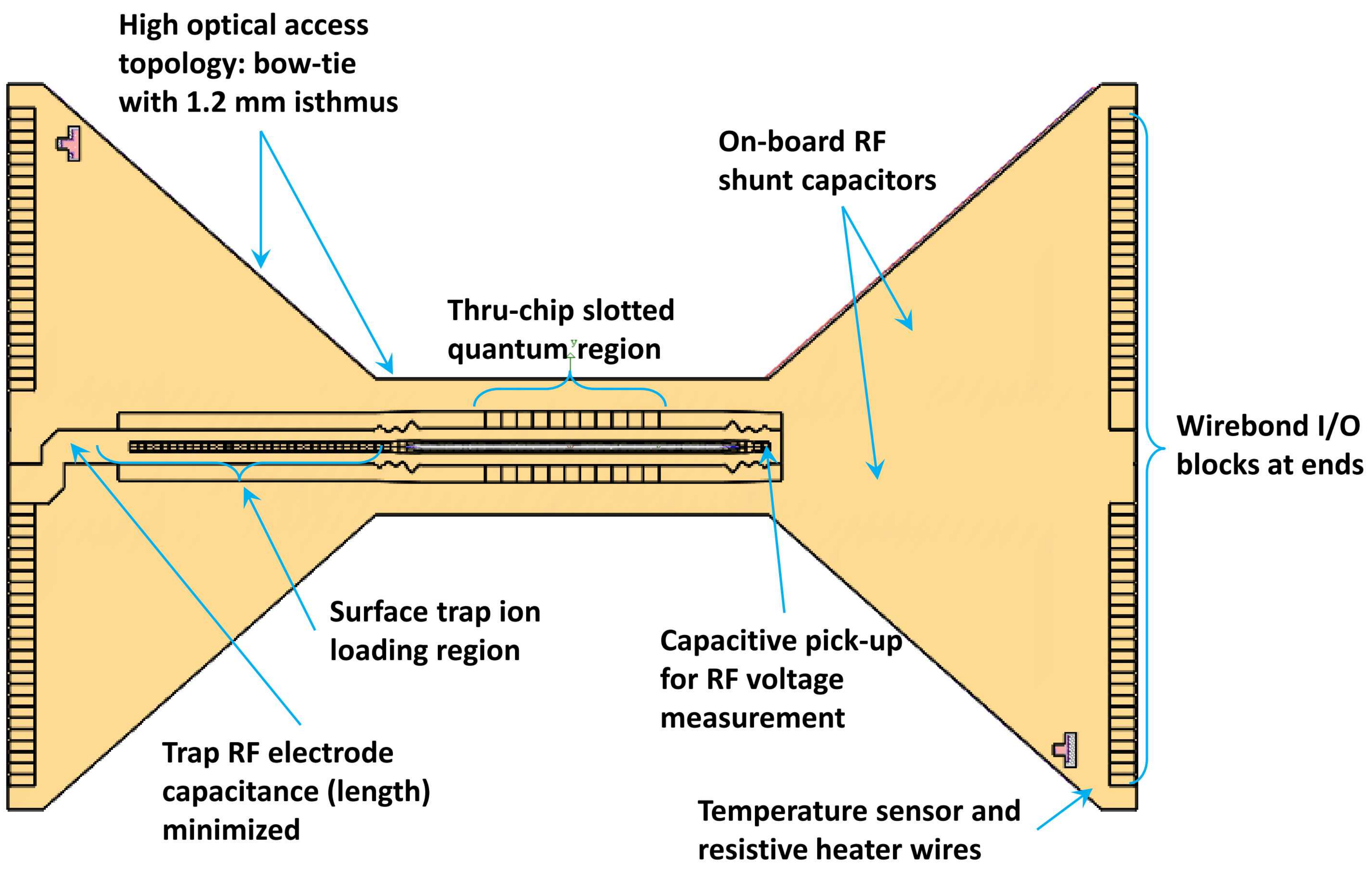
- 0.6 NA, 355-370 nm, 7.6 mm WD, 100 µm FOV
- 6-axis hexapod, trap-suited travel range, 40 K, non-mag

Ablation loading of ytterbium

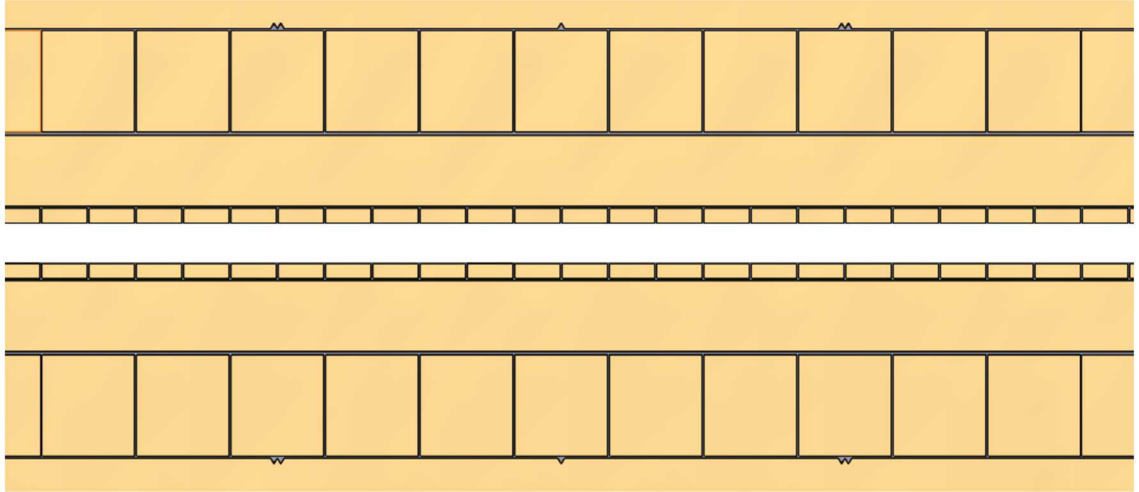
- Concern over thermal oven on cold plate (~3 W for 1-5 min.) provided impetus to investigate ablation loading
- Fluences < 300 mJ/cm^2 only locally heat in spot size for neutral atoms
- Yb target installed on microwave antenna support post
- SpectraPhysics ns-pulsed fiber laser (1064 nm, 3-250 ns pulses, variable rep rate, 4-1000 μJ pulse energy)



Phoenix trap fabrication
Original plans for Phoenix

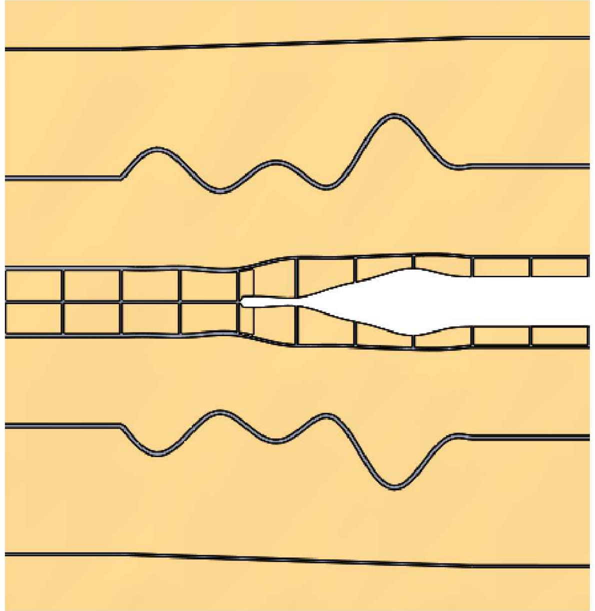


Phoenix trap fabrication
Trap features



Quantum region

- Segmentation of 22 inner electrode pairs and 11 outer pairs for better control of ion chains and spatial re-ordering of ions
- 22×70µm = 1540µm long
- Ion height 70µm

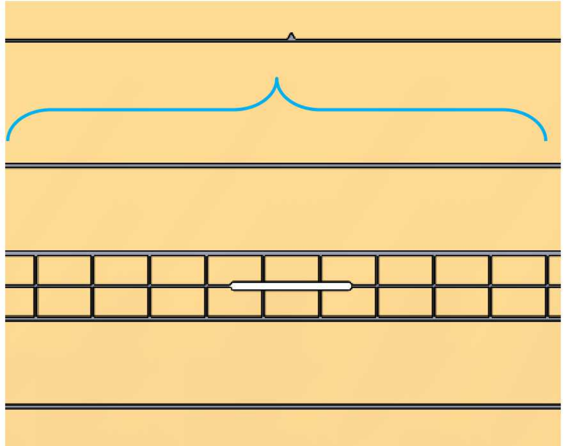


Transition

- 22 degrees of freedom
- Low spatial frequencies

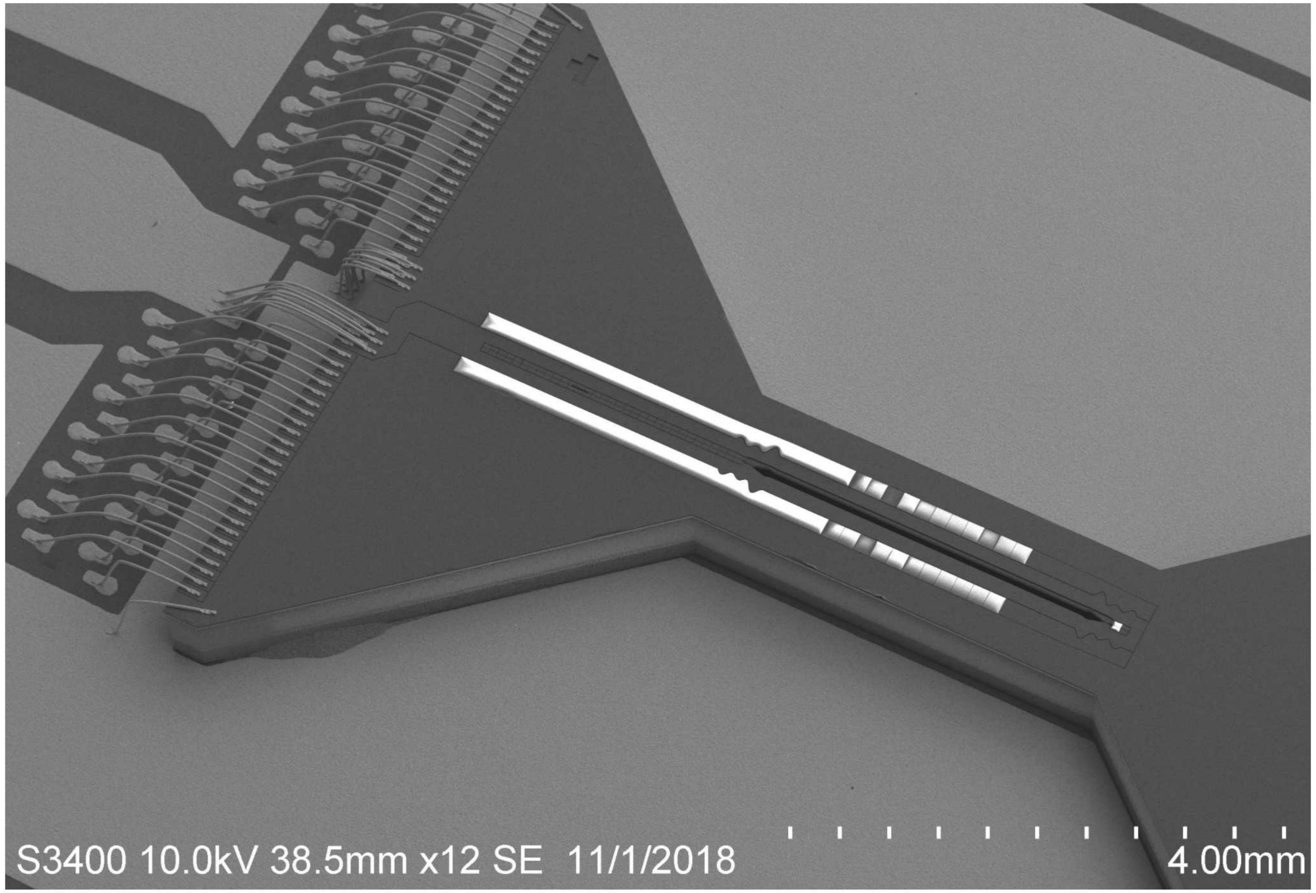
Loading region

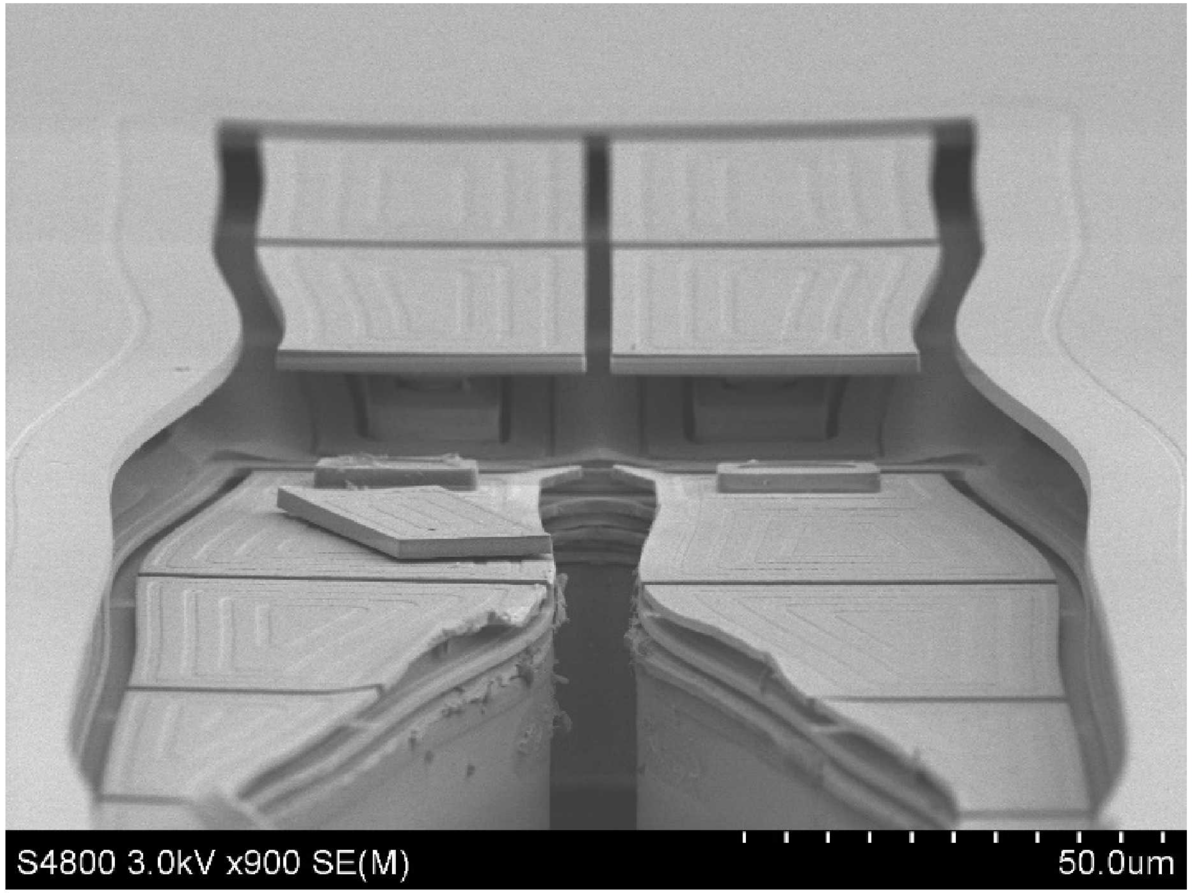
- 5 electrode pairs
- Loading slot 180um x 3um



Phoenix trap fabrication
Fabrication challenges

Problems in release of devices (oxide removal)
Likely due to problems in oxide deposition

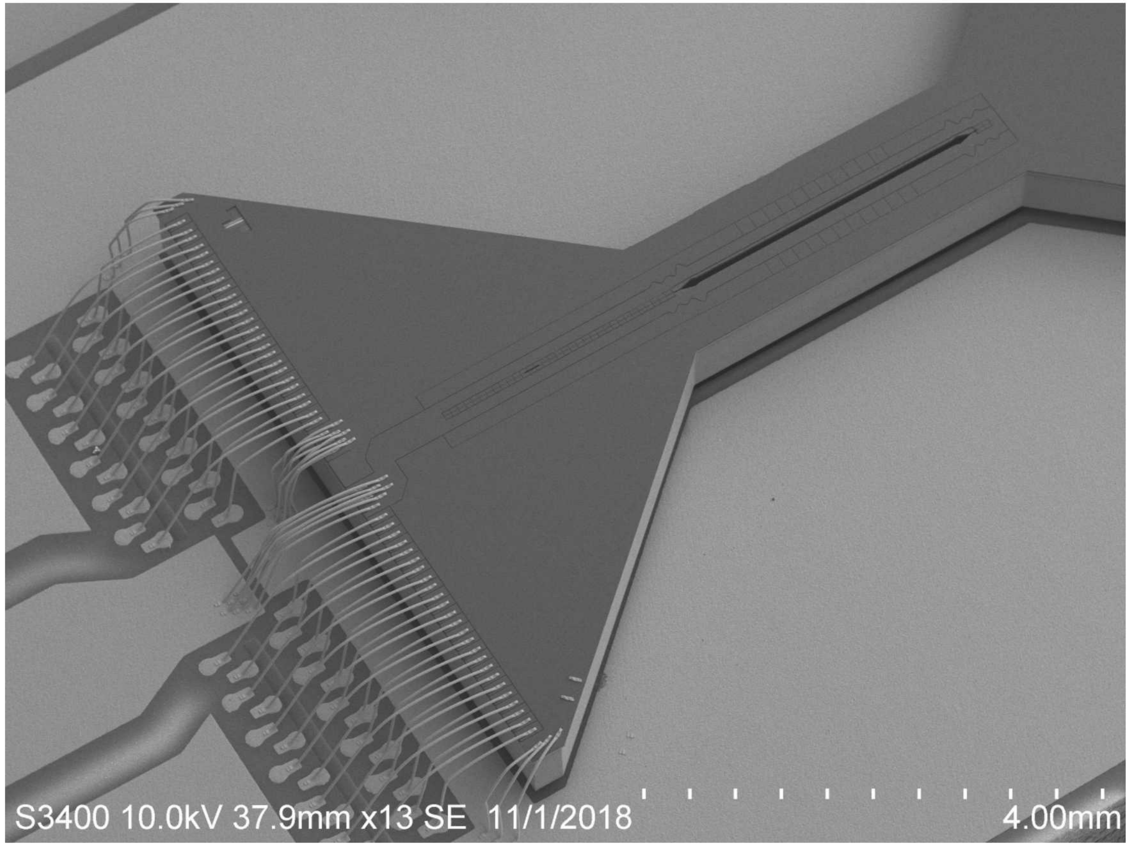


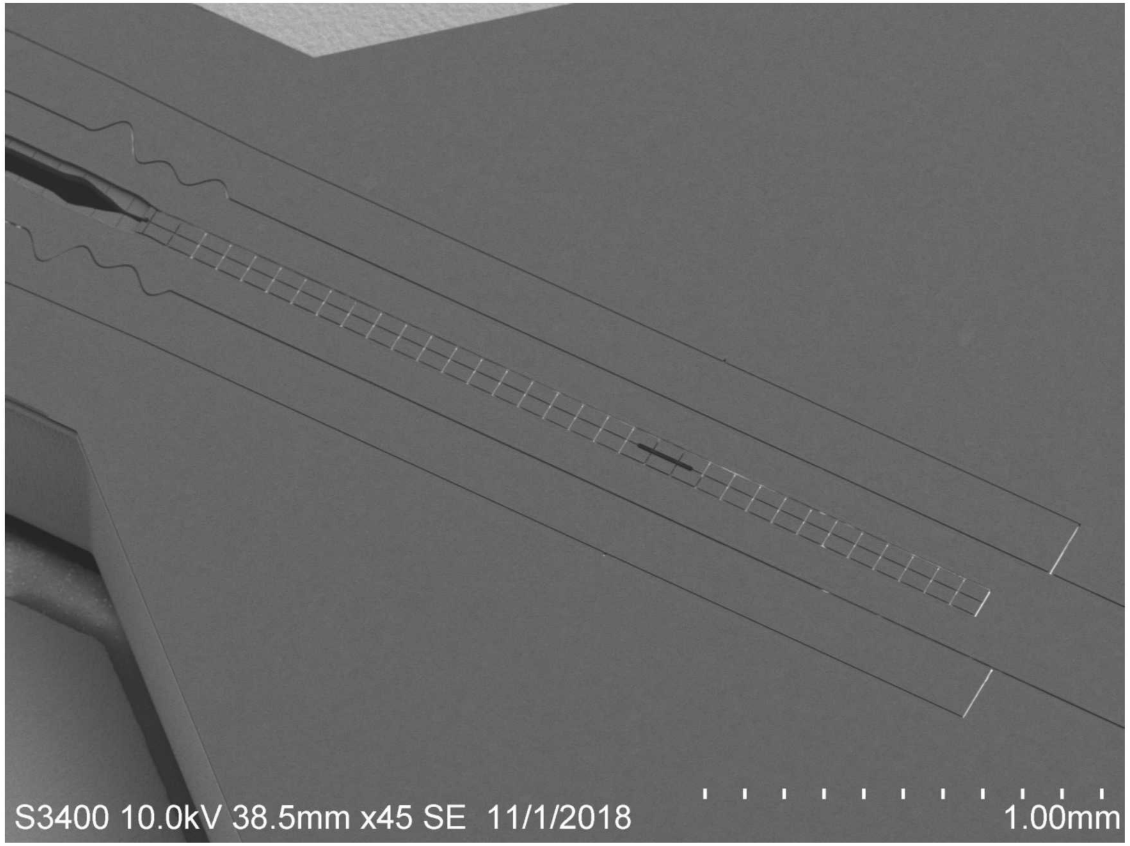


- Electrically unconnected (floating) electrodes
- Missing electrodes

Phoenix trap fabrication
Current status

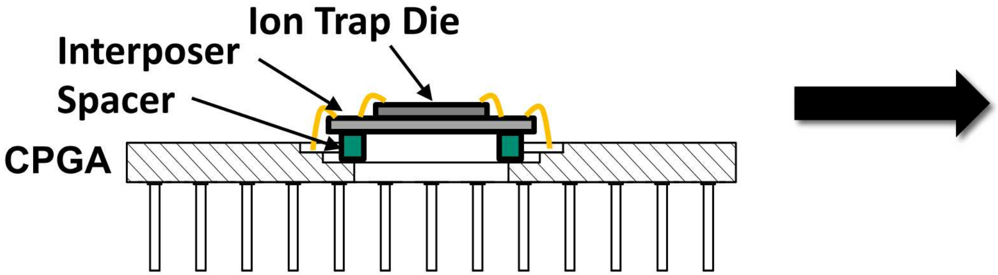
- Several optically good die are released
- To be packaged in January
- Might yield a small number of functional traps
- Traps might have remaining oxide between trap electrodes



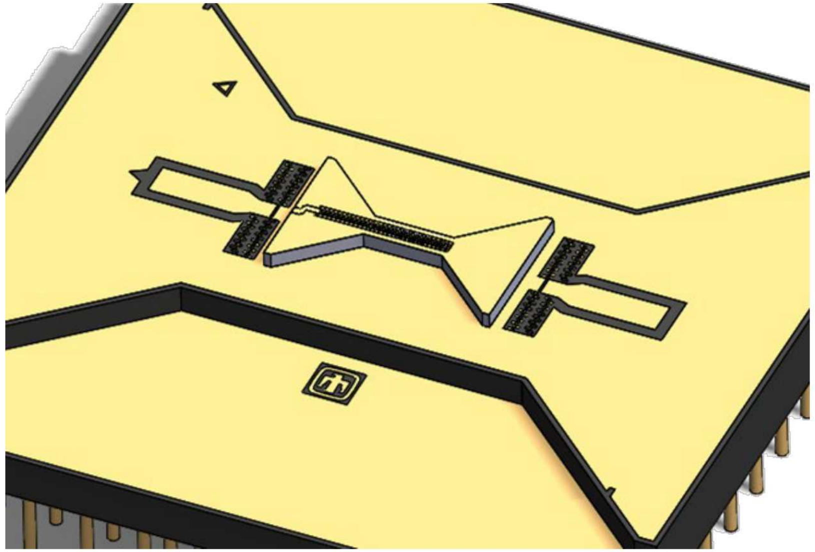


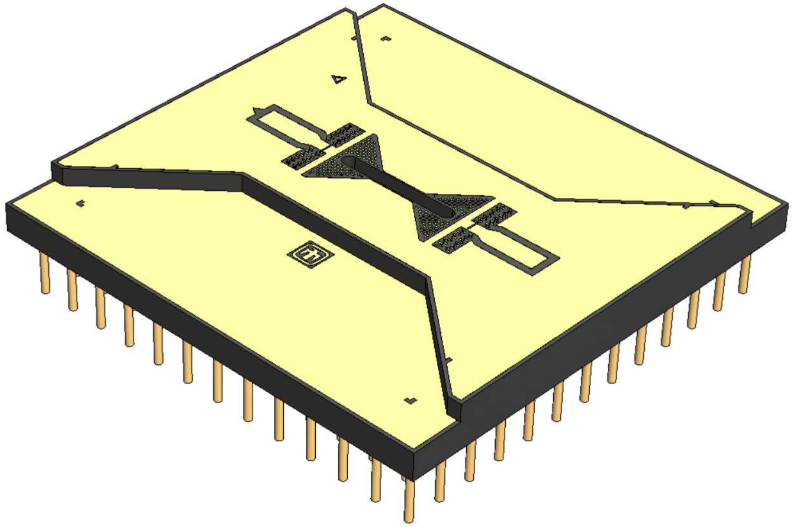
Custom trap package

Legacy 4 Level CPGA Packaging Assembly



Simplified 2 part assembly





Objectives:
- Improved rf- and ground performance
- Compatible with bowtie chip without interposer
- Simplified assembly
- Backwards compatibility with MQCO package

Properties:
- AlN for improved thermal conductivity and reduced thermal expansion vs Al_2O_3
- Two rf connections with minimized capacitance (3pF) and resistivity (50mOhm)
- Backwards compatible with prior HOA devices
- Metal coverage of top surface
- All metal is signal or ground (no floating metals)

Raising the Phoenix
Revised Phoenix designs

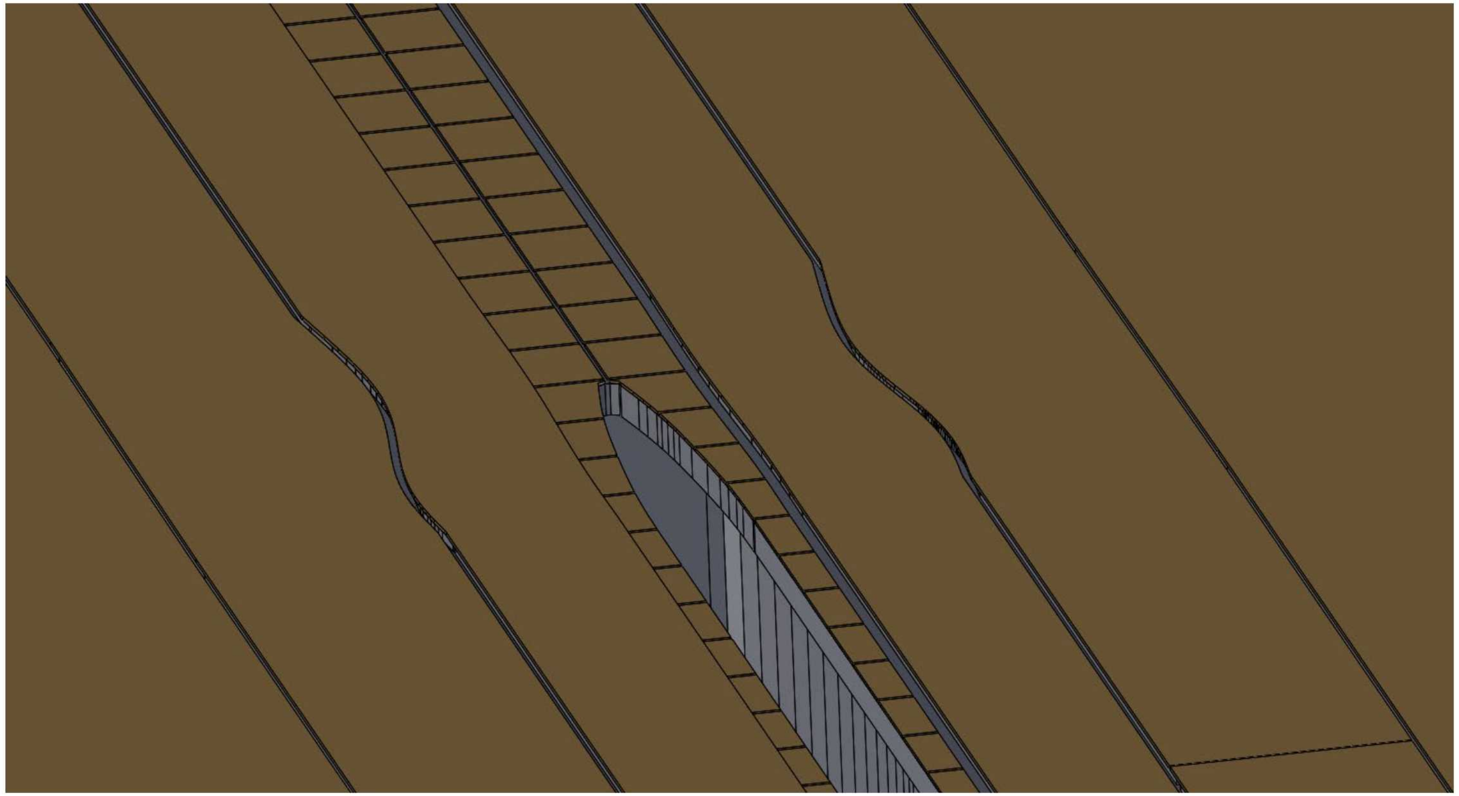
Objective is to refabricate Phoenix with low risk improvements to trap design

Phoenix changes:

- Use latest processes and design rules
- Modify design to reduce fabrication risk
- and resilient to fabrication errors

Trap changes:

- All inner control electrodes on lower metal layer
    - Smaller modulations on transition
    - Smaller potential barrier
    - Smaller variations on trace of curvature tensor



Conclusion

Instantaneous charging

- Thanks for your patience and excellent characterization of charging
- Solved charging of exposed silicon in slot by revising backside gold coating process
- All traps deployed at LogiQ performers have full sidewall coating
- Exposed silicon might lead to high heating rates at cryogenic temperatures

- However, charging and heating rates observed by at cryogenic temperatures by Innsbruck team in traps with gold-coated sidewalls needs to be investigated

Phoenix trap

- Challenges due to fabrication inconsistencies
- Expect to have traps for testing
- Fabrication lot to raise the Phoenix is running
  - Improved transition design
  - Surface trap version will also be available