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A summary of hybrid-CMOS (hCMOS) imaging sensor development at Sandia National Laboratories

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ABSTRACT

The hybrid-CMOS (hCMOS) effort at Sandia National Laboratories has worked to develop high-speed, multi-frame, time gated Read Out Integrated Circuits (ROICs), and a corresponding suite of photodetectors to image a wide variety of High Energy Density (HED) physics experiments for the nations primary HED research facilities which include; the Sandia Z-Machine, the National Ignition Facility (NIF) at Lawrence Livermore National Laboratories, and the Omega facility at the Laboratory for Laser Energetics (LLE). This multiyear effort has led to the establishment of a stable supply chain for the design, fabrication, integration, and testing of these sensors. The hCMOS program has created several different ROICs/detectors with 25µm pixel spatial resolution, 2-4 frames of in-pixel storage and minimum integration time of 1.5-2ns. Three different sensors have been deployed in multiple diagnostic systems across each of the HED research facilities. The architecture of the SNL hCMOS sensor will be presented along with details of each subcomponent. A listing of all fielded hCMOS sensors and a performance summary will also be presented.

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Keywords: ASIC, multi-frame, pixel, ROIC, hybrid-CMOS, high-speed, Ultra-fast X-Ray Imager

1. INTRODUCTION

Many existing High Energy Density (HED) physics diagnostic used for time gated X-ray imaging and spectroscopy in the 0.1-10 ns range rely on gated Micro-Channel Plate (MCP) detectors. The performance of these detectors are limited due to their ability to only capture a single image frame along each line of site, small to moderate dynamic range, and difficulty in establishing and maintaining calibration. Hybrid CMOS (hCMOS) sensors have the potential to overcome many of the existing MCP limitations. The need for high-speed shutters over multiple frames is required to image non-repeatable fast plasma evolution in HED physics experiments. The high-speed nature and single line of site needs for these experiments is conducive for implementing image sensors using a burst mode architecture [1]. This architecture implements multiple storage nodes with in each pixel that can capture an image at high-speeds and then read off the images at much slower speeds after the experiment has completed. The trade space for burst mode imagers are set by balancing the needs between pixel size, number of frames, dynamic range and array size. It is often the case that the imaging application often dictates which design trade space element is prioritized [1].

The development of hCMOS sensors at Sandia National Laboratories (SNL) has spanned multiple years with several sensors designs and cycles of learning. Design trade space targets have focused on 25µm pixels, 4 frames per pixel, 1000:1 dynamic range and a 1024 row by 512 column pixel array. Early sensor designs focused on the size, number of frames, dynamic range of the pixel, and the ability to detect photons in multiple spectrums (532 visible and 4-6 keV X-ray). These early designs also helped solidify the overall architecture used to create subsequent and better performing sensors that incorporated larger pixel arrays and the addition of unique high-speed shutter timing features that have made these sensors a transformational diagnostic in the HED physics community.

2. SNL hCMOS Sensor Architecture

The high-speed, multi-frame sensors developed at SNL are hybrid devices. This is to say that circuitry responsible for capturing, storing and reading out the image data is fabricated on one silicon substrate while the circuit that converts incident radiation into electrical current is fabricated on a different substrate. The two substrates are joined (hybridized) by a bonding layer. The bonding layer provides mechanical and electrical connections between pixels on each device to form the final "hybrid" sensor (Figure 1).

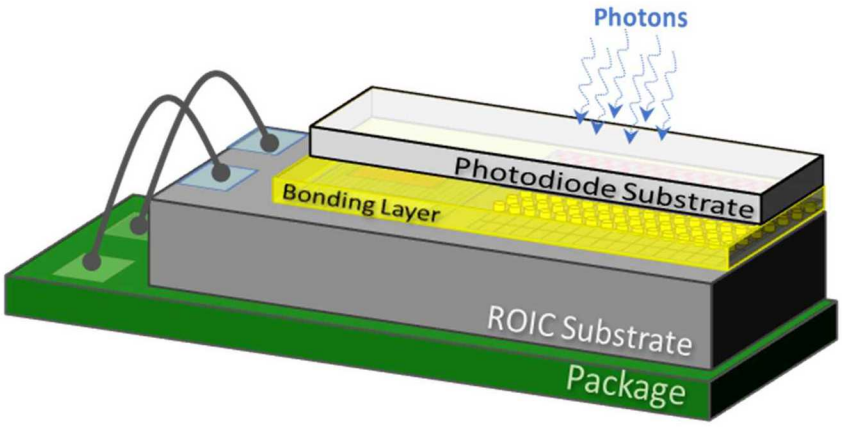

Figure 1 - Cross Section of hCMOS Sensor

The two circuits described and depicted above that make up a hybrid sensor are; the Readout Integrated Circuit (ROIC) and the photodiode array. Having the ROIC and photodiode array fabricated on different substrates enables the optimization of both devices for a given application or radiation. Conventional imaging sensor are limited in this respect because both the ROIC and photodiode are fabricated on a single substrate. The subsequent sections describe the general architecture and requirements of both the ROIC and photodiode array.

2.1. hCMOS ROIC Architecture

The primary function of the ROIC in the hCMOS sensor is to manage the capture, storage, and readout of multiple frames of electrical charge generated in the pixels of the photodiode array. The ROICs developed for the SNL hCMOS effort have been designed and fabricated at Sandia's Microsystem and Engineering Sciences Applications (MESA) facility using the CMOS7 350nm fabrication process. The primary goals that have guided the development of hCMOS ROICs and set the design trade space are listed in Table 1. These goals helped to

ROIC DESIGN TARGETS	VALUE
Number of Pixels	0.5 M-pixels
Number of Frames	4 or greater
Minimum Integration Time	2ns or less
Minimum Inter-frame Time	2ns or less
Dynamic Range	1000:1, 60dB (10-bit)

Table 1 – hCMOS ROIC Primary Design Targets

define a custom "Burst Mode" architecture that has established a foundation for all hCMOS ROICs created thus far. This architecture creates multiple high-speed shutter signals with cause the simultaneous sampling of charge generated by the photodiode by pixel (global shutter). The sampled charge is stored on multiple storage elements within each pixel (one storage element for each frame of data). The global shutter generation and sampling of the photodiode charge onto multiple frames happen at the integration and inter-frame time settings (Figure 2). After all shutter signals have been issued, the stored charge can be read off

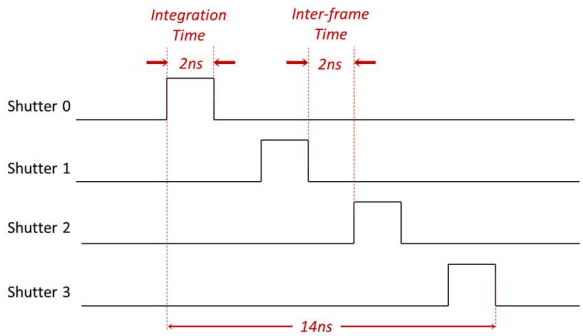

Figure 2 - High-speed Shutter Integration and Inter-Frame Time Example

the pixel array at much slower speeds. The hCMOS ROIC architecture has three primary phases of operation. These phases are;

Configuration
The shutter integration time and inter-frame time generation settings for each frame are configured by the user (Figure 2), all image storage elements in the pixel array are cleared, on-chip shutter diagnostic outputs are cleared, and the ROIC set to receive a trigger from the facility.

Image Capture
The high-speed shutter signals are created and propagated to the pixel array after receiving a trigger from the facility. Each shutter signal activates a corresponding electronic switch in the pixel which samples the input from the photodiode onto a corresponding charge storage element in the pixel.

Readout
The charge stored in each pixel storage element is read out of the pixel array in a random access manner by issuing a row, column, and frame address.

ROIC specifications such as pixel size, the amount of charge captured by each frame (frame full well), and high-speed shutter generation/distribution have been determined by balancing the interdependencies between the primary design targets and the ROIC imaging application. Table 2 lists design specifications that are common across all hCMOS ROICs.

SPECIFICATION	VALUE
Pixel Size	25µm x 25µm
Shutter Timing Skew	10% or less
Frame to Frame Gain Error	10% or less
Noise Floor	500 e^-
ROIC Triggering	Asynchronous

Table 2 - Common hCMOS Specifications

Figure 3 depicts the general architecture for hCMOS ROICs developed at Sandia. The next sections give a brief description of each design block thus outlining the primary functions of the ROIC.

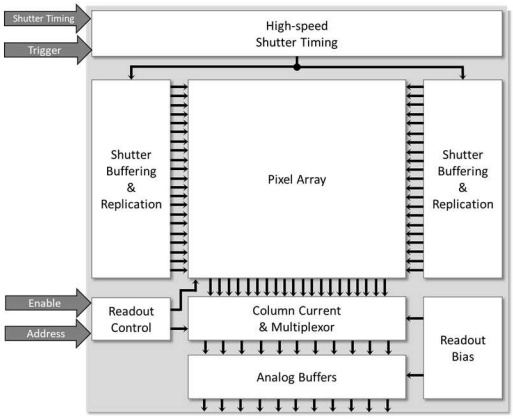

Figure 3 - SNL hCMOS ROIC Architecture

2.1.1. High-speed Shutter Timing

One of the primary design targets for the hCMOS ROICs called for the creation of on-chip, low jitter and repeatable high-speed shutters. This function is performed in the High-speed Shutter Timing (HST) block. During the ROIC configuration phase a user programs a desired shutter integration time and shutter inter-frame time for each frame into a pattern generator. The integration and inter-frame times can be different for each frame if the total sum of all frame integration and inter-frame times is less than the size of the pattern generator register. A fast start low jitter oscillator is used to clock the pattern generator once a trigger input is received from the facility.

2.1.2. Shutter Buffering and Distribution

This logic takes the shutters created by the HST block and buffers them across many millimeters and then replicates the shutter signal (one for each row in the pixel array). The replication is performed using a binary replication tree where a single input is buffered and driven to two outputs. The final shutter signals for each row then pass through a final buffering stage that is sized to provide adequate drive across the row of the pixel array.

2.1.3. Pixel Array

The pixel array is made up of N rows and M columns of pixels shown in Figure 4. The pixel is 25µm x 25µm and contains three to four frames of storage. A Metal-Insulator-Metal capacitor is used to store charge for each frame. All frames sample the same photodiode input and the sampling is controlled by the shutter

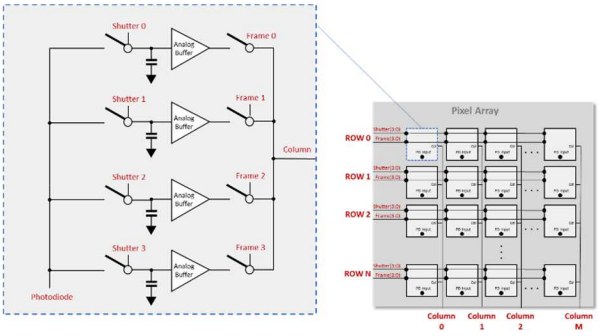

Figure 4 - hCMOS Pixel and Pixel Array

inputs. Readout of the charge stored on the capacitors is controlled with the frame control signals onto a common column output bus.

2.1.4. Readout (*Column Current & Mux, Readout Control/Bias, Analog Buffers)*

The blocks responsible for reading the stored data from the pixel array are the Readout Control/Bias, Column Current & Multiplexor and Analog Buffer. Random access addressing of the pixel array is accomplished by presenting a row, column, and frame address to the Readout Control block. The block decodes the addresses and sets the appropriate frame switches on the decoded row of the pixel array and activates the correct channel of the Column Multiplexor. The Column Current & Multiplexor block provides a current bias to the analog buffers in each pixel. The buffers convert the stored charge in each pixel to a voltage that can be read off the array. The Column Current & Multiplexor block also selects which column of the pixel array is sent to the Analog Buffer block based on the column address decoded by the Readout Control block. The Readout Bias block provides stable voltages and currents to the Column Current and Analog Buffer blocks. The Analog Buffer provides adequate drive current to the voltage that is being read off the pixel array and sent off-chip.

2.2. hCMOS Photodiode Architecture

The pixelated photodiodes created for the hCMOS sensors are fabricated on silicon substrates and act as a transducer converting photons of specific spectra into electrons which are collected by the ROIC. The photodiodes developed for the SNL hCMOS effort have been designed and manufactured at Sandia's MESA facility using a custom fabrication process. The primary goals that have guided the development of hCMOS photodiodes are listed in Table 3. These goals have driven the development of photodiodes that are sensitive

ROIC DESIGN TARGETS	VALUE
Visible Light Sensitivity	532nm
X-Ray Sensitivity	4-6 keV
Electron Sensitivity	4-5kV
Conversion Efficiency	60% or greater
Absorber Type	Silicon
Pixel Size	25µm x 25µm

Table 3- hCMOS Photodiode Primary Design Targets

to multiple spectra of radiation making them useful temporal and spatial detectors for HED applications where the radiation being detected is often present for a very short amount of time (nanoseconds). The hCMOS photodiodes are created as P-I-N diodes and used in a reverse bias configuration with either a common cathode or anode depending on the absorber doping (n-type or p-type). This configuration sets the photodiode into a current mode where the output current is proportional to the incident flux and energy of the radiation. The P-I-N structure of the diodes makes speed and efficiency dominated by drift (charge carrier velocity) rather than diffusion processes. A cross section of an hCMOS photodiode is depicted in Figure 5. The next sections describe the photodiode architecture in greater detail.

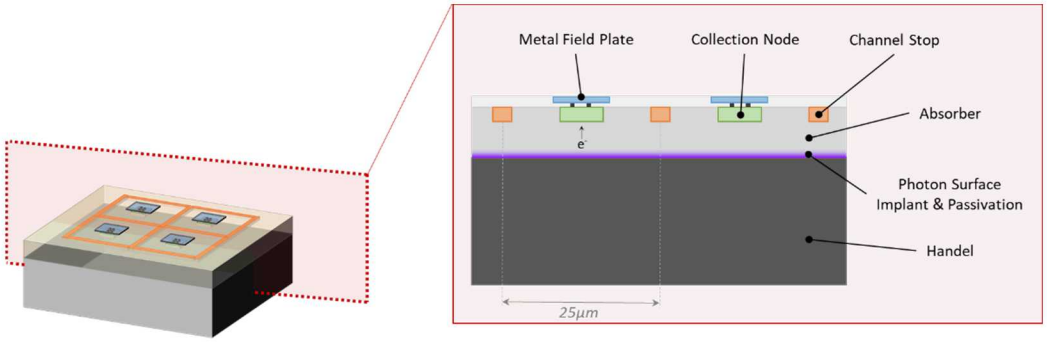

Figure 5- hCMOS Photodiode Cross Section

2.2.1. Handel

The function of the Handel is to act as a carrier that provide mechanical stability to the photodiode array while it is being fabricated. The Handel is typically a silicon wafer bonded to a high purity epitaxial absorber. The Handel can be 2-40X thicker than the absorber with the optimal fabrication height of the Handel and the absorber being less than 800 µm. The Handel Silicon is removed after the photodiode array is hybridized to a ROIC.

2.2.2. Absorber

The Absorber is a high purity layer of semiconductor material that is used to stop an incident photon and convert it into charge carriers. The thickness and material/surface properties of the Absorber determine how many photons of a given radiation energy are stopped and converted (conversion efficiency). The hCMOS sensors make use of silicon absorber layers with thicknesses of 8 to 200 µm. The absorber acts as the intrinsic area in the P-I-N diode and a 50V reverse bias is placed across the absorber to set-up the needed electric field to drift charge carriers generated across it.

2.2.3. Photon Surface Implant & Passivation

The Photon Surface Implant & Passivation region of the hCMOS photodiodes is the area that is exposed to incident photons after the photodiode is hybridized to the ROIC. This region is implanted (either P^+ or N^+) and is "common" (electrically shorted) across the entire photodiode array making it either the common cathode or common anode of the array. The reverse bias voltage used to create an electric field in the Absorber is applied to this surface. Passivation of this surface enhances the sensitivity of the photodiode to lower energy photons by reducing the number of surface traps. In addition, passivation of this surface using oxide or nitride layers can create anti-reflection coatings further increasing the overall efficiency of the photodiode to spectra in the visible wavelengths.

2.2.4. Collection Node

The Collection Node is doped the opposite polarity as Photon Surface Implant thus completing the formation of the P-I-N diode structure. The size of the collection node is adjusted to minimize diode junction capacitance seen by the ROIC as well as to maximize the diode breakdown voltage.

2.2.5. Metal Field Plate

The Field Plate of the diode is a layer of metal used to help shape the electric filed at the Collection Node. The sizing of this metal is also adjusted minimize diode junction capacitance seen by the ROIC as well as to maximize the diode breakdown voltage.

2.2.6. Channel Stop

The Channel stop is a structure in the photodiode used to minimize charge sharing between neighboring pixels by breaking the path for charge carriers to move along the Collection Node surface side of the diode. This area is implanted with the same polarity as the Photon Surface Implant.

3. SNL hCMOS Sensor Features and Performance

The SNL hCMOS effort has created a linear lineage of different sensors designs to satisfy the needs of imaging applications on HED facilities. The sensor designs are built upon the same general ROIC and photodiode architectures and each employ unique features that enhance it's performance over subsequent designs. Table 4

SPECIFICATION	Furi	Hippogriff	Icarus
Year Developed	2014	2015	2016
Minimum Integration Time	1.5ns	2ns	1.5ns
Minimum Inter-frame Time	1.5ns	2ns	1.5ns
Frames per Pixel	2	2	4
Pixel Array	1024 row x 448 column	1024 row x 448 column	1024 row x 512 column
Pixel Size	25µm	25µm	25µm
Capacitor Full Well	1,500,000 electron	1,500,000 electron	500,000 electron
Dynamic Range	1000:1	1000:1	1000:1
Photodiode Absorber	Silicon (p-type intrinsic)	Silicon (p-type intrinsic)	Silicon (n-type intrinsic)
Photodiode Absorber Thickness Variants	25µm	25µm, 100µm	8µm, 25µm, 100µm

Table 4 - hCMOS Sensors Developed and Fielded

lists the sensors that have been manufactured at SNL to date with subsequent subsections expanding on the features of each sensor [1][2][4].

3.1. Furi Sensor

The first large-scale sensor with a two-dimensional pixel array developed at Sandia was the Furi sensor (Figure 6). Furi was created with two frames of on pixel storage with a one and a half million electron full

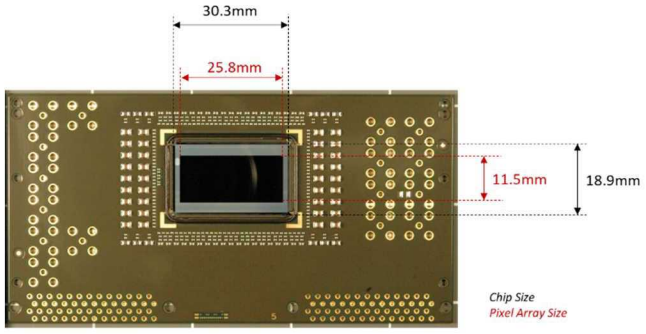

Figure 6- Furi Sensor

well. Furi was the first large scale imager to incorporate a unique shutter generation logic that gives a user discrete control of the integration time and inter-frame timing between both shutters. For example, a user can program the first shutter to have a 1.5ns integration time, an 10ns inter-frame time, and then a 5ns integration time for the second shutter. The variability in the timing of the integration and inter-frame time between the two shutters is given by the equation below:

$$20ns = \text{Shutter 1 Integration Time} + \text{Interframe Time} + \text{Shutter 2 Integration Time}$$

To enable it's use at much slower frame rates (µs integration/inter-frame times), Furi can use "manual shutters". This mode enables both shutter switches to be driven from an off-chip controller. The Furi sensor

demonstrates low jitter repeatable shutter generation with a 30ps RMS trigger to shutter jitter and a 15ps shutter to shutter jitter (Figure 7).

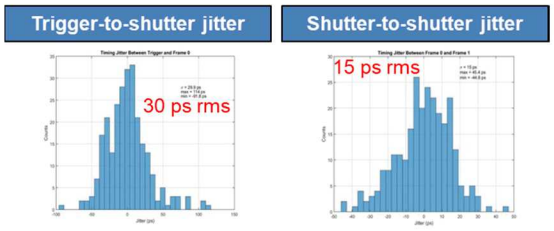

Figure 7- Furi Shutter Jitter

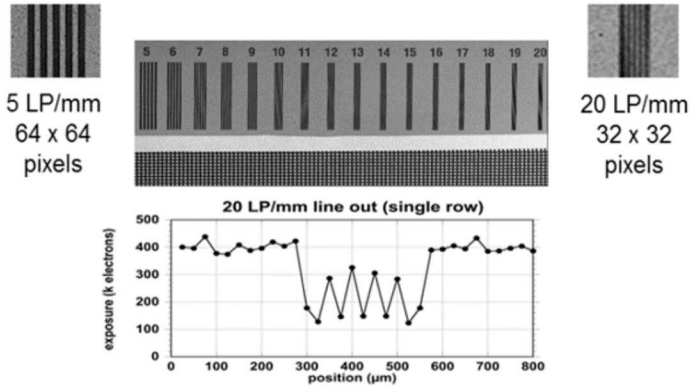

Figure 8- Furi Lineout and MTF

The Furi sensor is in use in diagnostic imaging systems at both the Sandia Z-Machine and The National Ignition Facility (NIF) where it has been used to measure blast waves in vacuum and laser entrance hole closure [3]. Examples of these experimental images are seen in the figures below.

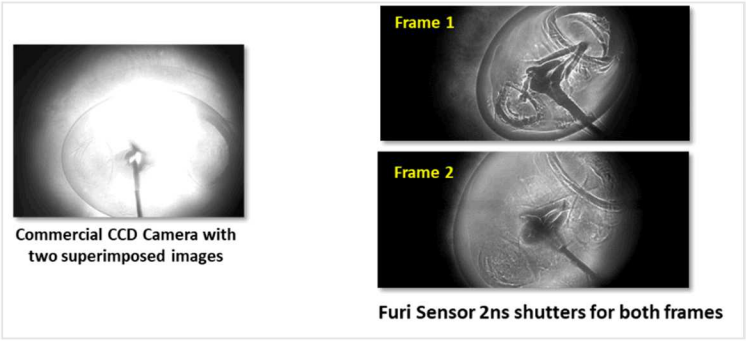

Figure 9 - Z-Machine Blast wave propagation experiments Commercial CCD vs. Furi sensor

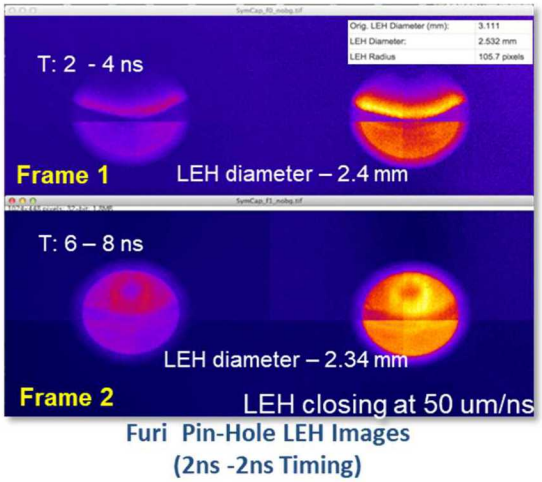

Figure 10 - NIF Laser Entrance Hole pin hole images

3.2. Hippogriff Sensor

The Hippogriff sensor was an iteration of Furi. The primary goals in the iteration was to add the ability to

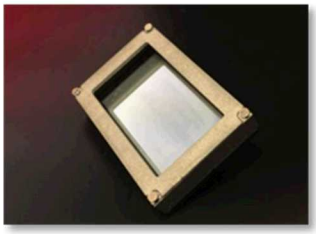

Figure 11- Hippogriff Sensor

capture more frames of data by adding an "interlacing" feature, improving timing offsets between the two half's of the pixel array, and add an anti-bloom feature to the pixel. The interlacing feature implemented into Hippogriff trades row spatial resolution for additional frames. Hippogriff can capture two frames of data at it's full 1024x448 resolution, or four frames of data at 512x448 resolution, or eight frames of data at 256x448 resolution. A shutter timing example of this is depicted in Figure 11.

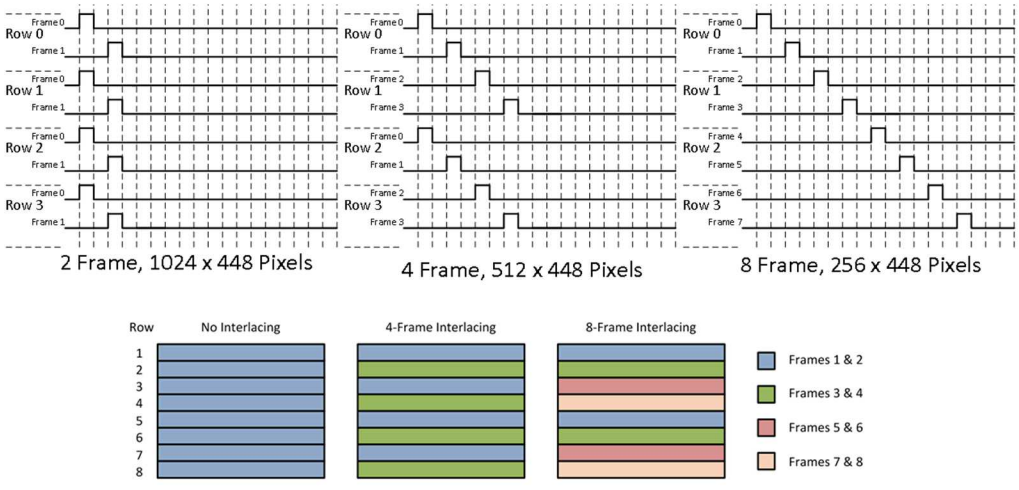

Figure 12 - Hippogriff row interlacing example

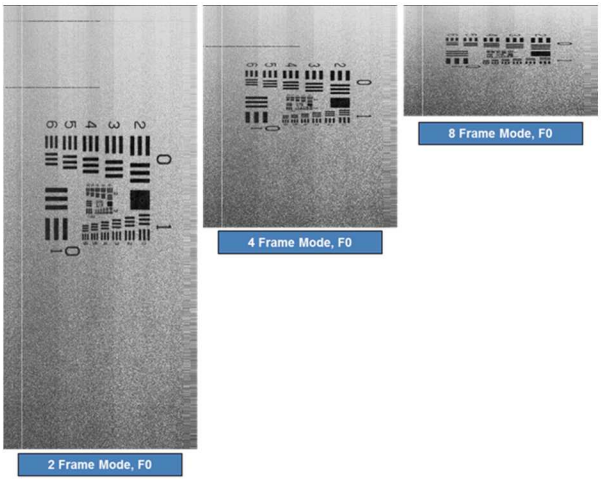

Figure 13- Reduced row spatial resolution during interlacing

Timing offsets found on the Furi sensor between the left and right half's of the pixel array was decreased by ~50% (500ps). The Hippogriff sensor is in use in the Z-machine target chamber and has been used to monitor deposition of laser energy into a gas in Magnetized Liner Internal Fusion (MAGLIF) experiments.

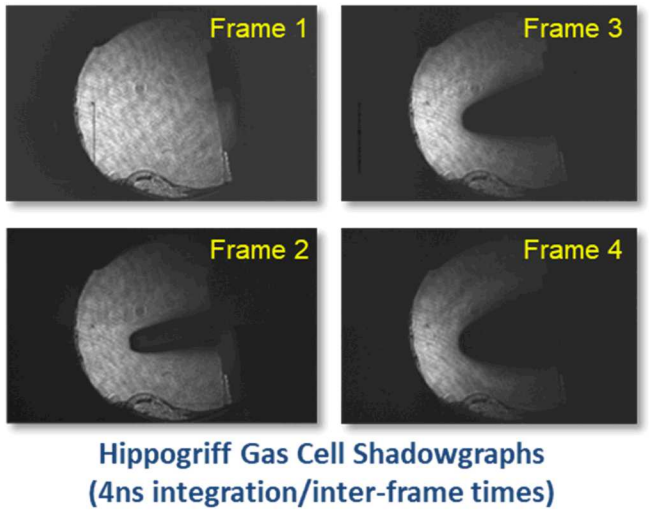

Figure 14- Hippogriff MAGLIF experiment

3.3. Icarus Sensor

The overall size of the Icarus pixel array was increased over Furi and Hippogriff (from 1024x448 to 1024x512). Icarus sensor can capture four frames of data per pixel. The addition of two frames (over Furi and Hippogriff)

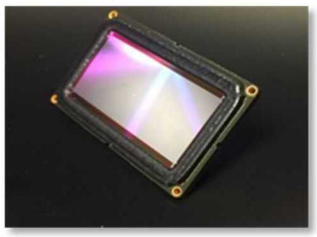

Figure 15 - Icarus Sensor

was accomplished by reducing the full-well capacitor size for each frame (from 1,500,000 to 500,000 electron). In addition, a tunable anit-bloom feature was added to the pixel. Independent timing for each half of the pixel array was added as a way to increase the number of frames without interlacing. The left half of the pixel array (columns 1-256) can capture images independent of the right half of the pixel array (columns 257-512). Figure 16 depicts an example of how a pin-hole image of a scene can be projected onto both half's of the pixel array and then eight images can be taken.

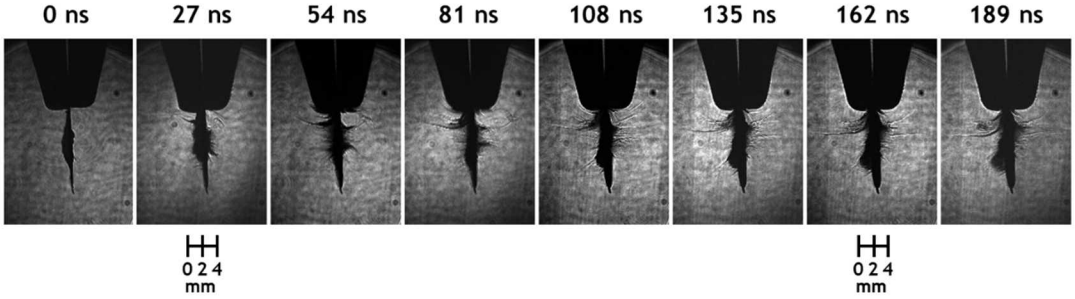

Figure 16 - Z-Machine Test Chamber Laser Pre-heat of gas, both half's of array timed sequentially

The depth of the timing register for shutter integration and inter-frame time was also increased. This allows for greater programmability of shutter integration and inter-frame times. The variability in the timing of the integration and inter-frame time between the four shutters is given by the equation below:

80ns = Shutter1 Intg. Time + Interframe1 + Shutter2 Intg. Time+ Interframe2 + Shutter3 Intg. Time + Interframe3 + Shutter4 Intg. Time

The Icarus sensor is used in several diagnostic imaging systems at Z machine, NIF and the OMEGA facility at the Laboratory for Laser Energetics (LLE).

4. Conclusion

The hCMOS effort at Sandia National Laboratories (SNL) has spanned multiple years and has been successful in fielding a suite of high speed, multi-frame imaging sensors for use in HED experiments. The sensors have focused on 25µm pixels, 2-4 frames per pixel, 1000:1 dynamic range and a 1024 row by 512 column pixel array. These sensors have been named the most transformation diagnostic in HED science by leadership at all national HED facilities. The hCMOS effort continues to move forward with the design and fabrication of new ROICs and photodiodes to capture images of higher energy photons. The current generation ROIC, named Daedalus, is scheduled to be tested on NIF facilities in Q2 of 2019. Daedalus is a three frame per pixel ROIC with a 1,500,000 electron full well and it employs novel new shutter timing distribution that enables different interlacing options. Daedalus will be bonded to photodiodes with silicon absorber layers of um to 200 µm in thickness. New photodiodes absorber materials are also being explored. Work on developing pixelated GaAs diodes in in progress. Discrete diodes of 20µm thickness have been demonstrated and work on a pixelated array is in progress. GaAs photodiodes would enable hCMOS sensors to capture X-ray photons in the 20keV range.

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