SAND2019-13564C

Sandia National Laboratories

Latest Developments in the Xyce Large-Scale Analog Circuit Simulator

Jason Verley, Eric Keiter, Tom Russo, Rich Schiek, Heidi Thornquist, Ting Mei, Pete Sholander and Aadithya Karthik

Introduction

Analog circuit simulation has historically been an important capability in the design and verification of Analog and Mixed Signal systems. With the advent of digitally-assisted analog/RF, and System On a Chip (SOC) technologies, the need for fast and accurate analog simulation has increased. While FastSpice methods allow for large-scale simulations, they sacrifice the fidelity of "true SPICE" simulation.

Xyce is a SPICE-compatible analog simulator designed for the accurate simulation of a wide range of circuit sizes, ranging from a few elements to millions of components. It achieves this scaling through Message Passing Parallelism (the method of choice in High Performance Computing). Recent and near-term development in Xyce is focused on compatibility with commercial tools, the simulation of modern technology nodes, frequency-domain simulations, and improved performance.

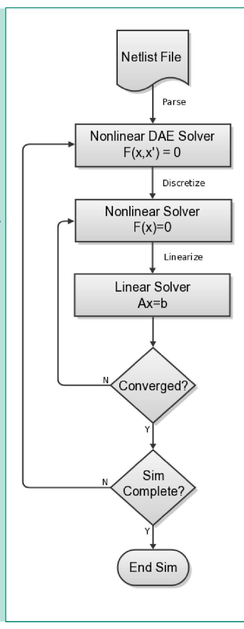
Analog Simulation

Traditional analog circuit simulators, such as SPICE, solve a coupled set of nonlinear differential-algebraic equations (DAEs):

$$f\big(x(t)\big) + \frac{d}{dt}q\big(x(t)\big) - b(t) = 0.$$

The solution approach follows the flow on the right. The *nonlinear solver* evaluates the output of each device (typically current) based on an input (typically nodal voltages). A Newton iteration step is taken, where the *linear solver* solves the resulting matrix equation. This process is continued until convergence, and the next step in the analysis is taken.

The traditional approaches do not scale well beyond tens of thousands of unknowns due to the reliance on a large single matrix that is treated by *direct matrix solvers*. As a result, the analog runtime scales super-linearly with increasing circuit size. For RF simulation, the scalability can be worse than for transient, because harmonic balance (HB) analysis generates larger, less sparse matrices.



Netlist Compatibility…

Over the last year, the Xyce team has made many enhancements to Xyce for feature compatibility with HSPICE netlists. Highlights of these improvements are:

- implementation of a new "charge expression" variant of the capacitor
- addition of the pattern (PAT) source function to the V and I devices
- allowing the expression library accept C-style ternary conditional operators
- improved support for .MEASURE
- allowing sweep loops for .NOISE analyses be specified using the .DATA command.

…and Translation

Outside of the Xyce code, itself, a **netlist translator** will be packaged with Xyce as part of the 7.0 release. Called **XDM**, the tool allows a user to translate the bulk of an HSPICE netlist into Xyce syntax. Certain features will still require some hand-processing of the netlists, but XDM will mark the non-translatable parts (often simulation specifications) to reduce the amount of time the user spends in the translation process.

PDK Compatibility

The analog circuit simulation portions of Process Design Kits (PDKs) are typically supplied in HSPICE or Spectre syntax. Therefore, PDK compatibility is purely a reflection of tool compatibility, both feature and syntax. The upcoming 7.0 release of Xyce with XDM will have been tested against the Global Foundry PDKs for:

- GF 55/65 nm (RFCMOS)
- GF 12 nm (3D FinFET)

Development Highlights Since WOSET '18

- All devices based on Verilog-A are ~5× faster (due to a major refactor of the Xyce backend to the ADMS model compiler).
- Improved direct solver performance and reductions in general memory usage.
- Many enhancements to the parameter sensitivity analysis capability.
- S-parameter analysis is now supported in Xyce, with the ability to calculate Y- and Z-parameters.
- The results of S-parameter analysis can be output to a file in either Touchstone 1 or Touchstone 2 format.
- The port device was developed to support S-parameter analysis and can be used with DC, AC and transient analyses.
- Enhancements to various output capabilities and formats.

Xyce Capabilities

- Standard capabilities: DC, transient, AC, noise, expressions, functions, parameterization…
- Analog Behavioral Modeling
- Post-processing:
  - Fourier transform of transient output (.FOUR)
  - Post-simulation calculation of simulation metrics (.MEASURE)
- Output: Text Files (tab or comma delimited), Probe, Gnuplot, TecPlot, RAW
- Harmonic Balance Analysis (.HB)
  - Steady state solution of nonlinear circuits in the frequency domain
- Random Sampling Analysis
  - Executes the primary analysis (.DC, .AC, .TRAN, etc.) inside a loop over randomly distributed parameters.
- Sensitivities (DC or Transient)
  - Computes sensitivities for a user-specified objective function with respect to a user-specified list of circuit parameters ($\partial O/\partial p$…); e.g., an output voltage's dependence on a capacitance.

Xyce Release 6.12

- Available at: `https://xyce.sandia.gov`

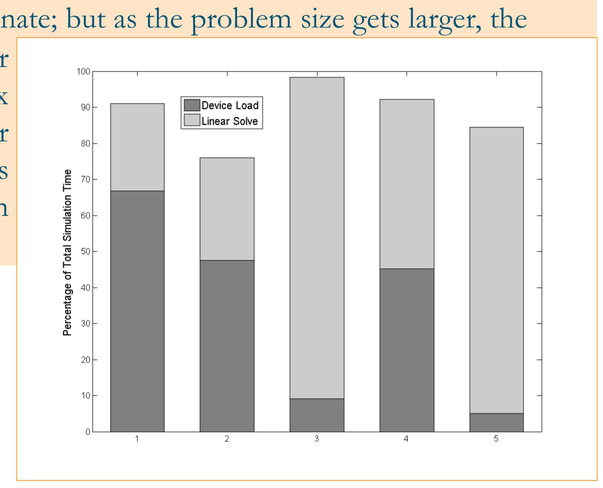
Open Source under the Gnu Public License, Version 3

- Xyce is also on GitHub: `https://github.com/xyce`

Xyce Parallel Simulation

Xyce has been designed to use distributed memory parallelism to address the scalability issues inherent to solving large nonlinear DAEs. From the beginning, the focus of Xyce development has been to provide scalable, numerically accurate analog simulation for large-scale circuits through the development and improvement of the algorithms at the core of SPICE-style simulation. Furthermore, Xyce has been designed to have a modular framework for integrating device models and developing state-of-the-art continuation algorithms, analysis methods, preconditioned linear solvers, and parallel partitioning techniques.

For optimal parallel execution speedup, Xyce can parallelize both the device evaluation and the linear system solve. The two modes can be invoked together or separately. In smaller problems, the device evaluation tends to dominate; but as the problem size gets larger, the matrix solve dominates the solve time. For large problems, Xyce uses specialized matrix preconditioners and iterative linear solvers for good scalability. The linear system solve is even more important in the frequency-domain due to the much larger matrices.



CIRCUITS: MATRIX SIZE(N), CAPACITORS(C), MOSFETS(M), RESISTORS(R), VOLTAGE SOURCES(V), DIODES (D).

Circuit	N	C	M	R	V	D
ckt1	15622	7507	10173	11057	29	0
ckt2	25187	0	71097	0	264	0
ckt3	116247	52552	69085	76079	137	0
ckt4	688838	93	222481	176	75	291761
ckt5	1944792	400234	211486	795827	36100	199992

Planned Developments

Continue to Improve Compatibility with Commercial Simulators

- Integration of the XDM translator into Xyce, itself
- Improving HSPICE feature compatibility
- Develop compatibility with Spectre (both netlist and feature)

PDK Support

- Continue to test PDKs from Global Foundries, and other foundries, as available

Performance Improvements

- Begin to incorporate FastSpice methods
- Continued improvements to the linear solver

Others

- Development of a device, which has a response defined by a Touchstone 1 or 2 file
- Continued improvement for mixed-signal simulation (Verilog via VPI, VHDL via VHPI)
- Coupling to the **gds2para** code for improved simulation of IC parasitics

We wish to acknowledge the Advanced Simulation and Computing (ASC) Project under the National Nuclear and Security Administration (NNSA), and the DARPA Posh Open Source Hardware (POSH) Project for funding the development of Xyce.

Xyce™ PARALLEL ELECTRONIC SIMULATOR

U.S. DEPARTMENT OF ENERGY
NNSA National Nuclear Security Administration

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.
SAND No. _____

Sandia National Laboratories