SAND2019-13111C

Void-Free Copper Electrodeposition in Full Wafer Thickness Through-Silicon Vias with 10:1 Aspect Ratios

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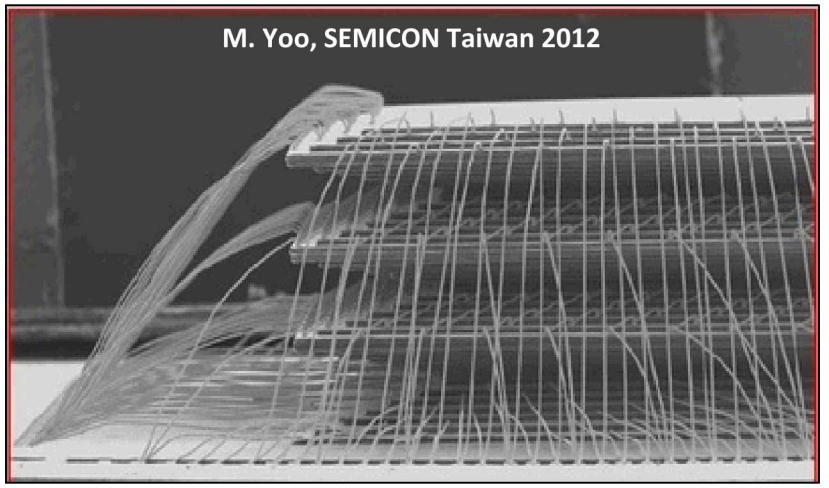
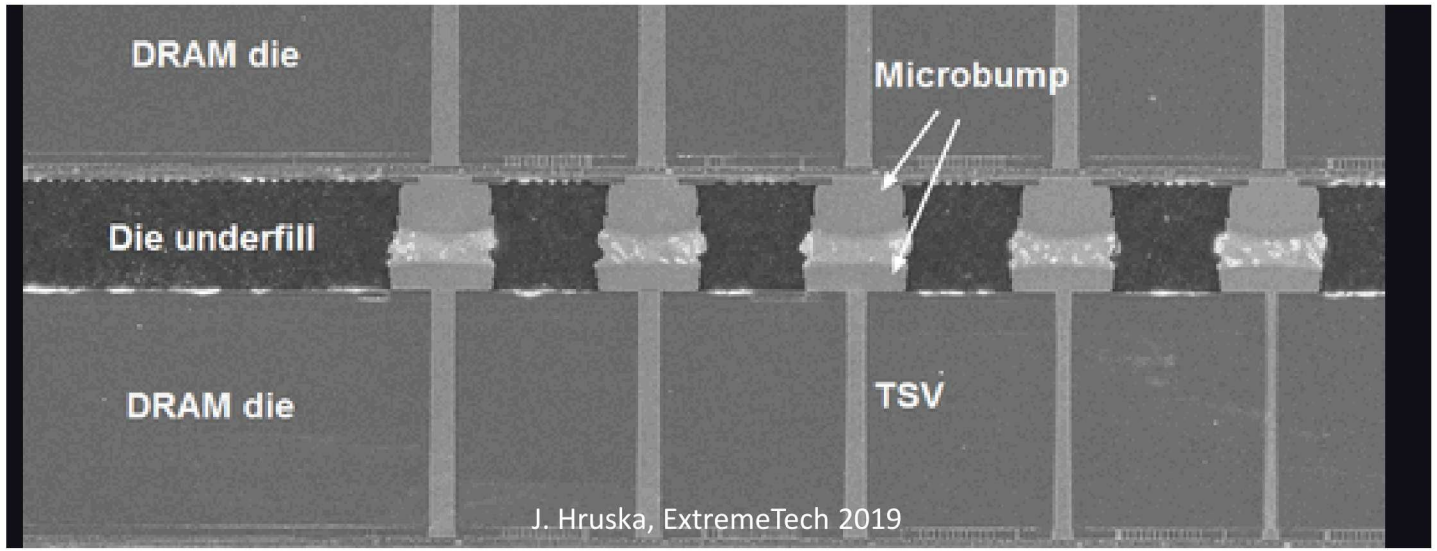
Supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

Through-Silicon Vias (TSVs) for MEMS Applications

- Benefits of mesoscale Cu TSVs
  - Increase I/O per unit volume
  - Simplify design and 3D packaging
  - Span full wafer thickness, required for MEMS applications
  - Improve thermal management
  - Reduce electrical parasitics



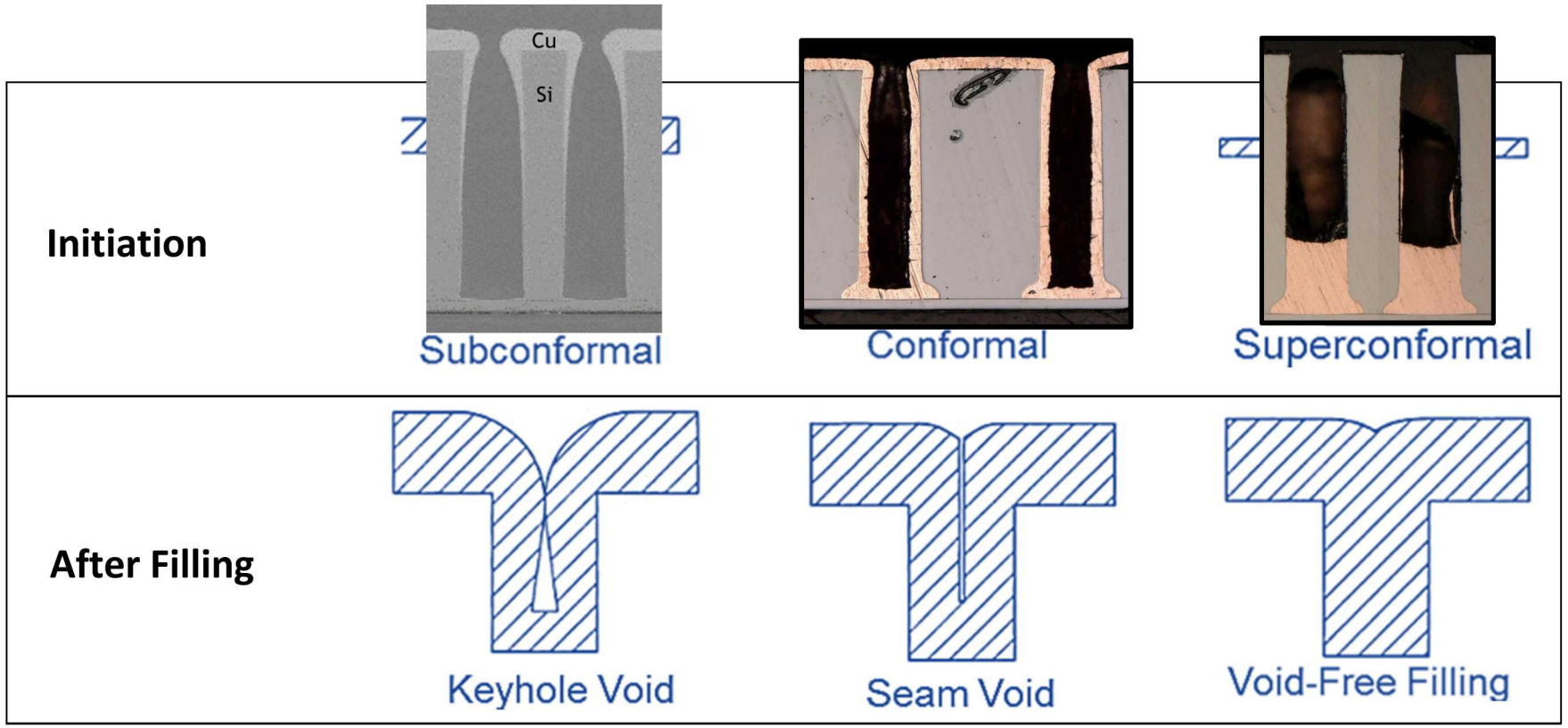
Wire bonded 3D Stacked Die



3D Stacked Die with integrated TSVs

Electroplating Fill Profiles

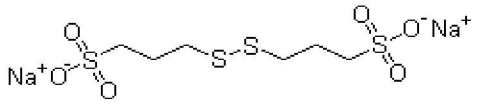
- Additive free ECD leads to subconformal fill
- Pulsed plating regime can establish a conformal fill profile
- Additives enable superconformal void-free filling



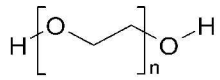
Common Electrodeposition Additives

Common Additives Used In Printed Circuit Board Plating

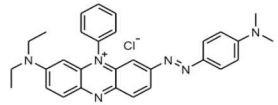
Accelerator
bis-(sodium sulfopropyl)-disulfide
(SPS)



Suppressor
Polyethylene
Glycol (PEG)



Leveler
Janus Green B
(JGB)



HCl, KCl
Or
NaCl

Accelerator –preferentially increases plating

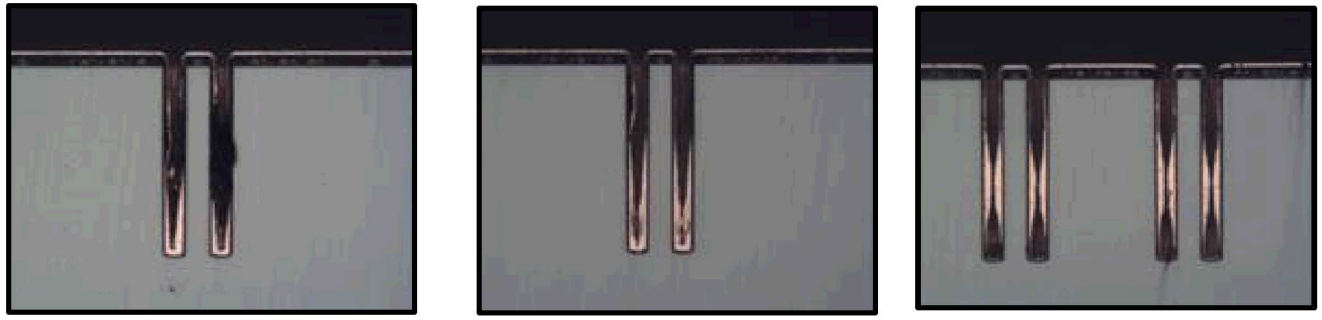
Leveler - Disables accelerator to reduce overburden thickness; grain refiner

Suppressor - Large chain polymer, slows plating rate higher in via

Only suppressor and chloride are needed to achieve void free TSV filling

S-NDR Electrolyte for Void Free Superfilling

S-Shaped Negative Differential Resistance (S-NDR) Approach[1]
Derived from work by Dan Josell and Tom Moffat at NIST Gaithersburg in bottom-up filling in IBM 56 µm deep TSVs[1,2]
At a given suppressor concentration more negative applied potential pushes deposition higher the TSV



More negative potential →

Pros of bottom-up plating

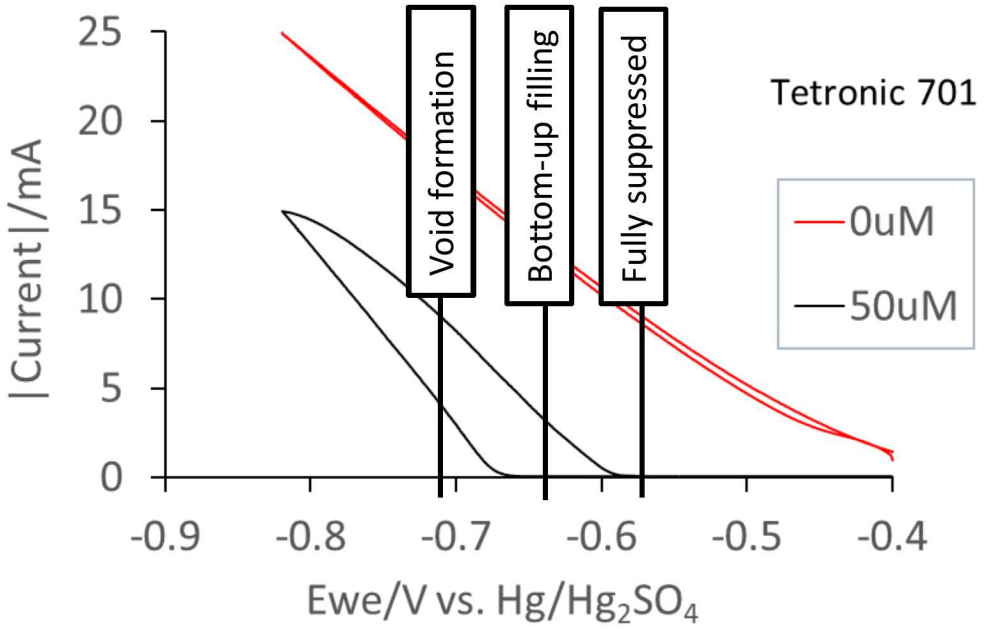
- Void-free filling
- Reasonable deposition times

Challenges with bottom-up plating

- Delicate balance between applied bias and electrolyte composition
- Geometry dependent plating conditions

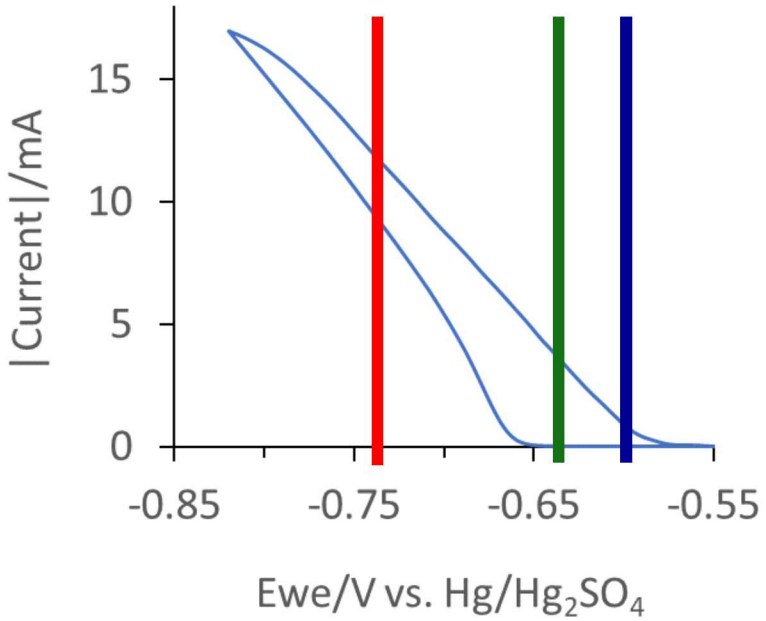
1. Journal of the Electrochemical Society, 159 (4) D208-D216 (2012)
2. Journal of the Electrochemical Society, 159 (10) D570-D576 (2012)

Suppressor Breakdown in MSA Electrolyte
1.25 M $CuSO_4$, 0.25 M MSA, 1mM KCl



Void-free Filling 100 µm Diameter TSVs[3,4]

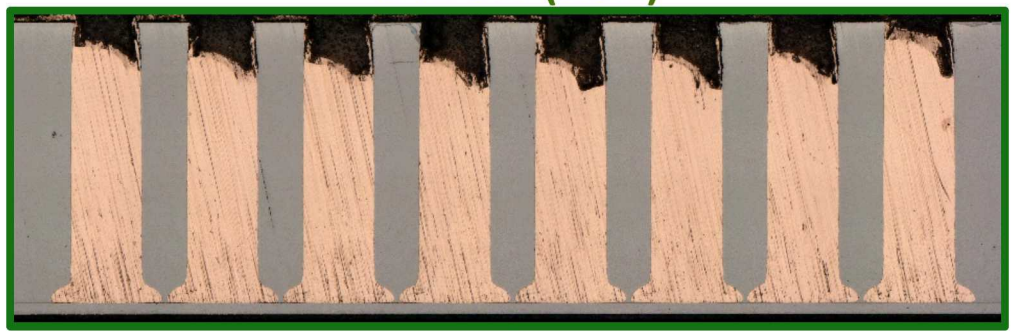
CV for 1.25 M $CuSO_4$, 0.25 M MSA, 1mM KCl, and 50 µM Tetronic 701



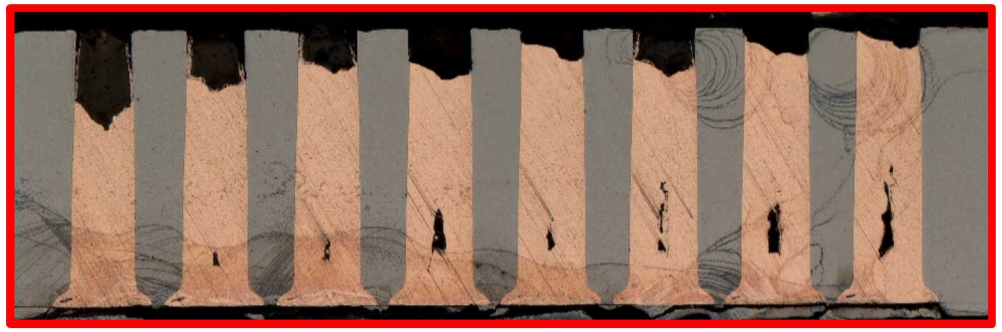
- Reference electrode used to finely tune applied potential
- Filling results are highly sensitive to applied voltage
- ~20mV window to obtain void free filling

-600 mV (MSE)

-640 mV (MSE)



-740 mV (MSE)

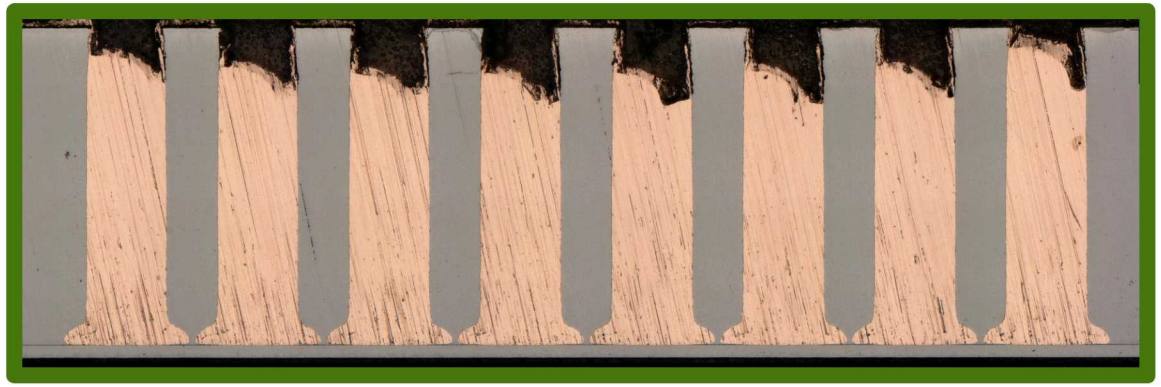


3. Journal of the Electrochemical Society, 166 (1) D3066-D3071 (2019)
4. Journal of the Electrochemical Society, 166 (1) D3226-D3231 (2019)

Fill Dependence on TSV Geometry

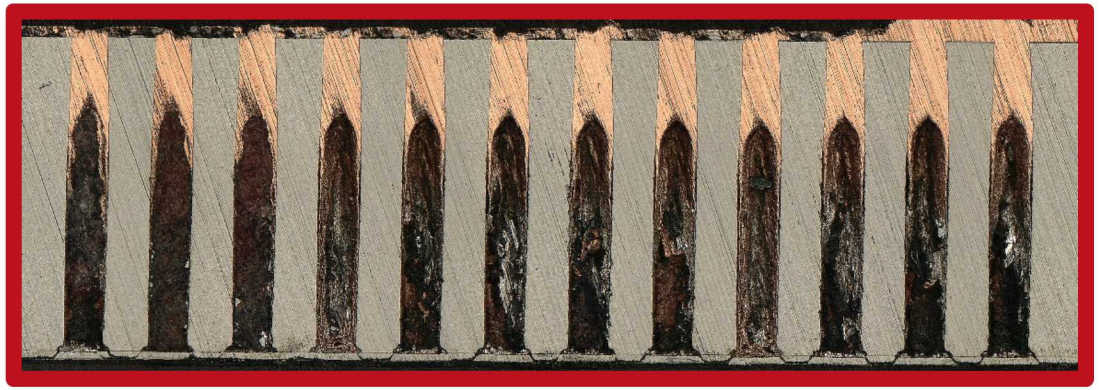
Parameters for filling 100um diameters TSVs did not work with 62.5um diameter TSVs[3,4]

100 µm TSV 6:1 aspect ratio



- Successful potentiostatic and galvanostatic plating procedures have been determined to fill 100 µm diameter, 625 µm thick TSVs.

62.5 µm TSV 10:1 aspect ratio



- Parameters that accomplish void-free, bottom-up filling in 100 µm diameter TSVs do not translate to uniformly fill 62.5 µm diameter TSVs

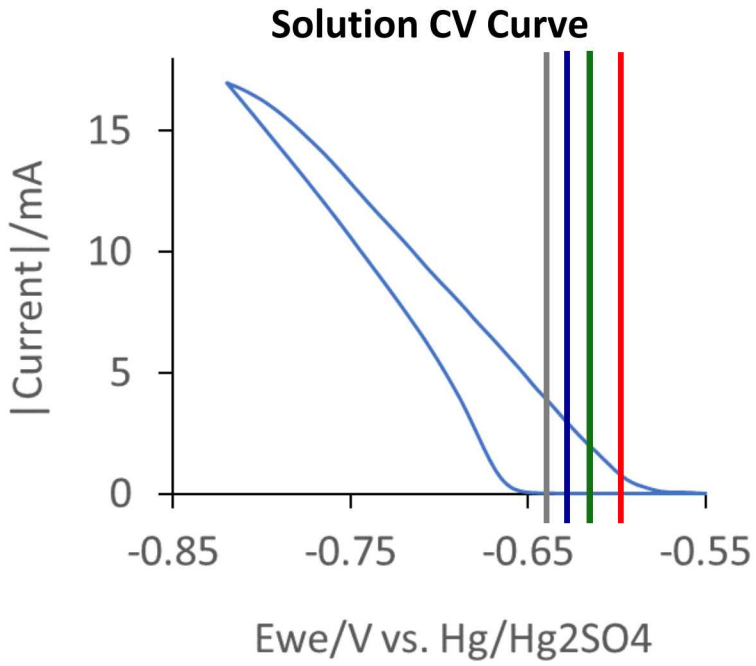
3. Journal of the Electrochemical Society, 166 (1) D3066-D3071 (2019)
4. Journal of the Electrochemical Society, 166 (1) D3226-D3231 (2019)

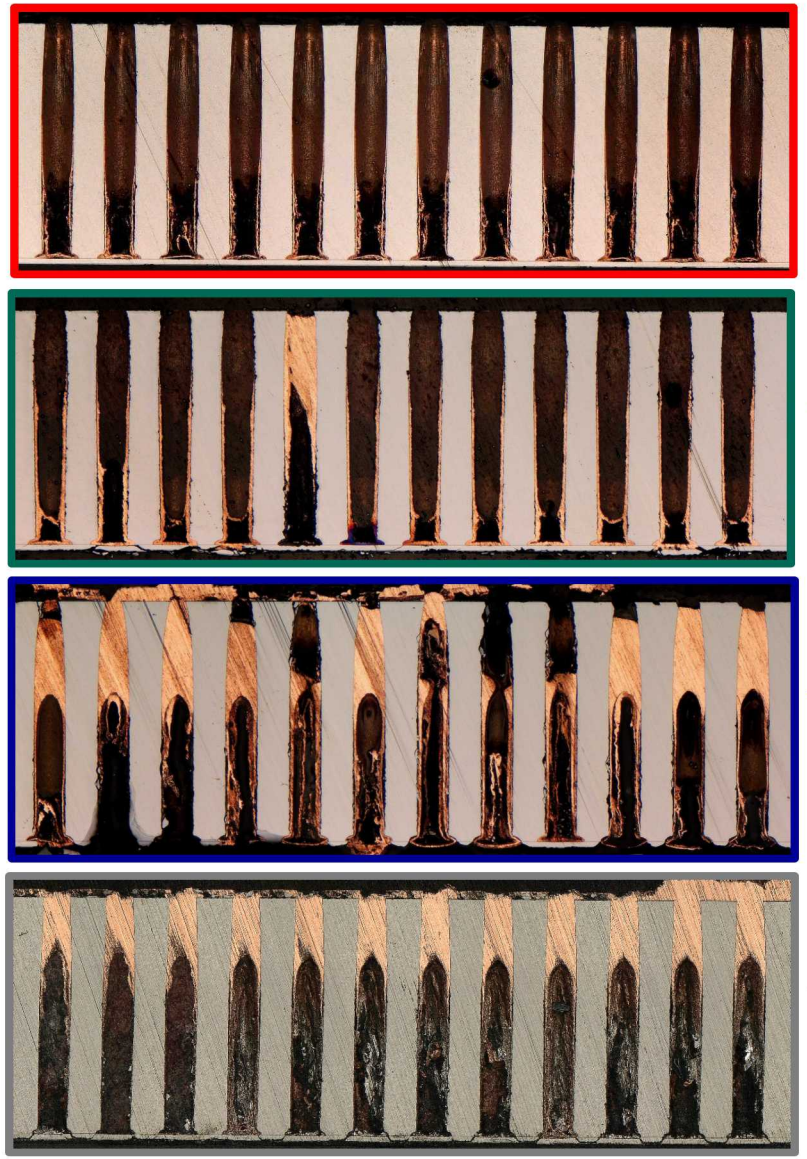
→ Change applied voltage to fill these higher-aspect ratio vias

Experiments in Initial Chemistry

1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, 50 µM Tetronic 701, 400 RPM, 4 hours

- Plated at potentials in increments of 10 to 20 mV
- Sufficient voltage must be applied to overcome suppression once breakdown voltage is reached, plating occurs rapidly
- -620 mV to -630 mV change resulted in drastic change in height of deposition



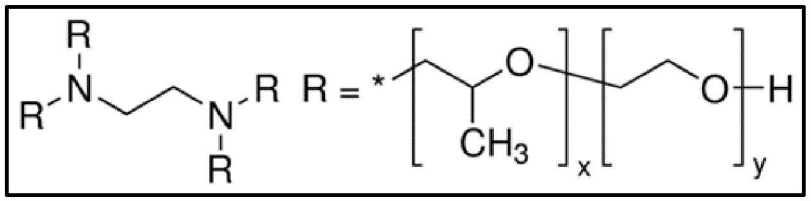


Additional experiments in high chloride solutions:

- Modified suppressor concentrations
- Current controlled vs voltage controlled
- Modified Rotation rate
- Dwell time

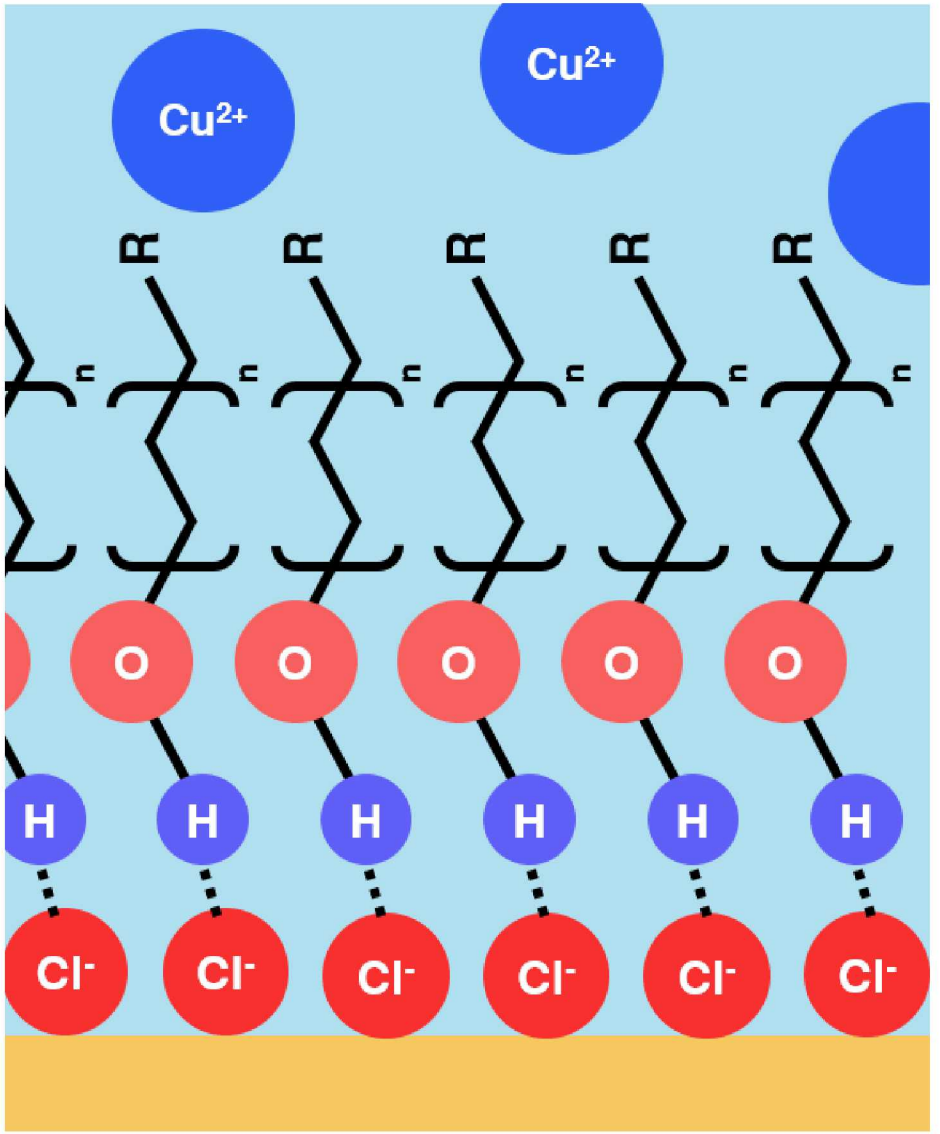
Impact of Chloride Concentration on Suppression

Tetronic 701



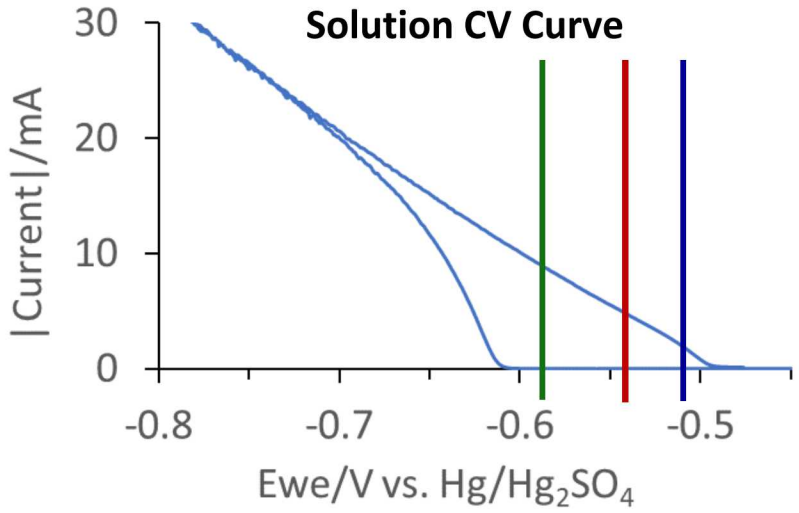
KCl

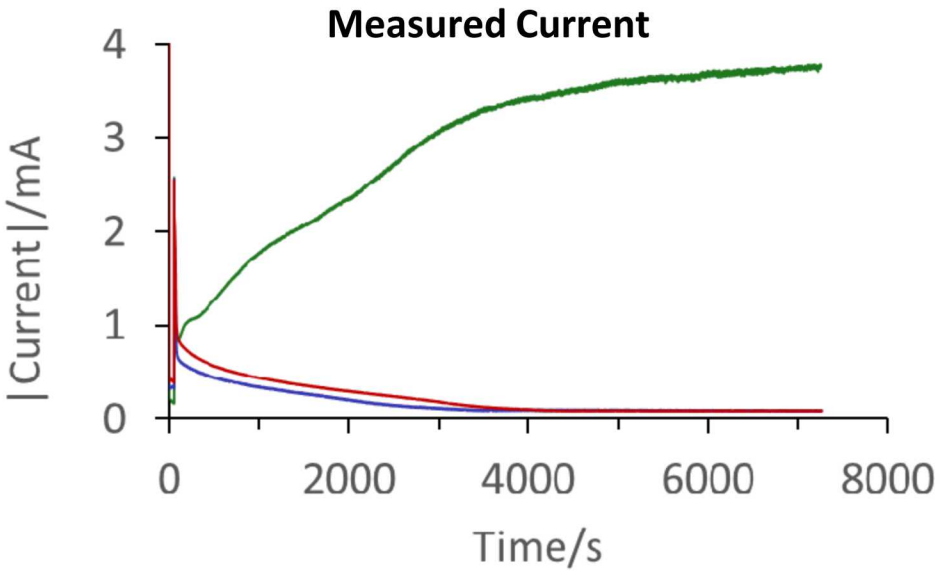
- Chloride facilitates suppressor surface adsorption
- Decreasing chloride concentration decreases suppression
- Low chloride chemistries are also useful for plating in high-aspect ratio features where solution replenishment is challenging

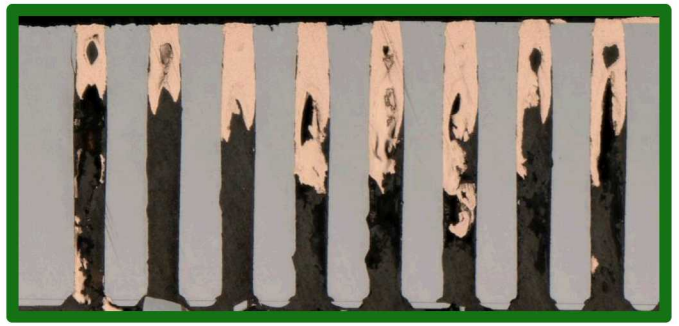


Potentiostatic Experiments in Low Chloride Chemistry

1 M $CuSO_4$, 0.5 M H_2SO_4, 40 uM Tetronic 701, and 80 uM KCl

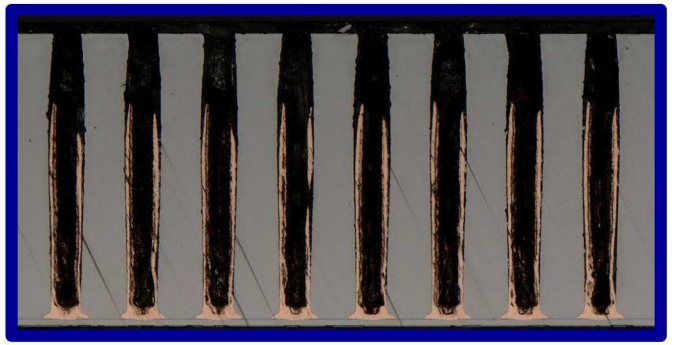






-570 mV (MSE)

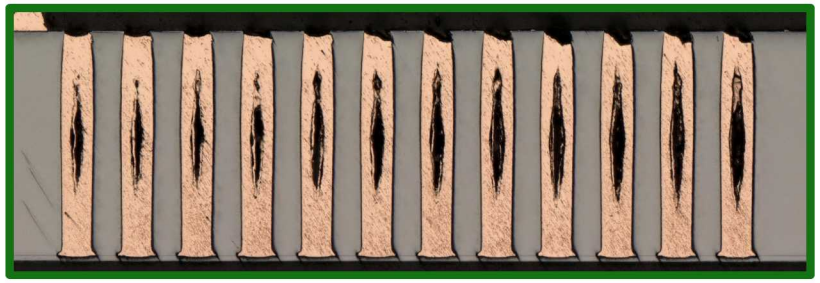
-540 mV (MSE)



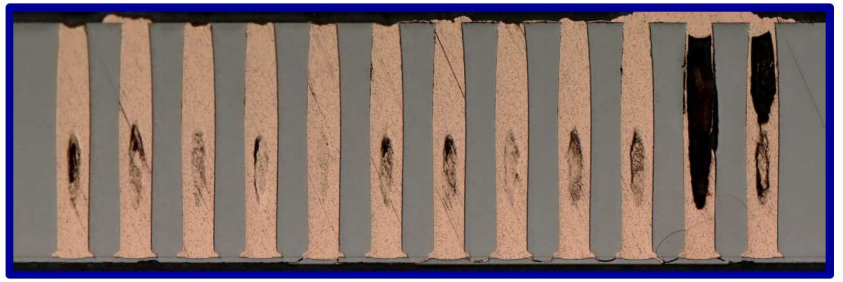
-520 mV (MSE)

Step Potential to Eliminate Voids

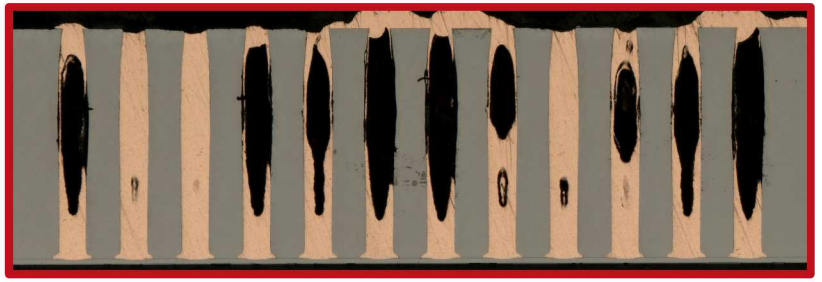
- “Potential stepping” – start at a more positive potential and gradually move to a more negative potential, moving the Cu growth front from the bottom of the via to the top.
- 10 mV steps from -500 V to -560 V (MSE) for steps 1-7
- Varied timestep duration for each sample



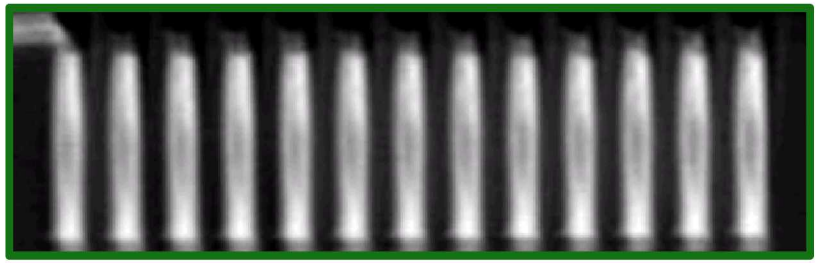
1.5 hour intervals

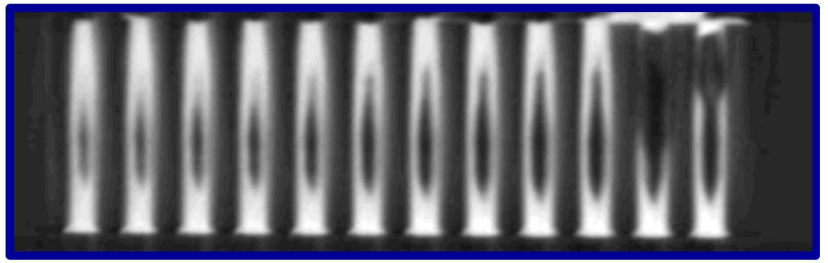


1 hour intervals



45 min intervals



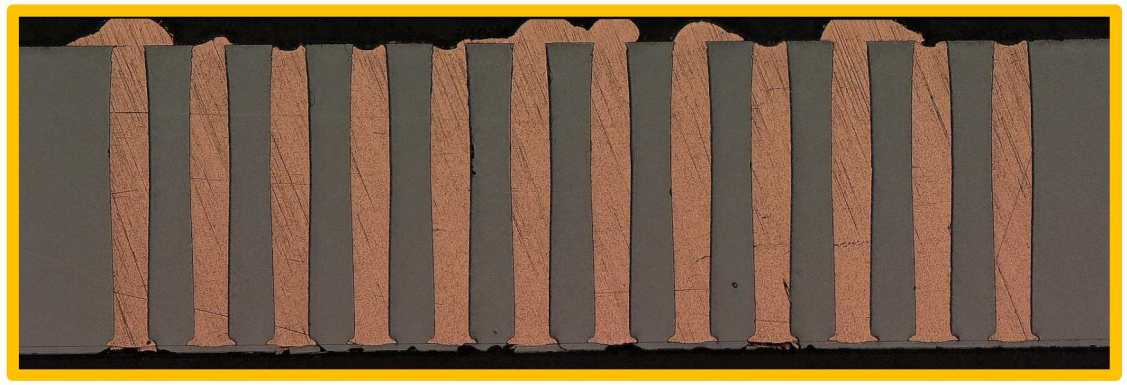


CT Scans

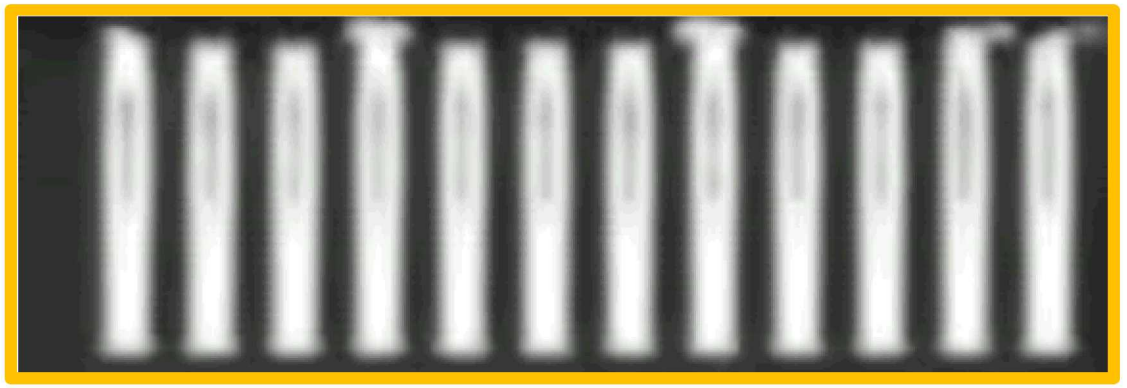
Longer intervals at each step reduce voids

Step Potential to Eliminate Voids

- “Potential stepping” – start at a more positive potential and gradually mov to a more negative potential, moving the Cu growth front from the bottom of the via to the top.
- 10 mV steps from -500 V to -560 V (MSE) for steps 1-7



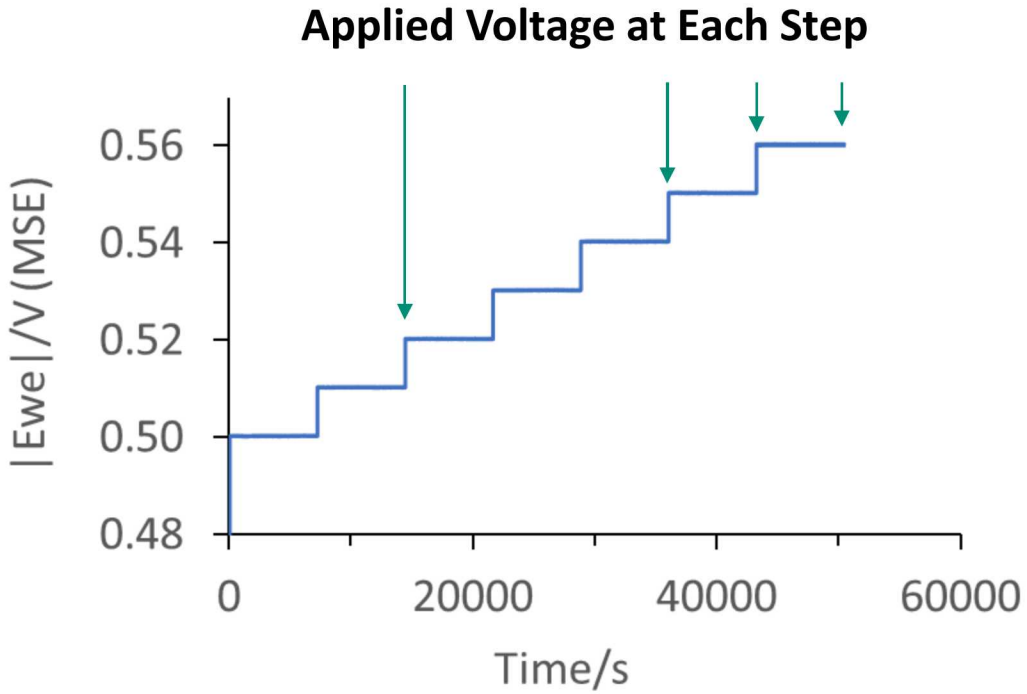
2 hour intervals



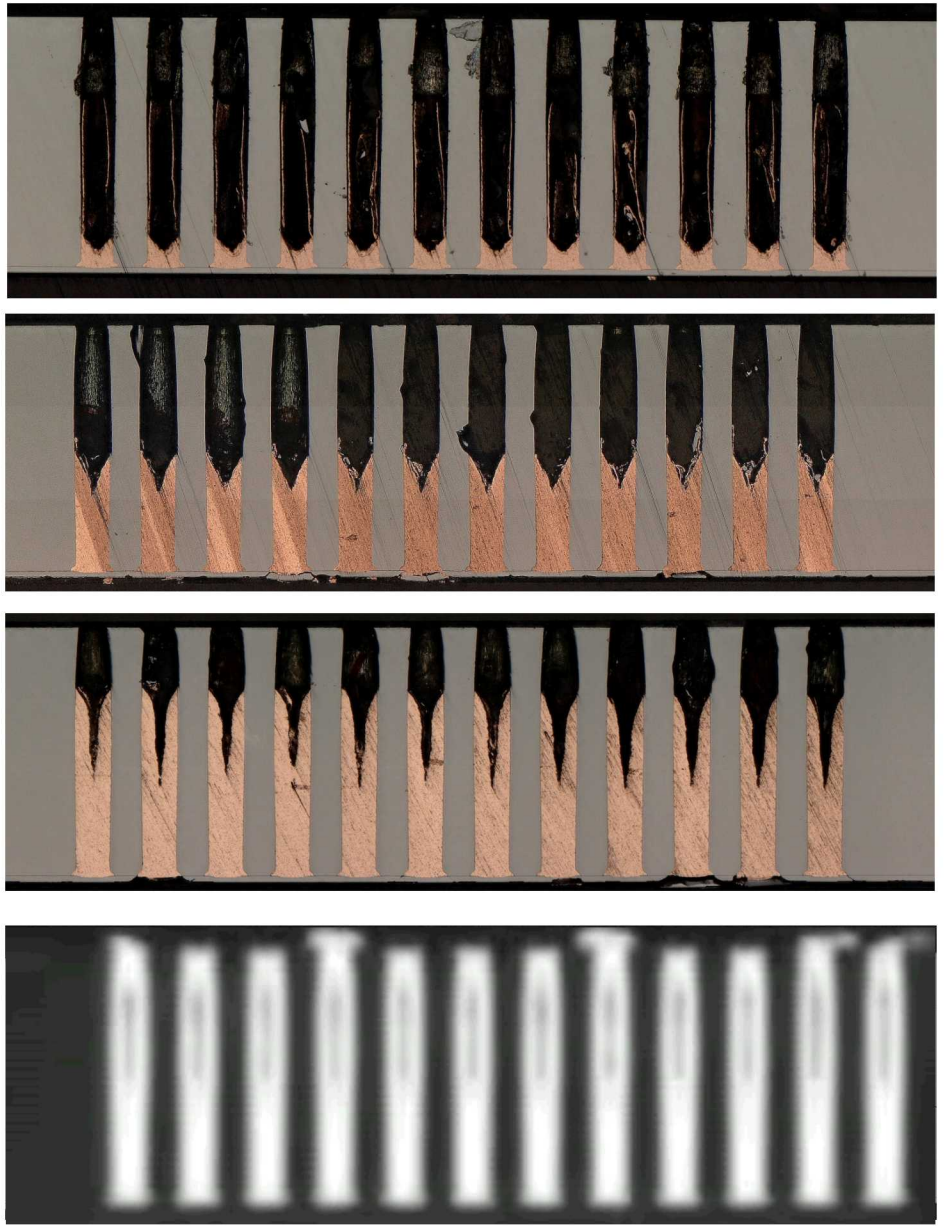
2 hour intervals CT Scan

Void Development

- Experiments were stopped at various points throughout the fill process
- Void formation initiates at step 5, grows during step 6

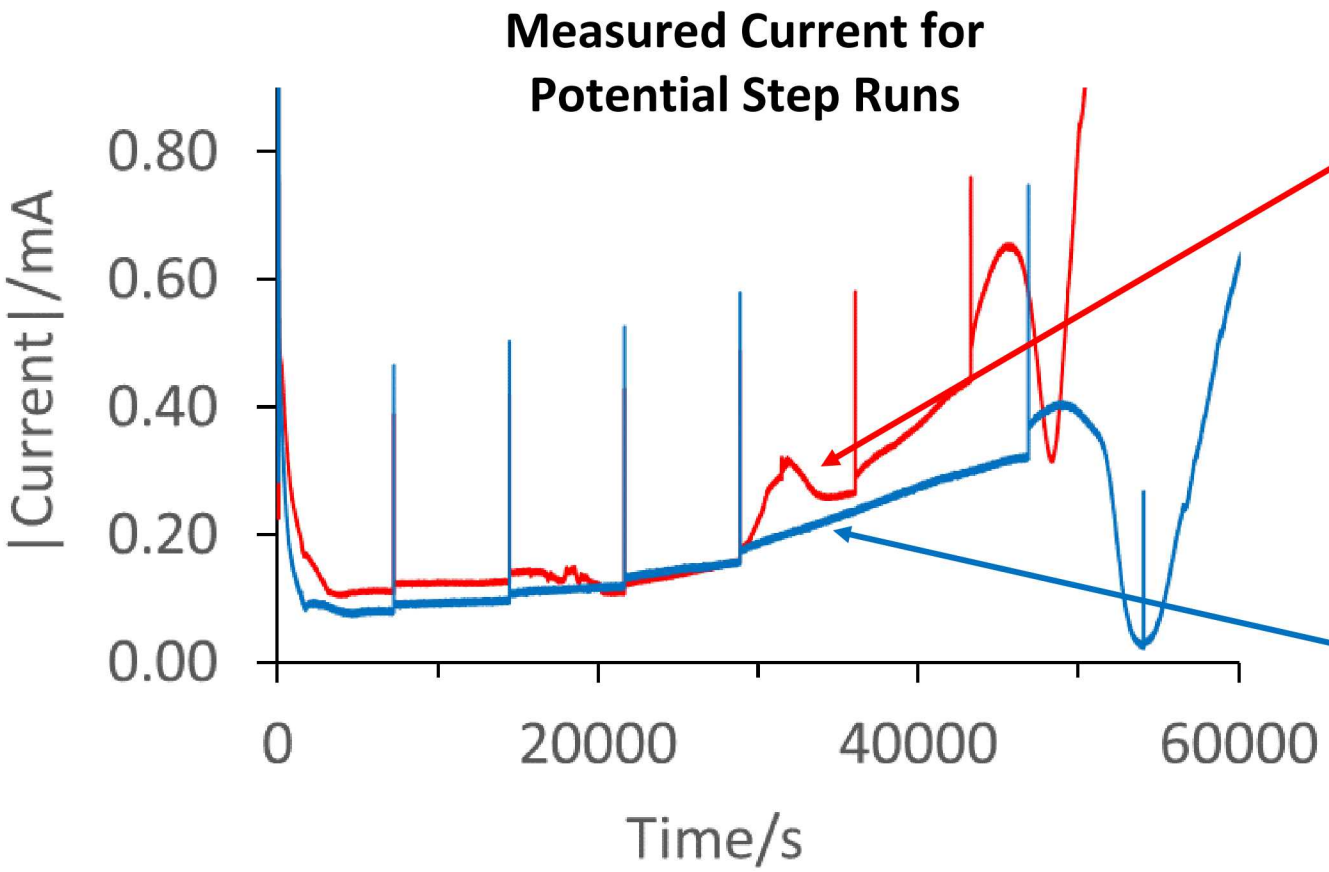


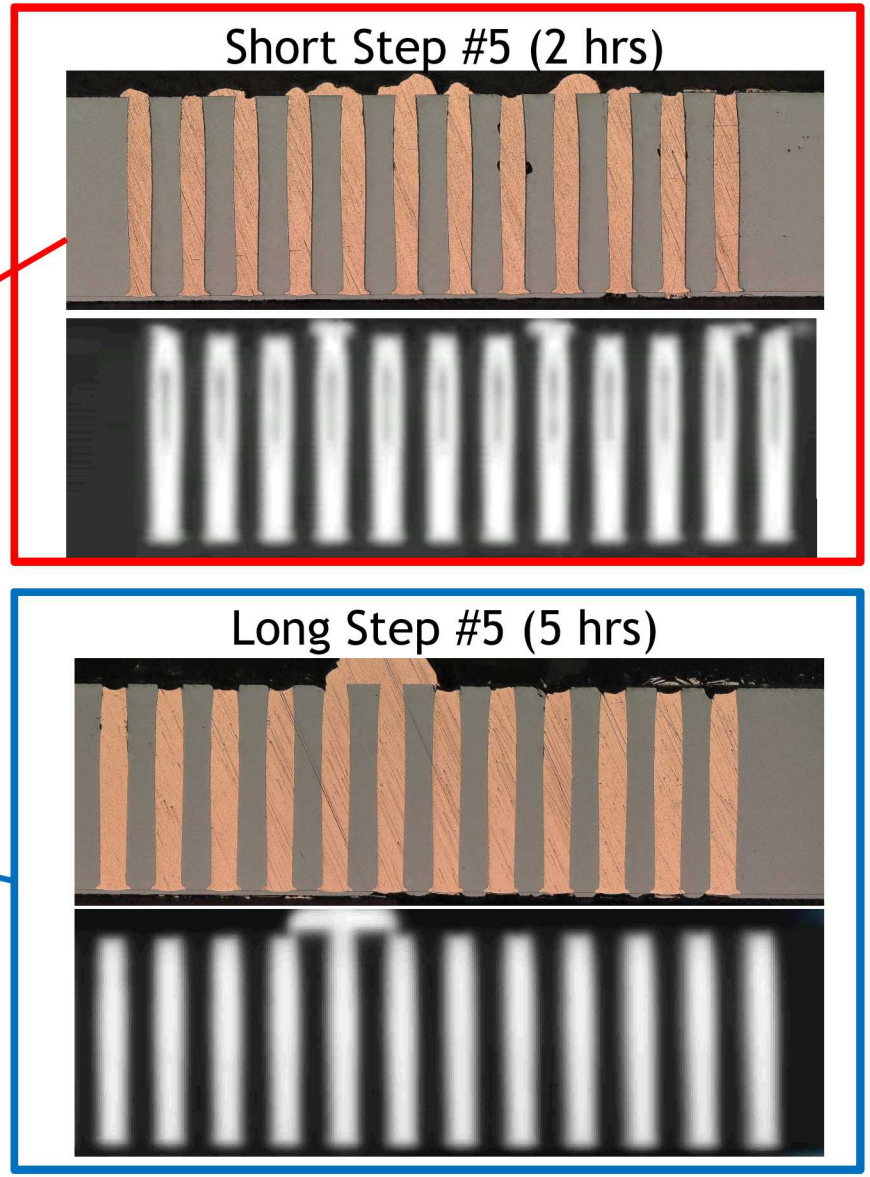
→ Increasing time held at step 5 may eliminate voids



Experimental Changes Leading to Void-free Filling

- Increase length of step number 5 (-540 mV) to mitigate void formation

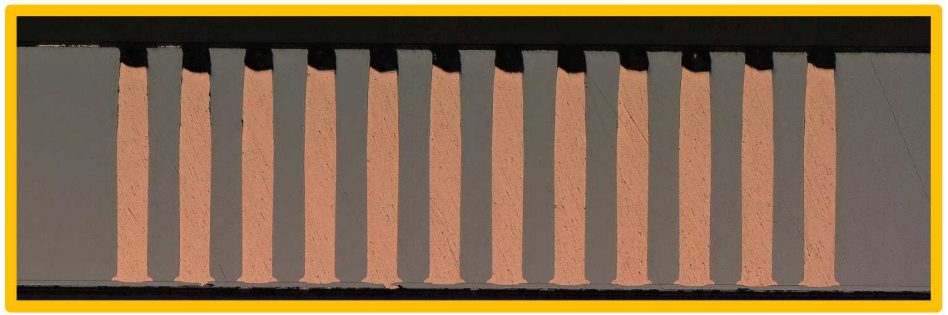


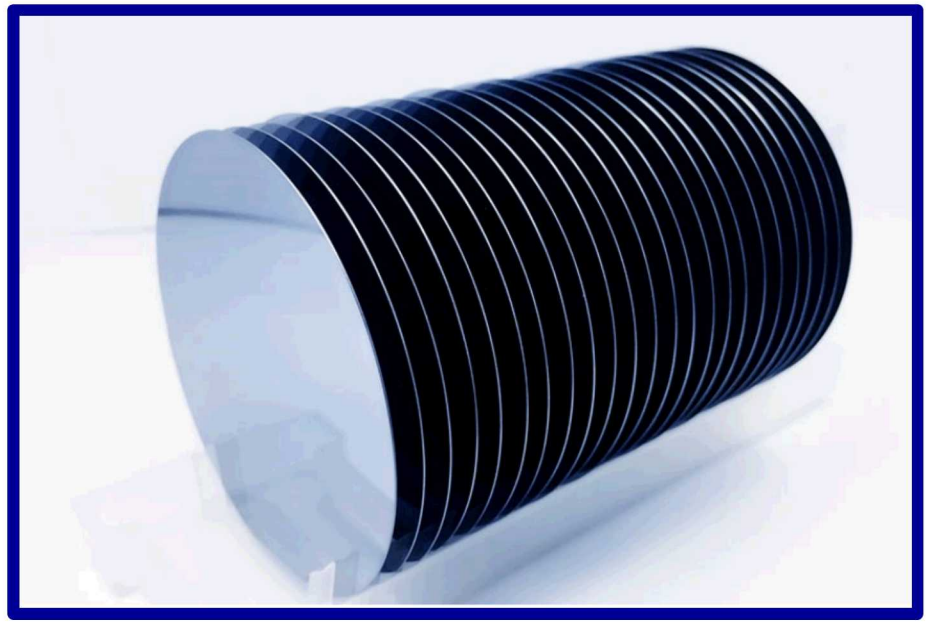


CT scan results confirm void-free, bottom-up filling

Steps Towards Full Wafer Plating

Potential controlled filling is not compatible with production scale plating tools

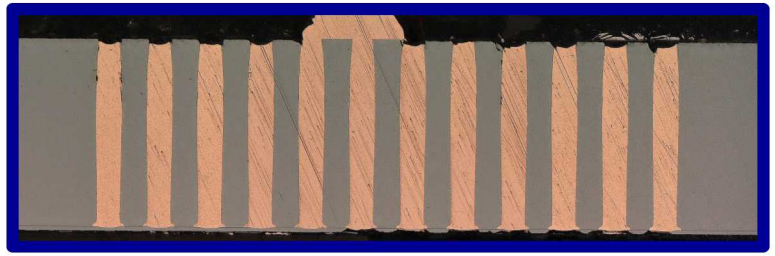




Developing a Current Controlled Filling Solution

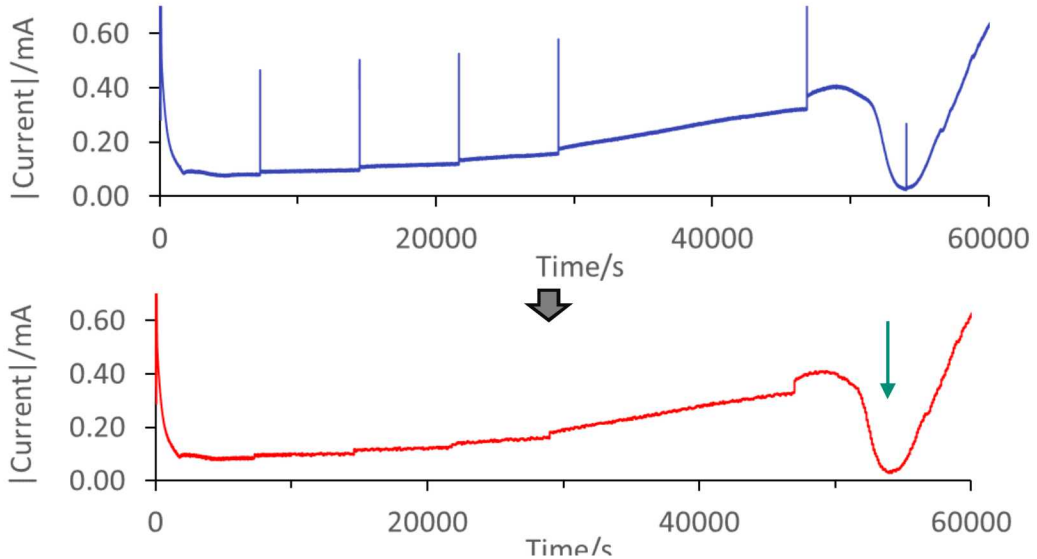
- Voltage controlled stepping resulted in void-free filling; however, this process is not compatible with production full wafer plating tools. A current controlled deposition is needed.

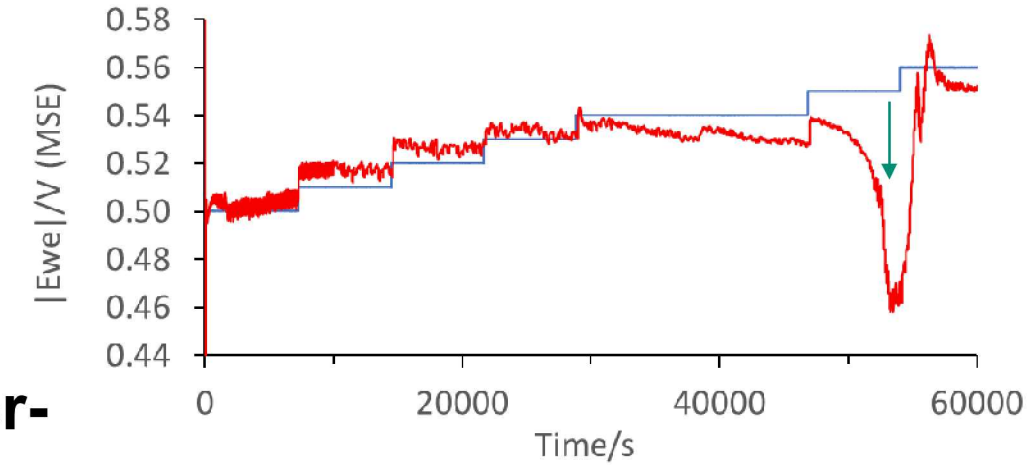
Voltage Controlled Cross-Section



Current Controlled Cross-Section

- Slower deposition did not reach top of vias for current controlled process
- Voltage drop seen with current drop





Future work: improve current controlled process and apply to wafer-level plating

Acknowledgements

Christian Arrington, Ehren Baca, Todd Bauer, Matthew Blain, Jason Dominguez, Ron Goeke, Edwin Heller, Andrew Hollowell, Robert Jarecki, Matthew Jordan, Becky Loviza, Jaime McClain, Kate Musick, Lyle Menk, Anathea Ortega, Jamin Pillars, Paul Resnick, Corrie Sadler, Sean Smith, Robert Timon

Thank you – Questions?

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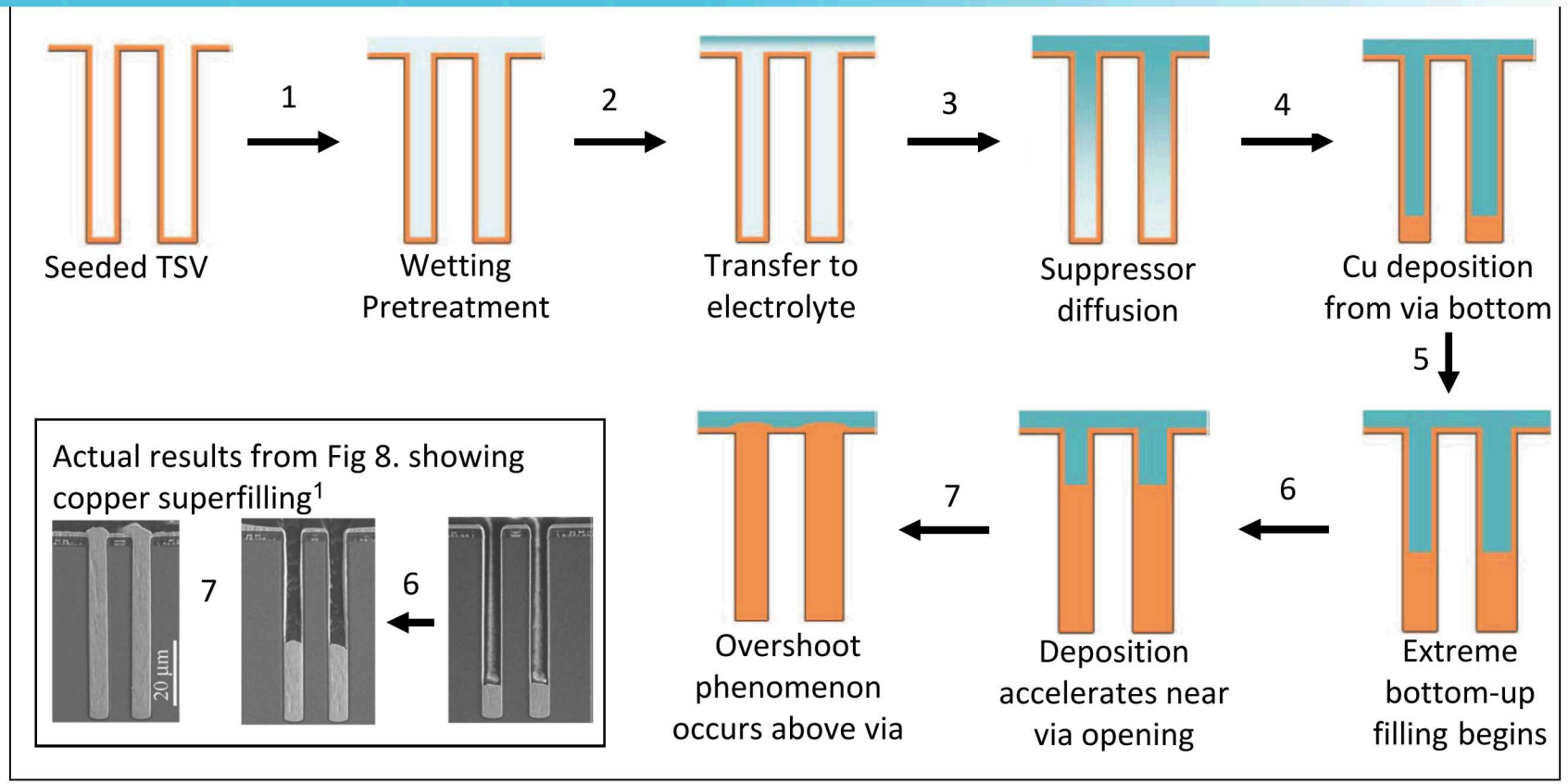
Supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

Back-up Slides

Bottom-up Filling Mesoscale TSVs

S-NDR Approach[1]

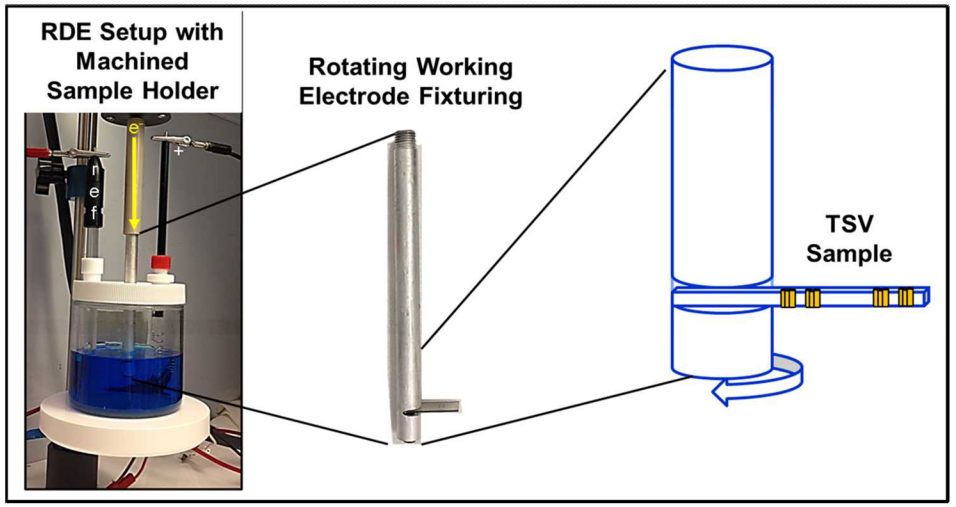
- Derived from work by Dan Josell and Tom Moffat at NIST Gaithersburg
- Single suppressor additive system
- Bottom-up growth arises from conformal seed metal



1. Journal of the Electrochemical Society, 159 (4) D208-D216 (2012)

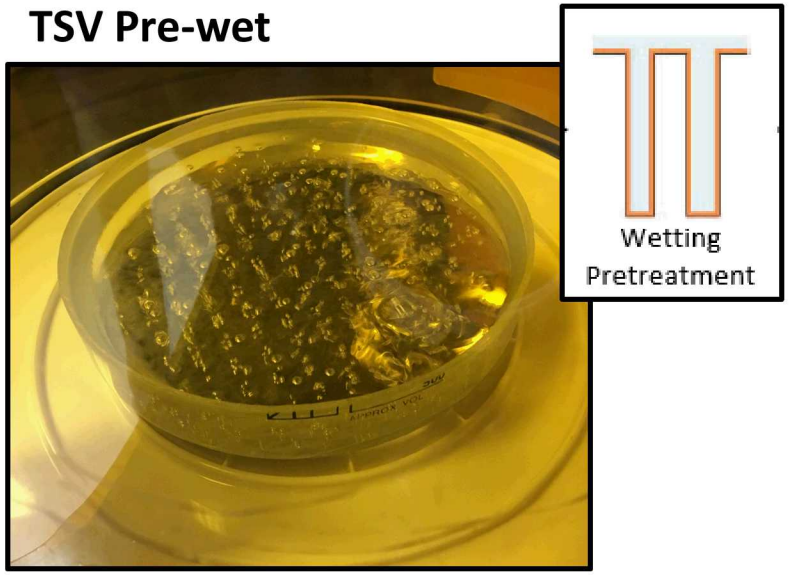
TSV Experimental Setup

Experimental Apparatus



- Hg/Hg_2SO_4 reference electrode
- Pt anode
- Al holder to rotate sample
- Pine rotating shaft to increase fluid flow and solution replenishment
- Bio-logic potentiostat and software

TSV Pre-wet



- TSV samples submersed in cooled IPA
- Vacuum chamber to evacuate air from TSVs
- TSV sample remains submersed in IPA until transferred directly into plating electrolyte

Potentiostatic runs in high chloride chemistry

1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, variable Tetronic 701, 400 RPM, 4 hours

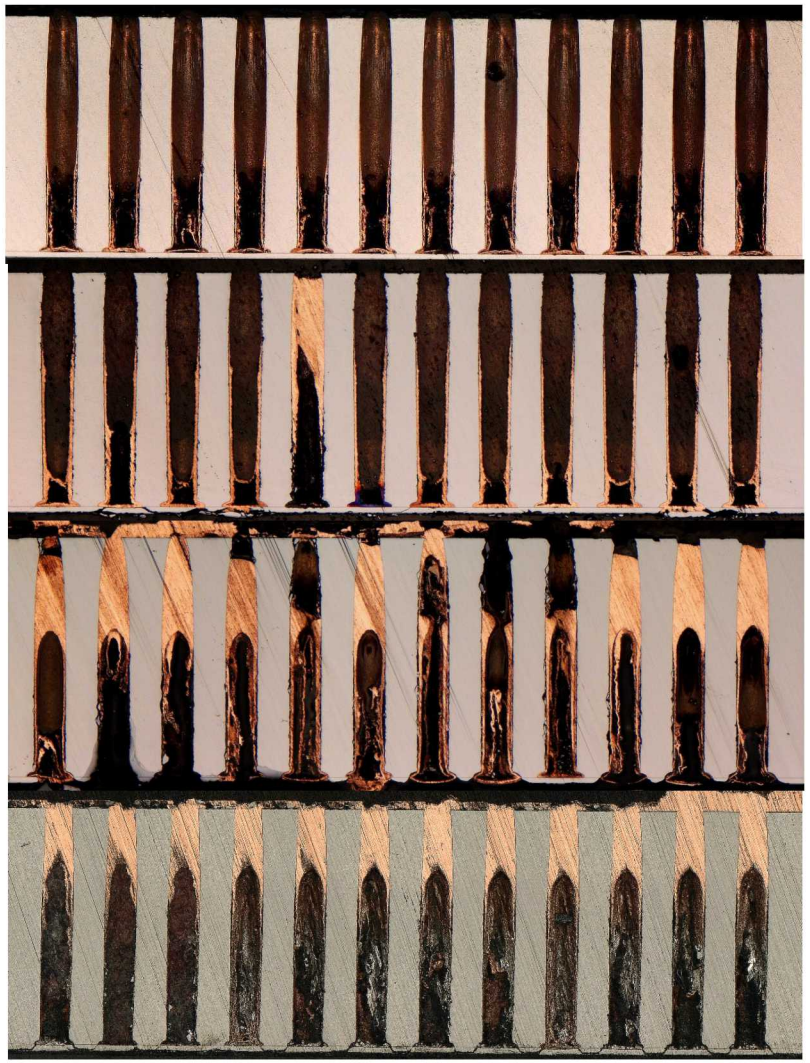
Bottom-up void-free filling difficult to achieve in chemistry with high chloride concentration

-640 mV

-630 mV

-620 mV

25 uM Tetronic701 plating solution



-600mV

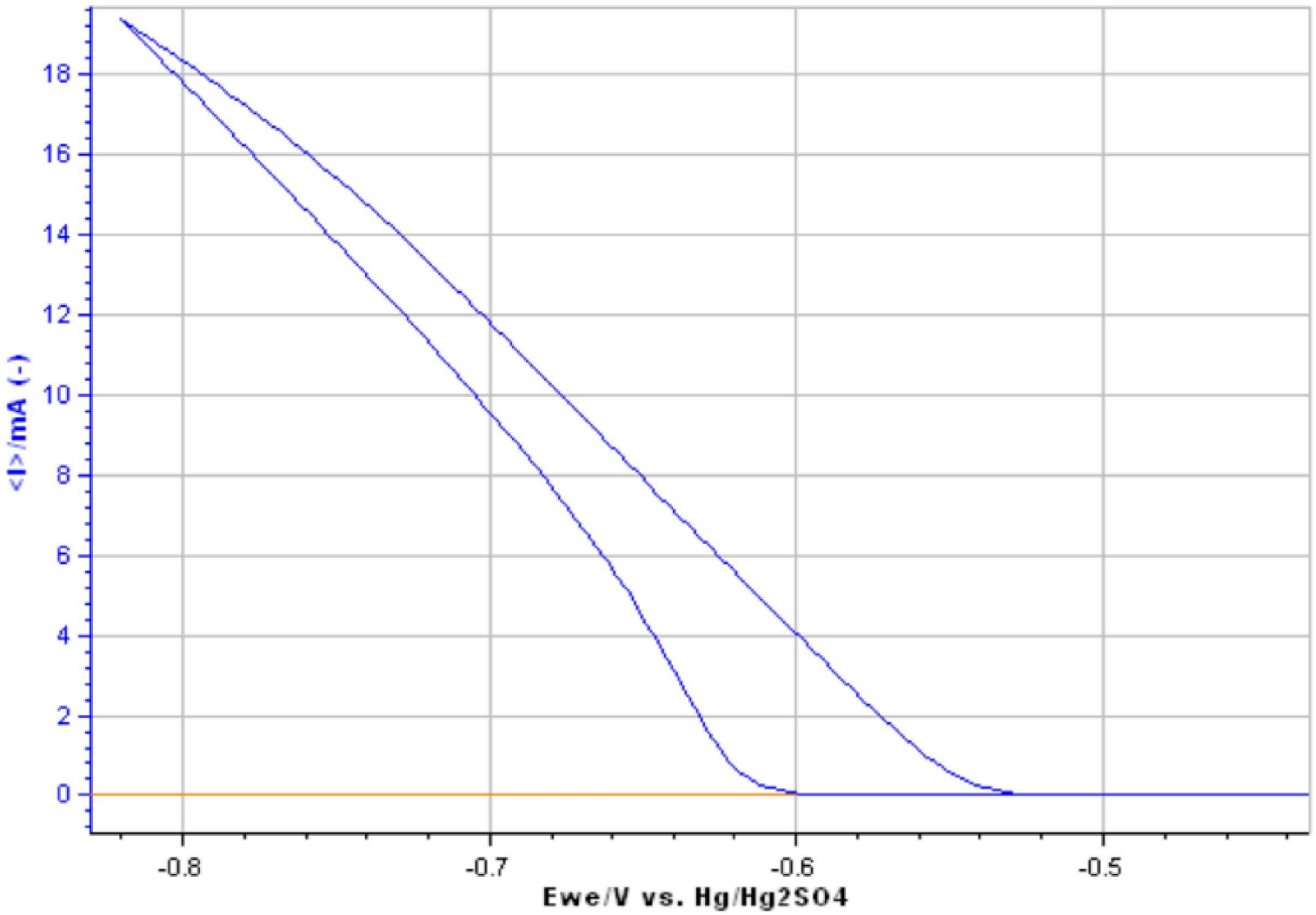
-620mV

-630mV

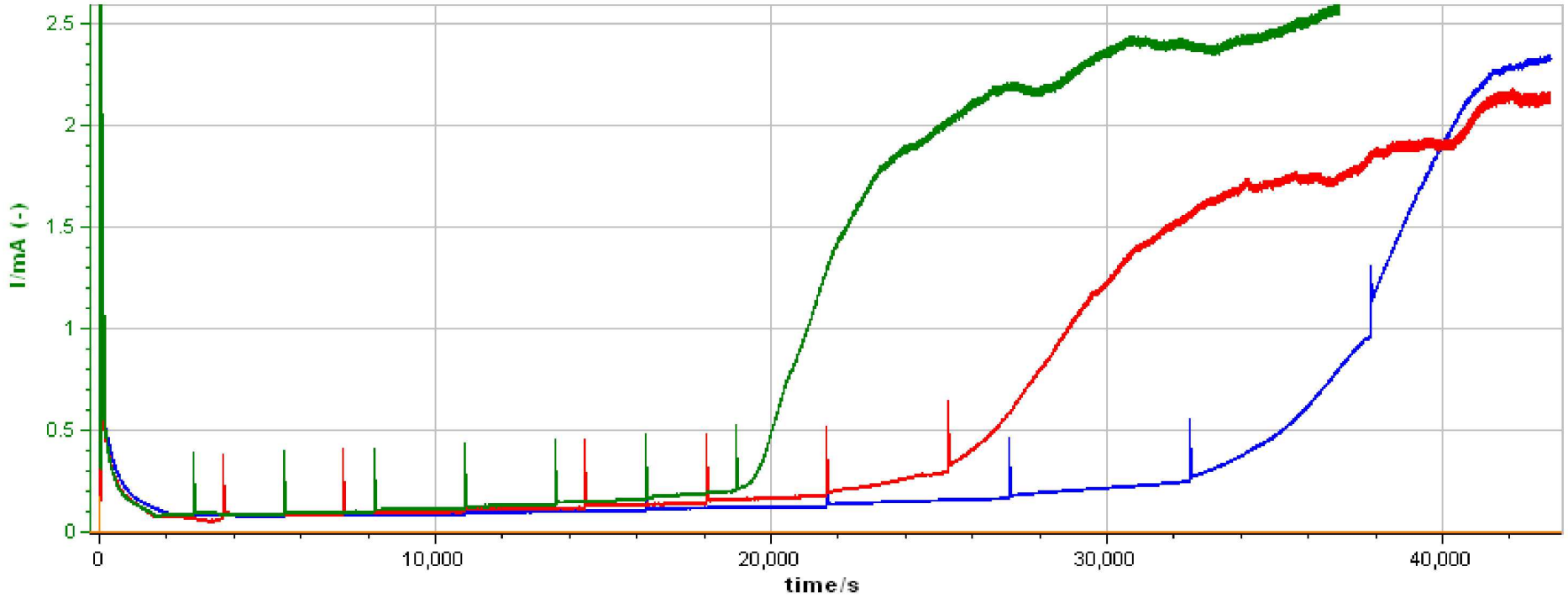
-640mV

50 uM Tetronic701 plating soultion

1.25 M $CuSO_4$, 0.25 M MSA, 1 mM KCl, 25 uM Tetronic 701, 400 RPM



Potential Stepping Runs - Current Data (45 min, 1 hr, 1.5 hr)

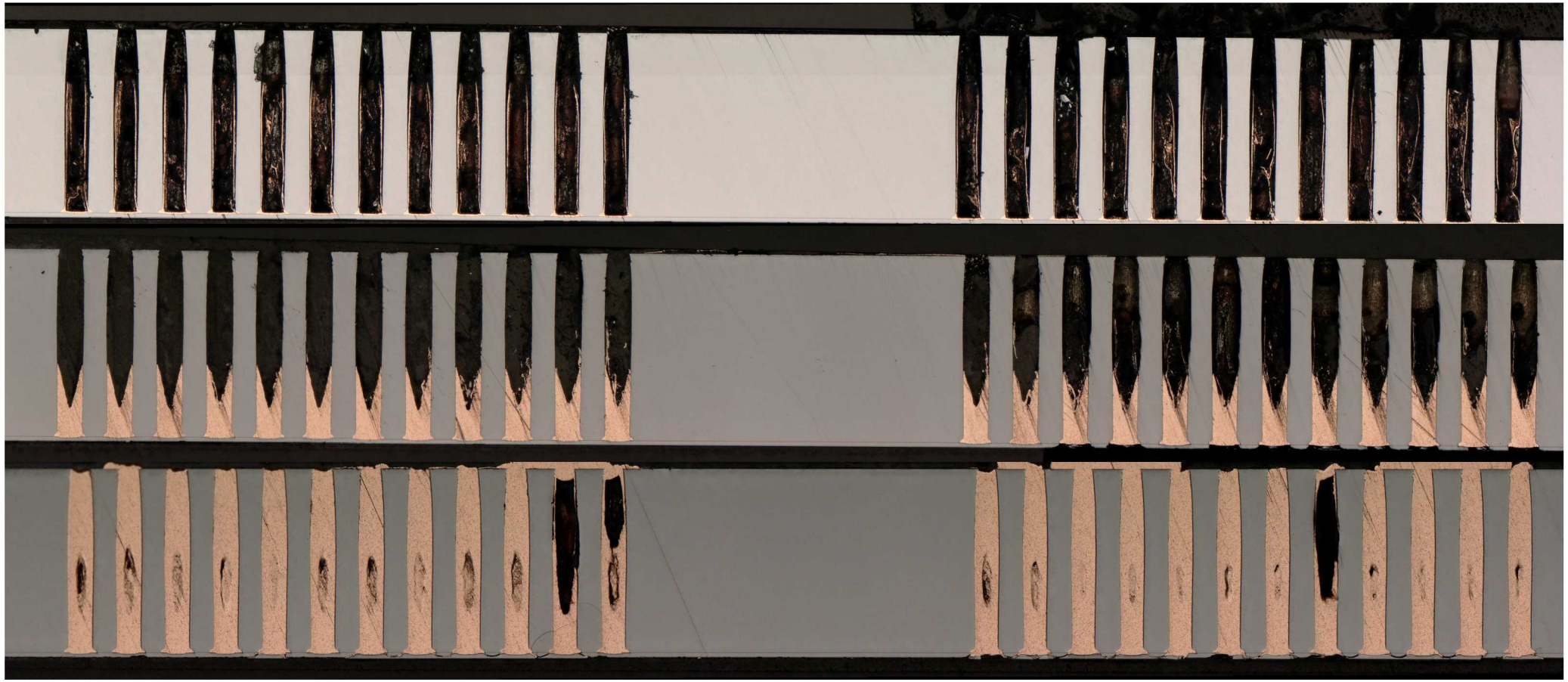


Sample	Soak	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8
(A) K4	-0.4 V	-0.50 V	-0.51 V	-0.52 V	-0.53 V	-0.54 V	-0.55 V	-0.56 V	-0.57 V
	1 min	1.5 hr each							
(B) K5	-0.4 V	-0.50 V	-0.51 V	-0.52 V	-0.53 V	-0.54 V	-0.55 V	-0.56 V	-0.57 V
	1 min	1 hr each							5 hr
(C) K8	-0.4 V	-0.4 V	-0.50 V	-0.51 V	-0.52 V	-0.53 V	-0.54 V	-0.55 V	-0.56 V
	1 min	45 min each							5 hr

Evaluation of Sample B Voiding

Steps for Sample B Plating Run

	Soak	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8
Voltage	-0.4 V	-0.50 V	-0.51 V	-0.52 V	-0.53 V	-0.54 V	-0.55 V	-0.56 V	-0.57 V
Time	1 min	1 hr each							5 hr



Step 1/8

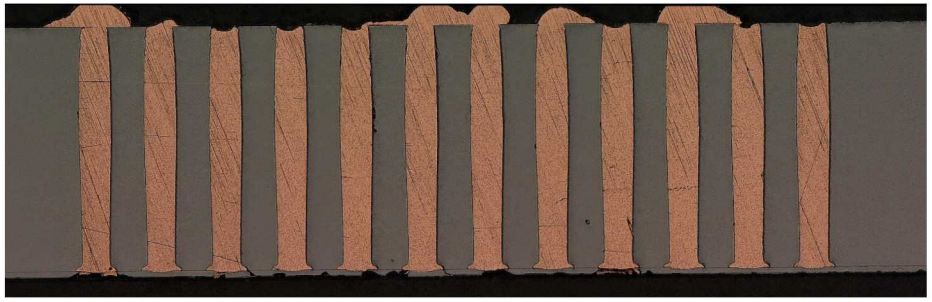
Step 7/8

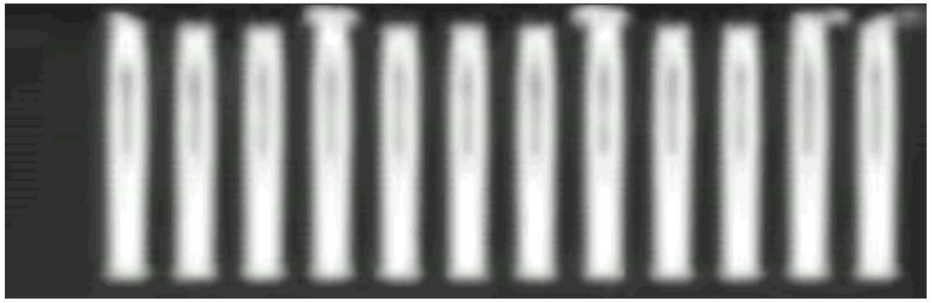
Step 8/8

Experimental Changes for Void Elimination

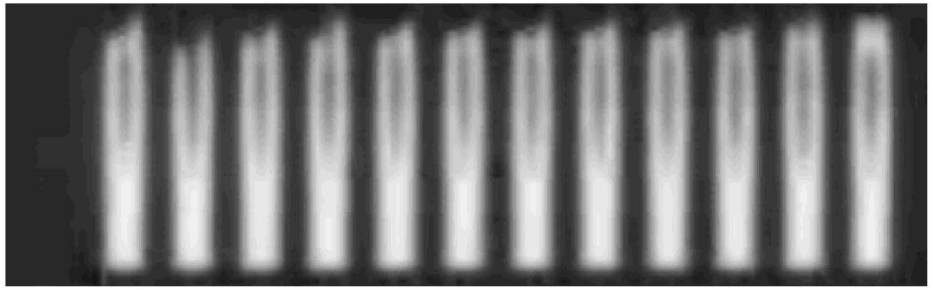
Longer time intervals and smaller voltage steps decreased voiding.

2 hr intervals
10 mV steps
-500 mV to -560 mV

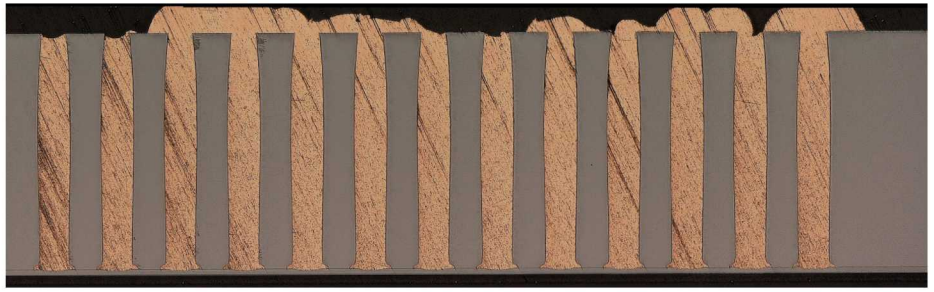


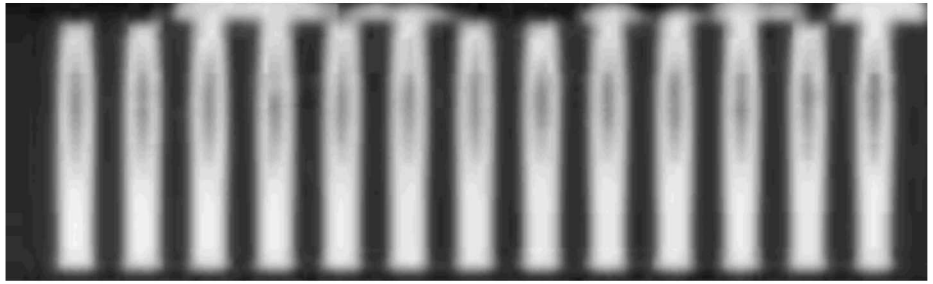


1 hr intervals
5 mV steps
-500 mV to -560 mV

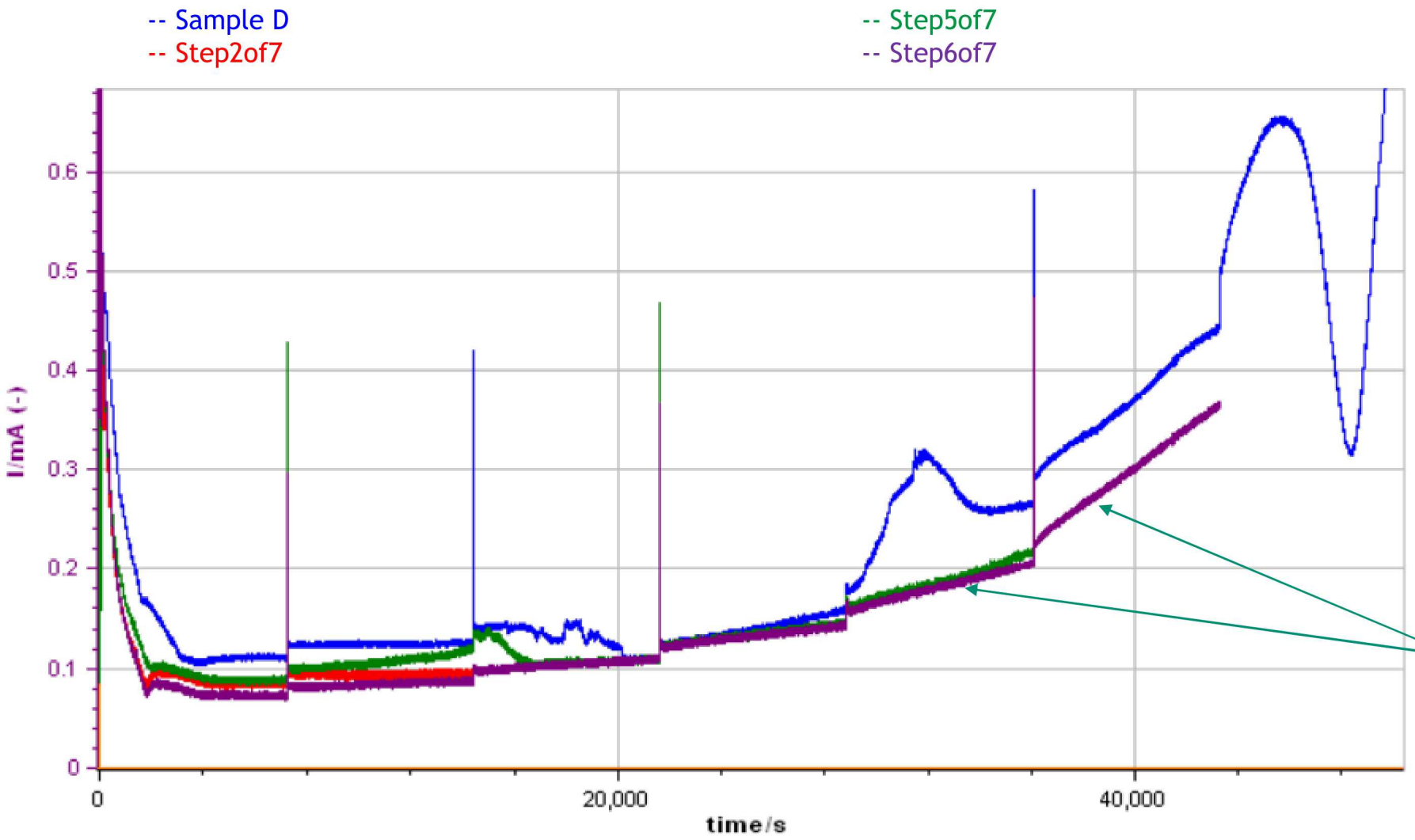


1 hr intervals
5 mV steps
-500 mV to -565 mV



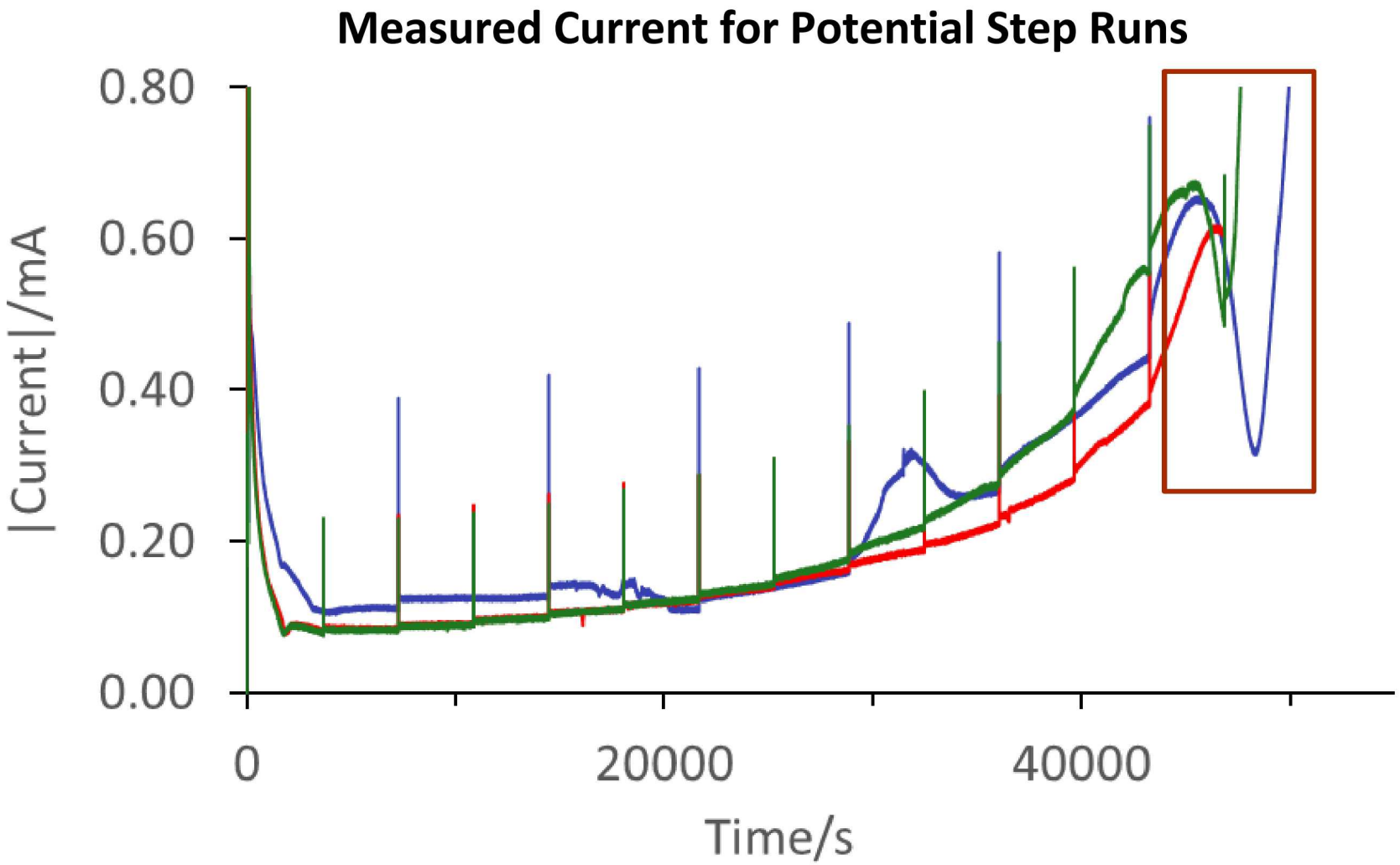


Void Formation Analysis – Current Data (2 hr sample)

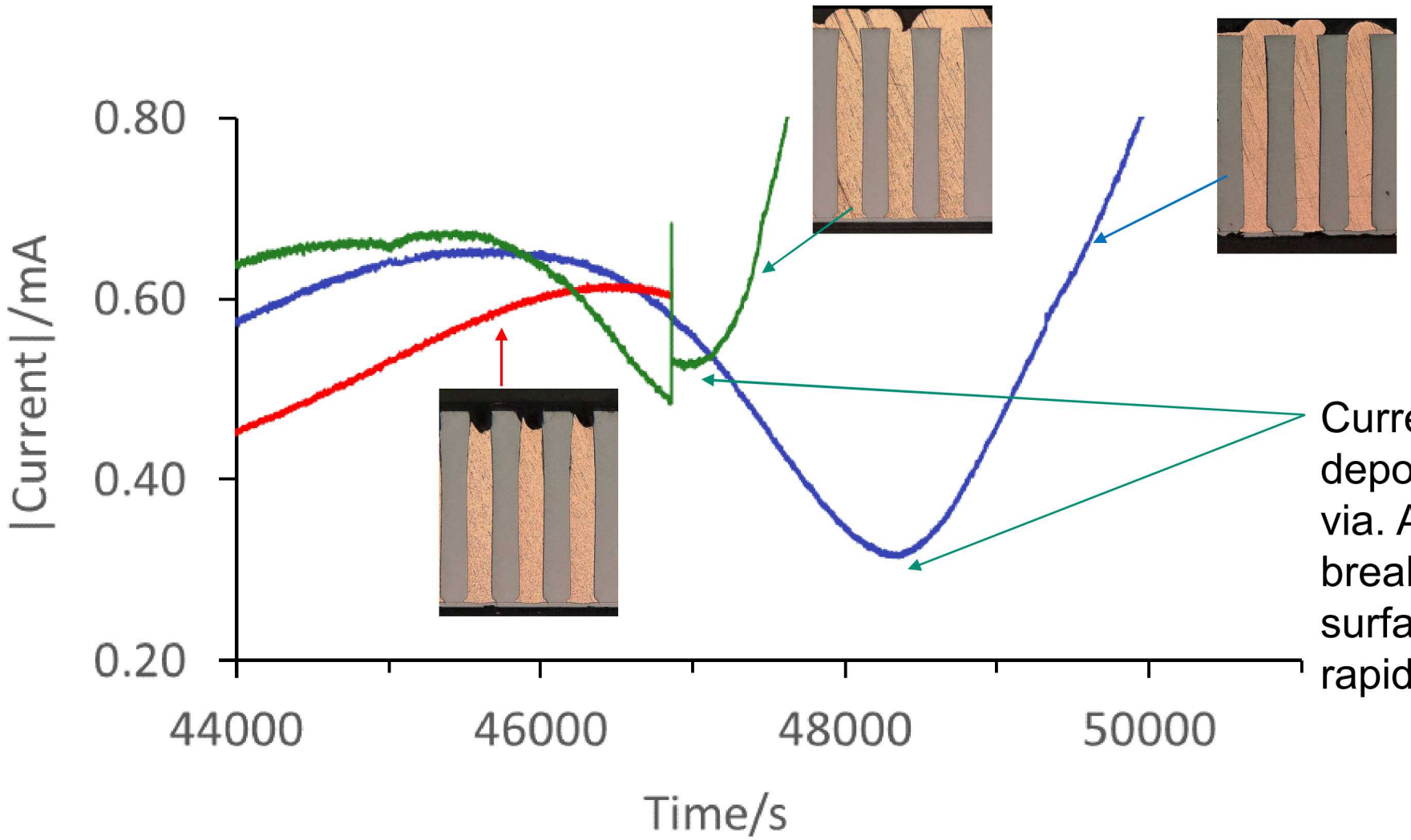


Void formation initiates at step 5 and grows in step 6.

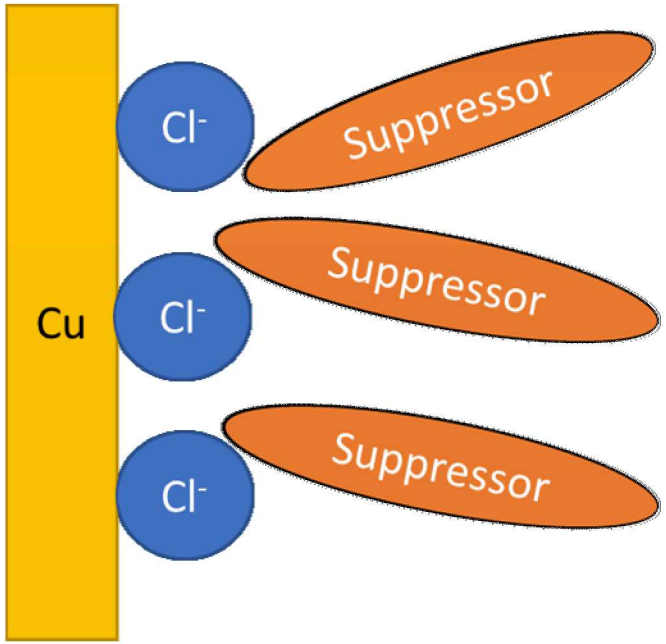
Analyzing Current Transient to Identify Fill Completion



Analyzing Current Transient to Identify Fill Completion



Current minima indicating deposition reached top of via. After suppression breakdown on the field surface, current increases rapidly.



Tetronic 701