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# *Formation of Ohmic Contacts to n-GaAs at Temperatures Compatible with Indium Flip-Chip Bonding*

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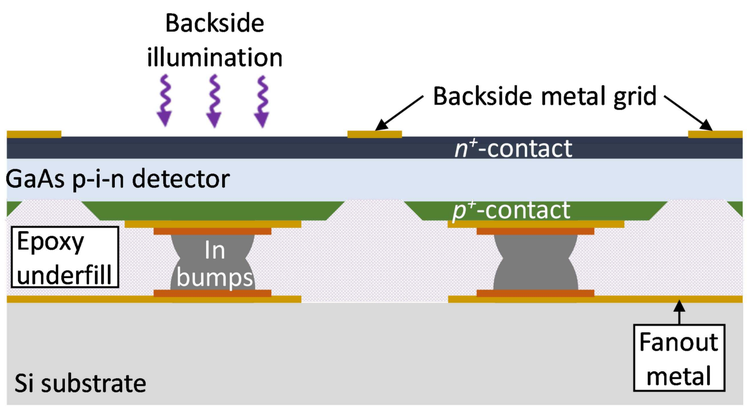
## Abstract and Background

### Backside-illuminated GaAs detectors

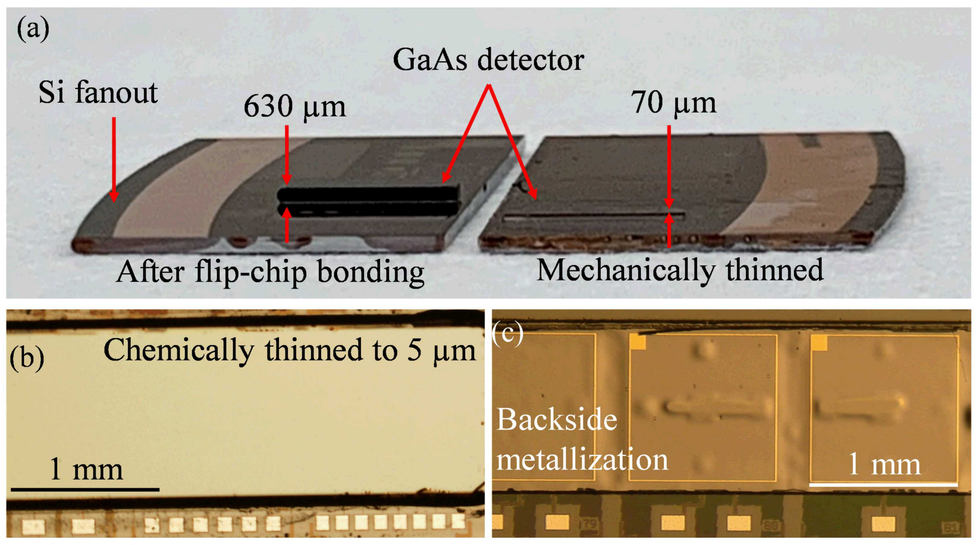
- III-V detectors integrated on Si ROICs have applications from the infrared to gamma rays
  - Backside illumination improves sensitivity at expense of challenging integration as biasing contacts must be formed after flip-chip bonding and substrate removal
  - In bump flip-chip bonded to Si allows for tight pixel pitch and advanced readout schemes
  - For maximum flexibility, detectors should be compatible with *p*- or *n*-pixelated readout



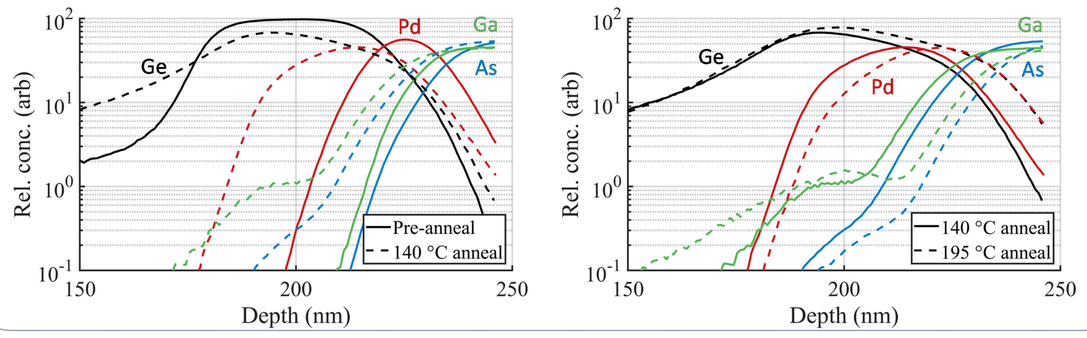

- Ohmic contacts to GaAs:
  - $p^+$-contacts are straightforward and don't required alloying at high temperatures
  - $n^+$-contacts are typically formed at 400 ℃ and are not compatible with the In melting point of 156 ℃ or the degradation point of many underfill epoxies
  - Prior work [1-4] has shown $n^+$-contacts formed at 150-250 ℃ using Pd/Ge/Au contacts
  - Here, we study PdGe contact formation at 140 ℃ for compatibility with In bump bonding

## Processing and Integration

- Pre-bond processing
  - $p^+$-contacts (Ti/Pt/Au), pixel isolation etch, underbump metal (Ti/Au/Ni/Au) and In bumps
- Flip-chip bonding
  - FC-150 flip-chip tool, $In_2O_3$ removed before bond with formic acid vapor
    - Bonding force: 2.5 mg/μm² of In bump area
  - Underfilled with Epotek 301 epoxy for mechanical stability, cured at room temperature
- Post-bond processing
  - Substrate mechanically thinned via lapping from full thickness to ~70 μm
  - Wet etching (1:5 citric:$H_2O_2$) removes the remaining substrate and stops in $Al_{0.4}Ga_{0.6}As$
  - Backside $n^+$-ohmic contacts: 7 nm Pd/ 50 nm Ge/ 200 nm Au, low-temperature anneal



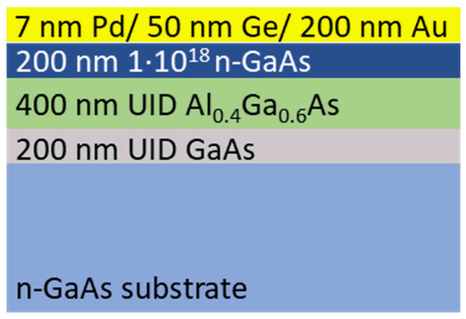

- Contact formation
  - SIMS analysis shows PdGe alloy formation after low-temperature annealing
  - Mechanism potentially different from high-temperature processing where Ge diffuses into GaAs to form a highly-doped ohmic contact layer [3]



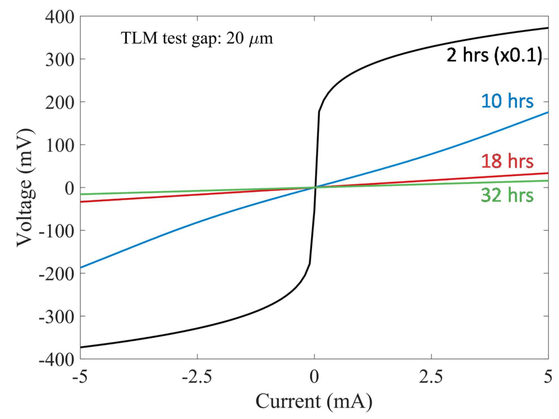

## Annealing Results

### Annealing study

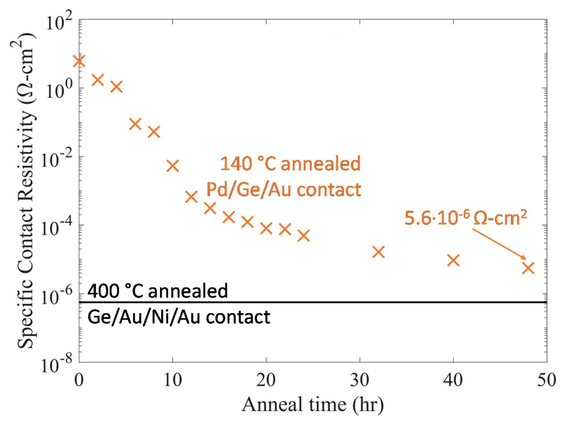
- Samples with patterned Pd/Ge/Au metal stack singulated and annealed in a $N_2$ furnace
- Transfer line method (TLM) test structures measured before annealing and vs. time
- At 140 ℃, we observe a transition to ohmic contact behavior after 10 hours annealing
  - Contact resistivity approaches standard alloyed contact after 50 hours of annealing
- Contact formation at higher temperatures:
  - For SCR ~5 μΩ·cm²: 48 hr @ 140 ℃, 7 hr @ 165 ℃, 0.5 hr @ 190 ℃
  - Extracted activation energy: 0.64 eV



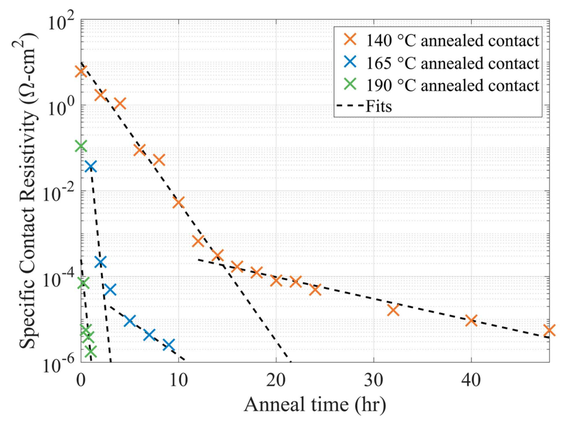

N-ohmic contact layer structure




TLM measurements vs. anneal time




Annealing at 140 ℃

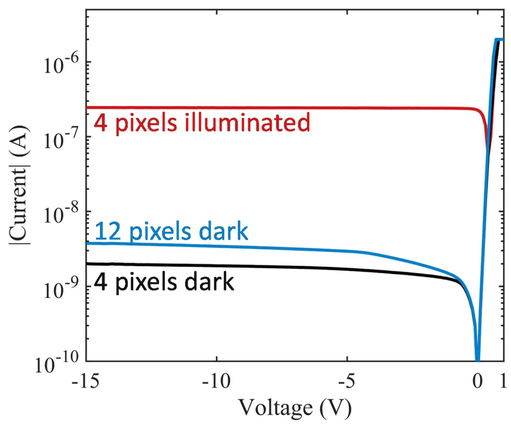



Contact resistance vs. temperature

## Integrated Detector Demonstration and Summary

**Backside optical illumination after integration and contact formation**

- Demonstrated device is a GaAs photodiode array flip-chip bonded to a Si fanout chip
- Backside illumination is achieved with probe station microscope illuminator
- Dark/light contrast >100x
- Dark current corresponds with number of chained pixels indicating integrity of In bumps




**High-quality $n^+$-ohmic contacts to GaAs enable heterogenous integration efforts with a wider array of temperature-sensitive materials such as In, epoxies, photoresist, and plastics**

## References

[1] M. Hinojosa, et al. *14th Intl. Conf. on Conc. Photov. Sys.*, 2012.
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[3] M. L. Lovejoy, et al., *J. Vac. Sci. & Tech. A*, vol. 13, pp. 758, 1995.
[4] L. C. Wang, et al., *J. Appl. Phys.*, vol. 79, pp. 4216, 1996.

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