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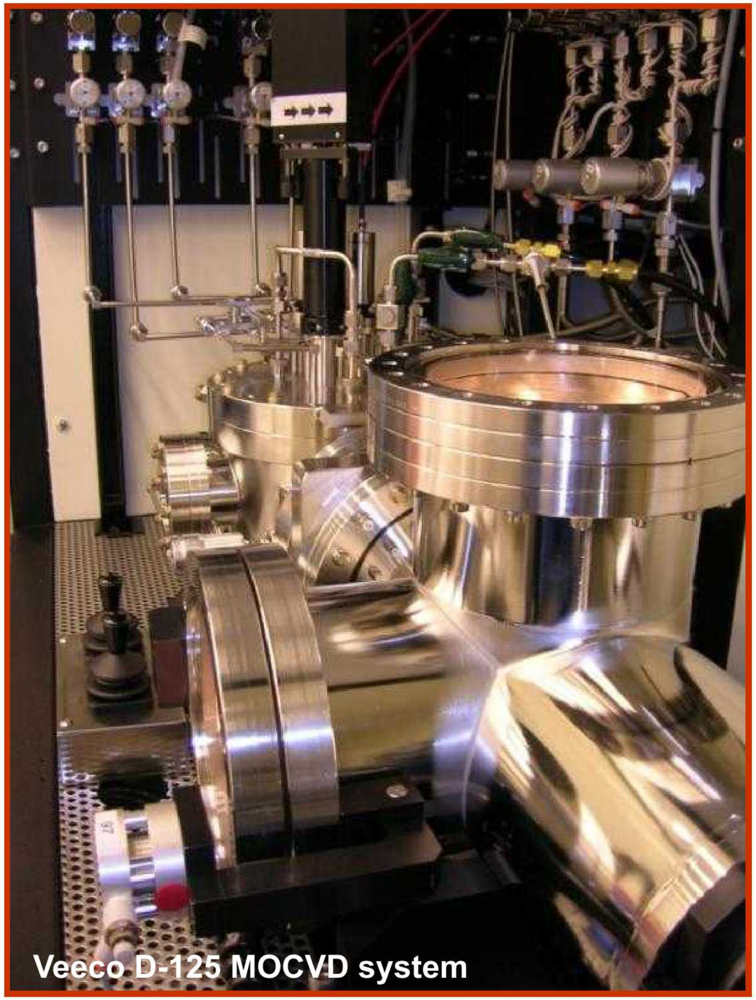

Selective Area Growth of p-type GaN for Gallium Nitride Power Switching Transistors

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U.S. DEPARTMENT OF ENERGY

Outline

- **Introduction**
  - Motivation for III-Nitrides for power electronics
  - Selective area p-type doping for diodes and transistors
- **GaN PN diode formation by regrowth of p-anode**
  - Regrowth of p-GaN on c- and m-plane
  - Regrowth of p-GaN in etched wells
- **Deep level optical spectroscopy**
- **Summary**

UWBG ULTRAWIDE BANDGAP POWER ELECTRONICS

Power Electronics are Ubiquitous

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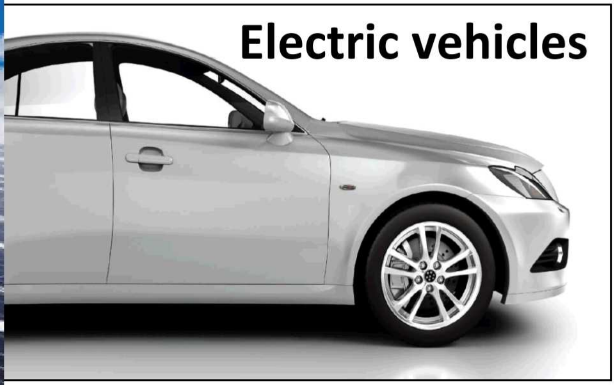
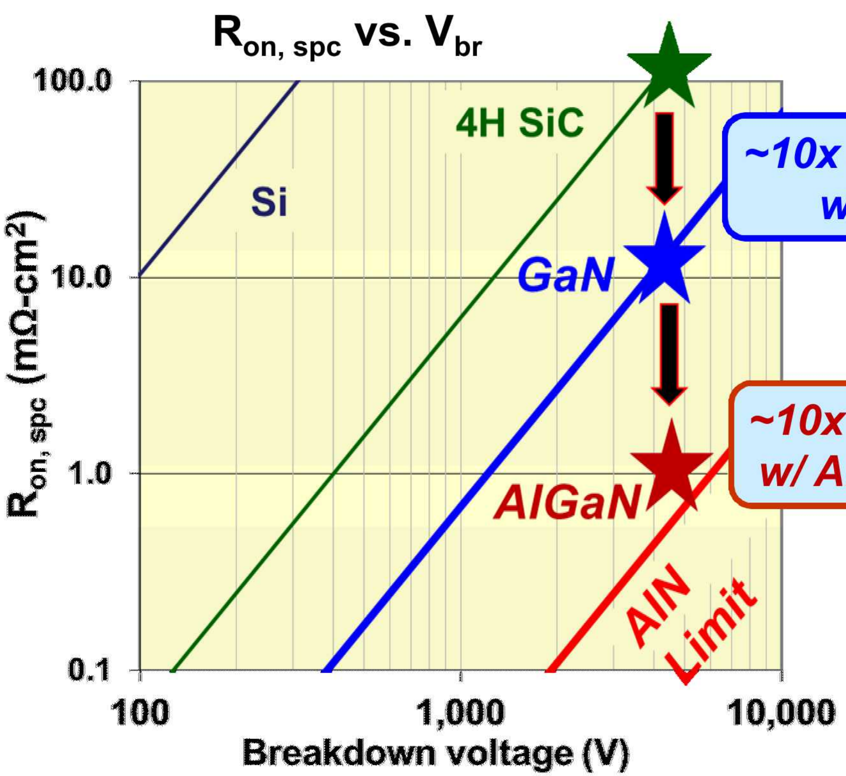


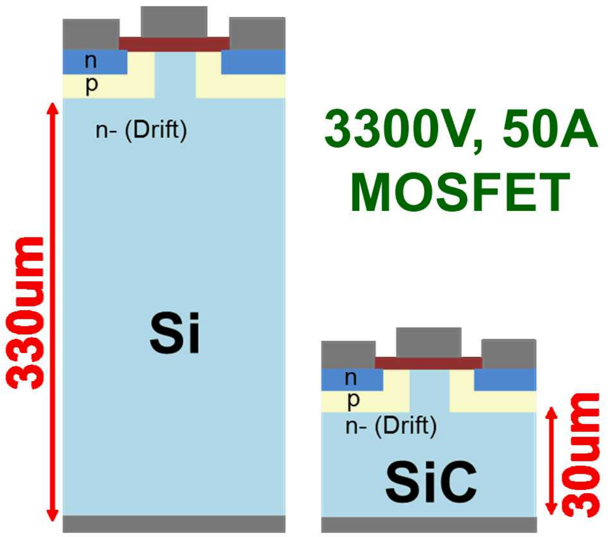
Why wide-bandgap semiconductors for power electronics?

Unipolar Figure of Merit (vertical devices)

$$UFOM = \frac{{V_{br}}^2}{R_{on,sp}} = \frac{1}{4}\varepsilon\mu {E_C}^3 \propto {E_g}^{7.5}$$



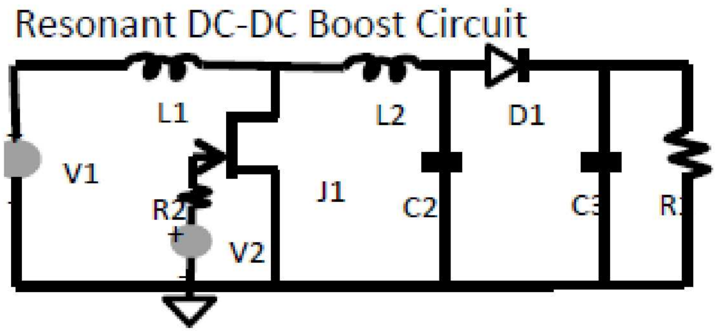
Si, SiC Power Transistors



	Si	SiC
V_{drop}:	250V	1.2V
P_{loss}:	*12,500W*	*60W*

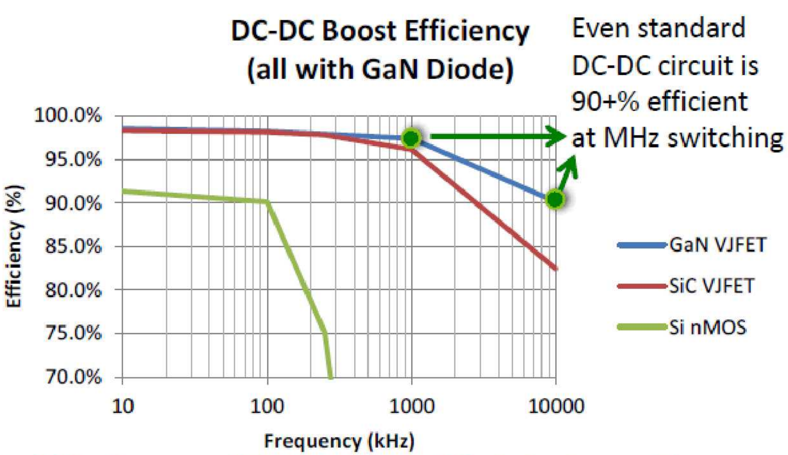
WBS devices:
➡ *Lower ohmic loss*

Why wide-bandgap semiconductors for power electronics?



➡ *New circuit designs*

➡ *Smaller components*



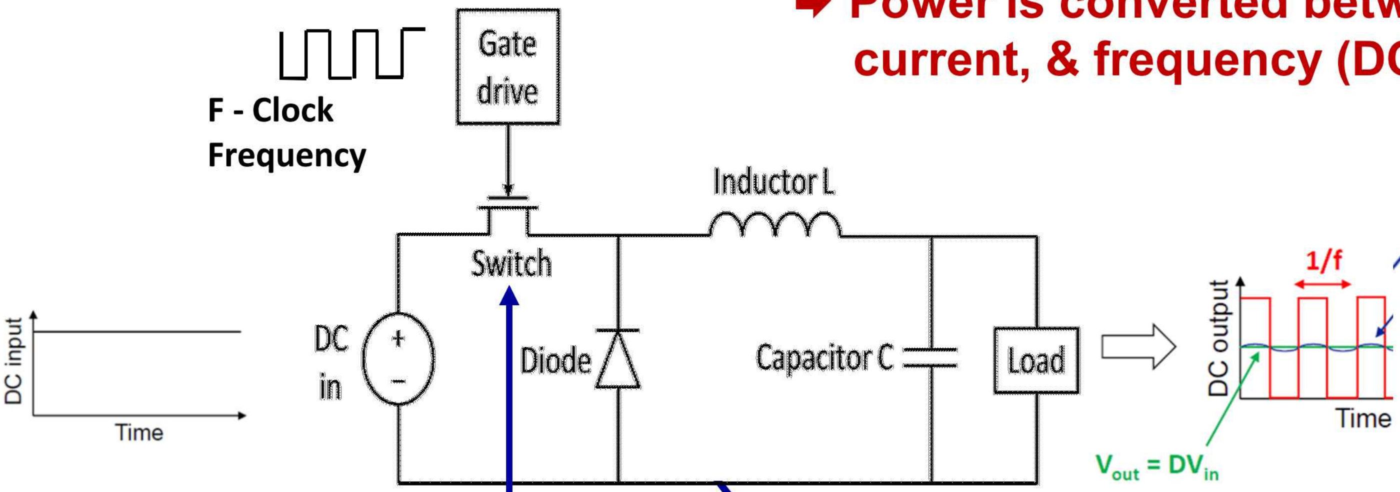
➡ *Higher efficiency @ higher frequency*

➡ *Smaller, more reliable systems*

Active electrical power switching for power management

Example: (Step down)DC to DC Buck converter

➡ **Power is converted between voltage, current, & frequency (DC & AC)**



$$\frac{V_{ripple}}{V_{out}} = \frac{1-D}{8LCf^2}$$

Increasing f allows one to reduce L and C while keeping the ripple constant

Switching transistor

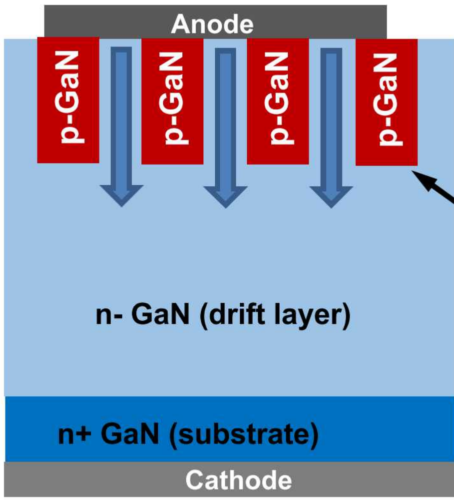
- **Vertical current flow for high-current & voltage**
- **Voltage dropped across thick drift layer**
- **D-MISFET, JFET, MOSFET ..etc..**

Diode

- **Vertical current flow**
- **SBD, PIN, and MPS diodes**

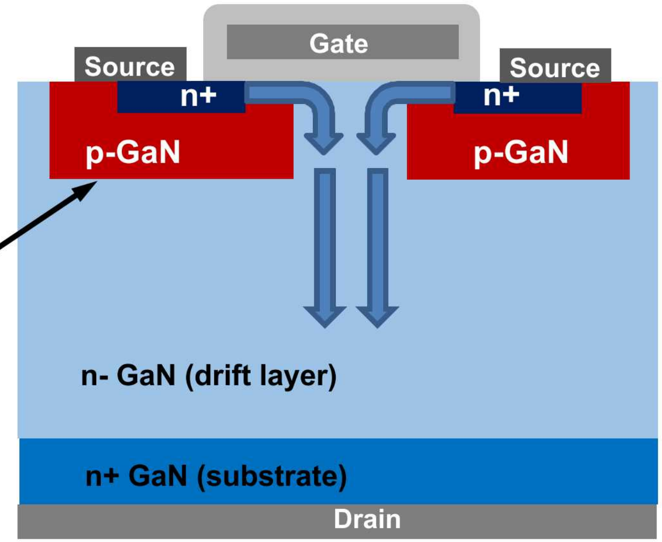
Practical high-voltage diodes and transistor require selective area p-type doping

Merged PIN Schottky (MPS) diode



p-well formed by selective area doping

Double-well Metal-Insulator-Semiconductor Field-Effect-Transistor (D-MISFET)

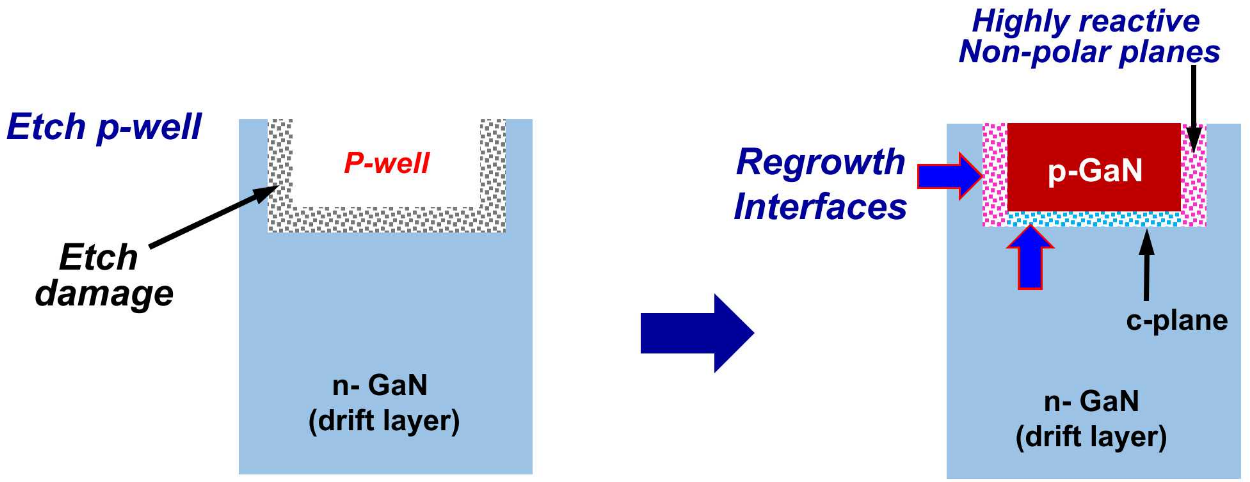


- **Reverse-bias PN junction key to multi-kilovolt blocking voltage (V_{br})**
  - ➡ **Must have low reverse leakage current**
- **P-layers formed by ion implantation and annealing for Si and SiC device**
  - ➡ **p-implant into GaN advancing but not sufficient to date**

➡ ***Form the p-well by selective-area-growth (SAG) of p-AlGaN***

Challenges to selective area regrowth of PN junctions

Sources of current leakage at regrown PN interface

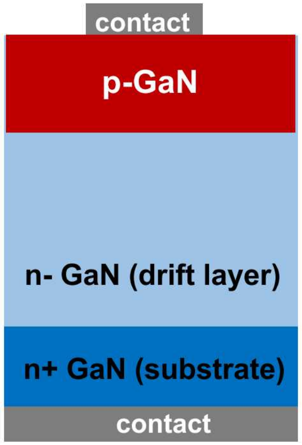


- **Electrically active impurities (Si, O, etc.)**
- **Damage to crystal structure from ICP etch resulting in extended (?) and point defects (e.g. vacancies).**
- **Incorporation rates of impurities and growth rates depend on crystal plane**
- **Impact of mask on regrowth and subsequent mask removal**

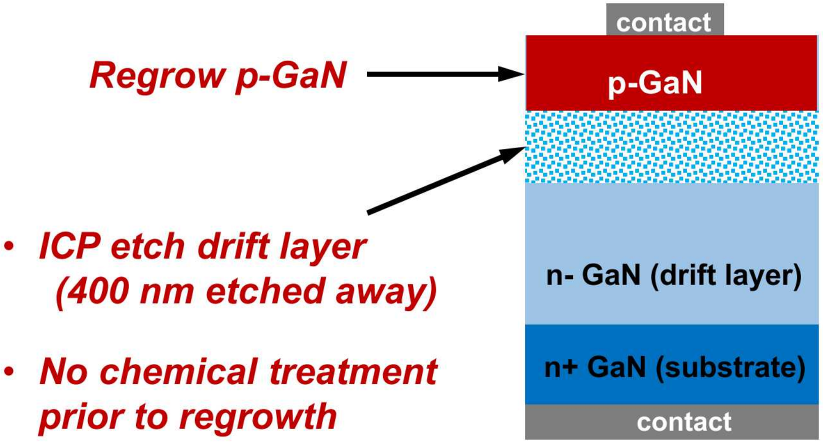
➡ ***Start simple, p-AlGaN regrowth only on c-plane drift layers***

P-GaN regrowth on ICP etched drift layer

Continuously Grown Diode



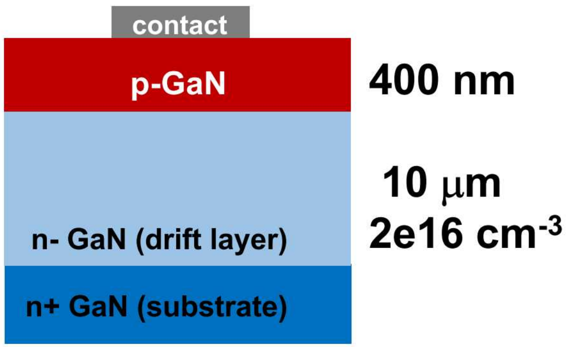
Dry-Etched and Regrown p-GaN



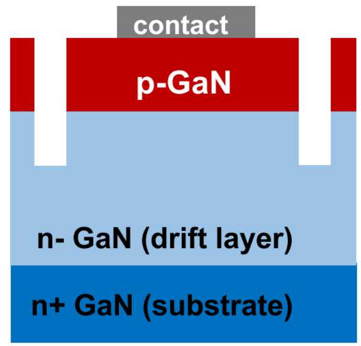
- **Compare electrical performance of continuously grown and etched/regrown diodes**
- **Low-damage inductively-coupled plasma (ICP) etch**
  - **ICP etch — $BCl_3/Cl_2/Ar$, ICP power — 125 W, RF power — 10 W**
  - **Optimized for improved ohmic contacts to etched AlGaN surfaces (Al > 0.6)**
- **Regrow p-GaN on ICP etched surface with same growth process**
  - **No chemical etch surface prior to p-GaN regrowth**
  - **Worst case scenario**

Diode fabrication: Quick-turn process

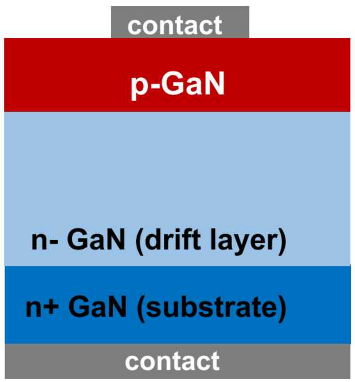
1) P-metal (Au/Pd, 600C, 60s)



2) Trench isolation (ICP etch)

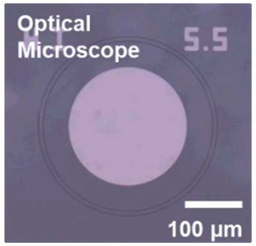


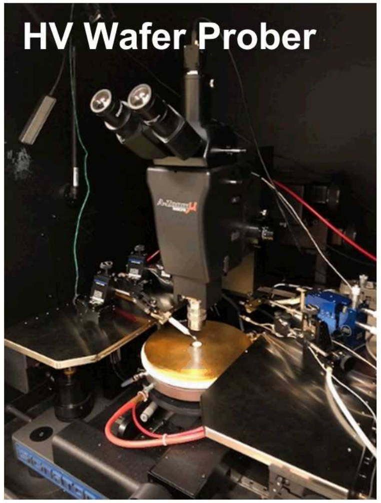
3) Backside metal (Ti/Al)



- Basic PN diode epi structure
- Simple process for rapid feed back
- No field management or passivation to increase breakdown voltage
- No wafer thinning to improve R_{on}
- Wafer-level current-voltage characterization

➡ *Focus on p-GaN regrowth*





Current-voltage characteristics of continuously grown and etched/regrown diode

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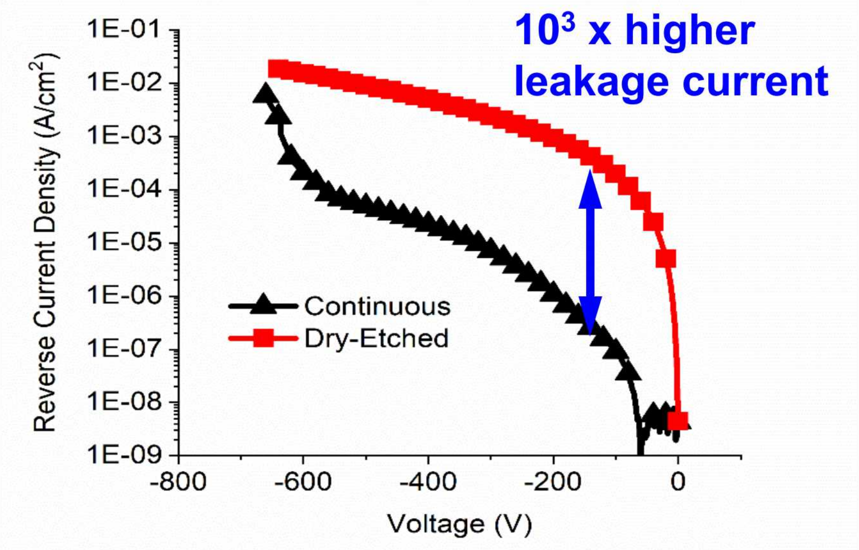
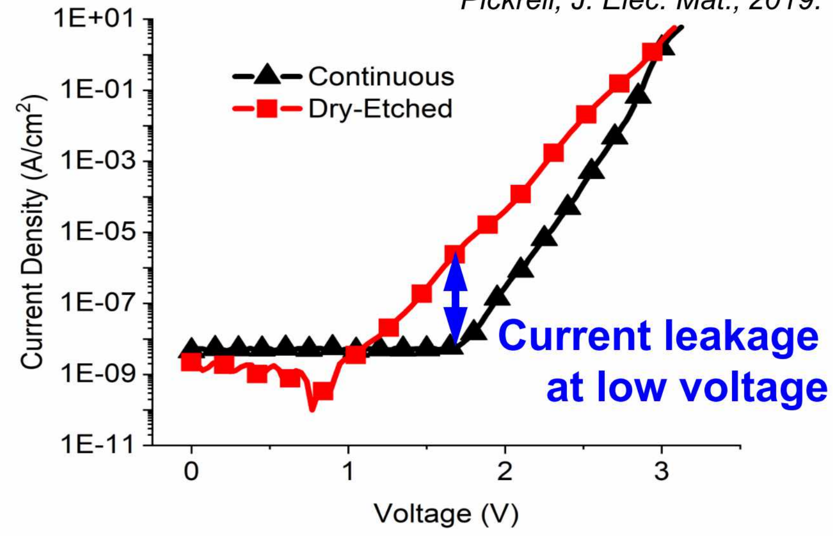
Reverse IV Characteristics



Forward IV Characteristics

Pickrell, J. Elec. Mat., 2019.



- **Etched and regrown diode have 10^3 x higher reverse leakage current**
- **High concentration of Si at regrowth interface (SIMS)**
- **Cause of leakage currents?**
  - **MOCVD regrowth process**
  - **Si "spike" at regrowth interface**
  - **Etch damage at regrowth interface**

➡ **1st study *MOCVD regrowth process***

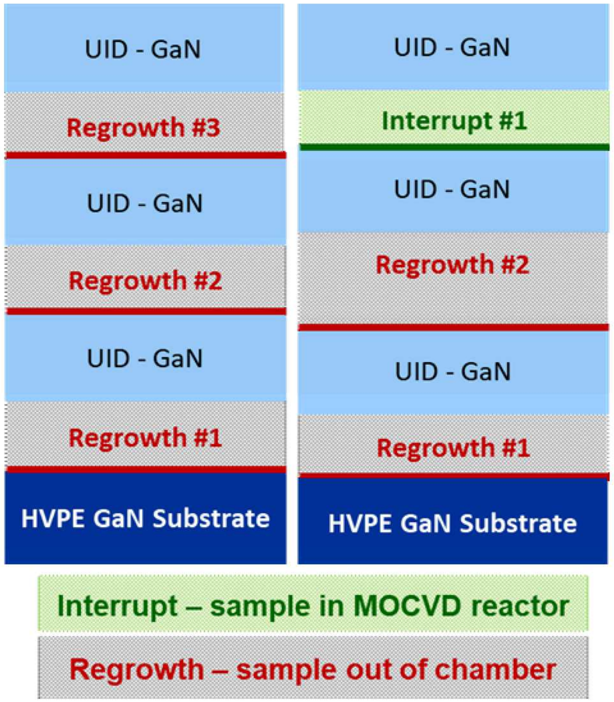
Impurities at regrowth and growth interrupt interface (GaN) — SIMS Studies

Characterize the extent of impurities (Si, O) at the regrown interface (GaN)

- **Is silicon (oxygen) coming from inside the reactor?**
  - **SiC platen**
  - **Backside of HVPE N+ GaN wafer**
  - **Si doped N-type GaN epilayer**
  - **Source material (TMGa, NH3)**
  - **Reactor parts**

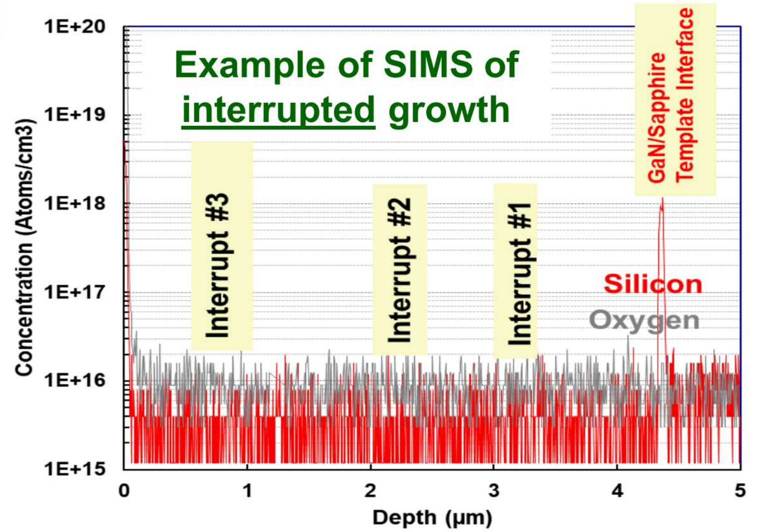
- **Studied many regrowth scenarios**
  - **In-chamber growth interrupts vs. out of chamber**
  - **Uid-GaN coated or uncoated SiC platen**
  - **Uid-GaN vs. Si-GaN surfaces**
  - **GaN substrate vs GaN/sapphire**
  - **Temperature & ramp-rate prior to regrowth**

Examples of SIMS interface structures



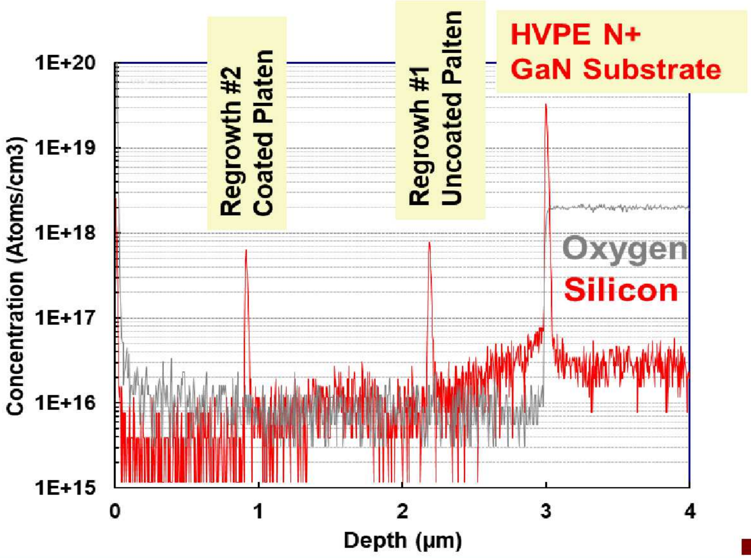
Impurities at regrowth and growth interrupt interface

- **Growth interrupts show MOCVD reactor is *not* a major source of silicon or oxygen**
  - All growth interrupts show:
    - [Si] < 5e16 cm^{-3} (N_s < 1 $e10^{10}$ cm^{-2})
    - [O] ~ at background level
  - Even when moving wafer to load lock and back into the chamber



- **Silicon is from *outside* the chamber but oxygen isn't incorporated**
  - Si is highly variable in concentration and time:
    - [Si] ~ 0.5-5 e18 cm^{-3} (N_s ~ 0.1-1 $e10^{12}$ cm^{-2})
    - [O] ~ at background level
  - HVPE GaN substrate (1st layer)
    - [Si] > 1.5e19 cm^{-3} (N_s > 4 $e10^{12}$ cm^{-2})

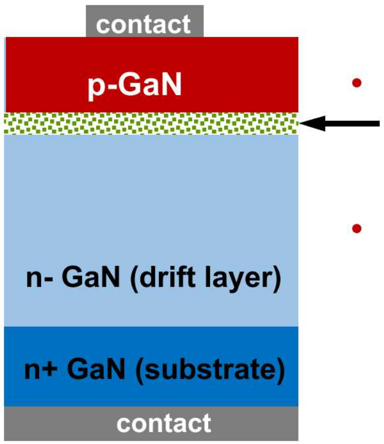
Example of SIMS of regrowth interfaces



Q: *Does Si "spike" matter?*

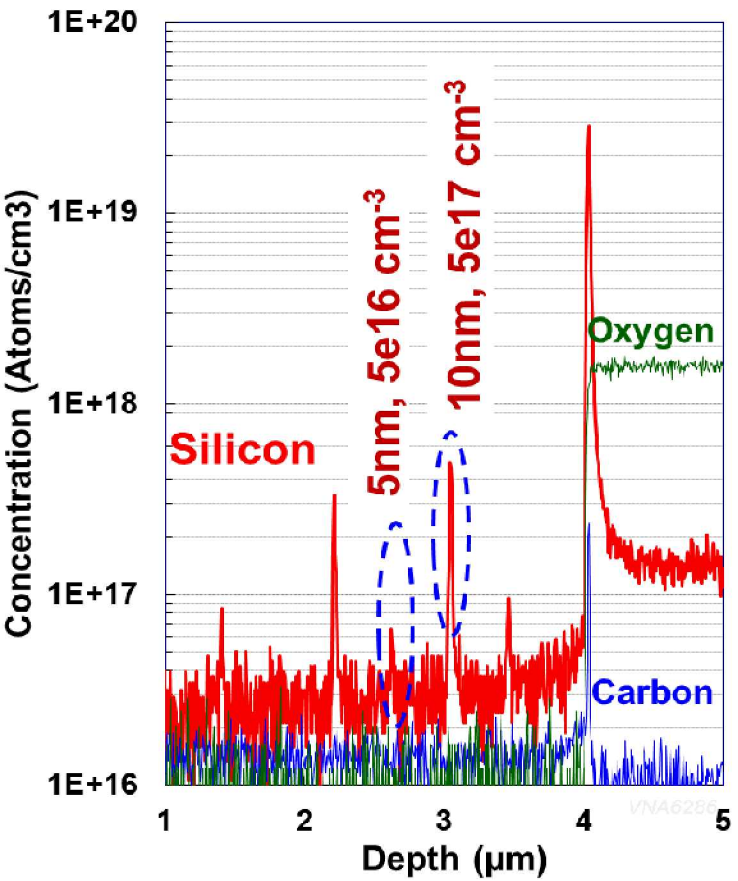
Determine effect of Si "spike" at PN junction

Continuously grown diode with simulated Si "spike"



- *Grow 5nm thick delta-doped layer*
- *Two samples*
  1. *5nm, [Si] ~ 5 e16 cm^{-3}*
  2. *10nm, [Si] ~ 5 e17 cm^{-3}*

SIMS of grown in Si "spike" (calibration of growth)



- **Simulate Si "spike" in regrown PN diodes**
  - ➡ **Add delta-doped Si layer prior to p-GaN growth**
- **Not perfect match to sheet Si in regrowth but avoids regrowth process**

IV Characteristics of continuously grown PN diodes with simulated Si "spike"

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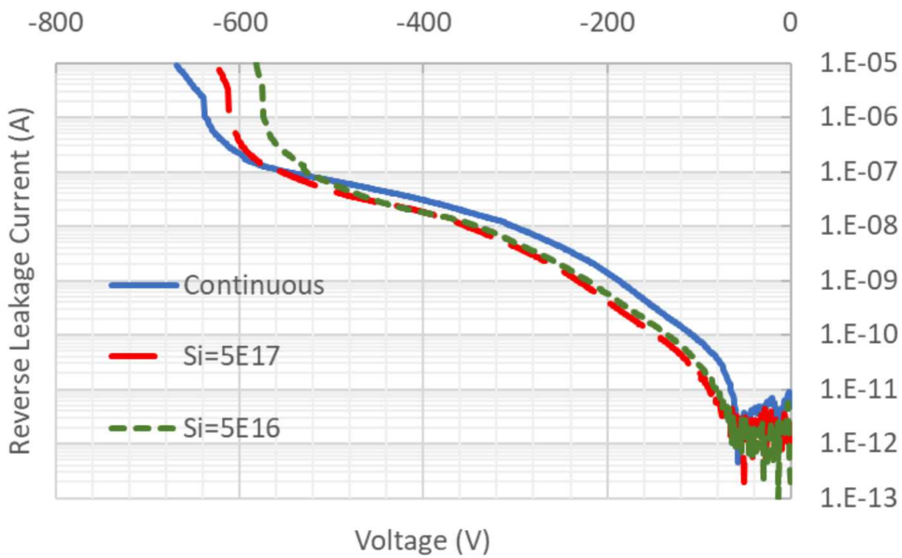
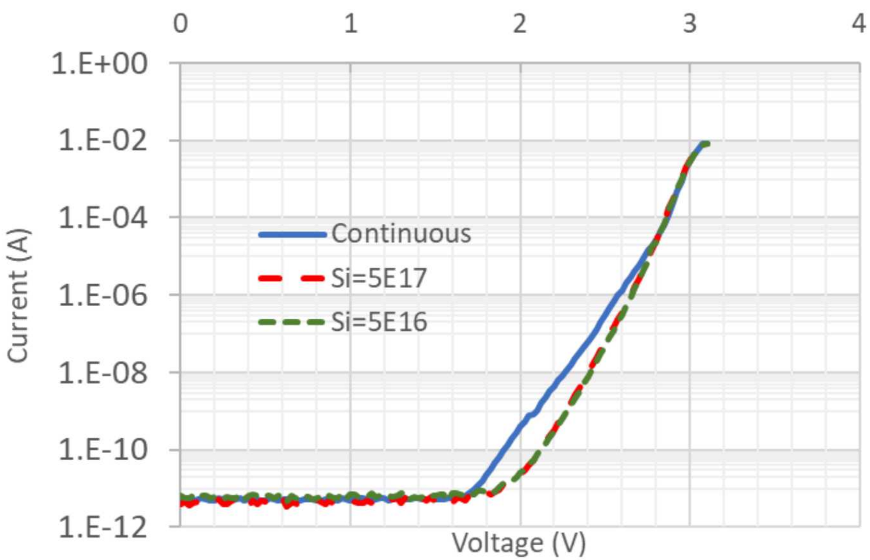
Reverse IV Characteristics



Forward IV Characteristics



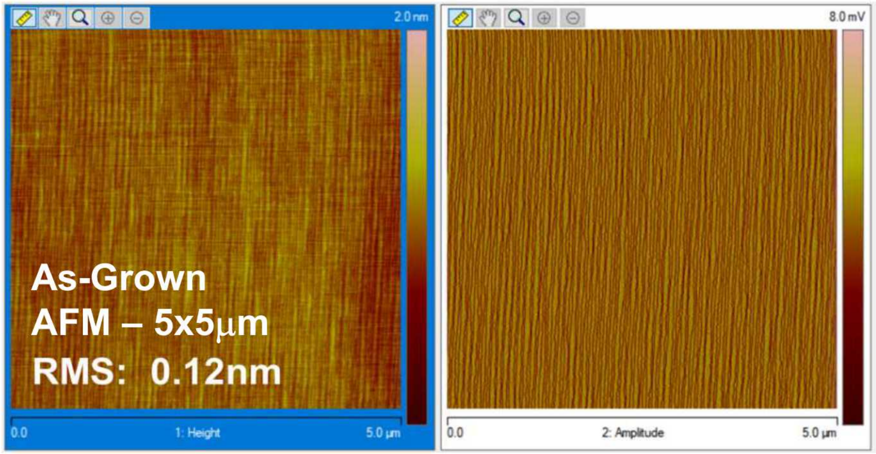
- **No significant difference in Fwd. & Revs. IVs**

➡ ***Diodes are tolerant to Si "spike" less than 5e17 cm^{-3} at pn junction***

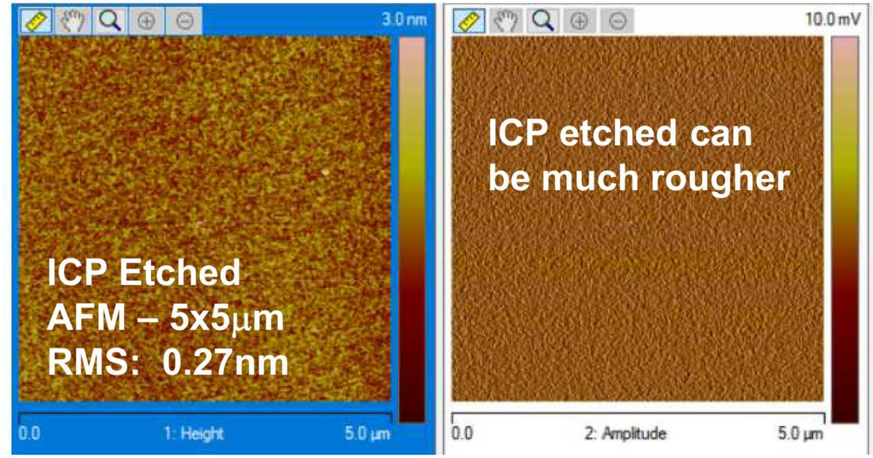
NEXT: Investigate MOCVD regrowth process

AFM of n-GaN drift layers prior to p-GaN regrowth

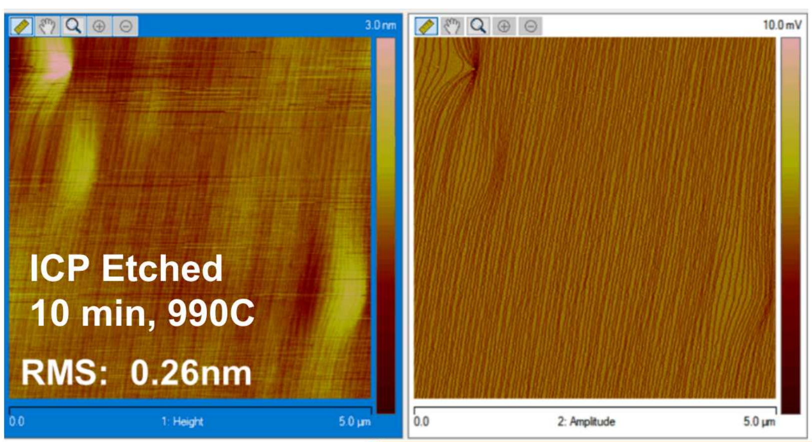
- ***As-grown GaN Drift layer***

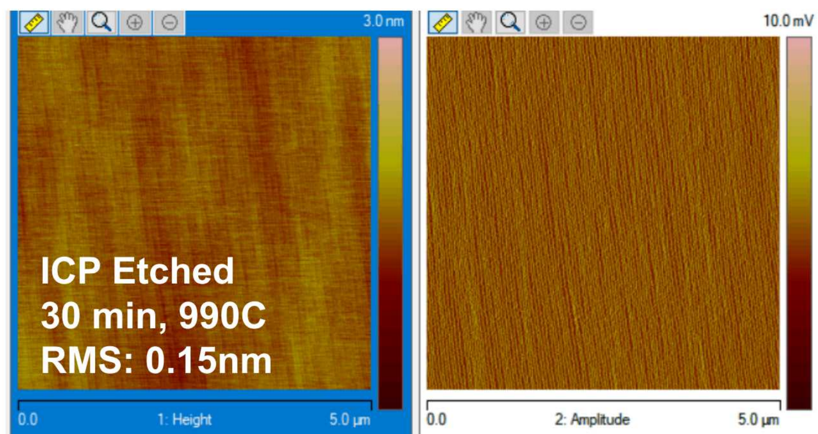


- ***ICP etched (400nm)GaN Drift layer***



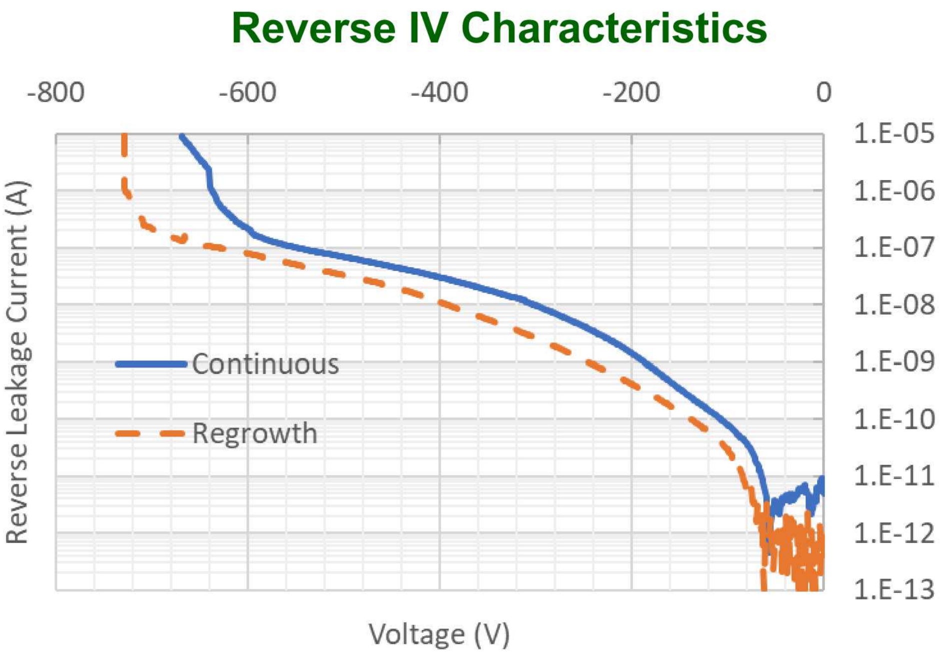
- ***Thermal process of GaN Drift layer***

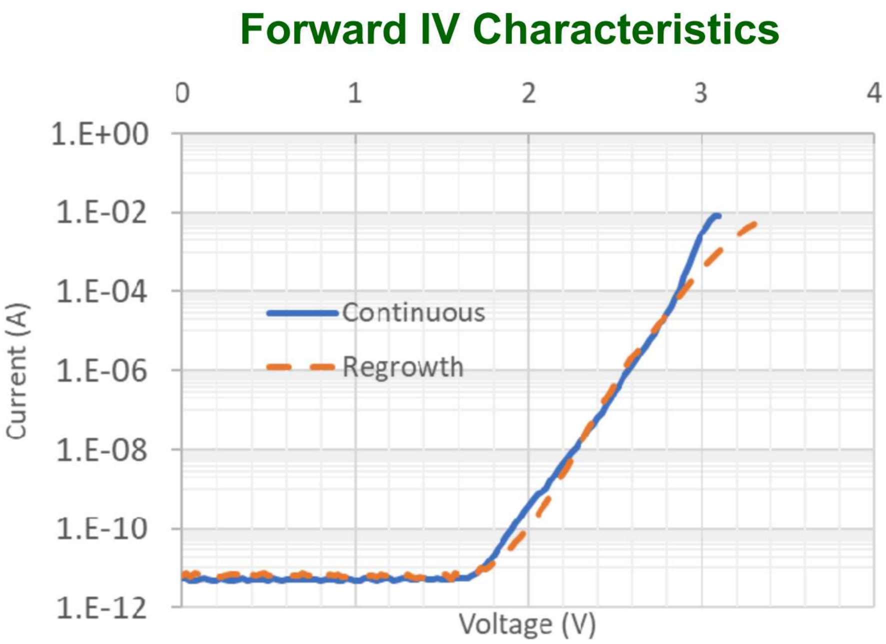




➡ **Thermal treatment of ICP etched drift layer recovers atomic steps similar to As-grown layer**

IV characteristics of continuous and regrown PN diodes





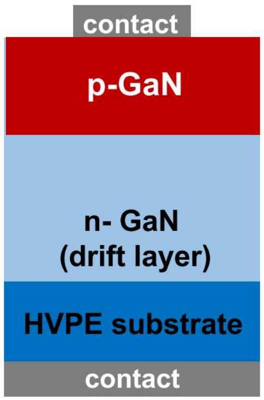
- **No significant difference in Fwd. & Revs. IVs**

➡ **MOCVD regrowth steps does not cause high reverse leakage**

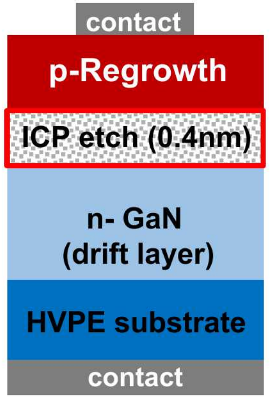
➡ **Sub-surface damage from ICP etch likely responsible for high reverse leakage current in etched/grown diodes**

Chemical treatment of ICP etched drift layers prior to p-GaN regrowth

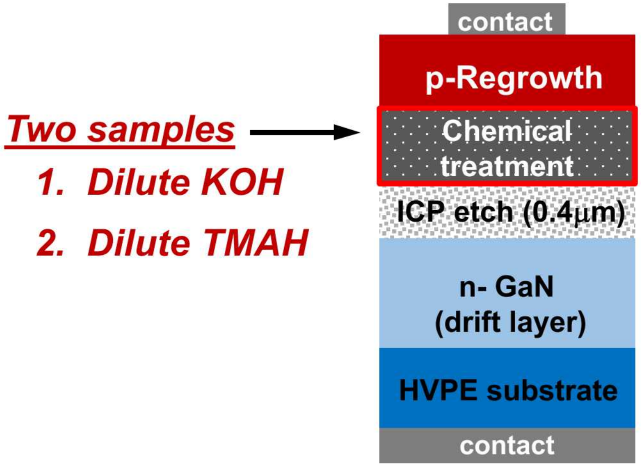
Continuously grown diode



Regrown diode on ICP etched drift



Regrown diode on chemically treated ICP etched drift



KOH treatment

- **AZ400K developer (2% KOH by wt. in water)**
- **10 min., 80 °C, DI rinse, N2 dry**

TMAH treatment

- **AZ300 MIF developer (<3% TMAH by wt. in water)**
- **20 min., 80 °C, DI rinse, N2 dry**

IV characteristics of regrown diodes on chemically treated ICP etched drift layers

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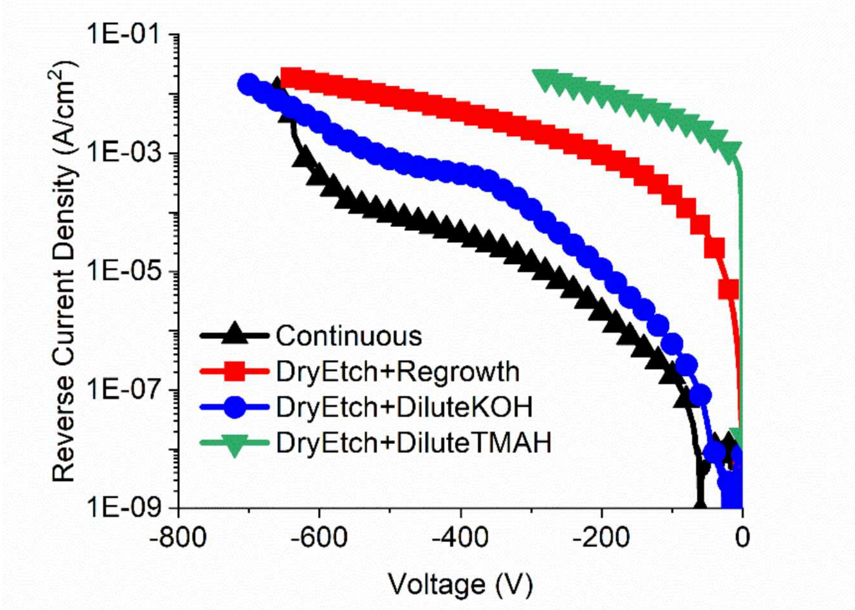
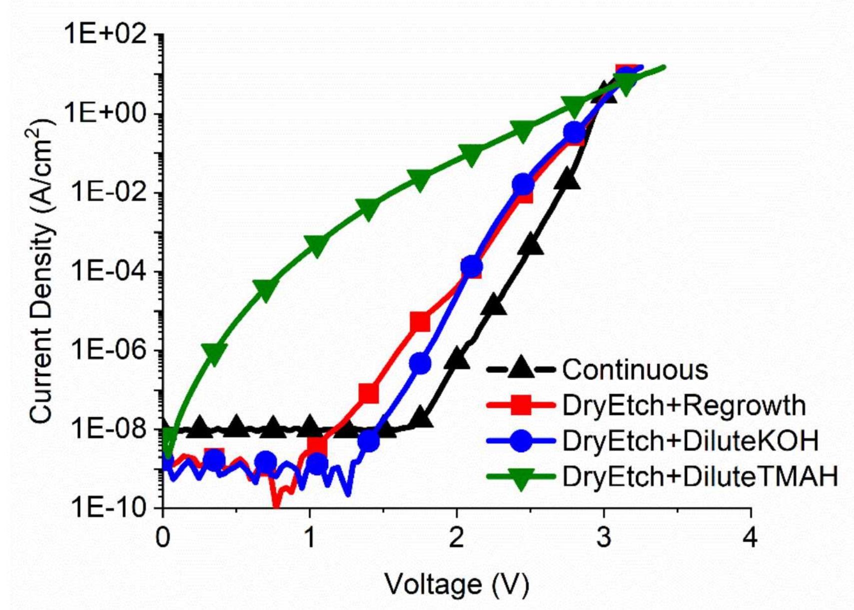
Reverse IV Characteristics

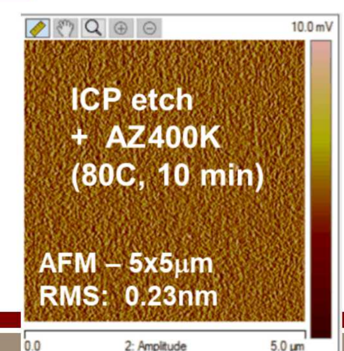


Forward IV Characteristics



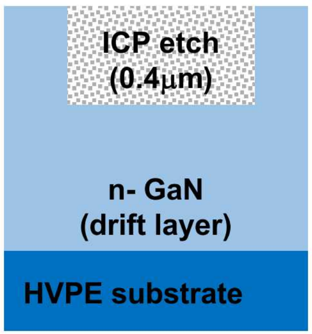
Diode with AZ400K treatment nearly matched continuously grown diode

- **No measureable removal of GaN or change in morphology was noted for 10 min. exposure**
- **Exposure to 3 hrs. did not improve IV characteristics but did reveal step edges.**

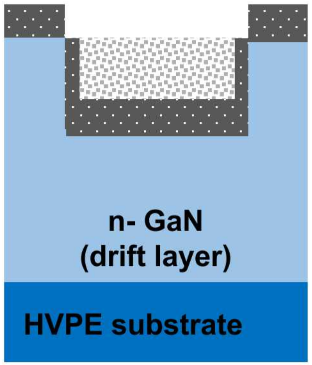


Regrowth of p-GaN in etched wells

1) ICP etch p-well



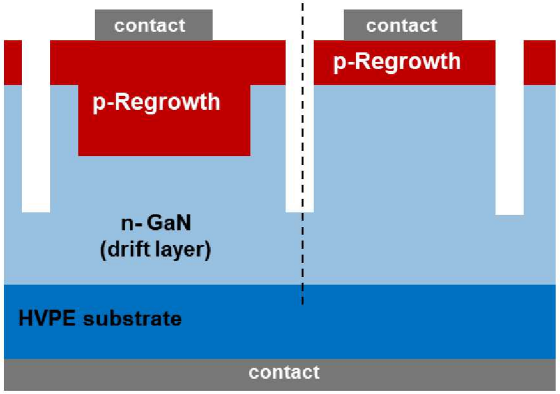
2) Remove PR KOH treatment



3) Quick-turn process

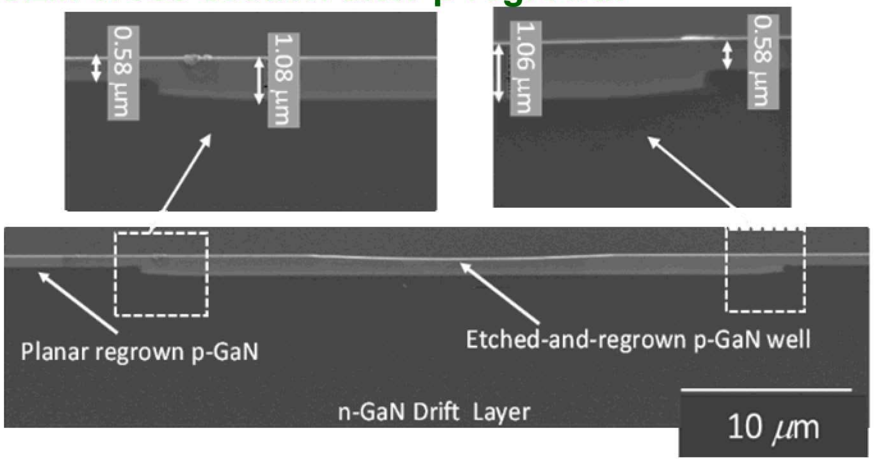
Etched, regrown diode in a ICP etched p-well

Planar regrown diode (ICP no etch)



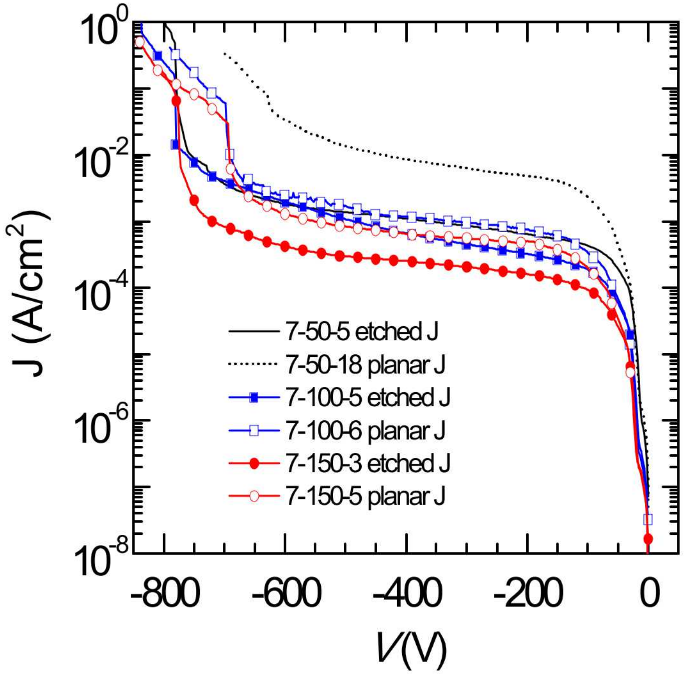
- ICP etch circular regions for p-well (50, 100, 150 μm)
- KOH treatment over all regrowth area
- P-GaN regrowth thickness — 0.65 μm
- P-metal diameter — 50, 100, 150 μm

SEM cross-section after p-regrowth

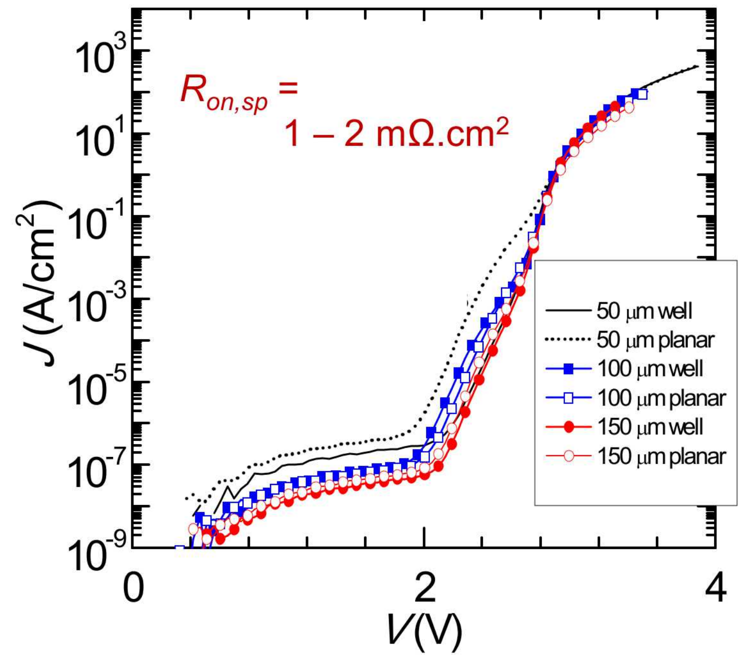


IV characteristics of regrown diodes in an etched well

Reverse IV Characteristics

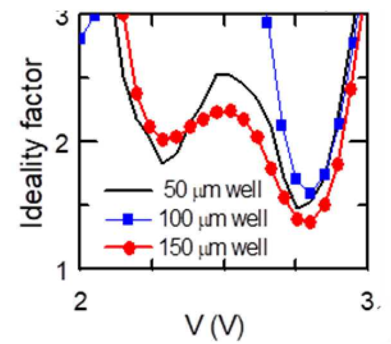


Forward IV Characteristics



Regrown diode in etch well has IVs similar to regrown planar diode

- **V_{revs} ~ 720 V @ 1mA/cm^{-2} (no field management, passivation)**
- **Ideality factor: η = 2 @ 2.3 V, η ~ 1.5 @ 2.8 V**
- **$R_{on,sp}$ = 1 – 2 mΩ-cm²**
- **Large increase in leakage current after -50 V**



IV characteristics of regrown diodes in an etched well

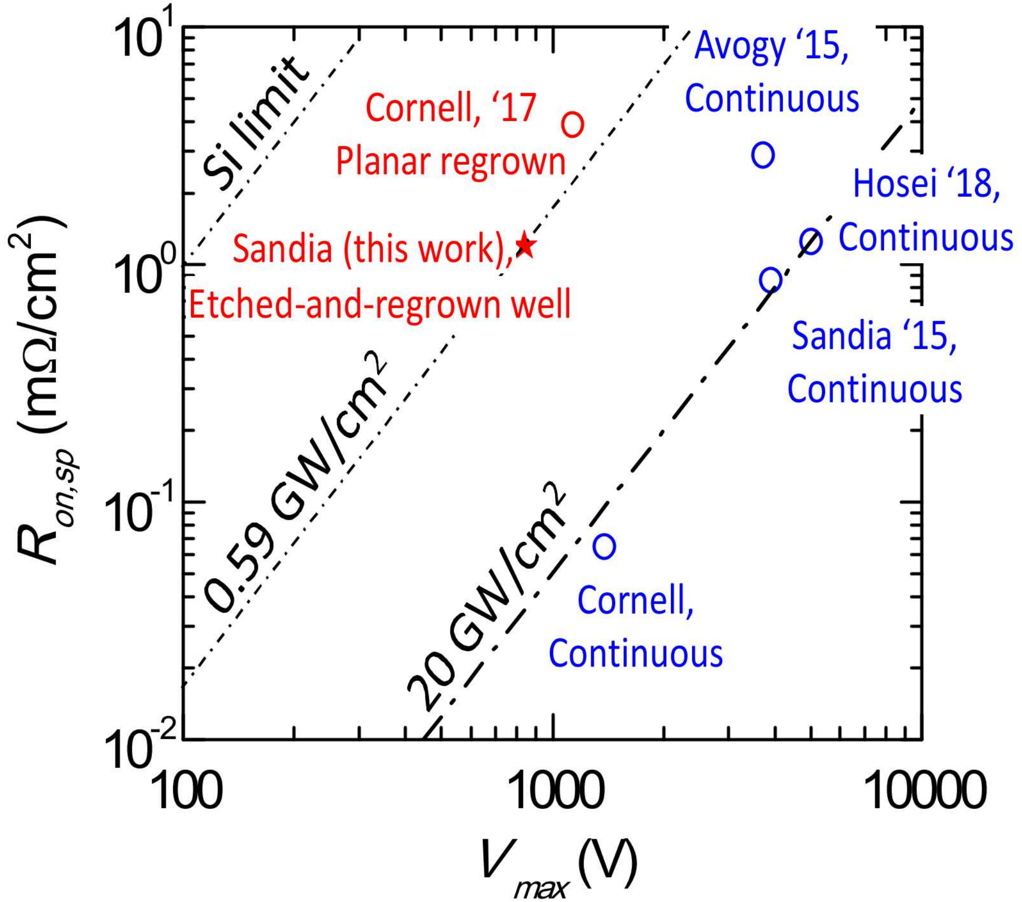
Estimating critical electric field (Ecrit)

- V_{revs} ~ 720 V @ 1mA/cm^{-2}
- $E_{crit} = (2qNV_{revs}/e)^{1/2}$ = 2.6 MV/cm^2

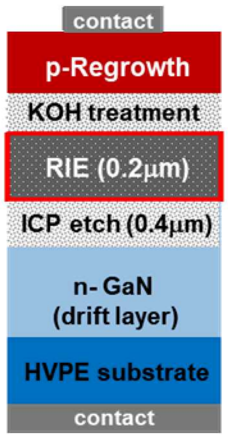
Figure of Merit

- V_{revs}^2 / $R_{on,sp}$ = 588 MW/cm^2

Figure of Merit — $R_{on,sp}$ vs. $V_{breakdown}$

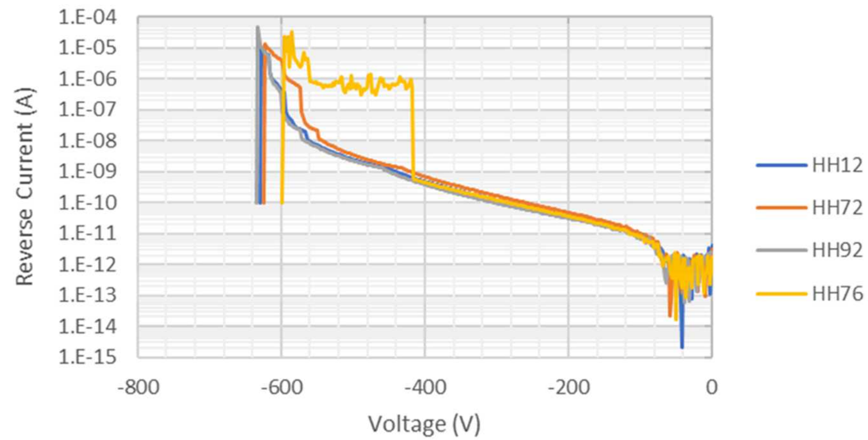


Reactive ion etch (REI) to "clean up" damage from ICP etch



Add reactive ion etch after ICP etch

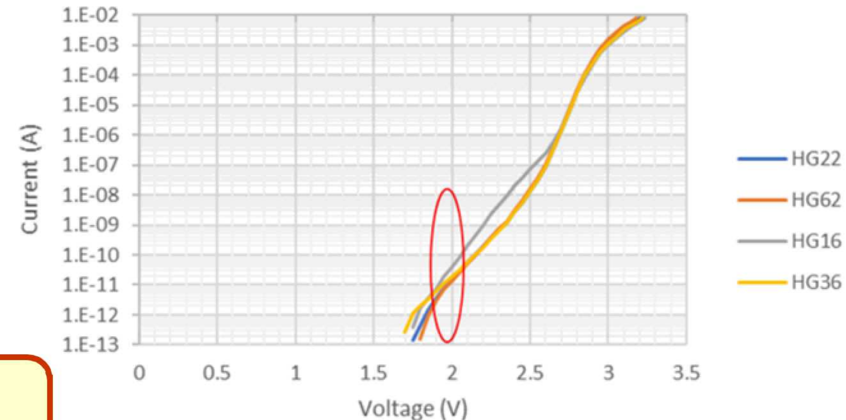
Reverse IV Characteristics



<u>Blanket etching of N-drift layer</u>

- **Low damage etch used for gate recess for HEMTs**
- **RIE 270 nm to remove sub-surface ICP etch damage**
- **Finish with KOH, 10 min., 80 °C, DI rinse, N2 dry**

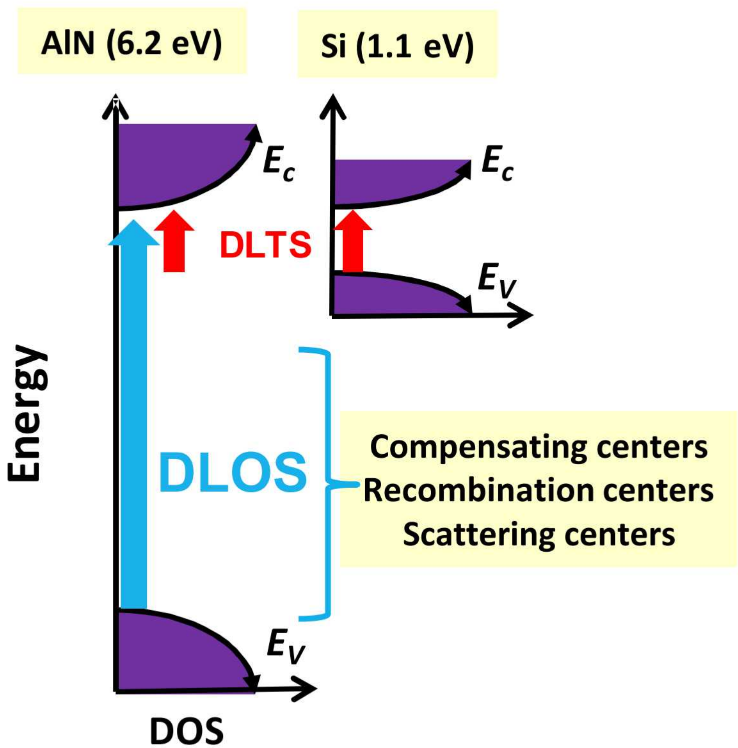
Forward IV Characteristics



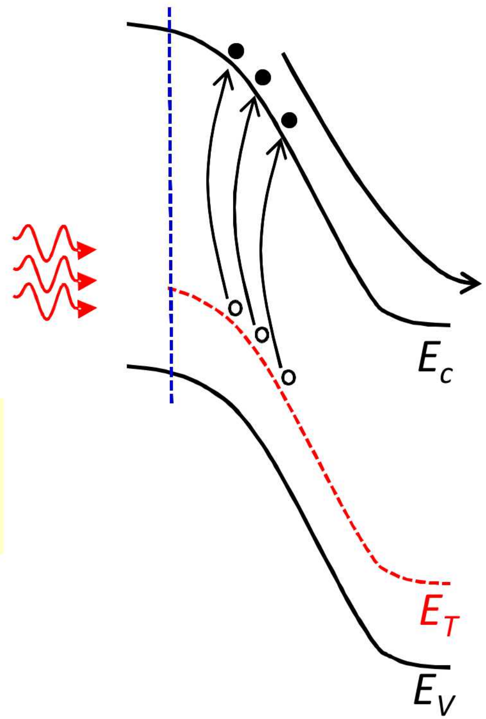
➡ ***RIE "clean-up" etch resulted in regrown diodes with IVs equal to continuously growth diodes***

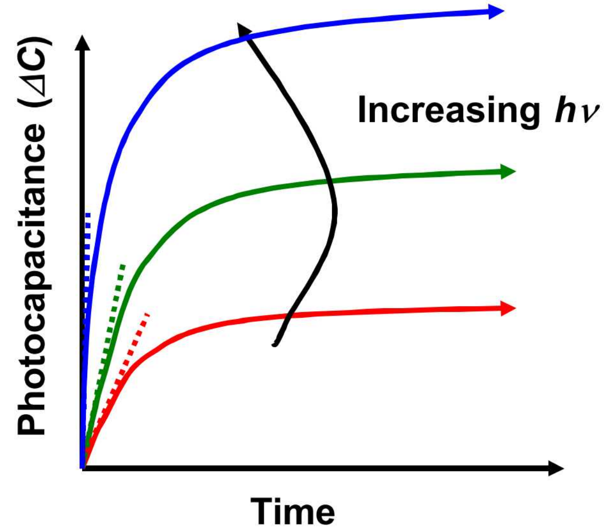
Deep Level Optical Spectroscopy (DLOS)

WBGs require DLOS



Photoemission from electron traps



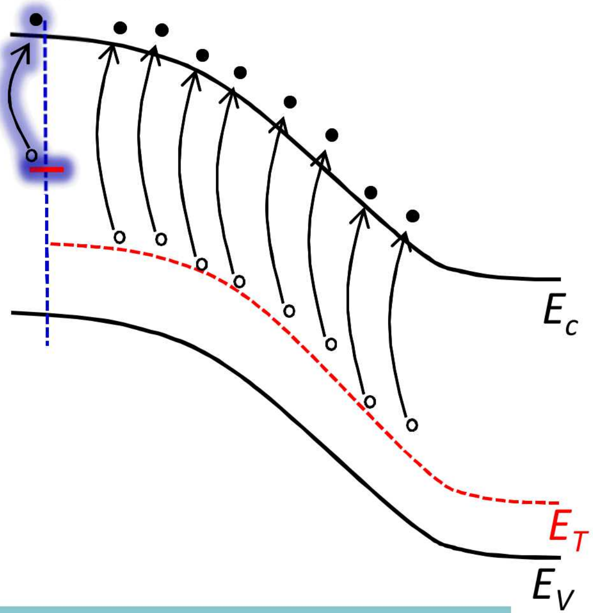


- DLOS required to probe mid-band gap and near-E_V defect levels in GaN
- Majority carrier photoemission from defect levels increases capacitance
- Magnitude of photocapacitance (ΔC) proportional to $N_t = 2N_d \, \Delta C/C_0$

DLOS Consideration for PNDIODES

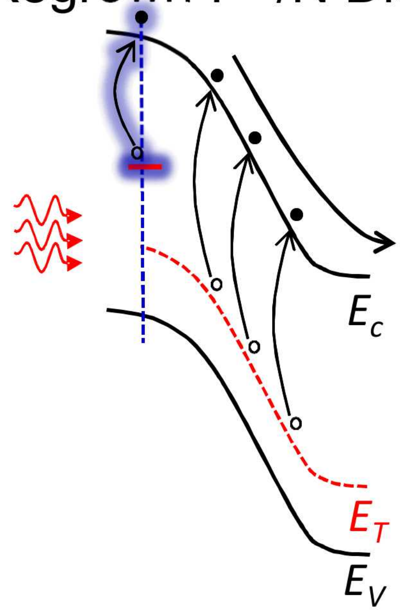
Sandia National Laboratories

Regrown P+/n- diodes



Bulk defects overwhelm interface defects

Regrown P+/N Diodes



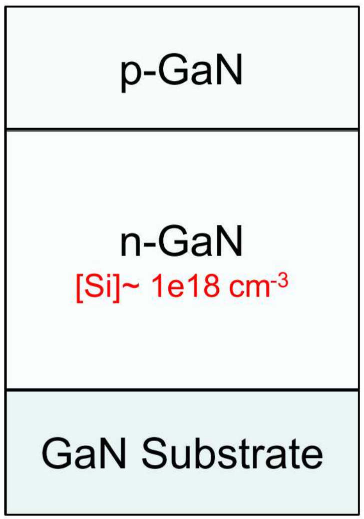
Increased sensitivity to interface defects relative to bulk defects

$$\Delta C_{int} = \frac{N_{t,int}}{2}\frac{C_0}{N_d}\frac{x_{int}^2}{x_d^2} \propto \frac{1}{N_d x_d^3} \propto \sqrt{N_d}$$

- DLOS sensitive to defects the lower-doped drift side of junction…but high doping required for near-junction sensitivity

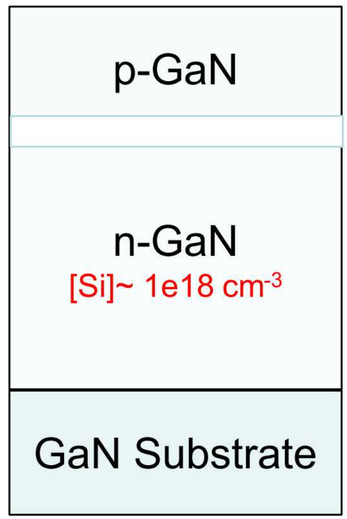
DLOS P-N Diode Structures

Continuously Grown P-N Diode



Dry Etch + Regrown P-N Diode

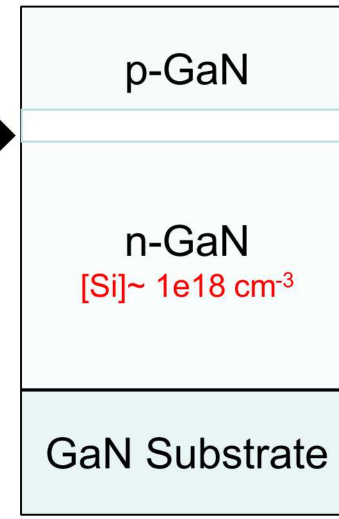
Dry Etched and Regrown Interface (no chemical treatment before regrowth)



Dry Etch + Treatment + Regrown P-N Diode

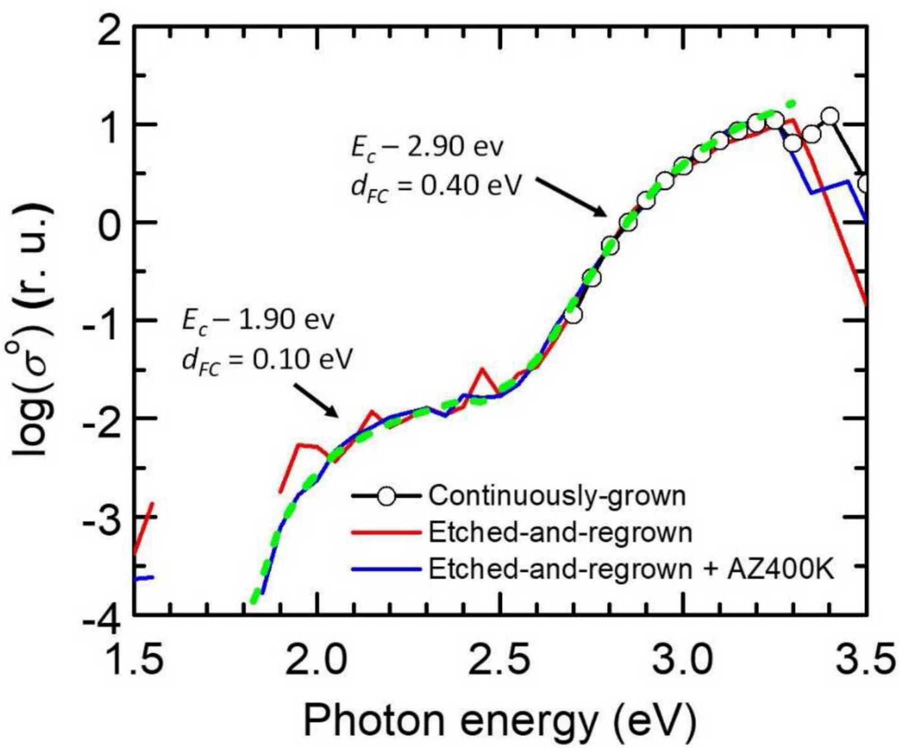
Dry Etched and Regrown Interface with chemical treatment

1) Dilute KOH



- Diodes for DLOS study grown using same growth conditions as other diodes
- Increased Si doping in n-GaN layer to ~ 1e18 cm^{-3} (from ~ 2e16 cm^{-3}) to improve DLOS sensitivity to localized defects near the P-N junction.
- Used KOH-based chemical treatment (AZ400K) for DLOS studies since it had I-V behavior closest to the continuously grown diodes.

DLOS Spectra Results



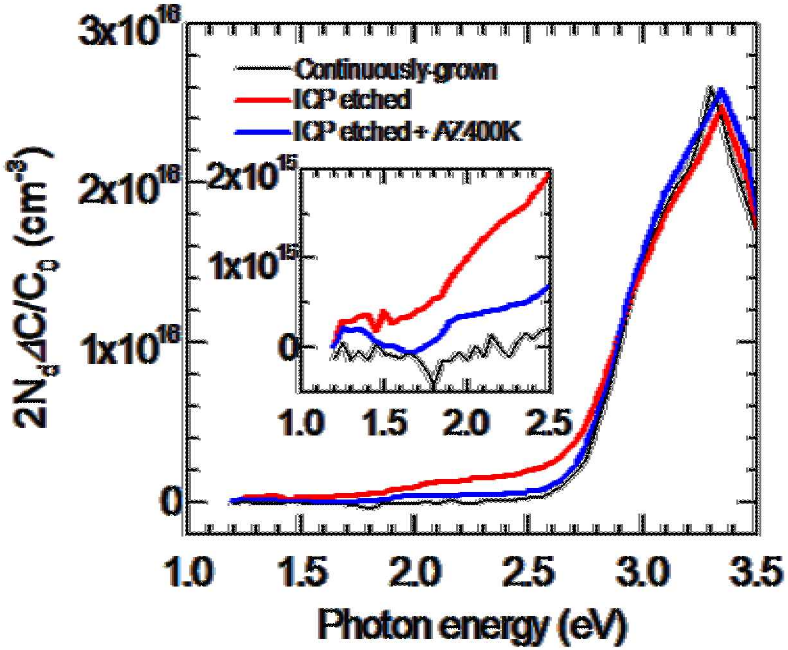
Three samples characterized:

1. Continuously grown (black with circle)
2. Etched + regrown (red)
3. Etched + AZ400K treated + regrown (blue)
4. Model fitting to data (green)

- Optical absorbance per unit defect (σ^0) vs. photon energy
- Single deep level absorption feature with E_C - 2.90 eV relative to E_c (conduction band)
- E_C - 2.90 eV in all three samples
- Spectral features for Photon energy > 3.2 eV obscured by heavy Mg doped layer

- Additional deep level absorption feature seen in both etched + regrowth samples with E_C - 1.90 eV relative to E_c (conduction band)
- ***Related to ICP etch damage***

DLOS Spectra Results



All structures have similar N_t for E_c - 3.20 eV and E_c - 2.90 eV levels
E_c - 1.90 eV trap level is increased for Etch + Regrown samples.

- AZ400K treatment reduced trap density by 3-4X

N_t likely *severely underestimated* with this technique

- Averages value over entire depletion region
- If defects within 5 nm of surface in 150 nm depletion (CV data), **N_t underestimated by ~900X**

	[E_c – 1.90 eV] (cm^{-3})	[E_c – 2.90 eV] (cm^{-3})	[E_c – 3.20 eV] (cm^{-3})
Continuously-grown	-	2.0×10^{16}	6.0×10^{15}
Etched-and-regrown	1.8×10^{15}	1.7×10^{16}	5.3×10^{15}
Etched-and-regrown + AZ400K	5.0×10^{14}	2.1×10^{16}	5.0×10^{15}

Summary

- **MOCVD System is *not the primary source* of the "Si spike" in regrowth (for our hardware)**

- **Dry etch before regrowth degrades performance significantly**
  - **Higher leakage currents**
  - **Likely due to crystalline defects induced by dry-etch process**

- **MOCVD regrown P-N junctions demonstrated**
  - **[Si] ≤ 5E17 cm^{-3} at P-N junction does not degrade electrical performance**
  - **Reverse breakdown > 600 V, no increase in leakage current**
  - **Same performance as continuously grown diodes**
  - **Regrowth process itself does not degrade electrical performance**

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